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Direct AC-AC Converters Using Commercial Power Modules Applied to Voltage Restorers

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Direct AC–AC Converters Using Commercial Power Modules Applied to Voltage Restorers

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***Abstract*—The focus of this paper is the study of direct alternating-current (ac)–ac converters, beginning by buck, half-bridge, full-bridge, and push–pull converters. From the basic converters, we apply a simple methodology to make the use of switches in commercial configurations possible. Following that, eight voltage restorers supplied either on the line side or on the load side are proposed. A comparative evaluation of these topologies concerning implementation, complexity, and component effort is presented. It is notable that some of the studied topologies are known in the literature and others are new. For one of the presented topologies, the design of a 3-kVA voltage restorer is developed, and experimental results are shown, certifying the correct operation of the drive strategy used.**

***Index Terms*—Ac-to-ac converters, alternating current (ac) choppers, commutation, voltage restorer.**

I. Introduction

NOWADAYS, voltage restorers or line conditioners are equipment used in various environments in order to regulate the voltage provided by the grid and, in some cases, to reduce the harmonic content of the output voltage.

It is well known that the main difficulty of employing alternating-current (ac) converters using fast switches and pulsewidth modulation (PWM) has always been the switching strategy, which remained without a solution for many years. Observing Fig. 1, it can be seen that, in order to commutate from S_1/S_3 to S_2/S_4, there are two alternatives: the superposition of the drive signals or the use of dead time. In the first case, a short circuit in the voltage source is provoked, while in the second case, the current through inductor L_o is interrupted, resulting in overvoltage across the switches [1]. One solution for these switching problems is the use of indirect converters [2], which inconveniently use larger number of switches than direct converters.

A switching proposal for ac-ac converters was presented in [3] and improved in [4]–[8], eliminating the need for clamping circuits. In this switching strategy, it is necessary to synchronize the drive signals with the converter's input voltage signal. In [9], a switching cell was proposed for direct ac-ac converters, which is studied later in [10]. These converters are robust, with few controlled switches, and solve the switching issue. However, there is a problem with average current through the inductors, and switches cannot be used in typical commercial module configurations.

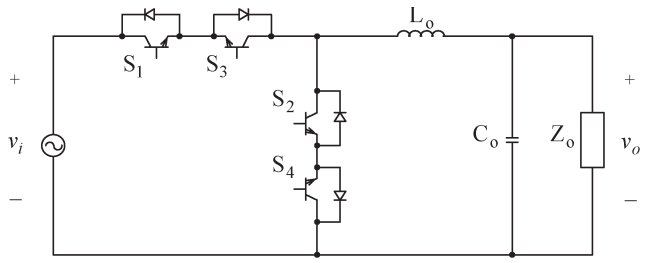

Fig. 1. Standard ac-ac buck converter.

The arrangements of the switches in commercial configurations for ac-ac converters were proposed in [5]–[8] and [11]. These arrangements allow the use of commercial power modules, an attractive feature particularly in a high-power application.

The main idea of this work is to employ the switching strategies in [4]–[8] in several topologies, among which some are well known and others are new, always using switches arranged in a way which permits the usage of commercial modules [5]–[8], [11].

In [12], several converter topologies were proposed; however, the main focus was neither on switching nor on the commercial arrangement of the switches. In this manner, among the topologies presented in this paper, one was chosen to implement a 3-kVA voltage restorer, controlled by the orthogonal detection principle [13], [14]. For an enhanced control performance, one recommends [15]–[21], where many control strategies that are suitable for ac-ac converters are presented; however, their evaluation is not the scope of this work.

In this paper, a comparative evaluation of the proposed voltage restorer concepts concerning characteristics, implementation complexity, and component effort is presented. In addition, expressions for the proposed converter topologies' component design are given.

II. Origin and Commutation of Proposed Topologies

To show the origin of the topologies, which will be presented, an ac-ac buck converter in a standard configuration is shown, as depicted in Fig. 1. Note that this converter is bidirectional in

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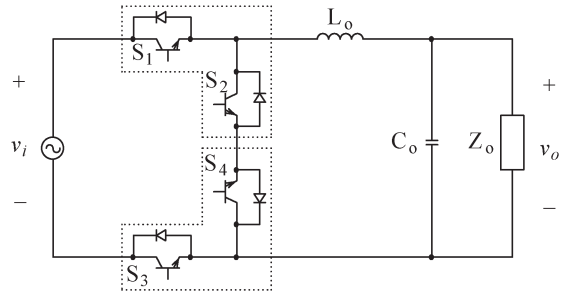
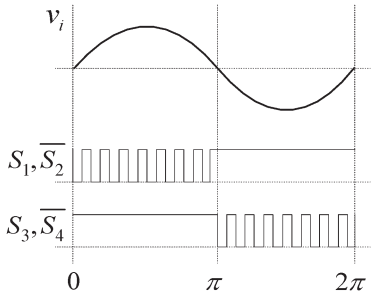


Fig. 2. AC-AC buck converter modified for the use of commercial switch modules.



	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
$\overline{S_2}$	*pwm*	*on*
S_3	*on*	*pwm*
$\overline{S_4}$	*on*	*pwm*

Fig. 3. Switching of the converter IGBTs in Fig. 2.

both voltage and current by using commercial switches. However, the usage of commercial modules is not possible. Altering the position of switch S_3, a configuration which allows the usage of commercial modules is obtained, as shown in Fig. 2.

The switching is performed, as shown in Fig. 3; note that, during the positive semicycle of the grid voltage, switches S_3 and S_4 are enabled to conduct and switches S_1 and S_2 are driven by PWM. During the negative semicycle of the grid voltage, switches S_1 and S_2 are now set to conduct, and switches S_3 and S_4 are modulated at high frequency. A dead time between the module switches, as for dc–dc converters, is used.

III. Proposed Topologies

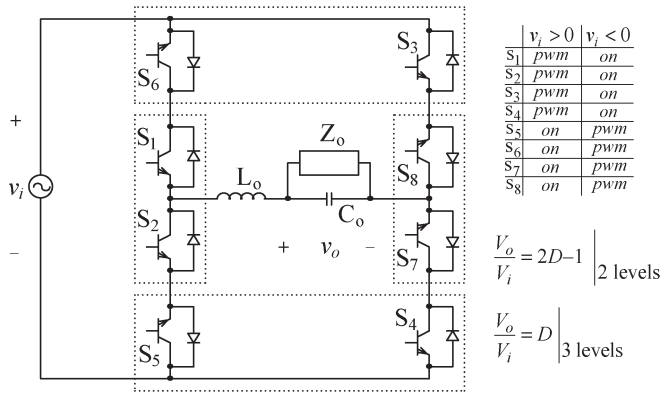
Using the same procedure adopted in Fig. 1, i.e., rearranging the switches in a way to obtain configurations that allow the usage of commercial modules, several ac-ac converter topologies can be obtained.

With these topologies, several ac-voltage-compensating restorers can be implemented, which have the advantage of processing only the difference between the desired output voltage and the input voltage, consequently, processing merely part of the load's power, guaranteeing a high performance of the system.

Here, one can note that the converter static gain is expressed as a function of the switches' duty cycle and the turns ratios, for the structures that use transformers.

In Fig. 4, the full-bridge ac-ac converter is shown, while Figs. 5 and 6 show the voltage restorers based on the converter shown in Fig. 4.

Figs. 7 and 8 show the converters based on the half-bridge converter shown in Fig. 9. Note that the transformer has two secondary windings and not just a tap, generally used in conventional converters [10]. This modification is performed so that switches in a modular configuration can be used.

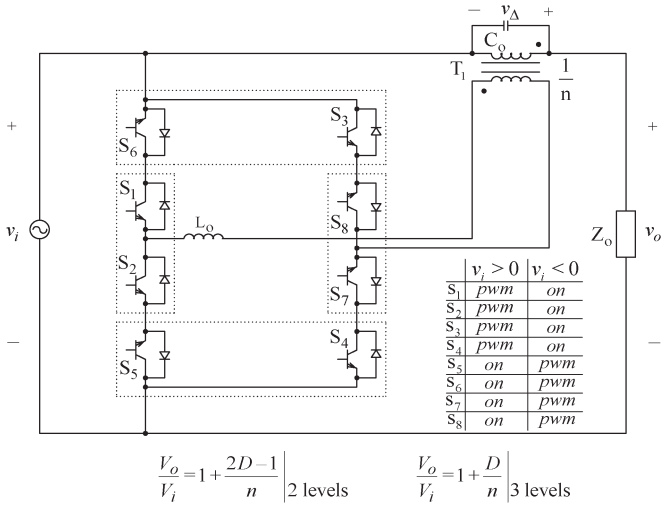


	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*pwm*	*on*
S_4	*pwm*	*on*
S_5	*on*	*pwm*
S_6	*on*	*pwm*
S_7	*on*	*pwm*
S_8	*on*	*pwm*

$\frac{V_o}{V_i} = 2D-1$ | 2 levels

$\frac{V_o}{V_i} = D$ | 3 levels

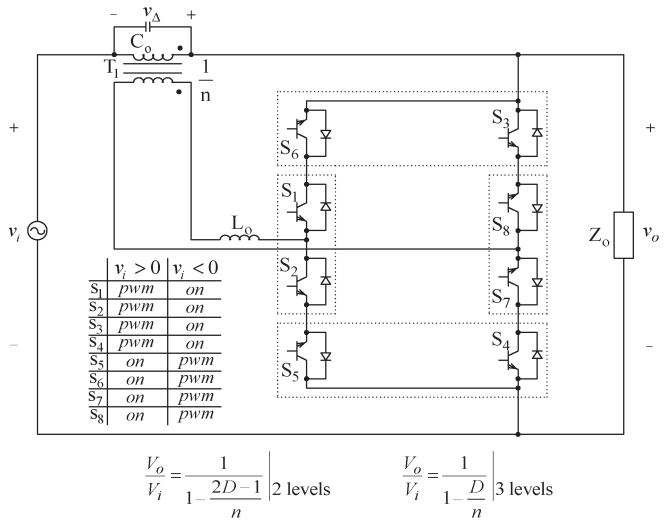
Fig. 4. Full-bridge converter.



	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*pwm*	*on*
S_4	*pwm*	*on*
S_5	*on*	*pwm*
S_6	*on*	*pwm*
S_7	*on*	*pwm*
S_8	*on*	*pwm*

$\frac{V_o}{V_i} = 1 + \frac{2D-1}{n}$ | 2 levels $\qquad$ $\frac{V_o}{V_i} = 1 + \frac{D}{n}$ | 3 levels

Fig. 5. Full-bridge converter supplied on the line side.



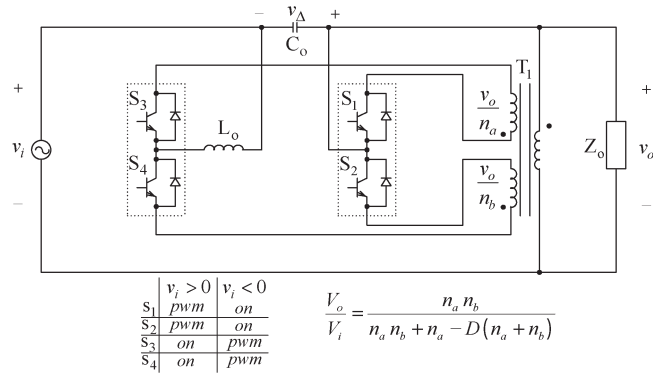
	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*pwm*	*on*
S_4	*pwm*	*on*
S_5	*on*	*pwm*
S_6	*on*	*pwm*
S_7	*on*	*pwm*
S_8	*on*	*pwm*

$\frac{V_o}{V_i} = \frac{1}{1 - \frac{2D-1}{n}}$ | 2 levels $\qquad$ $\frac{V_o}{V_i} = \frac{1}{1 - \frac{D}{n}}$ | 3 levels

Fig. 6. Full-bridge converter supplied on the load side.

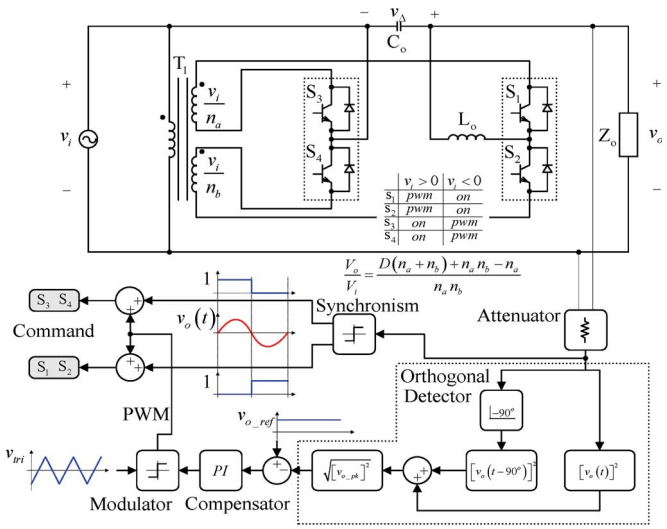
Topologies based on the push–pull converter are shown in Figs. 10–12. In Fig. 10, the ac-ac push–pull converter is shown, and Figs. 11 and 12 show the voltage restorers obtained from this converter.

In Fig. 8, the designed converter diagram is shown. The command circuitry for providing the switches gate signals can be seen in this figure as well.



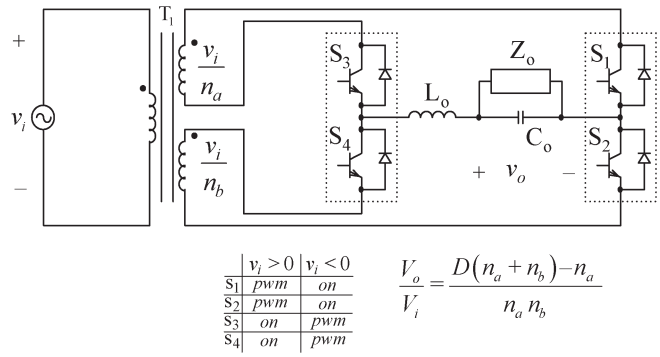
	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*on*	*pwm*
S_4	*on*	*pwm*

Fig. 7. Half-bridge converter supplied on the load side.



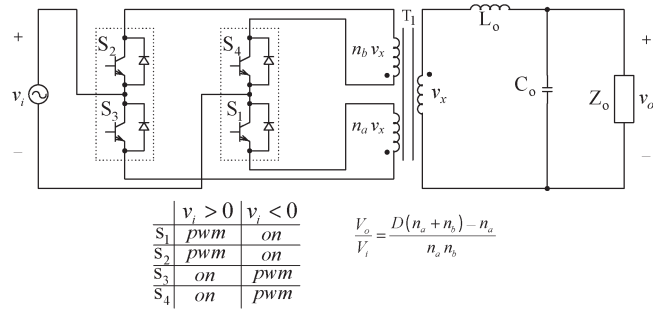
	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*on*	*pwm*
S_4	*on*	*pwm*

Fig. 8. Half-bridge voltage restorer supplied on the line side—implemented converter.



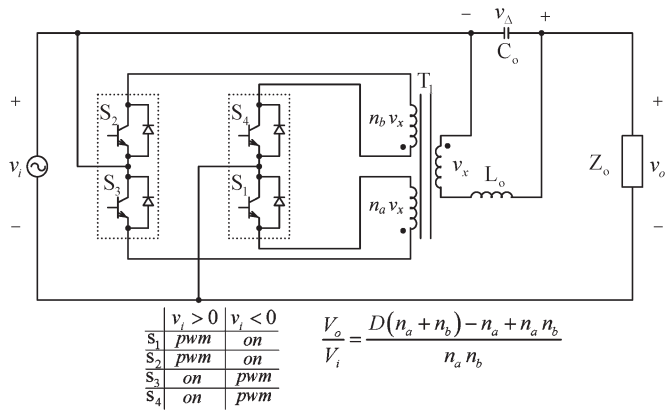
	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*on*	*pwm*
S_4	*on*	*pwm*

Fig. 9. Half-bridge converter.



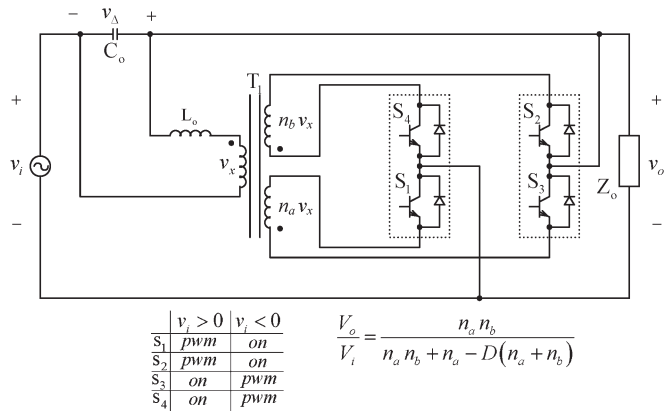
	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*on*	*pwm*
S_4	*on*	*pwm*

Fig. 10. Push–pull converter.



	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*on*	*pwm*
S_4	*on*	*pwm*

Fig. 11. Push–pull converter supplied on the line side.



	$v_i > 0$	$v_i < 0$
S_1	*pwm*	*on*
S_2	*pwm*	*on*
S_3	*on*	*pwm*
S_4	*on*	*pwm*

Fig. 12. Push–pull converter supplied on the load side.

Table I summarizes the proposed topologies and their component design characteristics: static gain, transformer turns ratio, inductor current, and capacitor voltage ripples.

IV. Topologies Comparative Evaluation

In this section, a comparison of the presented converter topologies regarding realization effort, stresses on the components, etc., is given. The evaluation criteria, characteristic quantities, and definitions are similar to the one presented in [23], where different three-phase rectifier systems were investigated.

A. Characteristic Quantities

Following [23], with respect to calculation effort when evaluating the converter systems, only integral characteristic quantities and/or the sum of component voltage or current average and *rms* values, apparent switching power, etc., are considered. The characteristic quantities are determined by electronic simulations for a given voltage restorer project specification (cf. Section IV-B) concerning the following:

1) implementation complexity (number of components);
2) voltage and current stresses on components.

Semiconductor's Losses: The transistor conduction losses are given by (1), where I_o denotes the *rms* value of the load current and $I_{T,\mathrm{avg},n}$ is the average current value across one

TABLE I
VOLTAGE RESTORER DESIGN CHARACTERISTICS

Figure	Converter	Static gain	Transf. Turn Ratios	Inductor Current Ripple	Capacitor Voltage Ripple
2	Buck	$\frac{v_o}{v_i}=D$	-	$\Delta i_{Lo}=\frac{V_o(1-D)}{L_o f_s}$	$\Delta v_{Co}=\frac{4\Delta i}{\pi^3 C_o f_s}$
4	Full-bridge - 2 levels	$\frac{v_o}{v_i}=2D-1$	-	$\Delta i_{Lo}=\frac{2V_o D(1-D)}{L_o f_s(2D-1)}$	$\Delta v_{Co}=\frac{4\Delta i}{\pi^3 C_o f_s}$
	Full-bridge - 3 levels	$\frac{v_o}{v_i}=D$	-	$\Delta i_{Lo}=\frac{V_o(1-D)}{2L_o f_s}$	$\Delta v_{Co}=\frac{2\Delta i}{\pi^3 C_o f_s}$
6	Full-bridge converter supplied on the line side – 2 levels	$\frac{v_o}{v_i}=1+\frac{2D-1}{n}$	$n=\frac{1-\Delta}{\Delta}$	$\Delta i_{Lo}=\frac{2V_i D(1-D)}{L_o f_s}$	$\Delta v_{Co}=\frac{4n\Delta i}{\pi^3 C_o f_s}$
	Full-bridge converter supplied on the line side – 3 levels	$\frac{v_o}{v_i}=1+\frac{D}{n}$	$n=\frac{1-\Delta}{\Delta}$	$\Delta i_{Lo}=\frac{V_i D(1-D)}{2L_o f_s}$	$\Delta v_{Co}=\frac{2n\Delta i}{\pi^3 C_o f_s}$
7	Full-bridge converter supplied on the load side – 2 levels	$\frac{v_o}{v_i}=\frac{n}{n-2D+1}$	$n=\frac{1}{\Delta}$	$\Delta i_{Lo}=\frac{2V_o D(1-D)}{L_o f_s}$	$\Delta v_{Co}=\frac{2I_o D(1-D)}{C_o f_s(N-2D+1)}$
	Full-bridge converter supplied on the load side – 3 levels	$\frac{v_o}{v_i}=\frac{n}{n-D}$	$n=\frac{1}{\Delta}$	$\Delta i_{Lo}=\frac{V_o D(1-D)}{2L_o f_s}$	$\Delta v_{Co}=\frac{I_o D(1-D)}{2C_o f_s(N-D)}$
5	Half-bridge	$\frac{v_o}{v_i}=\frac{D(n_a+n_b)-n_a}{n_a\cdot n_b}$	$n_a=1-\Delta \quad n_b=1+\Delta$	$\Delta i_{Lo}=\frac{2V_o D(1-D)}{L_o f_s(-1+\Delta+2D)}$	$\Delta v_{Co}=\frac{4\Delta i}{\pi^3 C_o f_s}$
12	Half-bridge converter supplied on the line side	$\frac{v_o}{v_i}=\frac{D(n_a+n_b)+n_a n_b-n_a}{n_a n_b}$	$n_a=\frac{1-\Delta}{\Delta} \quad n_b=\frac{1+\Delta}{\Delta}$	$\Delta i_{Lo}=\frac{2V_o D(1-D)\Delta}{L_o f_s(1-\Delta+2D\Delta)}$	$\Delta v_{Co}=\frac{4\Delta i}{\pi^3 C_o f_s}$
8	Half-bridge converter supplied on the load side	$\frac{v_o}{v_i}=\frac{n_a n_b}{n_a n_b+n_a-D(n_a+n_b)}$	$n_a=n_b=\frac{1}{\Delta}$	$\Delta i_{Lo}=\frac{2V_o D(1-D)}{n_a L_o f_s}$	$\Delta v_{Co}=\frac{I_o D(1-D)(n_a+n_b)}{C_o f_s(n_a n_b+n_a-D\cdot(n_a+n_b))}$
9	Push-pull	$\frac{v_o}{v_i}=\frac{D(n_a+n_b)-n_a}{n_a n_b}$	$n_a=1-\Delta \quad n_b=1+\Delta$	$\Delta i_{Lo}=\frac{2V_o D(1-D)}{L_o f_s(-1+\Delta+2D)}$	$\Delta v_{Co}=\frac{4\Delta i}{\pi^3 C_o f_s}$
10	Push-pull converter supplied on the line side	$\frac{v_o}{v_i}=\frac{D(n_a+n_b)-n_a+n_a n_b}{n_a n_b}$	$n_a=\frac{1-\Delta}{\Delta} \quad n_b=\frac{1+\Delta}{\Delta}$	$\Delta i_{Lo}=\frac{2V_o D(1-D)\Delta}{L_o f_s(1-\Delta+2D\Delta)}$	$\Delta v_{Co}=\frac{4\Delta i}{\pi^3 C_o f_s}$
11	Push-pull converter supplied on the load side	$\frac{v_o}{v_i}=\frac{n_a n_b}{n_a n_b+n_a-D(n_a+n_b)}$	$n_a=n_b=\frac{1}{\Delta}$	$\Delta i_{Lo}=\frac{2V_o D(1-D)}{n_a L_o f_s}$	$\Delta v_{Co}=\frac{I_o D(1-D)(n_a+n_b)}{C_o f_s(n_a n_b+n_a-D\cdot(n_a+n_b))}$

transistor. In a similar way, the diode conduction losses can be determined [see (2)].

To obtain the transistor's switching losses, one utilizes (3). Therein, the turn-on/turn-off losses are determined considering a constant turn-off voltage $U_{T,\mathrm{off},n}$, given by the *rms* value of the input or output voltage, depending where the converter is supplied from. In (3), P_o represents the system output power, and $|i_T|_{\mathrm{avg},n}$ represents the average value of the turn-on/turn-off current across the transistors

$$P_T=\frac{1}{I_o}\sum_n I_{T,\mathrm{avg},n} \tag{1}$$

$$P_D=\frac{1}{I_o}\sum_n I_{D,\mathrm{avg},n} \tag{2}$$

$$S_P=\frac{1}{P_o}\sum_n |i_T|_{\mathrm{avg},n}U_{T,\mathrm{off},n}. \tag{3}$$

Rated Power of Inductors and Transformers: The rated power of inductive components (inductors and transformers) is evaluated, in such a way that inductors are characterized by the rated power of an equivalent transformer [24], [25], as given by (4). For transformers, the rated power transferred is obtained by (5), where S_i denotes the apparent power of a partial winding [23]

$$S_{T,\mathrm{eq}}=\frac{1}{P_o}2.2 f_N L_o I_{Lo,\mathrm{rms}} I_{Lo,\max} \tag{4}$$

$$S_T=\frac{1}{P_o}\sum_n S_i. \tag{5}$$

Capacitor Current Stress: The stress across the capacitor is determined by the ratio between its current's *rms* values and the output current, as shown in

$$i_{Co}=\frac{I_{Co,\mathrm{rms}}}{I_o}. \tag{6}$$

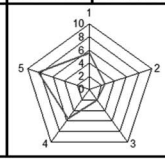
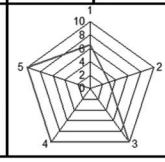
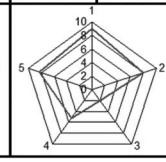
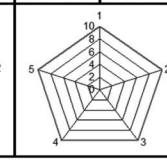
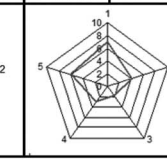
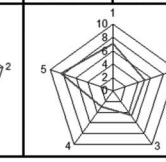
B. Simulation Results

For the sake of brevity, only converters which process merely a part of the load power are analyzed (Figs. 5–8 Fig. 11, and Fig. 12). These topologies have higher efficiency and reduced volume when compared to converters that handle 100% of the system power capability (Fig. 2, Fig. 4, Fig. 9, and Fig. 10).

All the analyzed converter topologies were designed according to the following specifications:

1) $v_i=220$ V $\pm 20\%/60$ Hz; $v_o=220$ V/60 Hz; $S_o=3$ kVA;
2) $f_s=20$ kHz; $\Delta i_{Lo}=10\%I_{Lo\_pk}$; $\Delta v_{Co}=1\%V_{o\_pk}$.

TABLE II
3-kW VOLTAGE RESTORER COMPARATIVE EVALUATION

Topology		Push-pull conditioner supplied on the line side	Push-pull conditioner supplied on the load side	Half-bridge conditioner supplied on the line side	Half-bridge conditioner supplied on the load side	Full-bridge 3 levels supplied on the line side	Full-bridge 3 levels supplied on the load side
Rectifier Implementation Complexity	n transistors	4	4	4	4	6	6
	n fast-recovery diodes	4	4	4	4	6	6
	n inductors	1	1	1	1	1	1
	n capacitors	1	1	1	1	1	1
	n transformers	1	1	1	1	1	1
	voltage sensors	1	1	1	1	1	1
	n gate drivers	4	4	4	4	6	6
Operation Point		V_i=220+20% / V_i=220-20%	V_i=220+20% / V_i=220-20%	V_i=220+20% / V_i=220-20%	V_i=220+20% / V_i=220-20%	V_i=220+20% / V_i=220-20%	V_i=220+20% / V_i=220-20%
Total semiconductor's rated power loss	transistors (cond./switch.)	0.21/1.05 / 0.29/0.95	0.2/0.8 / 0.3/1.2	0.9/1.18 / 0.9/0.8	0.75/0.8 / 1.12/1.2	0.48/1.15 / 0.48/0.77	0.36/0.72 / 0.54/1.08
	diodes	0.21 / 0.29	0.2 / 0.3	0.9 / 0.9	0.75 / 1.12	0.48 / 0.48	0.36 / 0.54
Capacitor current stress		0.037 / 0.034	0.155 / 0.22	0.037 / 0.034	0.155 / 0.22	0.032 / 0.0056	0.07 / 0.1
Transformer/Inductor rated power		0.28/0.0046 / 0.26/0.0046	0.22/0.004 / 0.33/0.009	0.28/0.0046 / 0.26/0.0046	0.22/0.004 / 0.33/0.009	0.2/0.0033 / 0.2/0.0033	0.185/0.001 / 0.28/0.0022
Summary of Characteristics: Scaled to the maximum value among analyzed structures (maximum value = 10) 1- Transistor Losses 2- Fast Diodes Losses 3- Capacitor Current Stress 4- Total rated power of inductor 5- Total rated power of transformer							
System Characteristics							
Inductive Filter L_0		0.4 mH	0.5 mH	0.4 mH	0.5 mH	4 mH	2 mH
Capacitive Filter C_0		4 μF	20 μF	4 μF	20 μF	2 μF	4.5 μF
Transformer Turns Ratio		n_a=3/ n_b=4.5	n_a=3.75/ n_b=3.75	n_a=3/ n_b=4.5	n_a=3.75/ n_b=3.75	3.75	4.5
Input / Output voltages		220 ±20%/220 V	220 ±20%/220 V	220 ±20%/220 V	220 ±20%/220 V	220 ±20%/220 V	220 ±20%/220 V
Mains/Switching frequency		60Hz / 20kHz	60Hz / 20kHz	60Hz / 20kHz	60Hz / 20kHz	60Hz / 20kHz	60Hz / 20kHz
Power Rating		3 kW	3 kW	3 kW	3 kW	3 kW	3 kW

The transformer turns ratios were defined in such a way that all systems have similar static gain for a given duty cycle D and maximal-voltage-compensation cases ($v_i = 220\ \text{V} \pm 20\%$). This allows the voltage restorer topologies to have equivalent control effort and dynamic behavior in the considered operation points. The load is considered purely resistive. Furthermore, the inductor and capacitors were adjusted to fulfill the ripple requirements on the maximal-compensation cases.

The simulations performed for determining the characteristic current *peak*, *average*, and *rms* values are based on the following assumptions:

1) mains' voltage is purely sinusoidal, with no inner mains impedance;
2) ideal components;
3) neglection of the switching frequency ripple for the calculation of component peak current values.

The simulation results, including the converter parameters, are compiled in Table II. These results are summarized graphically, where the evaluated characteristic (each pentagon axis) high values (in red or bold) are scaled to the maximum obtained value among the analyzed structures. The maximum value found is given a mark of ten. Therefore, the converter that has the minimum values/area is the most suitable for the considered design specification.

Analyzing the results, one can observe that the push–pull converter fed by the line side presented the best composition of characteristics, particularly regarding semiconductor losses. On the other hand, the full-bridge three-level topology fed by the line side presents lower passive component stress characteristics. The drawbacks of the latter topology are the number of components and, consequently, the implementation complexity. As a consequence, the total cost of the structure increases, while the reliability of the system reduces.

The main difference between the push–pull and half-bridge topologies is in the semiconductor stress characteristics. Due to the transformer configuration, in the latter one, the current across the semiconductor is higher than that for the push–pull converter, but the block voltage is lower. Therefore, the choice for one or the other topology is mainly dependent on the commercially available semiconductor loss characteristics. It is common that power modules with lower breakdown voltage have better power loss characteristics. For the specification being considered, the push–pull converter would employ 1200-V insulated-gate bipolar transistors (IGBTs), and for the half-bridge voltage restorer, it would use 600-V IGBTs.

It is important to point out that the topologies fed by the load side have outstanding performance for one region of voltage compensation ($+\Delta$), which is better than for the same topology fed by the line side. On the other hand, for the other voltage compensation region ($-\Delta$), the performance is considerably worse. However, since the components of the converter have to cope with the maximum stress situation, topologies fed by the load side need higher power rating elements. Therefore, for the considered specification, voltage restorers fed by the line side are less expensive and normally have lower volume than the ones fed by the load side (higher power density). Moreover, as can be observed in the results, this voltage restorer technology has more symmetric characteristic behavior for both voltage compensation regions than the ones fed by the load side.

V. IMPLEMENTED VOLTAGE RESTORER ANALYSIS AND EXPERIMENTAL RESULTS

A. Converter Design

The voltage restorer which will be implemented in the laboratory with the objective of certifying the operation of the proposed topologies is the converter shown in Fig. 8. This

is a half-bridge converter which uses a transformer with two secondary windings and four controlled switches. L_o and C_o comprise the converter's output filter. Voltage compensation, with proper amplitude and phase, is applied in series with the input voltage so that the output voltage has the desired amplitude.

The duty cycle (D) is defined as the ratio between the conducting interval of switches S_1 and S_2 and the total switching period $(T_s = 1/f_s)$, considering the positive semicycle of the grid voltage. During the negative semicycle, the duty cycle is the ratio between the conducting intervals of switches S_3 and S_4 and the total time, given by the switching frequency (f_s). The expressions for the voltage restorer's static gain, the transformer turns ratios (n_a and n_b), the inductor L_o current ripple, and the capacitor C_o voltage ripple are given in Table I.

Using these expressions, a voltage restorer with the following parameters was designed:

1) $v_i = 220 \pm 20\%$ V, $v_o = 220$ V, $S_o = 3$ kVA;
2) $f_s = 20$ kHz, $n_a = 3.2$, $n_b = 4.8$, $v_{\text{tri\_pkp}} = 12.6$ V;
3) $L_o = 400$ μH, S_1 to S_4 = IRG4PSC71UD, $C_o = 10$ μF.

Fig. 8 shows the simplified circuit of the implemented voltage restorer. In this figure, note that the output voltage is sampled in order to generate the synchronism signals to properly obtain the drive signals of the switches, according to the input/output voltage's polarity. The control technique using orthogonal detection is also shown, and the voltage controller is a classic proportional–integral (PI) [13], [14].

B. Line Impedance Problem

To verify the line impedance $Z_i(s)$ effects on the circuit operation, the mathematical model of the studied topology is derived considering the *ac* converter and transformer as a controlled source which compensates the voltage in series [cf. Fig. 13(a)]. In this model, the line impedance is represented by a pure inductance L_{eq}. In (7), shown at the bottom of the page, the output-voltage-to-control-voltage transfer function $(G(s))$ is presented, and so is the output-voltage-to-input-voltage transfer function $(F(s))$ in (8), shown at the bottom of the page. The aforementioned expressions can be used to study the closed-loop behavior of the converter [cf. Fig. 13(b)].

Analyzing (7), it can be seen that $G(s)$ contains a zero on the right side of the complex plane. The right-side zero problem, which is typical for boost converters in voltage mode, was studied in [26]. This kind of system, often referred to as nonminimum phase, has a unique step input response. An incremental step in duty cycle implies on an increase in compensation voltage v_Δ and also on the converter input current.

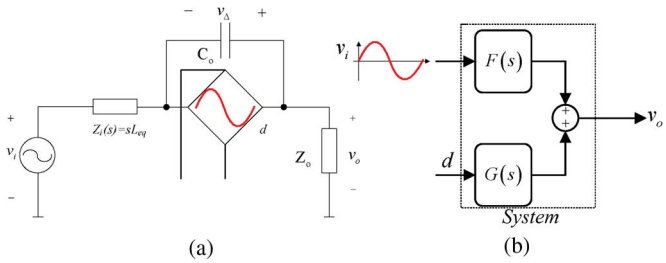


Fig. 13. (a) Converter model. (b) Converter block diagram.

This current flowing through the line impedance provokes a voltage drop, and so, the output voltage v_o initially decreases, during a Δt time interval, rising later as desired to reach steady state in a stable system [cf. Fig. 14(b)]. In this way, the effect of the positive zero can be interpreted as a delay on the output voltage response due to duty cycle variations. Note that, if a fast control loop is used, the changing dynamic of the control signal can lead the system to instability.

The voltage restorer sensitivity to load Z_o variation can be observed in $G(s)$ and $F(s)$. The system's dynamic is more oscillatory and less damped as the load impedance increases. Therefore, in closed-loop operation, the topology can have instability problems feeding nonlinear loads such as half-bridge rectifiers, where the current can become discontinuous and have abrupt variations. In practice, there are parasitic resistances, which lessen the effect of abrupt load variations since these elements work as dampers to the voltage oscillations.

Electronic simulations are performed to evaluate the effects of the line impedance on the system dynamic for duty cycle variation, and the results are shown in Fig. 14(b). From Fig. 14(b), it can be noticed that the system simulated without the line impedance has no delay and that the output voltage increases instantaneously with the increase in $d(t)$. The converter with the line impedance has delay Δt, and moreover, it has an output voltage oscillation due to the voltage drop in $Z_i(s)$ from the high-frequency circulating current. This voltage oscillation flows through the output voltage sensor, which could cause problem to the structure's control. As can be observed, both effects are attenuated when the input filter shown in Fig. 14(a) is used.

The effects of the positive zero and voltage oscillations can then be attenuated by using a filter in the converter input to decouple the line impedance from the system [cf. Fig. 14(a)]. Another solution is to design a slow control loop, which limits the converter's dynamic response. In the built prototype, the function of the input filter is performed by decoupling capacitors of 10 μF placed on the transformer secondary side.

$$G(s) = \frac{\frac{n_a n(n_a+n_b)V_o}{(D(n_a+n_b)-n_a+n_a n_b)^2} \cdot \left[\frac{n_a n_b}{D(n_a+n_b)-n_a+n_a n_b} - s\frac{L_{\text{eq}}}{Z_o}\frac{D(n_a+n_b)-n_a+n_a n_b}{n_a n_b}\right]}{s^2 L_{\text{eq}} C_o + s\frac{L_{\text{eq}}}{Z_o} + \left(\frac{n_a n_b}{D(n_a+n_b)-n_a+n_a n_b}\right)^2} \tag{7}$$

$$F(s) = \frac{\frac{n_a n_b}{D(n_a+n_b)-n_a+n_a n_b}}{s^2 L_{\text{eq}} C_o + s\frac{L_{\text{eq}}}{Z_o} + \left(\frac{n_a n_b}{D(n_a+n_b)-n_a+n_a n_b}\right)^2} \tag{8}$$

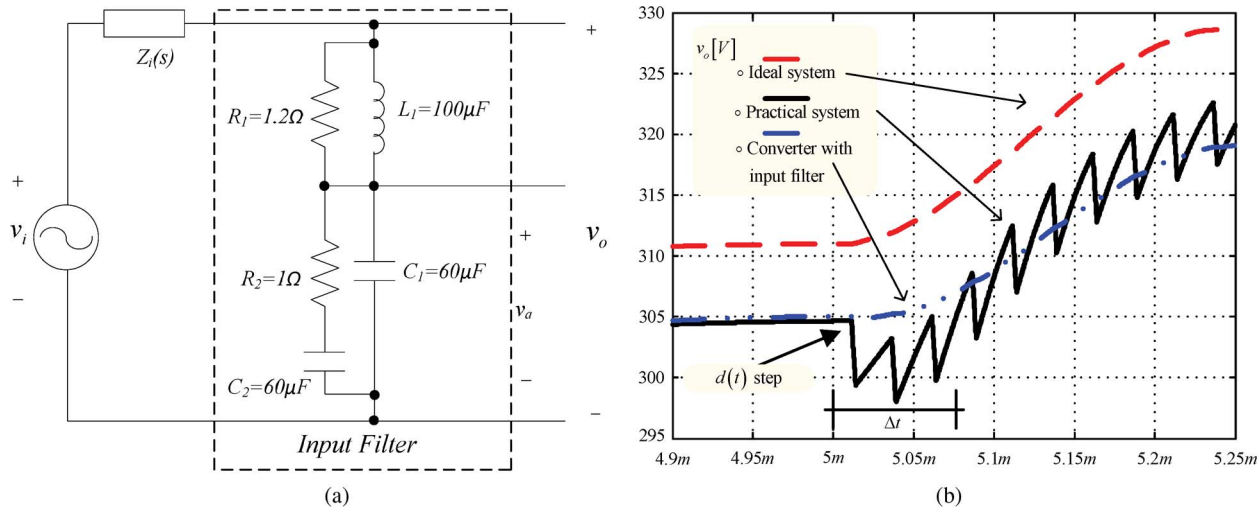


Fig. 14. (a) Converter input filter. (b) Response to a step in duty cycle.

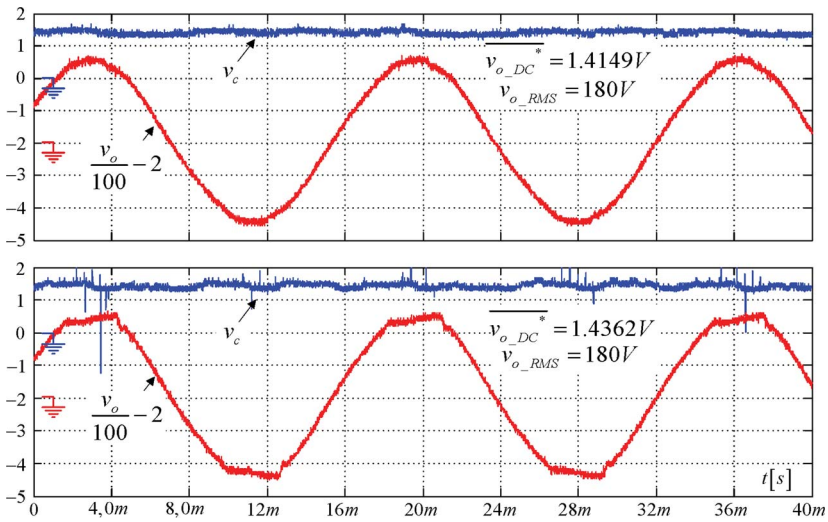


Fig. 15. Orthogonal detector output voltage with sinusoidal and distorted input voltage.

C. Orthogonal Detection Control

The orthogonal detection controller uses trigonometric relations to obtain a continuous voltage value, which is proportional to the input voltage *rms* value [13], [14]. If the measured voltage is sinusoidal, then the output of the orthogonal detector will be proportional to the *rms* value of the measured voltage (cf. Fig. 8). On the other hand, if the measured voltage is distorted with harmonics, the output value will not be the actual *rms* value of this voltage. This problem is shown in Fig. 15, where the difference in the output values can be seen, despite the same *rms* value of the voltages being applied at the input of the orthogonal detector. This drawback can be lessened if a prefilter stage is employed. Furthermore, this technique could present outstanding performance if one combines it with a feedforward control technique. In this case, the latter one would correct the output voltage against disturbances in the input voltage, while the orthogonal control would act to correct the *rms* value of the output voltage.

The orthogonal detection control was implemented in a PIC18F252 microcontroller. The converter output voltage is sampled (attenuated) and rectified with a precision rectifier, to then be applied to this microcontroller. The implemented algorithm determines the *rms* voltage value according to the principle of the orthogonal detection. Therefore, the required 90° phase shift is carried out by a time delay. At the output of PIC18F252, there is a practically continuous voltage, which will be compared to the reference voltage to generate an error signal. This error is compensated by a PI controller, which has a cutoff frequency of approximately 1.59 kHz, which is more than 12 times lower than the 20-kHz switching frequency. Note that, during the start-up, the control algorithm may generate the wrong control signal v_c, and to protect the system, the microcontroller must limit its value during this process.

D. Experimental Results

In Fig. 16, the drive signals (at low frequency) of switches S_1 and S_2 are shown, along with the synchronism signal. Note that, during the positive semicycle, these switches are controlled by means of a two-level PWM (as shown in details), while during the negative semicycle, they conduct continuously. In the same manner, Fig. 17 shows the drive signals of S_3 and S_4.

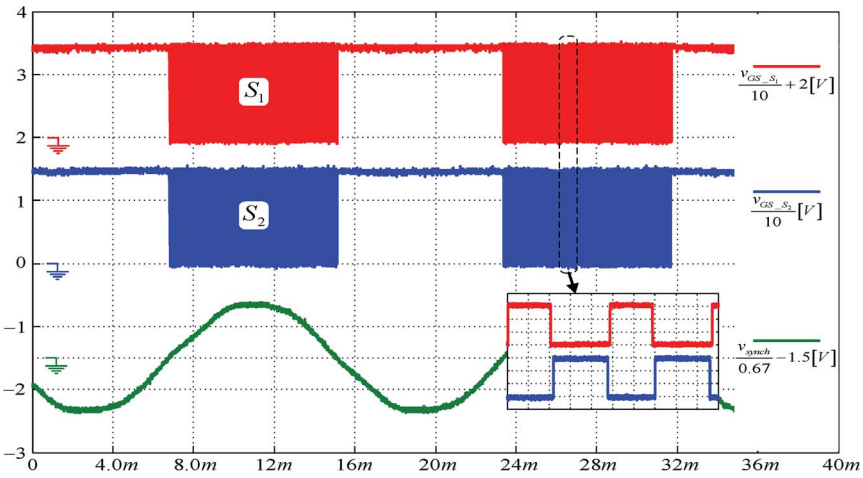


Fig. 16. Drive signals of switches S_1 and S_2.

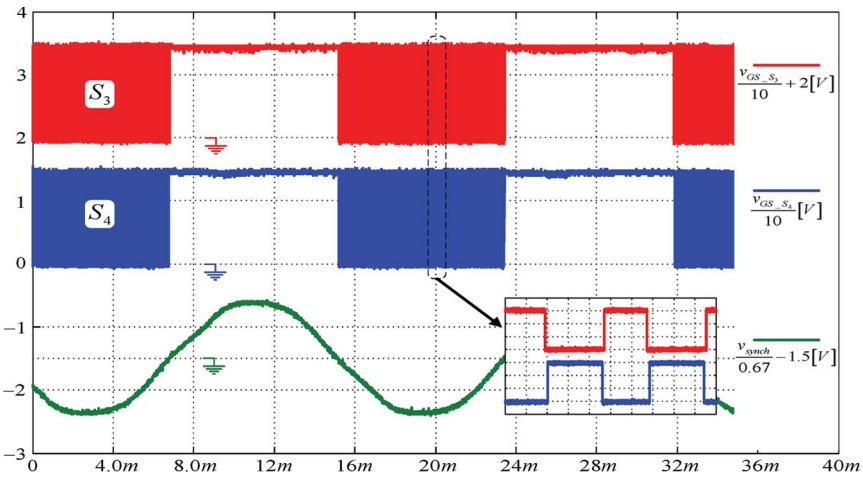


Fig. 17. Drive signals of switches S_3 and S_4.

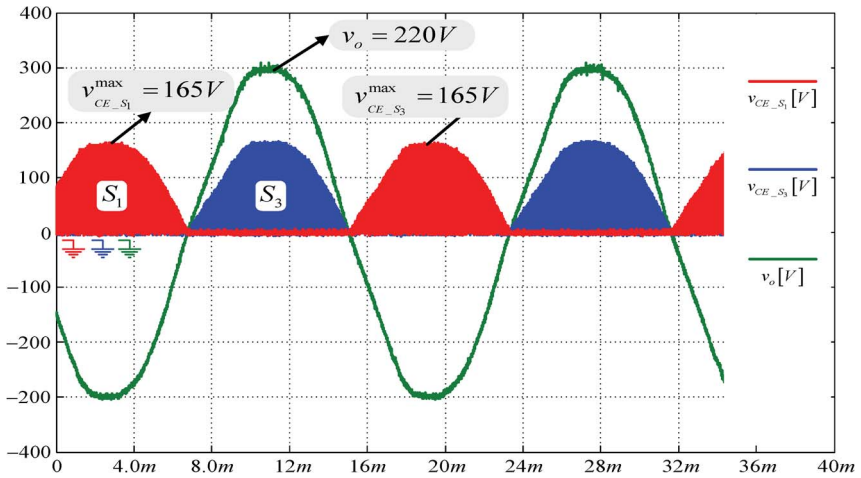


Fig. 18. Voltages across switches S_1 and S_3.

Fig. 18 shows the voltages across switches S_1 and S_3 without overvoltage, demonstrating the proper operation of the drive strategy used here. The input and output voltages are shown in Fig. 19; note that, for an input of -10%, the output voltage is being stabilized at 220 V, as desired. Fig. 20 shows the input and output voltages for a line voltage at 242 V, so the duty cycle is about 0.225.

Observing Figs. 16–20, it can be noticed that the control voltage is continuous during the whole line voltage period, which is a characteristic of direct ac-ac converters. As an example,

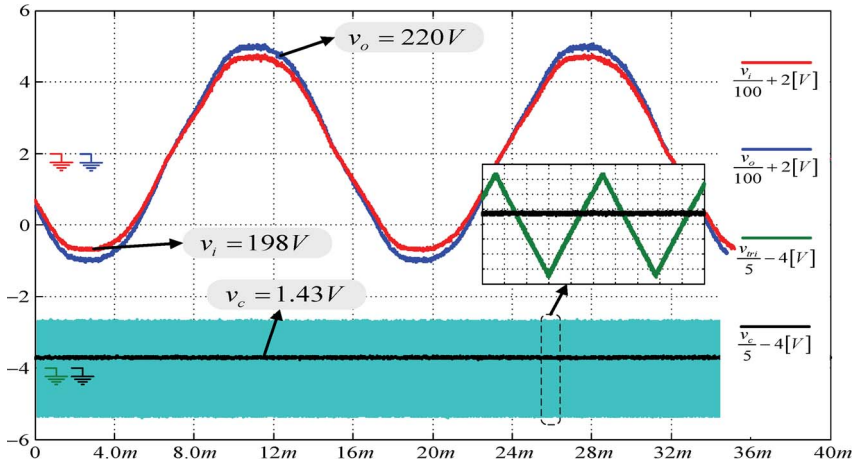


Fig. 19. Input and output voltages—($v_i = 0.9v_o, D = 0.613$).

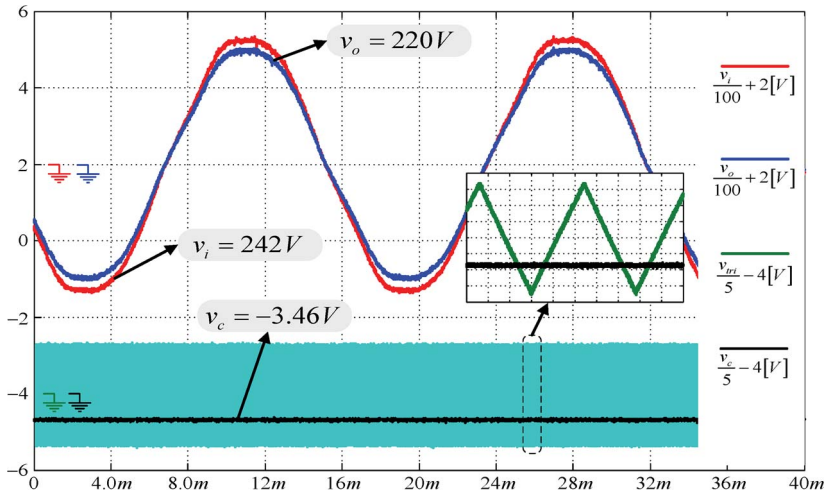


Fig. 20. Input and output voltages—($v_i = 1.1v_o, D = 0.225$).

for PWM inverters, the duty cycle varies in a sinusoidal shape, while for indirect ac-ac converters without dc link, variance occurs in a rectangular shape [2].

To evaluate the performance of the control technique during disturbances, three different tests were conducted: +20% step change in the input voltage, +50% step change in the loading, and operation with nonlinear load. These experimental results are shown in Fig. 21. Fig. 21(a) shows the results obtained with a +20% input voltage step change. As can be noted, the output voltage could be corrected to its reference value. For +50% load step, for which the results are shown in Fig. 21(b), one can observe that the system is practically insensitive to load variations. In fact, a small oscillation at the moment the load is changed can be noted; however, the control can quickly attenuate this disturbance, keeping the stability of the system.

The output voltage and the load current for operation with a nonlinear load are shown in Fig. 21(c). As one can observe, the orthogonal detection method does not allow correction of distortions in the output voltage, which is mainly caused by the voltage drop on the line impedance due to the high current peak circulation.

The prototype implemented in the laboratory is shown in Fig. 22. The power stage, drive circuits, control, and command circuitry can be seen there. Moreover, one can observe the two-secondary-winding transformer, the snubber capacitors, the output filter inductor, and capacitors.

VI. Conclusion

In this paper, several topologies for direct ac–ac converters permitting the use of commercial switch modules have been presented.

For all the basic converters (buck, full-bridge, half-bridge, and push–pull), we applied the proposed methodology, thus obtaining four converters which have the advantage of using commercial switch modules. These converters were used to implement a voltage restorer that can be supplied either on the line side or on the load side. In this way, eight voltage restorers were proposed. For all the converters, their characteristics are summarized in Table I, e.g., the static gain expressions, the transformer turns ratios, the current, and the voltage ripple across the converter output filter.

Furthermore, in Table II, a comparative evaluation of the studied voltage restorer concepts concerning implementation complexity and component efforts was presented. From these converter topologies, one was chosen for implementation as an experimental prototype.

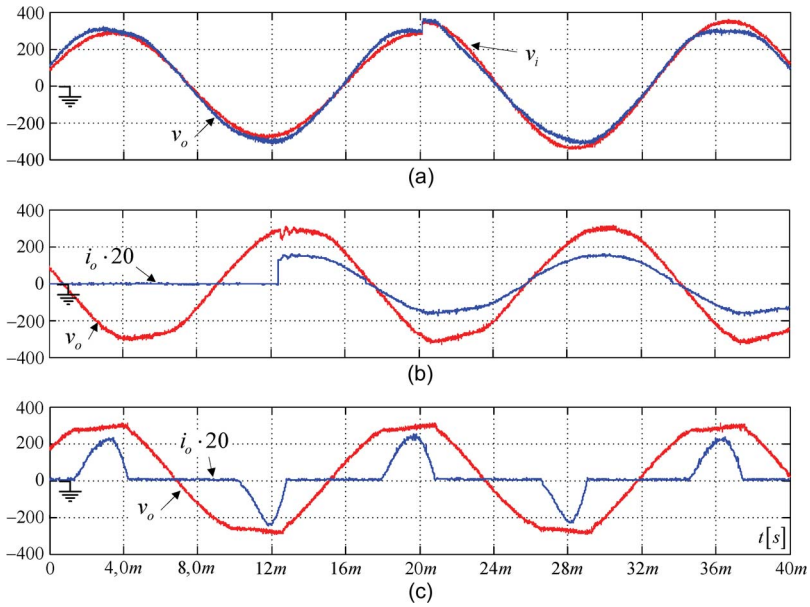


Fig. 21. Converter operations. (a) +20% step change in the input voltage. (b) +50% step change in the loading. (c) Operation with nonlinear load.

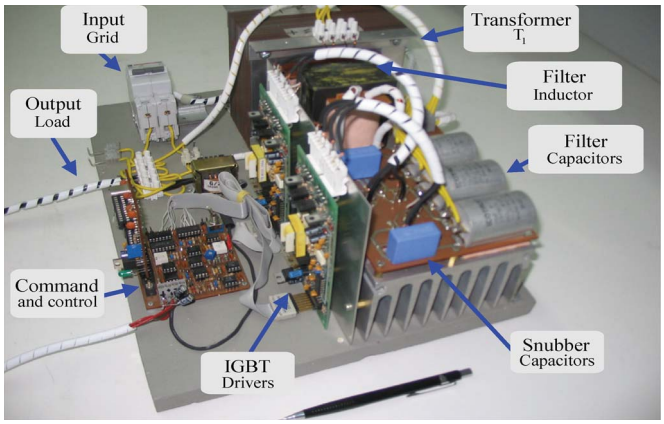


Fig. 22. Picture of the implemented voltage restorer prototype.

The experimental results of the half-bridge prototype are shown, demonstrating the proper operation of the drive strategy, as well as the orthogonal detection control.

The possibility of using commercial modules makes the studied topologies attractive for high-power applications, either as voltage restorers or harmonics, sags, and overvoltage compensators, among others.

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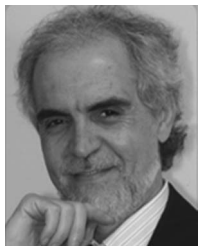

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