Power Electronic Systems
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Proceedings of the 26th Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2011), Ft. Worth, TX, USA, March 6–10, 2011.

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Towards a 99% Efficient Three-Phase Buck-Type PFC Rectifier for 400 V DC Distribution Systems

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***Abstract*— In telecom applications, the vision for a total power conversion efficiency from the mains to the output of PoL converters of 95% demands for an optimization of every conversion step, i.e. the PFC rectifier front-end should show an outstanding efficiency in the range of 99%. For recently discussed 400 V DC distribution bus voltages a buck-type PFC rectifier is a logical solution. In this paper, an efficiency-optimized, nearly 99% efficient, 5 kW three-phase buck-type PFC rectifier with 400 V output is presented. Methods for calculating losses of all components are described, and are used to optimize the converter design for efficiency at full load. Special attention is paid to semiconductor losses, which are shown to be dominant, with the parasitic device capacitance losses being a significant component. A prototype of the proposed rectifier is constructed which verifies the accuracy of the models used for loss calculation and optimization.**

I. INTRODUCTION

Three-phase PFC rectifier systems are frequently employed as active front-ends in utility interfaced systems such as power supplies in telecommunications and process technology. Broadly, two approaches to the design of these rectifiers are possible: a boost-type topology also known as a voltage source rectifier (VSR), or a buck-type topology also known as a current source rectifier (CSR). Compared to VSR topologies the CSRs provide a wide output voltage control range down to low voltages while maintaining PFC capability at the input, and allow for current limitation in case of an output short circuit [1]. Recent discussion on power distribution architectures for telecom and data centres has shown [2-3] the advantages that facility-wide 400 V DC distribution systems would have over traditional 48 – 54 V DC distribution architectures, especially when dealing with loads of tens to hundreds of kilowatts: lower load currents on the bus meaning less cables are required for transmission and/or the overall efficiency could be increased by 1 – 2%. A 400 V distribution architecture for telecom or data centre applications is shown in Fig. 1. For such a system a buck-type PFC rectifier is preferred since boost-type three-phase rectifiers produce an output voltage too high (typically 700–800 V) to directly feed a 400 V DC bus, necessitating a step-down DC/DC converter at their output. Usage of a buck-type PFC rectifier then allows potentially the removal of the DC/DC converter between the PFC and the distribution bus (cf. Fig. 1, if isolation at that point is not required), increasing efficiency and reducing costs. In order to achieve an overall efficiency from the mains to the chip (i.e. output of point-of-load converters) of 90 – 95% (whereas today it is typically below 80% [2]), all converter stages in the distribution system must be realized with highest possible efficiency – starting with 99% at the PFC rectifier stage. Currently commercially available three-phase rectifier systems with an isolated DC/DC output converter offer peak efficiencies ranging from 93% [4] for "true" three-phase systems to 97% [5] for systems built from three single-phase rectifier modules. Recent publications similarly report efficiencies of 94% for a "true" three-phase PFC rectifier [6], 95% for an unspecified design [7] and 97% for a modular three-phase PFC rectifier [8].

A different application of the buck-type PFC rectifier could be the charging of the battery of hybrid or electric vehicles (EVs), where a 400 V DC bus is a good approach [9] for the connection between the battery, motor and charger. Here again the use of a buck-type three-phase PFC rectifier operating from the 230 V mains would allow direct connection to the bus. If in either the telecom or EV application isolation of the PFC output from the bus is

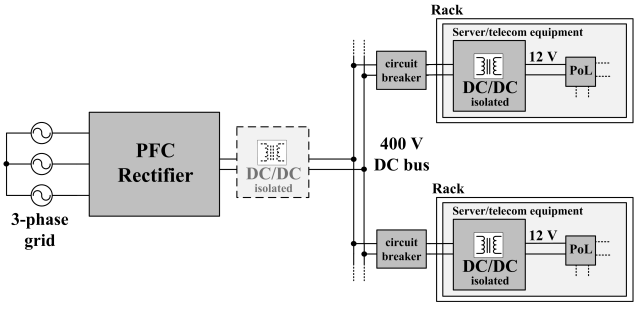


Figure 1 – Possible 400 V DC distribution architecture [2] for telecom and/or data centre applications. The DC/DC converter shown in light gray can be omitted if the PFC rectifier is buck-type (a CSR) with 400 V output and if no isolation is required.

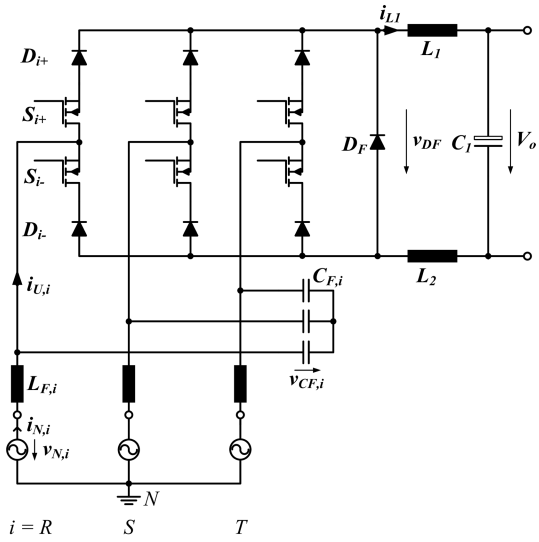


Figure 2 – Schematic of the three-phase buck-type PFC rectifier. The full EMI filter structure is shown in Fig. 9.

desired due to safety reasons, this can be accomplished with an isolated 400 V/400 V DC/DC converter (e.g. [10]) with very narrow voltage control range which could also be optimized for 99% efficiency using the approach presented in [11]. Other applications for the buck-type three-phase PFC rectifier where isolation at the output is not required include the power supplies of lamps or heaters [12] and inverters of variable speed AC drives [13].

In this paper, the design of a nearly 99% efficient, 5 kW, 400 V output, three-phase buck-type PFC rectifier is presented, optimized for nominal 230 V ±10% AC input phase voltage at 50 Hz and peak efficiency at full load. The topology of this CSR is presented in **Section II**. In **Section III** the methods for calculating losses of all the components, semiconductors and passives, are given along with a detailed loss breakdown for the converter by component type. Special attention is paid to all types of semiconductor losses, since many switches must be paralleled in order to achieve a high efficiency. **Section IV** presents the prototype with measurement results. An alternative implementation and conclusions are discussed in **Sections V** and **VI**, respectively.

II. Converter Topology

The converter topology of the PFC rectifier is given in Fig. 2. This topology and its derivation and principle of operation have been described previously in detail in [1, 14-16]. It is designed to provide the necessary 400 V DC output while guaranteeing sinusoidal input current and maintaining high efficiency. The topology presented here is slightly modified. Instead of IGBTs (cf. Fig. 1 in [16]) high-voltage MOSFETs are used as switches, due to their better switching performance and lower forward voltage when paralleled to increase efficiency. A line-to-line mains voltage amplitude of 566 V (for rated mains voltage) allows the realization of the converter with 900 V Si-MOSFETs and 1200 V SiC diodes. An EMI filter for the converter can be designed using the approach of [17]. Note also that the converter inductance is

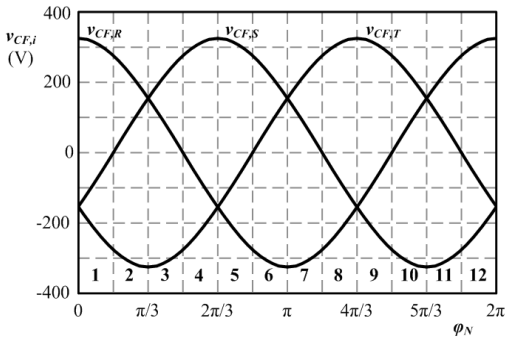


Figure 3 – Input capacitor voltages over one mains period, showing the division into 12 equal 30° sectors for the purpose of the SLO modulation scheme (see Fig. 4).

split evenly between the positive and negative output rail ($L = L_1 = L_2$) in order to provide symmetric attenuation impedances for conducted common mode noise currents.

A. Modulation Scheme

Modulation schemes for the topology of Fig. 2 have been developed [14-15] which guarantee minimum switching losses as well as minimum input filter capacitor voltage ripple and minimum DC current ripple. This was further improved in [1, 16] to eliminate sliding intersections of the input capacitor voltages and the resulting distortions. This results in the switching-loss optimized (SLO) modulation scheme which contains only a short interval t_d during which switch on-times overlap, where the duty ratios for the three bridge legs are set according to [1, 15-16]

$$\delta_i = \frac{V_{o,ref}}{\sum_{j=R,S,T} v_{CF,j}^2} \left| v_{CF,i} \right| \tag{1}$$

where $V_{o,ref}$ is the required rectifier output voltage and $i = R$, S, T. To apply (1), the input voltage mains period is divided into 12 equal 30°-wide sectors as shown in Fig. 3. The effective duty ratio $\delta_{eff,i}$ applied to each bridge leg is then calculated according to the present sector as shown in Table I. A switching sequence in Sector 1 is depicted in Fig. 4(a). The voltage generation can be characterized by the modulation index M [16]

$$M = \frac{2}{3} \frac{V_o}{\hat{V}_N} = \frac{\sqrt{2}}{3} \frac{V_o}{V_{N,RMS}} \tag{2}$$

ranging from 0 to 1, where V_N is the input phase voltage. The resulting waveform of the voltage across freewheeling diode D_F is shown in Fig. 4(b), showing that the SLO scheme results in the minimum possible voltage steps during state transitions for this circuit, therefore minimizing the switching losses.

The same duty ratio is applied always to both switches in a bridge leg (i.e. a single gate signal is connected to the gate drives of e.g. S_{R+} and S_{R-}). Accordingly, the half of the leg and the diode which conducts is determined by the input voltage conditions. Although this slightly decreases efficiency as the gates of all six MOSFETs are charged and

TABLE I. APPLIED DUTY RATIOS BY INPUT VOLTAGE SECTOR

Sector	$\delta_{eff,R}$	$\delta_{eff,S}$	$\delta_{eff,T}$
1, 7	δ_R	$1 - \delta_T + t_d$	δ_T
2, 8	δ_R	$1 - \delta_R + t_d$	δ_T
3, 9	$1 - \delta_S + t_d$	δ_S	δ_T
4, 10	$1 - \delta_T + t_d$	δ_S	δ_T
5, 11	δ_R	δ_S	$1 - \delta_R + t_d$
6, 12	δ_R	δ_S	$1 - \delta_S + t_d$

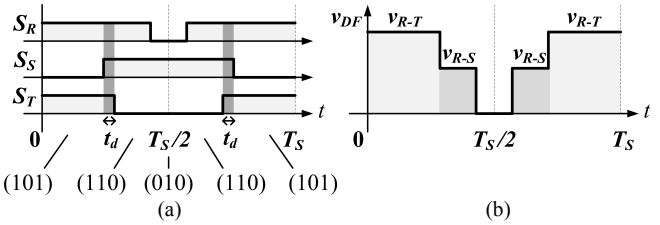


Figure 4 – SLO modulation scheme: (a) switching actions during a switching period T_S in Sector 1, showing overlapping time t_d and the switching states; (b) DC-link voltage during the switching states.

discharged while only three are active within one sector, it allows the use of only three gating signals and a simple software implementation of the control algorithm on a DSP.

III. CONVERTER DESIGN & LOSS CALCULATIONS

In order to achieve the highest possible efficiency, losses of all components must be calculated as precisely as possible and minimized during the design stage. The losses can be divided broadly into two categories: losses of the semiconductors, and losses of the passive components.

A. Semiconductor Losses

As the topology employs a large number of semiconductor devices, their losses are considered first and made the main focus of efficiency optimization for this converter. The RMS and average values of the series diode current I_{DS}, MOSFET current I_S, and freewheeling diode current I_{DF} can be calculated by (3)-(6) [1],

$$I_{DS,avg} = I_{S,avg} = \frac{\hat{I}_N}{\pi} \tag{3}$$

$$I_{DS,RMS} = I_{S,RMS} = \frac{\hat{I}_N}{\sqrt{M\pi}} \tag{4}$$

$$I_{DF,avg} = \left(\frac{1}{M} - \frac{3}{\pi}\right)\hat{I}_N \tag{5}$$

$$I_{DF,RMS} = \sqrt{\frac{1}{M^2} - \frac{3}{M\pi}}\,\hat{I}_N \tag{6}$$

where I_N is the input phase current. The total conduction losses in the converter $P_{c,S}$ and $P_{c,DS}$ of the MOSFETs and diodes, respectively are then

$$P_{c,S} = 6 \cdot I_{S,RMS}^2 \frac{R_{DSon}}{n_S} \tag{7}$$

$$P_{c,DS} = 6 \cdot \left(I_{DS,RMS}^2 \frac{R_D}{n_D} + I_{DS,avg} V_D\right) \tag{8}$$

where R_{DSon} is the MOSFET on-resistance, n_S the number of transistors paralleled for each switch S_i, R_D the diode on-resistance, n_D the number of devices paralleled for each diode D_i, and V_D the diode forward voltage. Equation (8) without the factor of 6 and with the corresponding currents is also used for the freewheeling diode conduction losses. To reduce conduction losses, each device (S_i, D_i, and D_F) is implemented with several MOSFETs or diodes in parallel. This however increases switching losses, especially that portion of switching losses occurring due to the parasitic output capacitances of the devices. Therefore, the transitions between the switching states in a pulse period (cf. Fig. 4) must be analyzed for all sectors (cf. Fig. 3) to determine where losses occur.

Fig. 5 shows the equivalent circuit of the transition from state (110) to (101) in Sector 1. The input voltage can be assumed constant during one switching cycle and represented with two voltage sources V_{R-S} and V_{S-T}. Sector 1 involves the switching of S_{R+}, S_{S-}, and S_{T-}. In the (110) to (101) transition, S_{T-} is turned on, then S_{S-} is turned off, and D_{S-} becomes reverse biased. Accordingly, S_{S-} is turned off at zero voltage and produces no switching losses. However losses occur at the turn-on of S_{T-} as its parasitic output capacitor is discharged due to being switched to zero from blocking voltage V_{S-T}. This also forces the blocking voltage V_{S-T} to occur across D_{S-} causing its capacitance to be charged from source V_{S-T}, producing a loss. Diode reverse recovery losses are avoided by using SiC diodes. Note also that while D_F and D_{R-} do not switch in this transition, the voltage across them changes from V_{R-S} to V_{R-T} partially charging their parasitic capacitors and therefore also causing a loss. Voltages across the remaining switches and diodes do not change for this transition.

During the transition, energy is dissipated in the MOSFET resistances, the resistance of the PCB traces, etc. Rather than analyzing exactly where the dissipation occurs, in a first step only the energy balance in the circuit is considered. In (9) and (10) the energy present in the circuit before and after the transition respectively is given. For the charging of the capacitors of D_F and D_{R-} the two sources are connected in series giving one source V_{R-T}. The energy exchanged with the sources is determined using the charge balance principle as shown in (11) and (12). The charge flow is considered positive if it flows from the source positive terminal. This hard-switched transition occurs too quickly to allow energy exchange with the converter output. The total energy loss $\Delta E_{(110)-(101)}$ occurring in this transition is then calculated by (13).

$$E_{(110)} = \frac{1}{2} C_{O,D_{R-}} V_{R-S}^{\ 2} + \frac{1}{2} C_{O,S_{T-}} V_{S-T}^{\ 2} + \frac{1}{2} C_{O,D_F} V_{R-S}^{\ 2} \tag{9}$$

$$E_{(101)} = \frac{1}{2} C_{O,D_{R-}} V_{R-T}^{\ 2} + \frac{1}{2} C_{O,D_{S-}} V_{S-T}^{\ 2} + \frac{1}{2} C_{O,D_F} V_{R-T}^{\ 2} \tag{10}$$

$$\Delta E_{V_{S-T}} = \Delta Q_{O,D_{S-}} V_{S-T} = C_{O,D_{S-}} V_{S-T}^{\ 2} \tag{11}$$

$$\begin{aligned} \Delta E_{V_{R-T}} &= \Delta Q_{O,D_{R-}} V_{R-T} + \Delta Q_{O,D_F} V_{R-T} \\ &= C_{O,D_{R-}} (V_{R-T} - V_{R-S}) V_{R-T} + C_{O,D_F} (V_{R-T} - V_{R-S}) V_{R-T} \end{aligned} \tag{12}$$

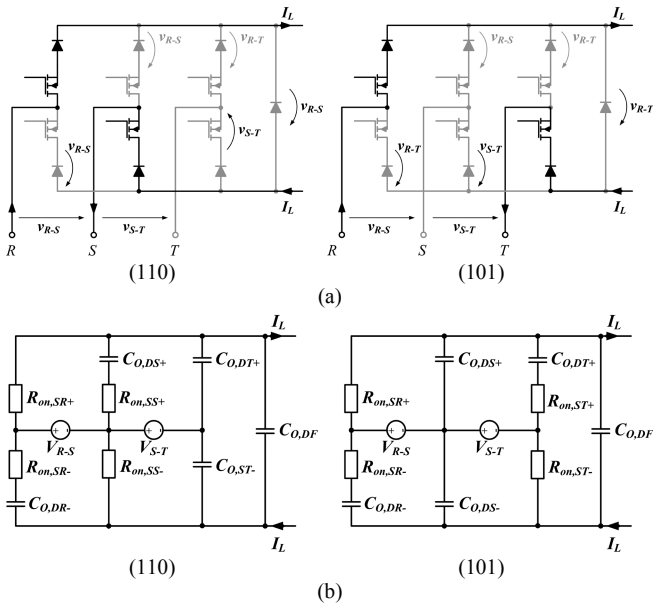


Figure 5 – (a) Current paths in states (110) and (101); (b) Equivalent circuit for states (110) and (101) showing parasitic output capacitances and MOSFET on-resistances; conducting diodes are neglected and replaced with a through-connection.

$$\begin{aligned}\Delta E_{(110)-(101)} &= E_{(110)} + \Delta E_{V_{S-T}} + \Delta E_{V_{R-T}} - E_{(101)} \\ &= \frac{1}{2} C_{O,S_{T-}} V_{S-T}{}^2 + \frac{1}{2} C_{O,D_{S-}} V_{S-T}{}^2 \\ &+ \frac{1}{2} C_{O,D_F} (V_{R-T} - V_{R-S})^2 + \frac{1}{2} C_{O,D_{R-}} (V_{R-T} - V_{R-S})^2\end{aligned} \tag{13}$$

For the reverse transition however, from (101) to (110), these switching losses do not occur. There, first S_{S-} is turned on at zero voltage, causing no losses, then S_{T-} is turned off. The inductor current I_L, taken as constant and initially flowing entirely through the *T*- branch, splits temporarily between four branches of the circuit, discharging $C_{O,DS-}$, partially discharging $C_{O,DR-}$ and $C_{O,DF}$, and charging $C_{O,ST-}$, until finally all of I_L is flowing through the *S*- branch. Due to the splitting of I_L to four branches, the losses which occur during this interval are lower than already accounted by the conduction loss calculations, in which the current flow is always taken to be via a single branch.

The remaining two transitions can be similarly analyzed: no switching losses occur at the transition from (110) to (010), while losses occur in the transition from (010) to (110) due to the discharging of $C_{O,SR+}$ (turn-on of S_{R+}), charging of $C_{O,DF}$ (due to blocking voltage V_{R-S} across D_F), charging of $C_{O,DS+}$ (blocking voltage changes from ~0 to V_{R-S}) and partial charging of $C_{O,DT+}$ (blocking voltage changes from V_{S-T} to V_{R-T}). Total capacitive energy loss in one switching cycle in Sector 1 is therefore given by

$$\begin{aligned}E_{Sec1} &= \frac{1}{2} C_{O,S_{R+}} V_{R-S}{}^2 + \frac{1}{2} C_{O,S_{T-}} V_{S-T}{}^2 + \frac{1}{2} C_{O,D_F} V_{R-S}{}^2 + \frac{1}{2} C_{O,D_{S-}} V_{S-T}{}^2 \\ &+ \frac{1}{2} C_{O,D_F} V_{S-T}{}^2 + \frac{1}{2} C_{O,D_{R-}} V_{S-T}{}^2 + \frac{1}{2} C_{O,D_{S+}} V_{R-S}{}^2 + \frac{1}{2} C_{O,D_{T+}} V_{R-S}{}^2 .\end{aligned} \tag{14}$$

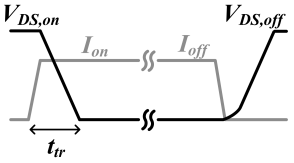


Figure 6 – MOSFET switching behaviour. For turn-off, as C_{oss} is very high at low voltage, I_L charges this parasitic output capacitor, giving a behaviour different from the turn-on transition and causing no losses.

The parasitic output capacitance of the diodes and switches is non-linear and voltage-dependent and is given in datasheets as the differential output capacitance $C_{oss}(v)$. For many switching devices, the $C_{oss}(v)$ characteristic becomes flat or nearly flat above a certain V_{DS}. If the blocking voltage is always or most of the time above this value, the output capacitor of a device can be approximated by a constant value equal to the flat portion of its $C_{oss}(v)$ curve. Over the entire sector the voltages are not constant but a function of angle φ_N (cf. Fig. 3). Inserting $v_{R-S}(\varphi_N)$ and $v_{S-T}(\varphi_N)$ for the appropriate voltage terms in (14) and averaging i.e. integrating the total losses in Sector 1 over 30° gives the total power loss due to the parasitic device output capacitances, since all 12 sectors are symmetric in terms of switching behavior and voltages. This total power loss $P_{Co,tot}$ is then approximated by

$$P_{Co,tot} \approx \frac{6}{\pi} \hat{V}_N{}^2 \left(\frac{1}{2} n_S C_{O,S} + \frac{3}{2} n_D C_{O,D} \right) \left(\frac{14\pi - 9\sqrt{3}}{32} \right) f_{sw}. \tag{15}$$

For some semiconductor devices, the $C_{oss}(v)$ characteristic does not lend itself to this approximation, e.g. rather than stabilizing, C_{oss} always sharply decreases with increasing voltage. In this case the energy $E_{Co}(V)$ stored in the output capacitor of a device at a voltage V must be calculated by [18]

$$E_{Co}(V) = \int_0^V v \cdot C_{oss}(v) dv. \tag{16}$$

Eqn. (14) must then be rewritten in terms of parasitic output capacitor energies as

$$\begin{aligned}E_{Sec1} &= E_{Co,S_{R+}}(V_{R-S}) + E_{Co,S_{T-}}(V_{S-T}) + E_{Co,D_F}(V_{R-S}) + E_{Co,D_{S-}}(V_{S-T}) \\ &+ E_{Co,D_F}(V_{S-T}) + E_{Co,D_{R-}}(V_{S-T}) + E_{Co,D_{S+}}(V_{R-S}) + E_{Co,D_{T+}}(V_{R-S}).\end{aligned} \tag{17}$$

Some datasheets give also explicitly an $E_{Co}(v)$ curve. Therefore in this case a polynomial fit for either curve is calculated. Accounting for the dependence of the voltage on φ_N, the total power loss $P_{Co,tot}$ due to parasitic device output capacitances is calculated by

$$\begin{aligned}P_{Co,tot} = f_{sw} \frac{6}{\pi} \Bigg[& n_S \left(\int_0^{\pi/6} E_{Co,S}(v_{R-S}(\varphi_N)) d\phi_N + \int_0^{\pi/6} E_{Co,S}(v_{S-T}(\varphi_N)) d\phi_N \right) \\ & + n_D \left(3 \int_0^{\pi/6} E_{Co,D}(v_{R-S}(\varphi_N)) d\phi_N + 3 \int_0^{\pi/6} E_{Co,D}(v_{S-T}(\varphi_N)) d\phi_N \right) \Bigg]\end{aligned} \tag{18}$$

where $E_{Co,S}$ is the energy in the parasitic switch capacitors, and $E_{Co,D}$ the energy in the parasitic diode capacitors. Additionally, switching losses P_{on} occur in the MOSFETs due to the gate-drain and gate-source capacitance causing a finite transition time t_{tr} at turn-on. This behavior is

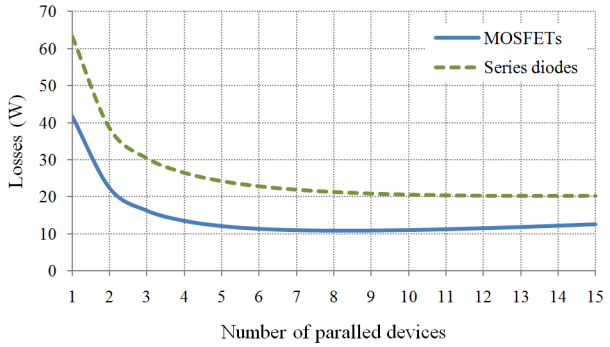


Figure 7 – Total losses of switches S_i and series diodes D_i depending on the number of devices in parallel to construct each. For e.g. $n_S = 7$, $n_D = 4$, total losses are 11 W + 26.5 W = 37.5 W.

approximated by the waveforms shown in Fig. 6. The power loss can then be approximated by

$$P_{on} = \frac{V_{DS,on} \cdot I_{on}}{2} \cdot t_{tr,on} \cdot f_{sw}. \tag{19}$$

Knowing the voltages from the previous analysis and that in this case $I_{on} = I_L/n_S$, the total P_{on} losses in the system can be calculated as

$$P_{on,tot} = \frac{6}{\pi} \hat{V}_N \frac{\sqrt{3}}{4} I_L t_{tr} f_{sw} \tag{20}$$

where I_L is the DC inductor (output) current.

Optimization of the Number of Paralleled Semiconductors

With these loss components defined, it is possible to vary n_D and n_S to find an optimum number of devices to place in parallel for each switch and diode in Fig. 2. Superjunction power MOSFETs with 900 V blocking capability (IPW90R120C3 from Infineon) were chosen for the implementation, with $t_{tr} = 20$ ns (determined from measurements) and a $C_{oss}(v)$ characteristic requiring the use of (18) to calculate losses. The diodes chosen were SiC 1200 V C2D10120A from Cree. A switching frequency of $f_{sw} = 18$ kHz at the edge of audible range was chosen to keep switching losses low. Fig. 7 shows the total losses for the MOSFETs and series diodes for different numbers of devices used in parallel for each switch. The minimum losses occur with $n_S = 8$ and $n_D = 14$, however as can be seen the curves are nearly flat for $6 \le n_S \le 11$ and $7 \le n_D \le 15$. The losses saved by going from 6 MOSFETs in parallel to 8 are not even 1 W. Setting $n_D = 14$ would be too costly and therefore for the implementation $n_S = n_D = 6$ was set in order to save costs. Fig. 8 gives a breakdown of the total semiconductor losses in the converter. Out of a total 38 W of losses, diode conduction losses are dominant with 21.2 W. Also note that the capacitive losses of the MOSFETs alone are larger than half the conduction losses and that for the MOSFETs the switching losses in total are almost equal to the conduction losses. This underlines the need to consider the switching, and in particular capacitive, losses carefully.

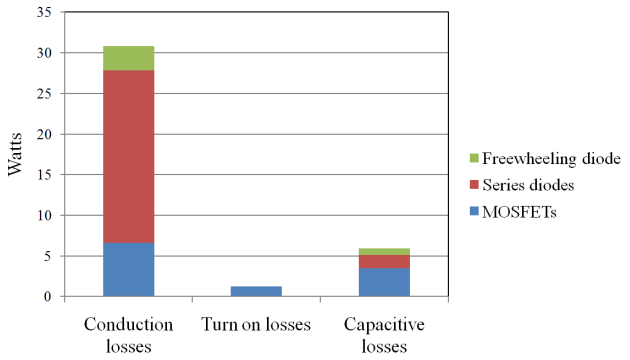


Figure 8 – Breakdown of total semiconductor losses by component and by loss type.

B. *Losses of the Output Inductors*

Inductor losses can be divided into three groups: losses due to DC winding resistance, core losses, and high-frequency (HF) losses due to skin and proximity effect. The configuration chosen for output inductors $L = L_1 = L_2$ consists of three pairs of ferrite E-cores wound with solid rectangular wire (cf. Fig. 11(b)). The inductor DC resistance $R_{L,DC}$ is therefore

$$R_{L,DC} = \frac{\rho N l_T}{A_w} \tag{21}$$

where N is the number of turns, l_T the average length of a turn, A_w the wire cross-sectional area and ρ its resistivity. The core losses can be calculated using the modified Steinmetz equation [19]. The losses P_{core} for the triangular current (switching ripple) present in L_1 and L_2 are

$$P_{core} = k \cdot f_{sw} \cdot \left(\frac{2}{\pi^2} \cdot 4 f_{sw} \right)^{\alpha - 1} \cdot \hat{B}^{\beta} \cdot V_{core} \tag{22}$$

where k, α, and β are Steinmetz parameters, given or extractable from core material datasheets, V_{core} the total core volume, and $\hat{B}$ the peak magnetic flux density, which can be calculated by

$$\hat{B} = \frac{L \cdot (I_L + 0.5 \cdot \Delta I_L)}{N \cdot A_e} \tag{23}$$

where I_L is the average inductor current, ΔI_L the inductor current ripple and A_e the inductor core cross-sectional area. For the HF losses, the rectangular wire used can be approximated closely as a conductor with a square cross section and the AC winding resistance $R_{L,AC,n}$ due to skin and proximity effect resulting from the nth harmonic of the inductor current ripple can be calculated using the Ferreira method [20]

$$R_{L,AC,n} = R_{L,DC} \frac{\xi(\eta)}{2} \frac{\sinh \xi(\eta) + \sin \xi(\eta)}{\cosh \xi(\eta) - \cos \xi(\eta)} + \sum_{m=1}^{m_{tot}} \frac{R_{L,DC}}{m_{tot}} \frac{\xi(\eta)}{2} \eta^2 (2m-1) \frac{\sinh \xi(\eta) - \sin \xi(\eta)}{\cosh \xi(\eta) + \cos \xi(\eta)} \tag{24}$$

for an inductor with m_{tot} layers of windings with porosity factor η and skin depth related term $\xi(\eta)$,

$$\eta = \frac{a N_m}{b} \tag{25}$$

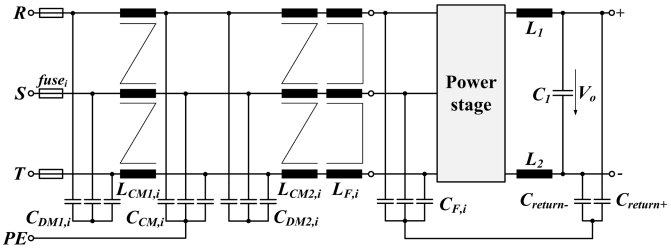


Figure 9 – EMI filtering concept and topology of the input filter.

$$\xi(\eta) = \sqrt{A_w \pi \mu_0 \sigma n f_{sw} \eta} \tag{26}$$

where a is the side length of the square conductor, b the width of a layer, N_m the number of turns in a layer, and σ the conductivity of the wire. Taking into account inductor current harmonics [11], the total losses $P_{L,tot}$ for a DC choke with triangular current then are

$$P_{L,tot} = I_L^2 \cdot R_{L,DC} + \sum_{n=1}^{n_{tot}} \frac{\Delta I_{L,n}^2}{3} R_{L,AC,n} + P_{core} \tag{27}$$

where $\Delta I_{L,n}$ is the amplitude of the nth harmonic. Knowing that at full load I_L = 12.5 A and selecting an inductor current peak-to-peak ripple of 25%, the inductance value $L_1 = L_2$ = 650 µH is obtained (for details see [1]). Using Ferroxcube E64 3C91 cores with N = 18, copper wire with A_w = 8.6 mm^2 and assuming an inductor temperature of 50°C, the total DC losses for the chokes L_1 and L_2 given by (21) are 5.7 W, and the total HF losses given by (27) are approximately 0.9 W. Core losses calculated by (22) do not take into account DC magnetic bias, which has been shown in [21] to have a non-negligible influence. Therefore, for higher accuracy the core losses were measured and confirmed to be approx. 0.5 W.

C. Losses of Output Capacitor

Losses in the capacitors are caused by their equivalent series resistance (ESR) and by leakage current. The ESR value is given in capacitor datasheets or can be calculated using the loss factor tan(δ) also given in datasheets as [11]

$$\mathrm{ESR} = \frac{\tan(\delta)}{2\pi f_{sw} C} \tag{28}$$

where C is the capacitance of the capacitor in question. The leakage current I_{leak} is determined using characteristic equations given in the capacitor datasheet. The total power losses P_C of a capacitor can then be calculated by

$$P_C = I_{C,RMS}^2 \cdot \mathrm{ESR} + I_{leak} \cdot V_C \tag{29}$$

where $I_{C,RMS}$ is the RMS current through the capacitor and V_C the average capacitor voltage. The output capacitor was selected to be C_1 = 376 µF (for selection criteria see [1]) and implemented with 8 parallel 47 µF KXJ capacitors from Nippon-Chemicon. As $V_C = V_O$ = 400 V, losses due to leakage current are about 1.3 W. With the paralleling of these low-ESR capacitors and with $I_{C,RMS}$ = 0.9 A, resistive losses of the output capacitors were found to be negligible.

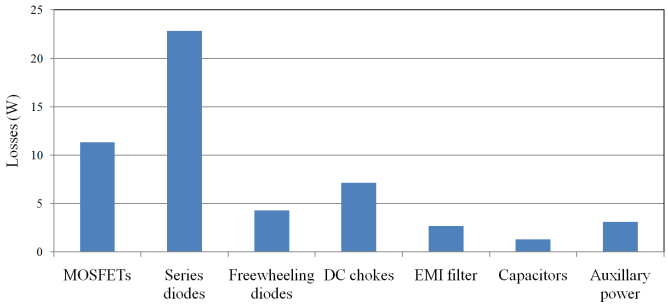


Figure 10 – Summary of loss components.

D. Other Losses

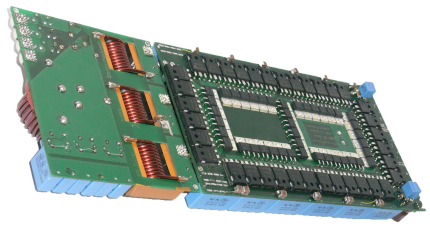
In order to make the rectifier prototype compliant to existing EMI norms, the EMI input filter depicted in Fig. 9 is used. From circuit simulations of the rectifier system, the expected differential mode (DM) and common mode (CM) noise was calculated as well as the necessary attenuation based on the limits for CISPR Class B. Following the approach of [17] the EMI filter was designed with C_{return} = 200 nF, $C_{F,i}$ = 13.2 µF, $C_{CM,i} = C_{DM1,i}$ = 4.7 nF, $C_{DM2,i}$ = 2 µF, $L_{F,i}$ = 50 µH, L_{CM1} = 900 µH and L_{CM2} = 800 µH. EPCOS film capacitors having a negligible leakage current were used producing 0.7 W of losses due to ESR. Each $L_{F,i}$ was implemented with a pair of EPCOS ETD49 cores with 10 turns of solid copper wire, a Vacuumschmelze VAC6123X240 CM choke was used for L_{CM2} and L_{CM1} was implemented with 3 8-turn windings around a Vacuumschmelze VAC 500F core. This gave in total 2 W of losses due to the DC resistance, with HF and core losses in the milliwatt range.

An auxiliary power supply – a flyback converter – was built to power the TI TMS320F2808 DSP system used for the control and the gate drives. This supply was also analyzed and found to operate at an efficiency of 77.6% consuming a total of 3.1 W.

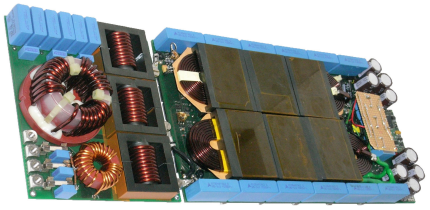
Finally, the FR-4 PCB material sandwiched between copper layers, i.e. the relatively wide tracks for the positive and negative rail of the converter, is considered, which creates essentially a plate capacitor in parallel to D_F, charged and discharged in the same manner as the capacitance of D_F. This adds another 0.5 W of losses. As will be seen in Section IV, no heat sink or fan is needed to cool the system and therefore any losses due to a cooling fan are avoided.

E. Total Losses

Total losses calculated for the converter were 52.7 W, giving an efficiency of 98.96%. A breakdown of the total losses is depicted in Fig. 10. As can be seen, semiconductor losses dominate and account for over 70% of the total. Clearly, for the CSR topology examined in this paper semiconductor technology is the most significant barrier to achieving 99% efficiency. While significant effort can be expended for example to optimize inductors for efficiency [11], in this case an improvement in the efficiency of semiconductors – either through decreased R_{DSon} or C_{oss} i.e.



(a)



(b)

Figure 11 – Constructed prototype of the converter (right) and EMI filter on separate board (left): a) top view b) bottom view. The power stage measures 283 x 155 x 31 mm^3 and the EMI filter board 135 x 155 x 42 mm^3 resulting in a total power density of 2.2 kW/dm^3.

an improved Figure of Merit – would be the only practical way to further significantly decrease losses.

IV. Experimental Results

A prototype of the proposed CSR design was constructed with the EMI filter implemented on a separate board. The prototype is shown in Fig. 11. In total 36 CoolMOS and 42 SiC diodes are mounted concentric on the top of the converter minimizing commutation inductances. The DC choke and output capacitors are mounted on the bottom of the converter. Thermal camera measurements after 30 minutes of operation at full load showed a maximum temperature of 71.7°C which confirms that the operation without heat sink is unproblematic and temperature is uniformly distributed across the semiconductors. The inductors reach 51.5°C. Fig. 12 shows the achieved sinusoidal input currents. EMI measurements were also performed (Fig. 13) confirming that the converter fulfils CISPR 22 Class B.

Electrical efficiency measurements, performed with an AC power analyzer (with an accuracy of 0.2%) at the converter input and a multimeter measuring converter output voltage and current (accuracy 0.05%) are given in Fig. 14(a). As can be seen, with 230 V nominal input voltage and at full load, an efficiency of 98.8% was measured, giving good agreement with the calculations in Section III. The difference between the calculation according to the models in Section III and the electrical efficiency measurement is about 8 W or 15%. Also it can be noted that across the whole load range and at a variety of input voltages a high efficiency of over 97% is always maintained. Furthermore, a calorimetric measurement using a precision calorimeter with an accuracy of ± 2 W [22] with the converter operating at full and 50% load for several hours was also performed. The results are summarized in Table II, showing a good agreement between the calorimetric and electrical measurement and once more

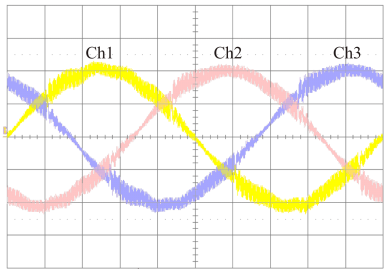


Figure 12 – Input currents $i_{N,R}$ (Ch1), $i_{N,S}$ (Ch2) and $i_{N,T}$ (Ch3) of the rectifier for rated load (P_O = 5 kW) and for input voltage $V_{N,RMS}$ = 230 V. Scale: 5 A/div; timescale: 2 ms/div.

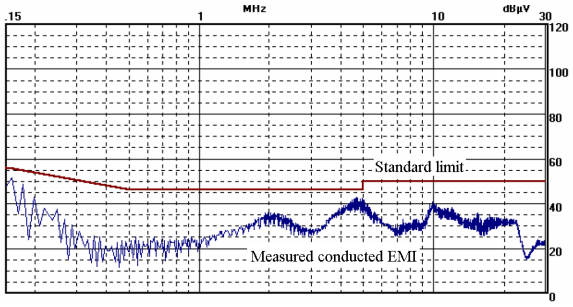
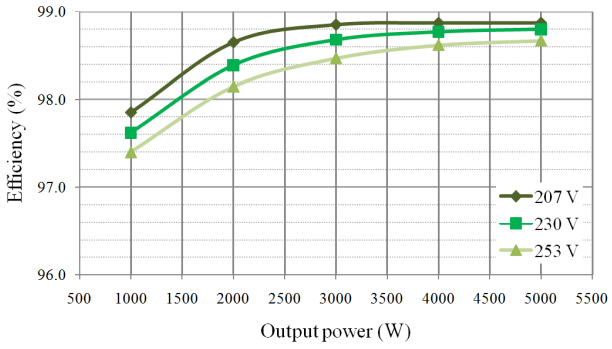
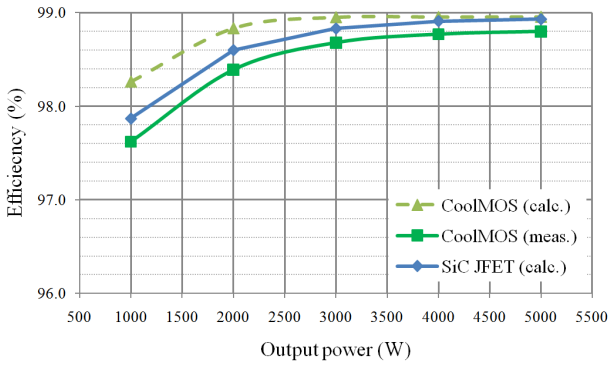


Figure 13 – EMI measurements of the converter using an average detector showing the CISPR Class B standard limit (red) and conducted EMI (blue).



(a)



(b)

Figure 14 – (a) Electrical measurements of converter efficiency at different loads and nominal input voltages. (b) Calculated efficiencies for a CSR where the MOSFETs are replaced with 1200 V SiC JFETs compared to the CoolMOS CSR for 230 V nominal input.

TABLE II. COMPARISON OF EFFICIENCY MEASUREMENTS

Measurement	Electrical	Calorimetric
Losses, 100% load	60.7 W	61.6 W
Efficiency, 100% load	98.80%	98.78%
Losses, 50% load	36.0 W	35.5 W
Efficiency, 50% load	98.58%	98.60%

validating the methods of Section III. The lower efficiency at low loads can be partly explained by the significant voltage-dependent loss components which are constant over the load range, i.e. the losses due to the parasitic capacitors.

V. ALTERNATIVE IMPLEMENTATION

In order to achieve a higher blocking voltage of the switches, one possibility is to replace the MOSFETs in the converter with 1200 V SiC JFETs from SiCED (R_{DSon} = 80 mΩ at a junction temperature of 25°C). A preliminary investigation was carried out where the losses of the CoolMOS calculated in Section III were replaced by the losses that SiC JFETs would have under the same operating conditions. Four JFETs, the optimal configuration for efficiency, were used in parallel for each switch, with the rest of the circuit unchanged i.e. n_D = 6, and the losses were calculated based on a characterization from earlier experimental conduction and switching loss measurements. The results are shown in Fig. 14(b). According to calculations an efficiency of 98.9% would be achieved at full load and f_{sw} = 18 kHz making an all SiC CSR a viable design that will be explored in future publications.

VI. CONCLUSIONS

A three-phase buck-type PFC rectifier was presented with 98.8% efficiency suitable for 400 V DC distribution systems. Models for calculating losses of all components were discussed and verified by experimental measurement of the converter's efficiency. The dominance of semiconductor losses indicates that the achieved efficiency is a limit for the presented topology obtainable with currently commercially available power semiconductors, and that further improvements in semiconductor components are the key to reaching the 99% efficiency target.

ACKNOWLEDGEMENTS

The authors would like to thank D. Christen for performing the calorimetric converter loss measurements and Dr. G. Deboy of Infineon Technologies for providing CoolMOS power transistors samples for research on ultra-high efficiency converter systems.

REFERENCES

[1] T. Nussbaumer, M. Baumann, J. W. Kolar, "Comprehensive Design of a Three-Phase Three-Switch Buck-Type PWM Rectifier," *IEEE Trans. on Power Electronics*, Vol. 22, No. 2, March 2007, pp. 551 - 562.

[2] A. Pratt, P. Kumar, T. V. Aldridge, "Evaluation of 400V DC Distribution in Telco and Data Centers to Improve Energy Efficiency," *Proc. 29th International Telecommunications Energy Conf. (INTELEC 2007)*, Rome, Italy, Oct. 2007, pp. 32-39.

[3] A. Matsumoto, A. Fukui, T. Takeda, K. Hirose, M. Yamasaki, "Development of 400 Vdc Power Distribution System and 400 Vdc Output Rectifier," *Proc. 31st International Telecommunications Energy Conf. (INTELEC 2009)*, Incheon, Korea, Oct. 2009, pp.1-5.

[4] "R48-11600 NetSure™ Rectifier," *Emerson Power NetSure™ 802 DC Power System* [Online document] (cited Nov. 3, 2010) Available at: http://tinyurl.com/25eqy67

[5] "3-phase WW (World Wide) PFC + DC/DC," *Fuji Electric Hot Topics: WWPFC* [Online document] (cited Nov. 3, 2010) Available at: http://www.fujielectric.com/fecoa/ps/topics/index.html

[6] J. Ying, B. Lu, J. Zeng, "High Efficiency 3-phase Input Quasi-Single-Stage PFC-DC/DC Converter," *Proc. 32nd IEEE Power Electronics Specialists Conf. (PESC 2001)*, Vancouver, Canada, Jun. 2001, Vol. 4, pp. 1785-1789.

[7] A. Fukui, T. Takeda, K. Hirose, M. Yamasaki, "HVDC Power Distribution Systems for Telecom Sites and Data Centres," *Proc. 2010 International Power Electronics Conf. (IPEC 2010)* Sapporo, Japan, Jun. 2010, pp. 874-880.

[8] J. Tan, Y. Li, Z. Jiang, L. Cai, J. Ying, "A Novel Three-Phase Three-Level Power Factor Correction (PFC) Converter Using Two Single-Phase PFC Modules," *Proc. 38th IEEE Power Electronics Specialists Conf. (PESC 2007)*, Orlando, USA, Jun. 2007, pp. 3060-3064.

[9] A. Emadi, S. S.Williamson, A. Khaligh, "Power Electronics Intensive Solutions for Advanced Electric, Hybrid Electric, and Fuel Cell Vehicular Power Systems," *IEEE Trans. on Power Electronics*, Vol. 21, No. 3, May 2006, pp. 567-577.

[10] R. Simanjorang, H. Yamaguchi, H. Ohashi, T. Takeda, M. Yamazaki, H. Murai, "A High Output Power Density 400/400 V Isolated DC/DC Converter with Hybrid Pair of SJ-MOSFET and SiC-SBD for Power Supply of Data Center," *Proc. 25th IEEE Applied Power Electronics Conf. and Expo. (APEC 2010)*, Palm Springs, USA, Feb. 2010, pp. 648-653.

[11] U. Badstuebner, J. Biela, J. W. Kolar, "Design of an 99%-efficient, Phase-Shift PWM DC-DC Converter for Telecom Applications," *Proc. 25th IEEE Applied Power Electronics Conf. and Expo. (APEC 2010)*, Palm Springs, USA, Feb. 2010, pp. 773-780.

[12] Y. Nishida, J. Miniboeck, S. D. Round, J. W. Kolar, "A New 3-phase Buck-Boost Unity Power Factor Rectifier with Two Independently Controlled DC Outputs," *Proc. 22nd IEEE Applied Power Electronics Conf. and Expo. (APEC 2007)*, Anaheim, USA, Feb. 2007, pp. 172-178.

[13] M. Baumman, F. Stögerer, J. W. Kolar, A. Lindemann, "Design of a Novel Multi-Chip Power Module for a Three-Phase Buck+Boost Unity Power Factor Utility Interface Supplying the Variable Voltage DC Link of a Square-Wave Inverter Drive," *Proc. 16th IEEE Applied Power Electronics Conf. and Expo. (APEC 2001)*, Anaheim, USA, Mar. 2001, Vol. 2, pp. 820-827.

[14] M. Baumman, U. Drofenik, J. W. Kolar, "New Wide Input Voltage Range Three-Phase Unity Power Factor Rectifier Formed by Integration of a Three-Switch Buck-Derived Front-End and a DC/DC Boost Convereter Output Stage," *Proc. 22nd International Telecommunications Energy Conf. (INTELEC 2000)*, Phoenix, USA, Sept. 2000, pp. 461-470.

[15] M. Baumann, J.W. Kolar, "Comparative Evaluation of Modulation Methods for a Three-Phase / Switch Buck Power Factor Corrector Concerning the Input Capacitor Voltage Ripple," *Proc. 32nd IEEE Power Electronics Specialists Conf. (PESC 2001)*, Vancouver, Canada, Jun. 2001, Vol. 3, pp. 1327 - 1333.

[16] T. Nussbaumer, J. W. Kolar, "Advanced Modulation Scheme for Three-Phase Three-Switch Buck-Type PWM Rectifier Preventing Mains Current Distortion Originating from Sliding Input Filter Capacitor Voltage Intersections," *Proc. 34th IEEE Power Electronics Specialists Conf. (PESC 2003)*, Acapulco, Mexico, June 2003, Vol. 3, pp. 1086 – 1091.

[17] T. Nussbaumer, M. L. Heldwein, J. W. Kolar, "Common Mode EMC Input Filter Design for a Three-Phase Buck-Type PWM Rectifier System," *Proc. 21st IEEE Applied Power Electronics Conf. and Expo. (APEC 2006)*, Dallas, March 2006, Vol. 3, pp. 1617 - 1623.

[18] U. Drofenik, A. Muesing, J. W. Kolar, "Voltage-Dependent Capacitors in Power Electronics Multi-Domain Simulations," *Proc. 2010 International Power Electronics Conference (IPEC 2010)*, Sapporo, Japan, Jun. 2010, pp. 643-650.

[19] J. Reinert, A. Brockmeyer, R. W. A. A. De Doncker, "Calculation of Losses in Ferro- and Ferrimagnetic Materials Based on the Modified Steinmetz Equation," *IEEE Trans. on Industry Applications*, Vol. 37, No. 4, July/August 2001, pp. 1055-1061.

[20] A. Reatti, M. K. Kazimierczuk, "Comparison of Various Methods for Calculating the AC Resistance of Inductors," *IEEE Trans. on Magnetics*, Vol. 38, No. 3, May 2002, pp. 1512-1518.

[21] J. Mühlethaler, J. Biela, J. W. Kolar, A. Ecklebe, "Core Losses under DC Bias Condition based on Steinmetz Parameters," *Proc. 2010 International Power Electronics Conf. (IPEC 2010)*, Sapporo, Japan, Jun. 2010, pp. 2430-2437.

[22] D. Christen, U. Badstuebner, J. Biela, J. W. Kolar, " Calorimetric Power Loss Measurement for Highly Efficient Converters," *Proc. 2010 International Power Electronics Conf. (IPEC 2010)*, Sapporo, Japan, June 2010, pp 1438-1445.