Closed-Loop Sinusoidal Input-Current Shaping of 12-Pulse Autotransformer Rectifier Unit With Impressed Output Voltage

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Abstract—This paper presents a novel closed-loop current-control strategy for a hybrid 12-pulse rectifier that uses a two-switch boost stage for output-voltage regulation. Unlike previous attempts to mitigate input-current distortion, e.g., by modulating the rectifier output voltage with open-loop control, this new closed-loop current-control scheme directly controls the line-interphase-transformer input voltage and/or impresses sinusoidal input currents. In this paper, the control strategy is explained and the modulation functions for each $(\pi/6)$-wide mains voltage sector are derived. The hardware implementation is described, and experimental results demonstrate that the control strategy ensures a high-quality input current for ideal as well as for distorted/unbalanced mains.

Index Terms—12-pulse rectifier, closed-loop current control, space-vector modulation.

I. INTRODUCTION

FOR the coupling of drive systems to the three-phase on-board mains of future More-Electric Aircraft (MEA) rectifier systems of high-input-current quality are required in order to avoid a distortion of the mains voltage or a disturbance of sensitive flight-control equipment. Their passive systems with higher pulse number or active systems, i.e., pulsewidth modulation (PWM) rectifiers with regulated input current can be employed. Remarkably, due to the high mains frequency in the range of 360–800 Hz, the missing electromagnetic interference (EMI) filter, and the low cooling effort and/or high efficiency, 12-pulse diode-rectifier units without galvanic isolation, i.e., with mains-side phase-shift autotransformers (also denominated as mains-side line interphase transformer, LIT) achieve similar power densities than active systems operating at medium switching frequencies [1]. Furthermore, passive systems have a higher pulse-load capability and a significantly lower com-

plexity. For multipulse rectifiers, no EMI filter is required as low-frequency harmonics are eliminated by mutual cancellation and not by high-frequency switching. Accordingly, there are no switching-frequency harmonics that would have to be attenuated by low-pass EMI filters. This also avoids a capacitive phase displacement of input current and mains voltage and/or a low power factor at partial load or high mains frequencies (800 Hz). Such phase displacement is caused by the capacitors employed in EMI filters and, in principle, cannot be compensated by unidirectional PWM rectifier systems.

A general classification of 12-pulse rectifier concepts is shown in Fig. 1, where in-view of low harmonic distortion of the input current and/or low effects on the mains-extended circuit topologies are of special interest. There interphase reactors or transformers and diodes are used on the dc side for increasing the pulse number from 12 to 24, while maintaining the conventional ac-side circuit topology. Due to the relatively low rated power of the additional inductive components, the overall realization effort, thereby, is still mainly determined by the basic 12-pulse structure. Accordingly, in contrast to conventional 24-pulse circuits, only two instead of four diode bridges and transformers have to be employed. Furthermore, by avoiding active switches, a control circuit can be omitted, i.e., the extended system is still characterized by a high robustness and low complexity.

Besides generating two-phase-shifted three-phase diode-rectifier input-voltage systems, the characteristic mains side Δ–Δ and a Δ–Y isolation transformer of 12-pulse systems is commonly used for voltage adaption, such as for supplying the 28 V dc bus from the 115 V aircraft mains. Therefore, for systems of higher voltage and/or power, the isolation transformer can be replaced by a phase-shift autotransformer that reduces the rated power of the inductive components from $\approx$1.0 to $\approx$0.2 PO, and therefore, results in a significantly lower system weight and volume. However, contrary to active rectifiers, the output voltage of conventional and extended multipulse rectifiers is not controlled. Accordingly, a supplied drive system has to be rated for the lowest voltage resulting from mains voltage tolerances and load-dependent variations of the dc voltage. This leads to an oversizing of the drive inverter stage and drive motor. A control of the dc voltage can only be achieved by introducing active switches, and/or is only given for hybrid 12-pulse rectifier systems. Thereby, it is near at hand to utilize the increased controllability for an increase in the pulse number also and/or for an improvement of the mains current quality.
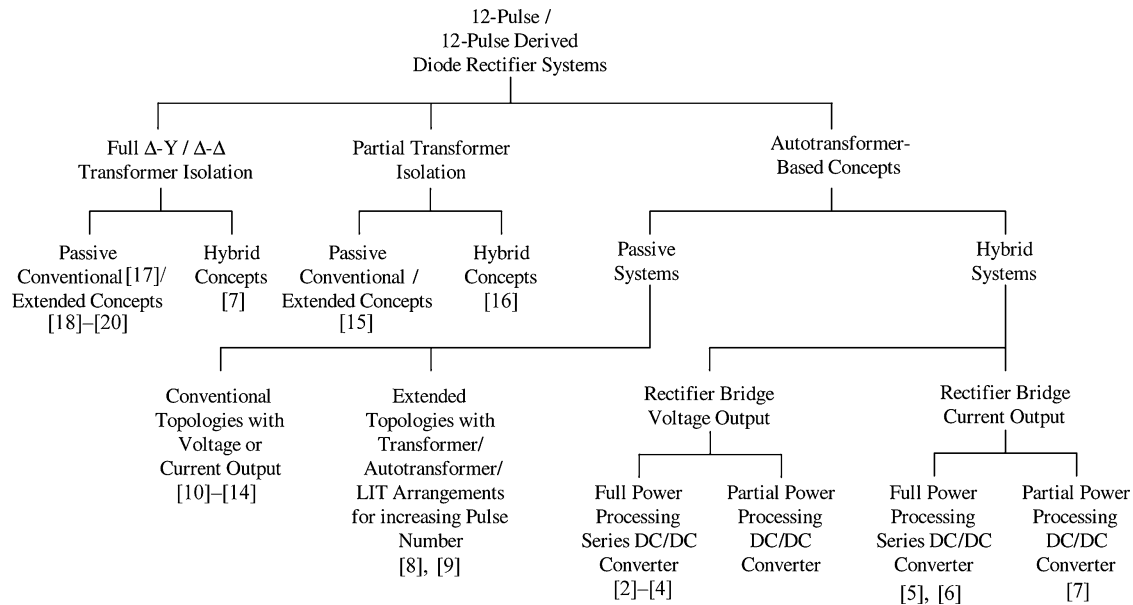
Fig. 1.   Classification of 12-pulse diode-rectifier systems. In each main category, purely passive, extended passive, and hybrid rectifier concepts have to be distinguished. Extended and hybrid systems show a pulse number higher than 12; accordingly, the denomination as 12-pulse system is related only to the structure of the ac-side part of the system.

Basically, as for passive 12-pulse systems, concepts with voltage or current output of the diode bridges have to be distinguished for hybrid autotransformer rectifier units (ATRUs) also. Thereby, the current on the mains side is impressed by series inductors, or the mains voltage is directly applied to the autotransformer input (cf., Fig. 2). The active switches are advantageously employed on the dc side. This allows a replacement of the passive smoothing and symmetrizing inductive components by high-frequency voltage or current-impressing dc/dc converters of low volume and enables to control the dc output voltage to a constant value. Furthermore, the voltage or current output of the rectifier bridges can then be modulated such that a purely sinusoidal mains current is achieved. Thereby, the complexity of the control is still limited as ultimately only a dc/dc converter function has to be implemented.

In [5], a hybrid multipulse ATRU with impressed diode-bridge output current has been proposed. There the interphase reactors required for a conventional ATRU to support the difference of the instantaneous diode-bridge output voltages and to symmetrize the dc currents are replaced by current-impressing dc/dc boost converters connected in parallel at the output side. This facilitates a significant system size reduction and enables output-voltage control. However, as the rectifier-bridge output currents are controlled to a constant value, no higher pulse number is achieved. According to [6], an increase of the pulse number and/or ideal sinusoidal mains current shape of a 12-pulse realization of the circuit topology shown in [5] can be obtained for approximately triangular modulation of the dc current [cf., Fig. 2(a)]. Here, it is important to note that the triangular shaping of the current could also be achieved by means of electronic inductors [21] and/or electronic interphase reactors [22], which would require a conversion of only a fraction of the total output power. This would result in a relatively higher overall system ef-

ficiency as the main power conversion would be still performed purely passive by the rectifier bridges. An according concept is described in [7] for a conventional transformer-isolated 12-pulse rectifier systems, but has not been analyzed for hybrid ATRU so far.

For supplying a voltage-source PWM inverter stage, a hybrid ATRU with direct voltage output is advantageous. In [4] with reference to [11], a corresponding concept comprising three active switches per diode bridge connected to the output-voltage center point has been proposed. The resulting three-level characteristic of the diode-bridge legs leads to a 24-pulse behavior of the overall system. An alternative hybrid concept formed by combination of two discontinuous conduction mode (DCM) rectifier units [23] and a 12-pulse autotransformer is described in [3]. There, due to the immediate parallel connection of the diode bridge outputs a single active switch is sufficient for constant duty-cycle modulation of the rectified voltage. As for conventional 12-pulse systems, the autotransformer is used for the cancellation of the fifth and seventh rectifier-bridge input-current harmonics, which show a comparably high amplitude for low values of the voltage-transfer ratio [24]. Due to the DCM, the autotransformer and the ac-side inductors can be realized with ferrite cores; however, on the other hand, an EMI filter of high attenuation and/or large size is required [25] that limits the applicability of the circuit.

As shown in [2], a system of same topology can also be operated in continuous conduction mode (CCM) with controlled output voltage, in case conventional 12-pulse magnetic components are employed. However, no improvement in the mains behavior is thereby achieved compared to a conventional 12-pulse ATRU. According to [26], a sinusoidal shaping of the mains current can be achieved for CCM by arranging an active switch at the output of each diode bridge [see Fig. 2(b)] and tri-
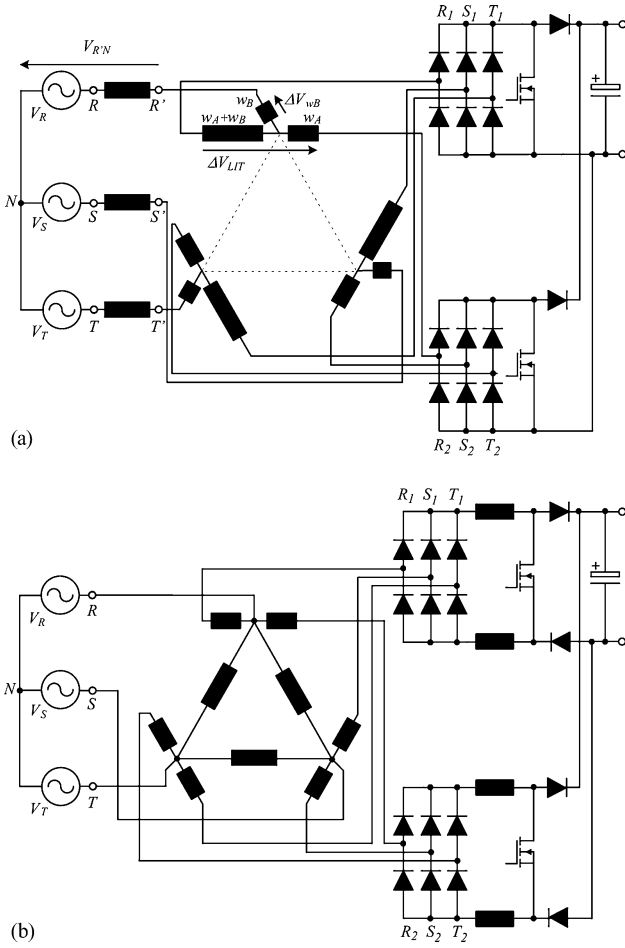
Fig. 2. Circuit topologies of hybrid 12-pulse ATRUs. (a) Impressed/modulated diode-bridge output current and impressed ac-side voltage [2]. (b) Impressed/modulated diode-bridge output voltage, ac-side current impressed by series inductors [6]. *Remark*: Inductors with parallel axes are magnetically coupled.

TABLE I
SPECIFICATION OF THE 10-KW PROTOTYPE SYSTEM

Input Voltage Range	$115\text{V} \pm 15\% \approx 98 - 132 V_{RMS}$
Input Frequency Range	360-800Hz
Input Inductor	$188\mu\text{H}$
LIT	$w_A + w_B : w_A : w_B = 29{:}21{:}8$
Output Power	10kW
Switching Frequency	40kHz
Nominal V_{DC}	250V (Passive) / 520V (Closed Loop)

modulation functions is shown. The implementation of the controller is described in detail in Section III. Experimental results given in Section IV verify the theoretical considerations and demonstrate the advantageous applicability performance of the proposed concept.

II. SPACE-VECTOR MODULATION

For purely passive operation, i.e., switches S_1 and S_2 remaining in the turn-OFF state, the system depicted in Fig. 2(a) shows a typical 12-pulse input-current shape with a THD of 6.5%.This 12-pulse operation results due to the 30° phase shift of the input voltages of the two rectifier stages, which is generated by the LIT [28]. The LIT is assumed to have an ideal coupling of the related windings in a first approximation in the following. The influence of nonideal coupling is considered in Section III-D.

The ideal sinusoidal input currents of the two diode bridges, which are phase-shifted by 30°, are shown in Fig. 3.Based on the signs of the six sinusoidal currents $i_{R\kappa}$, $i_{S\kappa}$, and $i_{R\kappa}$ ($\kappa = 1, 2$), 12 different sectors (0. . .11) are defined. There, e.g., in sector 0, i_{R_1}, i_{S_1}, and i_{R_2} are positive and i_{T_1}, i_{S_2} and i_{T_2} are negative. The zero crossing of i_{S_2} to positive values defines the beginning of the subsequent sector 1.

With the currents of the rectifiers also, the conducting diodes and the input voltages of the rectifiers are defined. In Fig. 4(a), the voltages of the rectifiers are replaced by voltage sources, which are split into zero-sequence voltages $v_{0,\kappa}$ and the remaining current-forming voltages in the three phases $v_{\nu_{1N}}$ and $v_{\nu_{2N}}$ ($\nu = R, S, T$). With the general definitions of voltage and current space vectors and the zero-sequence quantities, the two equivalent circuits shown in Fig. 4(b) and (c) can be derived. There, voltages $v_{\nu_{1N}}$ and $v_{\nu_{2N}}$ and/or $\underline{v}_\kappa$ determine the currents flowing in phases R, S, and T, and the zero-sequence voltages $v_{0,\kappa}$ determine the zero-sequence and/or common-mode (CM) current as well as the circulating current, as will be discussed later.

With the rectifier voltages, the rectifier input-voltage space vector could be calculated by

$$\underline{v}_1 = \frac{2}{3}\left(v_{R_{1N}} + \underline{a}v_{S_{1N}} + \underline{a}^2 v_{T_{1N}}\right) \tag{1}$$

$$\underline{v}_2 = \frac{2}{3}\left(v_{R_{2N}} + \underline{a}v_{S_{2N}} + \underline{a}^2 v_{T_{2N}}\right) \tag{2}$$

and with

$$\underline{a} = e^{j2\pi/3}.$$

angular modulation of the switch duty cycle. Thereby, an output voltage of approximately twice the value given for passive operation is required. However, this is of no disadvantage for drive systems of higher power. Furthermore, as compared to Fig. 2(a), only a single boost diode is introduced into the output current path that results in lower conduction losses. In case of only open-loop control of the duty cycles d_1 and d_2 of T_1 and T_2, as described in [2], the current shaping is only passive, i.e., mains voltage distortions or asymmetries make direct influence on the mains current shape and may lead to low-frequency harmonics of large amplitude or to an unbalanced current consumption of the phases. Accordingly, a closed-loop current control is required to ensure a sinusoidal input current in case of distorted mains also. This also allows to control the output voltage to a constant value.

In this paper, the closed-loop input-current control is discussed and analyzed, as well as measurement results for a system with the specifications given in Table I are presented. In Section II, the operating principle of the control concept that is based on space-vector modulation, e.g., applied in [27] for active PWM rectifiers, is explained and the derivation of the
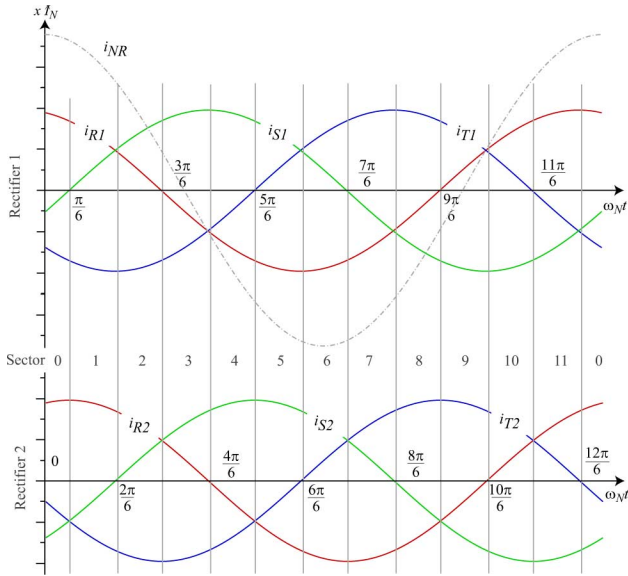
Fig. 3. Sector definition in relation to ideal sinusoidal rectifier input currents. Current i_{NR} denotes the sum of the rectifier input currents of phase R, i.e., $i_{NR} = i_{R_1} + i_{R_2}$.
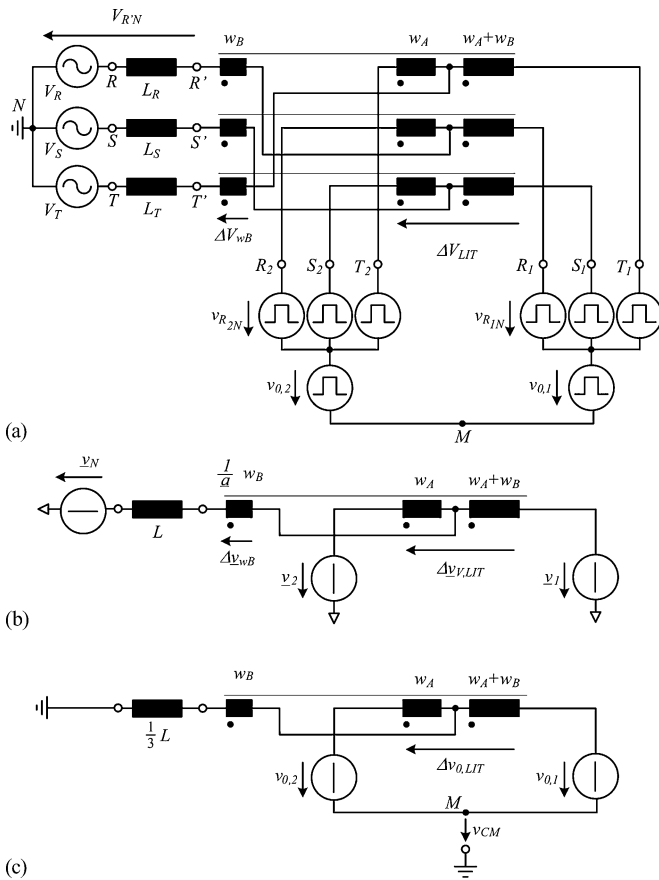

Fig. 4. (a) Schematic of the hybrid 12-pulse rectifier according to Fig. 2(a), where the diode rectifiers and the switches are replaced by voltage sources. By calculating the space vectors and the zero-sequence component of the voltages and currents, (b) space-vector and (c) zero-sequence equivalent circuit are derived.
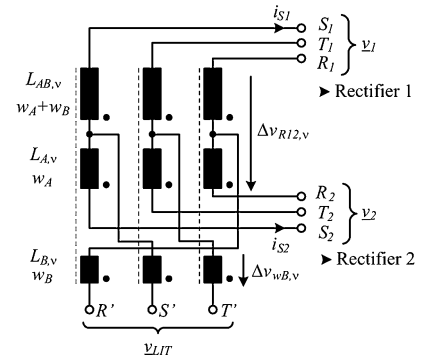

Fig. 5. Calculation of the voltage transformation of an ideal LIT.
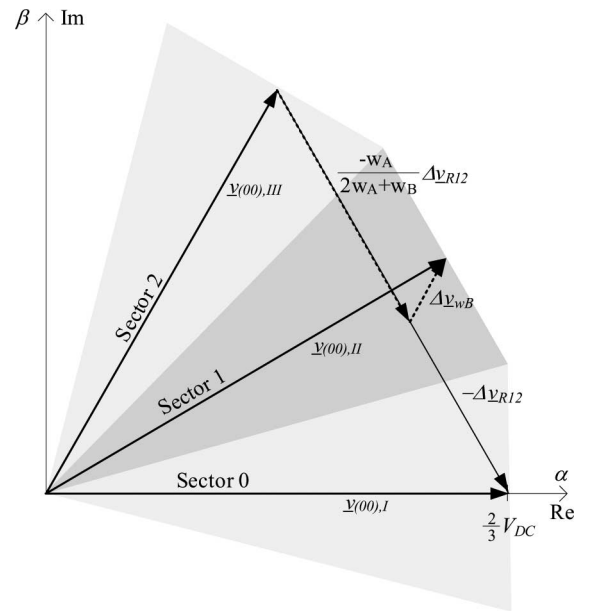

Fig. 6. LIT input-voltage space-vector diagram for the passive conduction states, where both switches are turned off. Only three sectors, i.e., sectors 1–3, as defined by the signs of the input currents of the two rectifiers (cf., Fig. 3), are shown.

Based on these space vectors and the schematic given in Fig. 5, the operation of the LIT is described in the following paragraph.

In sector 0, the input voltages of both rectifiers, and therefore, also the space vectors are the same, so that the voltage difference between the two rectifiers $\Delta v_{R12,\nu}$ ($\nu = R, S, T$) (cf., Fig. 5) is zero. With $\Delta v_{R12,\nu} = 0$, the voltage $\Delta v_{wB,\nu}$ across $L_{B,\nu}$ is also zero, and the input-voltage space vector $\underline{v}_{\mathrm{LIT}}$ of the LIT at nodes R', S', and T', which is defined by

$$\underline{v}_{\mathrm{LIT}} = \frac{2}{3}\left(v_{R'N} + \underline{a}v_{S'N} + \underline{a}^2 v_{T'N}\right) \qquad (3)$$

is equal to the input-voltage space vector of the two rectifiers, as shown in Fig. 6. There, $\underline{v}_{(00),I}$ denominates the LIT input-voltage space vector in sector 0.

In sector 1, the input-voltage space vector of rectifier 1 changes to $\underline{v}_{(00),II}$ due to the changing rectifier input-current signs. Now, there is a voltage difference $\Delta v_{R12,\nu}$ between the two rectifier inputs, which is transferred to the nodes R', S', and T' by the LIT. In order to calculate the resulting input-voltage

space vector of the LIT, first the transfer function of the LIT is derived by setting up the mesh equation

$$\underline{v}_{\text{LIT}} = \underline{v}_2 - \Delta\underline{v}_{wB} + \frac{w_A}{2w_A + w_B}\Delta\underline{v}_{R12} \qquad (4)$$

where $\Delta\underline{v}_{R12}$ is the space vector of voltages $\Delta v_{R12,\nu}$ between the two rectifiers. By assuming an ideal coupling of the related LIT windings, the voltages $\Delta v_{wB,\nu}$ across the inductors $L_{B,\nu}$ can be expressed by

$$\Delta v_{wB,R} = \frac{w_B}{2w_A + w_B}\Delta v_{R12,S}$$

$$\Delta v_{wB,S} = \frac{w_B}{2w_A + w_B}\Delta v_{R12,T}$$

$$\Delta v_{wB,T} = \frac{w_B}{2w_A + w_B}\Delta v_{R12,R} \qquad (5)$$

which reveals that the voltages are phase-shifted by $120°$, due to the cyclic-exchanged connections, i.e., the connection of $L_{B,R}$ to $L_{A,T}$ and $L_{AB,T}$. With (5), the related space vector $\Delta\underline{v}_{wB}$ results as

$$\Delta\underline{v}_{wB} = \frac{2}{3}\left(\Delta v_{wB,R} + \underline{a}\Delta v_{wB,S} + \underline{a}^2\Delta v_{wB,T}\right)$$

$$= \frac{2}{3}\frac{w_B}{2w_A + w_B}\left(\Delta v_{R12,S} + \underline{a}\Delta v_{R12,T} + \underline{a}^2\Delta v_{R12,R}\right). \qquad (6)$$

By multiplying this result by $\frac{\underline{a}}{\underline{a}}$, (6) results in

$$\Delta\underline{v}_{wB} = \frac{w_B}{2w_A + w_B}\Delta\underline{v}_{R12}\frac{1}{\underline{a}}$$

$$= \frac{w_B}{2w_A + w_B}\Delta\underline{v}_{R12}e^{j(-2\pi/3)}. \qquad (7)$$

Consequently, the space vector $\Delta\underline{v}_{wB}$ is formed by scaling and rotation of $\Delta\underline{v}_{R12}$ by $120°$. Considering (7), mesh equation (4) could be simplified to

$$\underline{v}_{\text{LIT}} = \underline{v}_2 - \frac{w_B}{2w_A + w_B}\underline{a}^2\Delta\underline{v}_{R12} + \frac{w_A}{2w_A + w_B}\Delta\underline{v}_{R12}$$

$$= \underline{v}_2 + (\underline{v}_1 - \underline{v}_2)\left(\frac{w_A - w_B\underline{a}^2}{2w_A + w_B}\right) \qquad (8)$$

which allows the calculation of $\underline{v}_{\text{LIT}}$ in dependence of the rectifier input-voltage space vectors $\underline{v}_1$ and $\underline{v}_2$.

With (8), the resulting space vector $\underline{v}_{(00),I}$ for sector 1 at the LIT input could also be graphically derived, as shown in Fig. 6. In sector 2, the two rectifiers have again the same input voltage and the space vector at the LIT input is equal to $\underline{v}_{(00),I}$. Consequently, a new voltage space vector in each $30°$ wide sector, which result in total of 12 discrete space vectors and/or in a 12-pulse behavior of the passive system. The state where both switches are turned off is designated by (00).

By turning both switches ON at the same time, i.e., applying state (11), the rectifier input voltages become zero, and therewith, also the LIT input-voltage space vector $\underline{v}_{\text{LIT}(00)}$ shows zero magnitude (cf., Fig. 7). In this state, the voltage between the nodes R', S', and T' is zero, so that it could be used for increasing the input current and/or for boosting the output voltage.
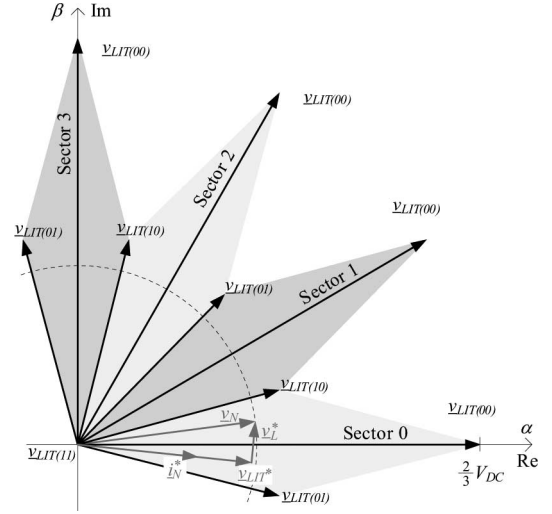

Fig. 7. Space vectors that can be generated by the rectifier system.

Besides states (00) and (11), there are two further possible switching states: (01) ($S_1 = $ OFF and $S_2 = $ ON) and state (10), where always only one switch is turned on, i.e., one rectifier input voltage is zero. Based on (8), the resulting input-voltage vector of the LIT $\underline{v}_{\text{LIT}(01)}$ and $\underline{v}_{\text{LIT}(10)}$, which are rotated by $\pm 15°$ ($\pm\pi/12$) with respect to vector $\underline{v}_{\text{LIT}(00)}$, can be calculated (cf., Fig. 7).

By applying proper selection of the relative on times $\delta_{(00)}$, $\delta_{(01)}$, $\delta_{(10)}$, and $\delta_{(11)}$ of the switching states (00), (01), (10), and (11), respectively, within a pulse period, any voltage space vector in the gray-shaded areas shown in Fig. 7, defined by the voltage space vectors, could be generated in time average over a pulse period. There

$$1 = \delta_{(00)} + \delta_{(01)} + \delta_{(10)} + \delta_{(11)} \qquad (9)$$

and

$$0 \leq \delta_{(\mu\nu)} \leq 1 \qquad (10)$$

must be considered.

In a next step, the reference space vector $\underline{v}^*_{\text{LIT}}$, which is required for the sinusoidal input-current formation is derived based on the equivalent circuits shown in Fig. 4(b) and (c).

For providing sinusoidal input currents, the two switches must be controlled in a way, such that the local average of the voltage across the boost inductors $L_{b,\nu}$ exhibits a sinusoidal shape. Considering Fig. 4(b), the current in the boost inductors is defined by

$$\underline{v}_L = L\frac{i_N}{dt} = \underline{v}_N - \underline{v}_{\text{LIT}}. \qquad (11)$$

As the mains' star point N is not connected to the rectifier dc output and/or load, the sum of the three mains currents is always forced to zero $\sum i_{N,i} = 0$. Therefore, the zero-sequence component of the boost inductor voltage

$$v_{L,0} = \frac{1}{3}\left(v_{L,R} + v_{L,S} + v_{L,T}\right) \qquad (12)$$
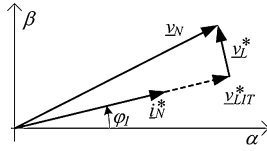
does not influence the phase currents.

Fig. 8.   Calculation of input-current reference space vector $\underline{i}_N^*$.

Fig. 9.   Time behavior of the relative ON-times $\delta_{(11)}$, $\delta_{(01)}$, and $\delta_{(10)}$ for sector 0 and sector 1.

For calculating the reference space vector $\underline{v}_{\text{LIT}}^*$ resulting in sinusoidal input currents, the phase of the input-current space vector $\underline{i}_N^*$ is required. Due to the ohmic fundamental behavior of the three-phase rectifiers $Rectifier 1$ and $Rectifier 2$ [29], which is transferred by an ideal LIT to nodes R', S', and T', the reference vector $\underline{i}_N^*$ for the input current must be aligned with $\underline{v}_{\text{LIT}}^*$ (cf., Fig. 8). Thus, $\underline{i}_N^*$ could be defined as follows:

$$\underline{i}_N^* = \widehat{I}_N^* e^{j\varphi_I} \tag{13}$$

with

$$\varphi_I = \arctan\left(\frac{\widehat{v}_L^*}{\sqrt{\widehat{V}_N^2 - \widehat{v}_L^{2*}}}\right)$$

resulting in a reference vector $\underline{v}_{\text{LIT}}^*$

$$\underline{v}_{\text{LIT}}^* = \widehat{V}_{\text{LIT}}^* e^{j\varphi_I} \tag{14}$$

with

$$\widehat{V}_{\text{LIT}}^* = \sqrt{\widehat{V}_N^2 - \widehat{v}_L^{2*}} \tag{15}$$

which must be generated in the time average over a switching period T_P.

The tip of the reference vector $\underline{v}_{\text{LIT}}^*$ describes a circle in the α–β-plane (cf., Fig. 7) for sinusoidal mains voltages. Thus, only states (00), (01), and (10) are used for the generation of $\underline{v}_{\text{LIT}}^*$. Considering Fig. 8 and assuming zero-input current, $\underline{v}_{\text{LIT}}^*$ must have the same amplitude as $\underline{v}_N$, and the circle described by the tip of $\underline{v}_{\text{LIT}}^*$ and/or $\underline{v}_N$ must fit in the gray-shaded triangle defined by states (00), (01), and (10). In order to fulfill this limitation, the dc output voltage must be

$$V_{\text{dc}} \geq \frac{3}{\cos(\pi/12)} \widehat{V}_N \tag{16}$$

in case of zero-input current. However, with zero or small input current, the rectifier input currents are not continuous, so that the rectifier diodes do not always conduct, and the rectifier input space vector deviates from the vectors shown in Fig. 7. With increasing input current, the conduction time of the rectifier diodes increases, until always one of the two diodes in a bridge leg of the rectifier is conducting, i.e., the space vectors shown in Fig. 7 are given, and the input current could be controlled, as described previously.

For increasing input current, the voltage v_L drop across the input inductor increases and the length of $\underline{v}_{\text{LIT}}^*$ decreases according to (15). For the specifications given in Tables I and III, the minimal output voltage is slightly below 490 V at nominal output power and slightly above 560 V at zero-input current.

The ON-times if the three switching states can be calculated with simple geometrical considerations and are a function of
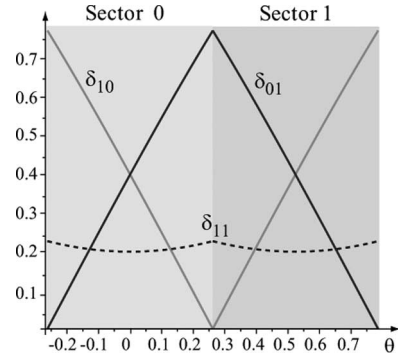
the angle θ_{LIT}^* of $\underline{v}_{\text{LIT}}^*$ and are of the magnitude $|\underline{v}_{\text{LIT}}^*| = \widehat{V}_{\text{LIT}}^*$. The resulting ON-times for sector 0 are

$$\delta_{(01)} = \frac{3}{2}\frac{\widehat{V}_{\text{LIT}}^*}{V_{\text{dc}}}\left(\cos\theta_{\text{LIT}}^* + \left(2+\sqrt{3}\right)\sin\theta_{\text{LIT}}^*\right) \tag{17}$$

$$\delta_{(10)} = \frac{3}{2}\frac{\widehat{V}_{\text{LIT}}^*}{V_{\text{dc}}}\left(\cos\theta_{\text{LIT}}^* - \left(2+\sqrt{3}\right)\sin\theta_{\text{LIT}}^*\right). \tag{18}$$

$$\delta_{(11)} = 1 - 3\frac{\widehat{V}_{\text{LIT}}^*}{V_{\text{dc}}}\cos\theta_{\text{LIT}}^*. \tag{19}$$

Similar equations can be derived for the other sectors.

In spite of calculating the ON-times for each sector separately, it is also possible to rotate the reference vector $\underline{v}_{\text{LIT}}^*$ always back to sector 0. There, the relative angles of $\underline{v}_{\text{LIT}}^*$ to the sector boundaries must be retained. Furthermore, it is important to note that in odd-numbered sectors, the switching vectors $\underline{v}_{\text{LIT}(01)}$ and $\underline{v}_{\text{LIT}(10)}$ are transposed, so that the relative ON-times also must be transposed.

For a simpler implementation of the equations defining the relative ON-times in a DSP, an approximation

$$\delta_{(01)} = \frac{\widehat{V}_{\text{LIT}}^*}{V_{\text{dc}}}\left(\frac{3}{2} + \frac{18}{\pi}\theta_{\text{LIT}}^*\right) \tag{20}$$

$$\delta_{(10)} = \frac{\widehat{V}_{\text{LIT}}^*}{V_{\text{dc}}}\left(\frac{3}{2} - \frac{18}{\pi}\theta_{\text{LIT}}^*\right) \tag{21}$$

$$\delta_{(11)} = 1 - \delta_{(01)} - \delta_{(10)} \tag{22}$$

could be utilized. Time behavior of the relative ON-times is shown in Fig. 9 for sectors 0 and 1. With (20), (21), and (21), it is now possible to generate arbitrary space vectors at the input of the LIT, which are located inside the triangle defined by the tips of voltage space vectors $\underline{v}_{\text{LIT}(00)}$, $\underline{v}_{\text{LIT}(01)}$, and $\underline{v}_{\text{LIT}(10)}$. The reference for the space vector is determined by the current controller and a feed-forward signal according to Fig. 10, which is described in the following section.

III. CONTROLLER

Based on the space-vector modulation described in the previous section, in the following section, first the input current controller, as shown in Fig. 10, is explained. Thereafter, an extension of the controller for limiting the zero-sequence current
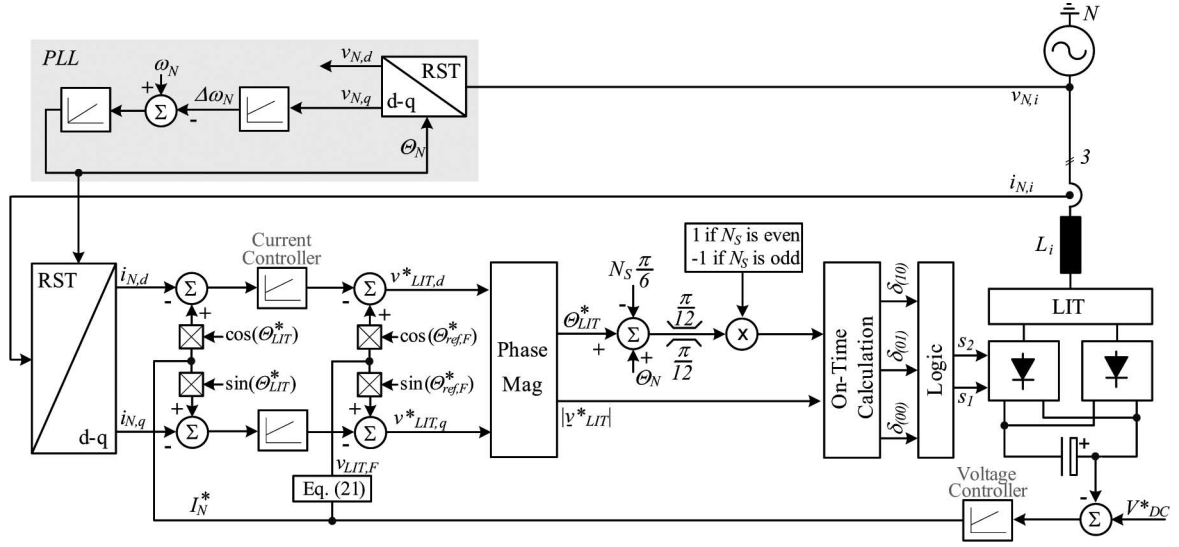
Fig. 10. Basic structure of the controller for the 12-pulse rectifier system with sinusoidal input currents and output-voltage regulation.

and limitations of the space-vector modulation for unbalanced and/or distorted mains. Finally, a more detailed model of the LIT also including parasitic elements is presented.

A. Input-Current Control

In the control structure, as shown in Fig. 10, a phase-locked-loop (PLL) controller is used to determine the d-component, i.e., the magnitude $\hat{V}_N$ and the phase angle θ_N of the line voltage V_N, while the q-component of V_N is regulated to zero. With θ_N, the d- and the q-components of the line current are also calculated. These values are compared with their reference values $I_N^* \cos \theta_{\mathrm{ref},P}$ and $I_N^* \sin \theta_{\mathrm{ref},P}$ and the difference is fed into the PI-controllers for the d- and the q-components of the line current.

The reference value I_N^* is determined by an output-voltage controller. Angle $\theta_{\mathrm{ref},F}$ between the mains voltage vector $\underline{v}_N$ and the reference current vector $\underline{i}_N^*$ is calculated using

$$\theta_{\mathrm{ref},F}^* = \arctan \frac{\omega_N L I_N^*}{\sqrt{v_{N,d}^2 - \omega L I_N^*}} \qquad (23)$$

which could be derived from Fig. 8. The feed-forward signals $v_{\mathrm{LIT},F}^* \cos \theta_{\mathrm{ref},F}$ and $v_{\mathrm{LIT},F}^* \sin \theta_{\mathrm{ref},F}$ for the d- and the q-components are added to the controller output. The amplitude $v_{\mathrm{LIT},F}^*$ is given by

$$v_{\mathrm{LIT},F}^* = \sqrt{v_{N,d}^2 - \omega_N L I_N^*} \qquad (24)$$

as can also be seen from Fig. 5. After the summation, the d- and the q-components of the reference vector, i.e., $v_{\mathrm{LIT},d}^*$ and $v_{\mathrm{LIT},q}^*$, are defined and the amplitude $|\underline{v}_{\mathrm{LIT}}^*|$ and the angle θ_{LIT}^* of the reference vector of the LIT input voltage are calculated.

In the next step, the reference vector is rotated back to sector 0 by adding the mains phase angle θ_N and subtracting $N_s(\pi/6)$ from θ_{LIT}^*. N_s is the number of the current sector in which the reference current is located. Neglecting numerical errors, the result lies within the allowed region $\pm 15°$ ($\pm \pi/12$), which is

determined by the sector boundaries. For coping with numerical/measurement errors, the angle is limited to $\pm 15°$. Thereafter, the angle is multiplied by 1 if the sector N_s is even and by -1 if N_s is odd in order to obtain a triangular time behavior of the reference angle, which starts at $-15°$, rises up to $15°$, and then, ramps down to $-15°$ again instead of a sawtooth-like behavior, which would step to $-15°$ as soon as it reaches $15°$. This time behavior of the reference angle is required to obtain modulation signals, as shown in Fig. 9, which can be calculated using (17), (18), and (19).

B. Zero-Sequence-Current Control

In the 12-pulse rectifier system shown in Fig. 2(a), a circulating zero-sequence current is flowing via L_A, L_{AB}, $Rectifier1$, the output capacitor, and $Rectifier2$ [28], which is driven by the voltage difference between $Rectifier1$ and $Rectifier2$ due to the 30° phase shift. Due to the phase shift, this current is intrinsic for this kind of 12-pulse system and could not be reduced without impairing the mains current quality. However, the amplitude of the current could increase in case of unequal switching times, asymmetries, and offsets. Therefore, an additional control loop is implemented for limiting the zero-sequence current.

In order to show how such a control loop could limit the zero-sequence current, in Table II, the zero voltages $v_{0,1}$ and $v_{0,2}$ of both rectifiers (cf., Fig. 4) and the resulting voltage difference between the two rectifiers $\Delta v_{0,\mathrm{LIT}}$ are given for the two active switching states $\underline{v}_{\mathrm{LIT}(01)}$ and $\underline{v}_{\mathrm{LIT}(10)}$, where always one of the two switches is turned on and the other switch is turned off. In this table, it could be seen that $\Delta v_{0,\mathrm{LIT}}$ is always positive for $\underline{v}_{\mathrm{LIT}(01)}$ and always negative for $\underline{v}_{\mathrm{LIT}(10)}$. Consequently, for decreasing, for example, a positive-circulating zero-sequence current $i_{0,c12}$, which flows from $Rectifier1$ via the LIT to $Rectifier2$ and back via the output parallel connection, $\Delta v_{0,\mathrm{LIT}}$ must be slightly negative in average. This means that $\underline{v}_{\mathrm{LIT}(10)}$ must be turned on slightly longer than $\underline{v}_{\mathrm{LIT}(01)}$ in average.

TABLE II
ZERO VOLTAGE OF $Rectifier1$, $v_{0,1}$ AND $Rectifier2$, $v_{0,2}$, AS WELL AS THE DIFFERENCE VOLTAGE $\Delta v_{0,\mathrm{LIT}}$ (CF., FIG. 4) FOR THE SWITCHING STATES, WHERE ALWAYS ONE OF THE SWITCHES IS TURNED ON AND THE OTHER ONE IS TURNED OFF

	$\underline{v}_{LIT(01)}$			$\underline{v}_{LIT(10)}$		
	$v_{0,1}$	$v_{0,2}$	$\Delta v_{0,LIT}$	$v_{0,1}$	$v_{0,2}$	$\Delta v_{0,LIT}$
Sector 0	$-\frac{1}{6}V_{DC}$	$-\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{1}{2}V_{DC}$	$-\frac{1}{6}V_{DC}$	$-\frac{1}{3}V_{DC}$
Sector 1	$\frac{1}{6}V_{DC}$	$-\frac{1}{2}V_{DC}$	$\frac{2}{3}V_{DC}$	$-\frac{1}{2}V_{DC}$	$-\frac{1}{6}V_{DC}$	$-\frac{1}{3}V_{DC}$
Sector 2	$\frac{1}{6}V_{DC}$	$-\frac{1}{2}V_{DC}$	$\frac{2}{3}V_{DC}$	$-\frac{1}{2}V_{DC}$	$\frac{1}{6}V_{DC}$	$-\frac{2}{3}V_{DC}$
Sector 3	$-\frac{1}{6}V_{DC}$	$-\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{1}{2}V_{DC}$	$\frac{1}{6}V_{DC}$	$-\frac{2}{3}V_{DC}$
Sector 4	$-\frac{1}{6}V_{DC}$	$-\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{1}{2}V_{DC}$	$-\frac{1}{6}V_{DC}$	$-\frac{1}{3}V_{DC}$

In case both switches are turned on or both are turned off $\Delta v_{0,\mathrm{LIT}}$ = 0. Based on this table, the required action of the zero-current controller could be derived. The voltages repeat periodically for the other sectors.
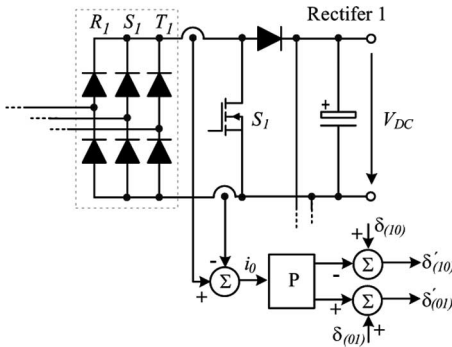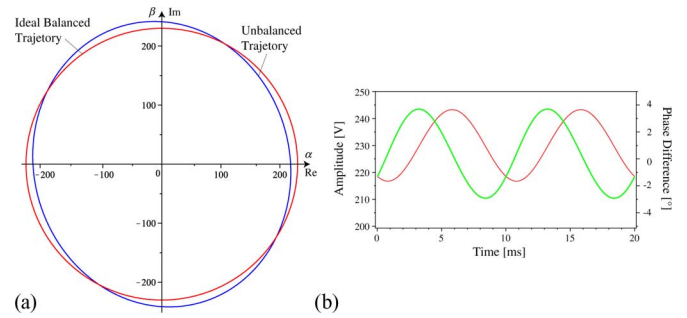

Fig. 12. (a) Trajectory of the mains voltage space vector for ideal balanced sinusoidal mains voltages and for $\pm10\%$ unbalanced mains voltages. (b) Amplitude of the space vector and phase difference between unbalanced and ideally balanced space vector.

Fig. 11. Controller for limiting the circulating zero-sequence current in $L_{A,\nu}$, $L_{AB,\nu}$, $Rectifier1$, and $Rectifier2$ [cf., Fig. 4(c)].

Such behavior could be, for example, achieved with the controller shown in Fig. 11, where the zero-sequence current is measured by subtracting the currents in the positive and negative rail of $Rectifier1$. The result is amplified, and then, added to/subtracted from the relative ON-times of switching states (01) and (10), implementing a P-type control. By controlling the circulating current, the relative ON-times of the two active switching states (01) and (10) is changed and deviates slightly from the ideal ON-times for sinusoidal currents. In order not to impair the THD of the mains current, the gain of the P-controller has to be limited to low values. Due to the limited number of degrees of freedom for the control of the considered system, this mutual influence of input phase current and zero-sequence-current control cannot be avoided.

C. Unbalanced and/or Distorted Mains Voltage

Based on the described space-vector modulation and the controller, a voltage at the input of the LIT could be generated, so that purely sinusoidal mains current shape is guaranteed also in case of distorted or unbalanced mains voltages. For example, for an unbalance where the mains phase voltages have different amplitudes, the tip of the mains voltage space vector $\underline{v}_N$ is not any more describing a circle, but an ellipsoid, as shown in Fig. 12(a). Consequently, the amplitude of the space vector as well as the angular speed is varying over the one mains period [see Fig. 12(b)].

Considering Fig. 8, the shift between $\underline{v}_N$ and $\underline{v}_{\mathrm{LIT}}^*$ is only determined by $\underline{v}_L^*$ and for purely sinusoidal input currents, the amplitude of $\underline{v}_L^*$ must be constant and the space vector $\underline{v}_L^*$ must rotate with a constant angular speed defined by the mains frequency. Thus, with a varying amplitude and angular speed of $\underline{v}_N$, the amplitude and angular speed of $\underline{v}_{\mathrm{LIT}}^*$ must also vary and $\underline{v}_{\mathrm{LIT}}^*$ is no more in phase with $\underline{i}_N^*$, i.e., $\underline{v}_{\mathrm{LIT}}^*$ must oscillate around $\underline{i}_N^*$ for a sinusoidal input current.

Assuming, for example, that the ideal current space vector $\underline{i}_N$ is in the middle of sector 0, i.e., pointing in the direction of the real axis (cf., Fig. 7), vector $\underline{v}_{\mathrm{LIT}}^*$ could slightly oscillate around $\underline{i}_N^*$, since in sector 0, all vectors, which are located in the gray-shaded area of sector 0 (cf., Fig. 7), can be generated by the controller. However, when the input-current space vector $\underline{i}_N^*$ approaches the boundary between sectors 0 and 1, $\underline{v}_{\mathrm{LIT}}^*$ will sooner or later cross the border and enter in sector 1 during its oscillations, while $\underline{i}_N^*$ is still in sector 0. However, with $\underline{i}_N^*$ in sector 0, vectors in the gray-shaded area only, i.e., sector 0, can be generated, so that the required reference vector $\underline{v}_{\mathrm{LIT}}^*$ in sector 1 could not be realized and a slight distortion of the mains current occurs each time $\underline{i}_N^*$ is close to a sector boundary. Due to the relatively large inductance of the input inductor and the operation of the LIT, this limitation only results in a relatively small distortion, as will be shown by measurements in Section IV.

In Fig. 13, the maximal phase difference between $\underline{i}_N^*$ and $\underline{v}_{\mathrm{LIT}}^*$ for unbalanced mains, where one phase is lower in amplitude by $x\%$, another phase is higher by $x\%$, and the third phase is left unchanged, is compared to the ideal value. There, it could be seen that the maximal phase difference is relatively small for amplitude differences up to a few percent, so that the distortion due to this limitation is relatively small.

Similar conditions are given in case of mains voltages with harmonics, which also results in a $\underline{v}_N$ that has a varying amplitude and angular speed. Consequently, in this case also, a small distortion of the mains current occurs, when $\underline{i}_N$ is close to the sector border. Again, the input inductor and the LIT limit these distortions, as will be shown in Section IV.

D. Line Interface Transformer

In all the previous discussions, an ideal coupling of the LIT has been assumed for deriving the equations. In practice,
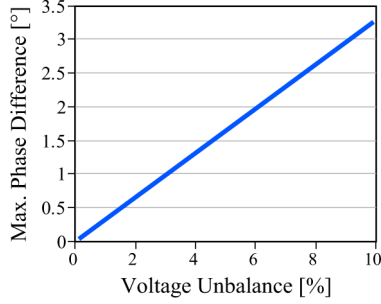
Fig. 13. Maximal phase difference between $\underline{i}_N$ and $\underline{v}_{\text{LIT}}^*$ for unbalanced mains. There one phase-voltage amplitude is assumed to be lower by $x\%$, one phase-voltage amplitude is higher by $x\%$, and the third phase is left unchanged at the nominal value.

TABLE III
COMPONENTS FOR 10-kW PROTOTYPE SYSTEM

Component	Parameter
Input Inductor	188μH
	Core: S3U 48b / Trafoperm N2/0.1mm
LIT	$w_A + w_B : w_A : w_B$= 29:21:8
	Core: 2×SM65 / Trafoperm N2/0.1mm
	L_{AB}=5.2mH, L_A=2.5mH, L_B=0.35mH
Current Sensors	Sensitec CMS4050, 50A
Diode Bridge	IXYS VUE75-12NO7, 1200V, 75A
IGBT	Infineon 2×IPW90R120C3, 900V, 36A
Output Diode	C2D20120D, 1200V, 31A, SiC
Output Capacitor	680μF, 2x400Vdc
Controller	TMS320F2808 DSP board

however, due to the leakage flux, the coupling coefficient of the individual windings is always lower than one. Assuming three identical LITs for the three phases, i.e., same coupling coefficients for all three LITs, the resulting leakage inductances can be transferred to R', S', and T' (cf., Fig. 5), so that they act as if they would be connected in series to the boost inductors. The value of the resulting additional boost inductance $L_{b,\text{add}}$ is

$$
\begin{aligned}
L_{b,\text{add}} = &\left[L_A \sqrt{L_B L_{AB}} \left(K_{AB,A} K_{A,B} - K_{AB,B} \right) \right. \\
&- 2L_B \sqrt{L_A} \left(K_{A,B} K_{AB,B} - K_{AB,A} \right) \\
&+ L_{AB} \sqrt{L_B L_A} \left(K_{A,B} - K_{AB,A} K_{AB,B} \right) \\
&+ L_{AB} \left(L_A - K_{AB,B}^2 L_B - K_{AB,A}^2 L_A + L_B \right) \\
&\left. + L_A L_B \left(1 - K_{A,B}^2 \right) \right] \bigg/ \\
&\left[L_A + 2K_{AB,A} \sqrt{L_A L_{AB}} + L_{AB} \right] \quad (25)
\end{aligned}
$$

where $K_{\nu,\lambda}$ are the coupling coefficients between two respective inductors.

In case the coupling coefficients between the three inductors of the phases of the LIT are not equal, the currents in the two rectifiers become slightly unbalanced, but the additional inductances seen at the ports R', S', and T' are still equal for all three phases. In case the three LITs are not identical, i.e., the coupling coefficients of the three LITs are different, the currents of the two rectifiers are unbalanced and the additional inductances in the three phases are not identical any more. Slightly different values of the inductors/coupling coefficients can be compensated by the controller without impairing the line current quality, but larger deviations will lead to a distorted mains current.

IV. MEASUREMENT RESULTS

In order to validate the presented closed-loop current-control strategy, a 10-kW prototype system with a switching frequency of 40 kHz was constructed. The main components are listed in Table III. A photograph of the experimental system is shown in Fig. 14.
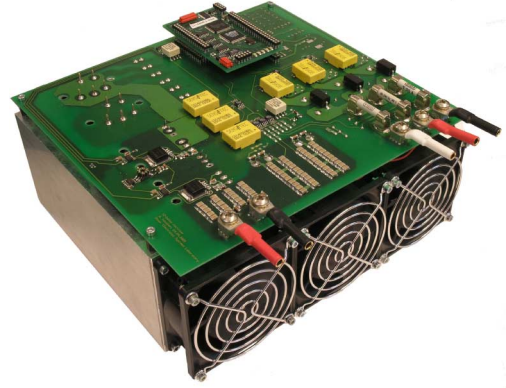

Fig. 14. Photograph of the 10-kW hardware prototype (24 cm × 22 cm × 10 cm).

The prototype system comprises two PCBs with the input inductors and the LIT mounted beneath on the chassis. The main power PCB not only hosts the power circuit, but also an auxiliary power supply, a precharge circuit, and analog measurement and level-shifting circuits for use by the DSP control board. The control board based on a Texas Instruments TMS320F2808 fixed-point DSP running at 100 MHz implements the control scheme, which is shown as a block diagram in Fig. 10, and is mounted on top of the power PCB.

A. Closed-Loop Control

The closed-loop control strategy was tested to determine its ability to directly control the input current. In Fig. 15, the simulated input currents for symmetric mains voltages of 115 V_{rms}/400 Hz, a load of 27 Ω, an output voltage of 520 V, and a reference current of $\widehat{I}_N^*$ 41 A, i.e., for approximately 10-kW output power are depicted. The resulting THD of the input current is approximately 2.8% for the simulation, which increases slightly in case the switching frequency is reduced.
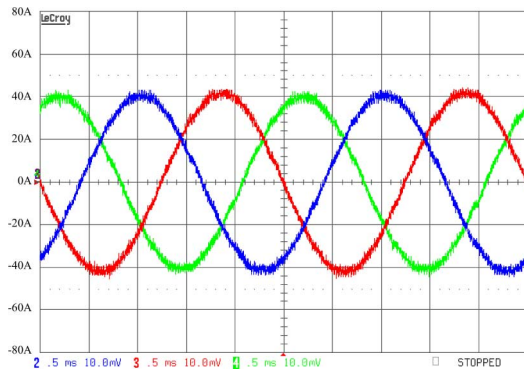
Fig. 15. Measured input currents for symmetric mains voltages and a switching frequency of 40 kHz at full load, i.e., 10 kW. (Scales: 20 A/div. and 0.5 ms/div.)
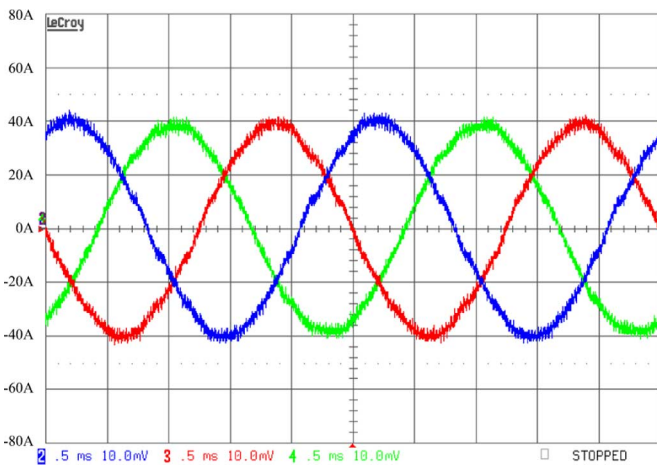

Fig. 16. Measured input currents at full load for mains voltages containing 5% of fifth harmonic and a switching frequency of 40 kHz. (Scales: 20 A/div. and 0.5 ms/div.)

Measurement results showing the behavior of the system during transient operation can be found in [30] and are omitted here for the sake of brevity.

B. Asymmetric Mains/Harmonic Rejection

The strength of the closed-loop current-control strategy lies is ability to track a sinusoidal reference current despite varying input-voltage space-vector amplitude and angular frequency. To demonstrate this feature, a simulation was performed with the input voltage containing 5% of the fifth harmonic. The resulting input current THD was 3.1%. In case the harmonic content is increases to 10% fifth harmonic, the THD increases to 4.7%. The related measurement results are shown in Fig. 16, which also show nearly sinusoidal mains currents. There, the distortions due to the control limitations of v_{LIT}^* are relatively small, as mentioned in Section III-C.

Also for unbalanced mains voltages, the closed-loop-controlled 12-pulse rectifier draws sinusoidal input currents, as shown in Fig. 17, where an unbalance of ±5% of the mains phase-voltage amplitudes is assumed. There, a THD of approx-
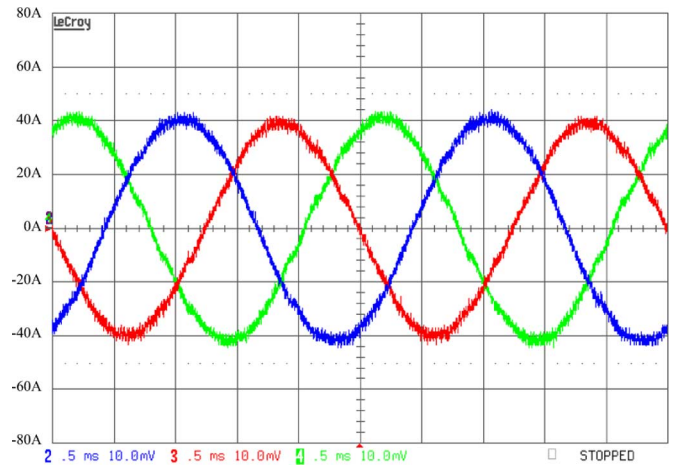

Fig. 17. Measured input currents at full load and an amplitude unbalance of ±5%. (Scales: 20 A/div and 0.5 ms/div.)

imately 3% results. Again, the measurement results verify that the controller is able to track a sinusoidal reference current.

V. CONCLUSION

This paper presents a novel current-control scheme for a hybrid 12-pulse rectifier employing an LIT. Starting from the basic principle of operation, the space-vector modulation and closed-loop control structure, which allows a direct control of the input-current space vector, are derived. The practical implementation of the control scheme has been explained, and experimental results are presented to verify the theoretical considerations.

The closed-loop current-control scheme not only allows the converter to draw a high-quality sinusoidal mains current, but also provides controllability of the current magnitude and/or of the output voltage. In a next step, a direct power control will be implemented and the integration of the boost inductors in the LIT will be investigated.

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