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***Abstract*—For realizing bidirectional and isolated AC/DC converters, soft-switching techniques/topologies seem to be a favourable choice as they enable a further loss and volume reduction of the system. Contrary to the traditional dual-stage approach, using a power factor corrector (PFC) stage in series with a DC/DC isolation stage, we showed recently that the same functionality can be achieved under full soft-switching operation using a single-stage dual active bridge (DAB) AC/DC converter. This paper investigates the performance of this single-stage approach by comparing it with a state-of-the-art conventional dual-stage concept (both soft-switching converters), where a bidirectional interleaved triangular current mode (TCM) PFC rectifier was chosen in combination with a DAB DC/DC converter. The advantages and drawbacks of each concept are discussed in detail, focusing on the impact of the utilized semiconductor technology and silicon area on the converter efficiency. Furthermore, a comprehensive comparison of power density is allowed by the analytical models that correlate the component losses with their respective volume.**

***Index Terms*—AC/DC converter, bidirectional, Dual Active Bridge, DAB, isolated, soft-switching**

I. Introduction

Isolated AC/DC converters are frequently employed in utility interfaced systems such as power supplies in telecommunication and data centers [1], [2], plug-in hybrid electrical vehicles (PHEVs) and battery electric vehicles (BEVs) [3], [4]. For these types of grid interfaced systems there is an increasing need for bidirectional functionality since the traditional electricity grid is evolving from a rather passive to a smart interactive service network (customers/operators) where the traditional central control philosophy is shifting to a more distributed control paradigm. Energy systems become active elements, providing different types of support to the grid [4], [5]. In all mentioned applications a storage element connected to the high-voltage (HV) DC-bus can facilitate this need for power feed-in into the grid [2], [4].

Recently we showed that bidirectional and isolated AC/DC converters can be realized under full soft-switching operation using a single-stage dual active bridge (DAB) topology (Fig. 1(a)) [6], allowing a possible enhancement of the performance (in terms of efficiency, volume, number of components and cost) compared to the traditional dual-stage topologies. In [6] a half bridge - full bridge DAB (Fig. 2(a)) was used. A similar analysis using a full bridge - full bridge DAB (Fig. 2(b)) was performed in [7], providing higher low load efficiency. In order to investigate the performance of both single-stage approaches, a comprehensive comparison with a state-of-the-art conventional dual-stage topology (PFC for rectification and power factor correction in series with a DC/DC converter for galvanic isolation and output voltage regulation) is presented in this paper. For the latter, an interleaved triangular current mode (TCM) PFC rectifier [8] in combination with an isolated full bridge - full bridge DAB DC-DC converter [9], [10], is selected (Figs. 1(b) and 2(b)), both bidirectional, soft-switching, and proven to have an excellent performance (in terms of efficiency and power density). Soft-switching techniques/topologies are preferred in every conversion stage as they enable further reduction of the losses and the volume of the system [11]. A direct comparison of the three converter concepts based on published data is not feasible due to different system specifications and technology standards. Performance indices of a power electronics converter (e.g. efficiency and power density) are competing and moreover strongly dependent on the underlying specifications and technology node. Therefore this paper focusses on a comparison which is based on common specifications, technology standards and detailed analytical loss and volume models. Converter models with the corresponding dimensioning criteria of the components are presented in Section II. Analytical loss and volume models of the main converter components are comprehensively discussed in Section III, allowing for a complete comparison of converter efficiency and power density in Section IV. Section IV also includes a Semiconductor chip Area based Converter Comparison (SAC^2) [12], enabling for optimal selection of the semiconductors with respect to the topology and the operating point, and providing a common Figure of Merit (FOM) for comparison: the required total semiconductor area.

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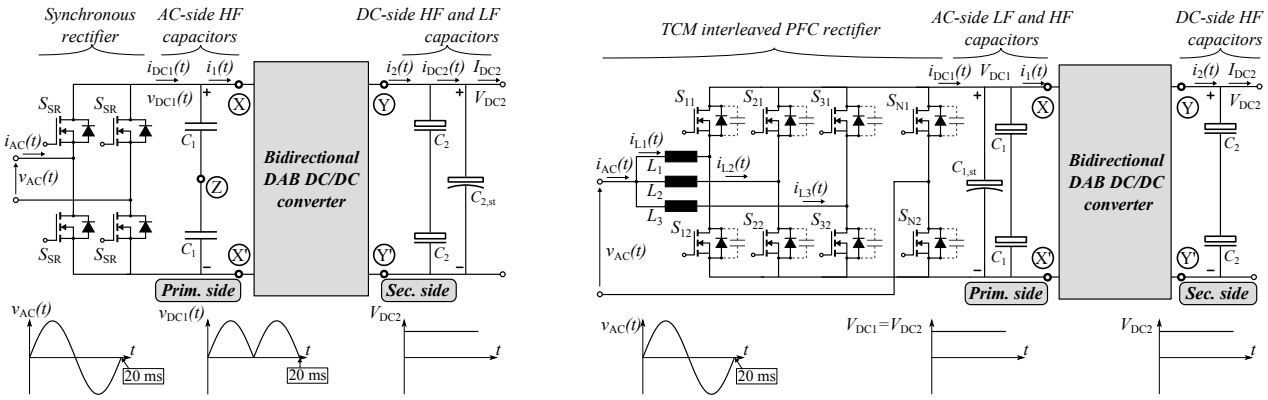


(a) Single-stage DAB AC/DC converter.

(b) Dual-stage AC/DC converter

Fig. 1. Schematics of the analyzed converter topologies.

II. Analytical Modeling and Control of the AC/DC Converter Concepts

The dimensioning criteria for each of the components in the following analysis are derived using common system specifications (Table I), covering the above mentioned application areas. A switching frequency of $f_s = 120$ kHz is assumed for all three topologies (i.e. the average frequency at nominal power for the variable frequency TCM PFC), being a trade-off between frequency related losses and volume. The three systems analyzed in this paper are controlled and designed in order to achieve unity power factor at the AC-side,

$$i_{AC}(t) = I_{AC} \sin(\omega t) \tag{1}$$

$$v_{AC}(t) = V_{AC} \sin(\omega t) \tag{2}$$

while satisfying the soft-switching constraints in the whole operating range. The soft-switching principle of the converter concepts is based on a quasi-resonant ZVS switching. Thereby, each high-frequency switch S_{xx} consists of a power transistor T_{xx}, a diode D_{xx}, and a parasitic nonlinear capacitor C_{xx}. Soft-switching operation occurs when a voltage transition is initiated by turn-off of the respective switch S_{xx}, commutating the current from the transistor T_{xx} to the opposite diode D_{xx} of the leg [11] (e.g. commutation from T_{p1} to D_{p2}, in Fig. 2(b), and turn-on of T_{p2} under ZVS (anti-parallel diode is conducting) after completion of the momentaneous resonant transition (quasi-resonant ZVS)). A faster commutation can be facilitated by setting a minimum to the switch turn-off current ($I_{comm,ref} = 2$ A is used), avoiding voltage transition delay and shoot through. It was shown in [10] that for the high voltage MOSFET transistors that are under consideration in this paper (Table III), low currents (0 A $\leqslant I_{comm} \leqslant$ 2 A) are insufficient to recharge the parasitic drain to source capacitors within a 200 ns dead-time interval, leading to increased switching losses. Whenever in the following considerations the semiconductor (active) chip area $A_{Si,act}$ is scaled, also a scaled minimum commutation current is used in all converter models:

$$I_{comm} = I_{comm,ref} \sqrt{A_{Si,act} / A_{Si,act,ref}} \tag{3}$$

TABLE I
Converter operating range

Property		*Value*
AC-side	$V_{AC,rms}$	230V (nominal) 207V $\leqslant V_{AC,rms} \leqslant$ 253V
	$I_{AC,rms,nom}$	16 A
	f_{grid}	50 Hz
DC-side	V_{DC2}	400V (nominal) 360V $\leqslant V_{DC2} \leqslant$ 440V

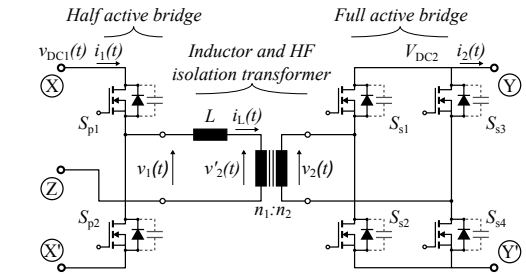
The commutation charge, and therefore also I_{comm} (3), scales with the square of the chip area $A_{Si,act}$ as the current crossing is triangular shaped. Distinction is made between the total Si area A_{Si} (thermal models) and the active chip area $A_{Si,act}$ (electrical models) of the semiconductor devices:

$$A_{Si,act} = 0.9864 \cdot A_{Si} - 1.3662 \text{ (mm}^2\text{)} \tag{4}$$

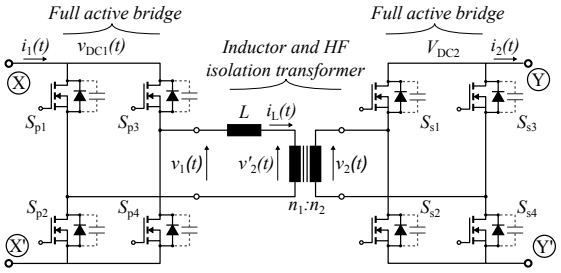
Relation (4) is derived from manufacter data of the considered semiconductor devices.

A. Single-Stage DAB AC/DC Converter Using a Half Bridge - Full Bridge DAB (SSHF converter)

Fig. 1(a) shows the general schematic of the single-stage DAB AC/DC topology, where a DAB DC/DC converter is used in combination with a synchronous rectifier, putting a small high-frequency (HF) filter capacitor C_1 in between. Here a half bridge - full bridge DAB DC/DC converter (Fig.2(a)) is used and the topology is further referred to as the SSHF (Single-Stage, Half bridge - Full bridge). The DAB receives the rectified AC line voltage $v_{DC1}(t)$ via the synchronous rectifier. It comprises HF transformer coupled primary side and secondary side active bridges, performing the DC voltage (V_{DC2}) regulation at the output, while maintaining unity power factor at the AC side by actively wave-shaping the line current $i_{DC1}(t)$. The control strategy presented in [6] for the SSHF enables soft-switching operation over the whole voltage and power range.



(a) Half bridge - full bridge DAB DC/DC converter



(b) Full bridge - full bridge DAB DC/DC converter

Fig. 2. Schematics of the bidirectional isolated DAB DC/DC converters used in the three analyzed converter concepts.

B. Single-Stage DAB AC/DC Converter Using a Full Bridge - Full Bridge DAB (SSFF converter)

In a second implementation of the single-stage DAB AC/DC topology, the half bridge - full bridge DAB DC/DC converter of the SSHF is replaced by a full bridge - full bridge DAB DC/DC converter (Fig. 2(b)). This topology is further referred to as the SSFF (Single-Stage, Full bridge - Full bridge). The control strategy to operate the SSFF is similar to the one for the SSHF and is presented in [7]. However, by using two full bridges, a higher flexibility in shaping the inductor current $i_{\mathrm{L}}(t)$ is achieved, resulting in lower partial load component RMS currents (partial load efficiency), at the expense of a higher number of active devices (volume, reliability, cost).

C. Dual-Stage AC/DC Converter Using an Interleaved TCM PFC in Series with a DAB DC/DC Converter (DS converter)

The dual-stage AC/DC converter in Fig. 1(b), and further referred to as the DS (Dual Stage) converter, uses an interleaved triangular current mode (TCM) PFC in series with a DAB full bridge - full bridge DC/DC converter (Fig. 2(b)). The TCM PFC [8] consists of several interleaved boost stages operating with variable switching frequency. The high TCM inductor current ripple is not transferred to the mains as the superposition of all boost cell input currents results in a smooth mains current waveform. It was shown in [8] that a number of three boost cells is a good compromise between volume and mains current distortion. The DAB DC/DC converter is operated with the same switching control strategy as the SSFF, adapted for constant input and output voltages ($V_{\mathrm{DC1}} = V_{\mathrm{DC2}}$).

The objective function for the derivation of the optimum values of the passive components is the average (over one half of the AC input period) of the square of the instantaneous switch RMS currents ($I^2_{\mathrm{S,eq,rms}}$, equation (7), minimization problem), resulting in the inductance values and transformer ratios depicted in Table II. The inductance values (L_{1-3}) for the TCM PFC are determined to obtain an average switching frequency of 120 kHz in the nominal operating point, applying a limit of $f_{\mathrm{s,max}} = 250\mathrm{kHz}$. It should be noted that for reaching the minimum commutation current in the secondary side active bridges of the DAB converters within the whole AC operating range, the HF transformer magnetizing inductances L_{M} depicted in Table II are used [6], [7]. Fig. 3 shows the typical current and voltage waveforms for the full bridge - full bridge DAB DC/DC converter (left) and the TCM PFC (right). In Fig. 4 the RMS currents $i_{\mathrm{S,rms}}(\omega t)$ occuring in the high-frequency switches during a half input sinewave interval (50 Hz) for the three converter concepts, at nominal input and output voltage, and 100%, 50% and 10% of the nominal input current is depicted.

TABLE II
INDUCTANCE VALUES AND TRANSFORMER RATIOS

DS converter		*SSHF converter*		*SSFF converter*	
L_{1-3}	60 μH				
L	27.6 μH	L	3 μH	L	11.2 μH
L_{M}	193 μH	L_{M}	33.8 μH	L_{M}	105.45 μH
n_1/n_2	1.25	n_1/n_2	0.5	n_1/n_2	1

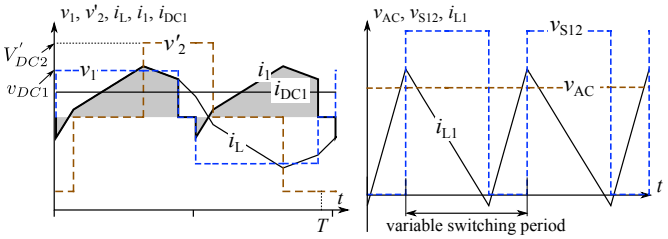


Fig. 3. Typical current and voltage waveforms for the full bridge - full bridge DAB converter (left) and the TCM PFC (right).

III. Loss and Volume Models

The switching losses for the soft-switching converter topologies presented in Section II are low, especially as the control equations assure a minimum switch commutation current. Therefore the most important loss contributions are the semiconductor conduction losses, the gate losses, and the losses in the passive components. As components losses and volume are mutually coupled (e.g. a large-sized transformer naturally has lower losses), accurate models that correlate these two quantities are required to analytically calculate the performance indices of a converter, such as efficiency and power density.

A. Semiconductor Losses

Conduction losses of a MOSFET are proportional to the on-resistance $R_{\mathrm{DS(on)}}$. However, for allowing direct comparison of different devices and device technologies it is more convenient to consider specific device characteristics by referring them to

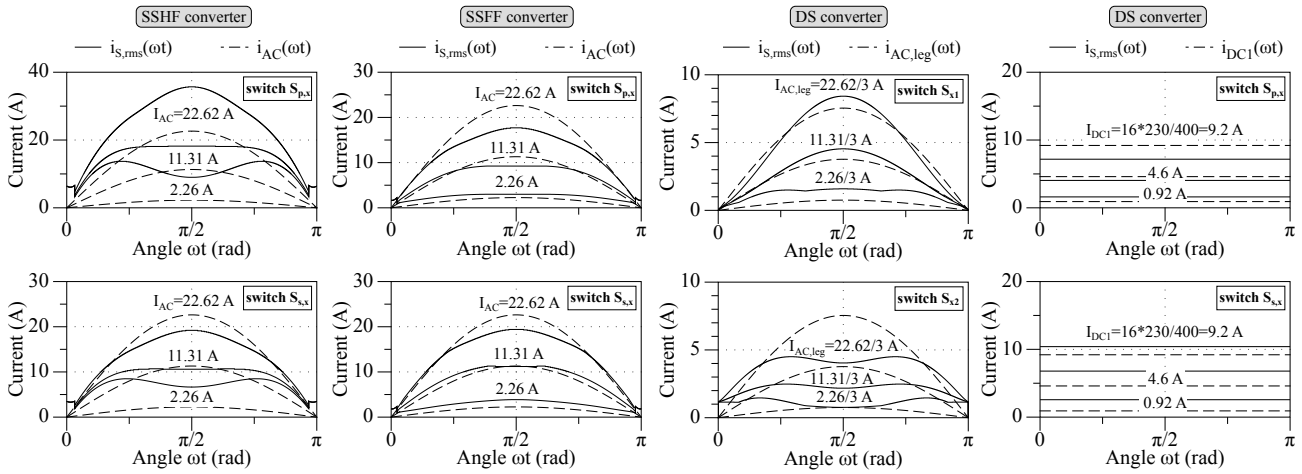


Fig. 4. RMS currents $i_{\mathrm{S,rms}}(\omega t)$ in the high-frequency switches at nominal input and output voltage, and 100%, 50% and 10% of the nominal input current.

the utilized active Si area $A_{\mathrm{Si,act}}$ (4). The conduction losses of a power MOSFET are then given by:

$$P_{\mathrm{S,cond}} = \frac{R^*_{\mathrm{DS,on}}}{A_{\mathrm{Si,act}}} I^2_{\mathrm{S,eq,rms}} \tag{5}$$

with $R^*_{\mathrm{DS,on}}$ the specific on-resistance, being a function of the juntion temperature T_{j} and the drain current density J_{D}:

$$\begin{aligned} R^*_{\mathrm{DS,on}} = R^*_{\mathrm{DS,on}} \,|_{T_{\mathrm{j}}=T_{\mathrm{j,ref}},\, J_{\mathrm{D}}=J_{\mathrm{D,ref}}} \\ \cdot (1 + \alpha_1 \Delta T_{\mathrm{j}} + \alpha_2 \Delta T_{\mathrm{j}}^2) \\ \cdot (1 + \beta_1 \Delta J_{\mathrm{D}} + \beta_2 \Delta J_{\mathrm{D}}^2) \end{aligned} \tag{6}$$

and

$$I^2_{\mathrm{S,eq,rms}} = \frac{1}{\pi} \int_0^{\pi} \left(i_{\mathrm{S,rms}}(\omega t)\right)^2 \mathrm{d}(\omega t) \tag{7}$$

ΔT_{j} and ΔJ_{D} are deviations from the reference junction temperature $T_{\mathrm{j,ref}}$ and the reference drain current density $J_{\mathrm{D,ref}}$. The specific on-resistance in dependence of J_{D} for different commercially available 600V MOSFET devices is presented in Fig. 5. Conduction losses in the internal body diodes are neglected as in normal operation they only conduct current during a very small time interval. As it is assumed that the transistor switching losses can be neglected (i.e. the turn-off commutation current is controlled to be high enough to assure lossless ZVS operation), the only switching frequency related losses are the gate losses:

$$P_{\mathrm{S,sw}} = P_{\mathrm{S,gate}} = f_{\mathrm{s}} \cdot \frac{Q^*_{\mathrm{G}} A_{\mathrm{Si,act}}}{U_{\mathrm{gs,ref}}} U^2_{\mathrm{gs}} \tag{8}$$

where Q^*_{G} is the specific total gate charge. A turn-on gate voltage of $U_{\mathrm{gs}} = 12\mathrm{V}$ is assumed for every switch. The MOSFET junction temperature T_{j} depends on the total MOSFET losses ($P_{\mathrm{S}} = P_{\mathrm{S,cond}} + P_{\mathrm{S,sw}}$) and the thermal resistance $R_{\mathrm{th,j\text{-}b}}$ between the die and the coolant (coldplate with isothermal bottom temperature $T_{\mathrm{b}} = 80°\mathrm{C}$), and is calculated by:

$$T_{\mathrm{j}} = P_{\mathrm{S}} R_{\mathrm{th,j\text{-}b}} + T_{\mathrm{b}} \tag{9}$$

Thermal equilibrium can be found by solving the interlinked equations for the power losses and the junction temperature (5), (8), (9). The specific parameters required for the calculation of the MOSFET losses are depicted in Table III.

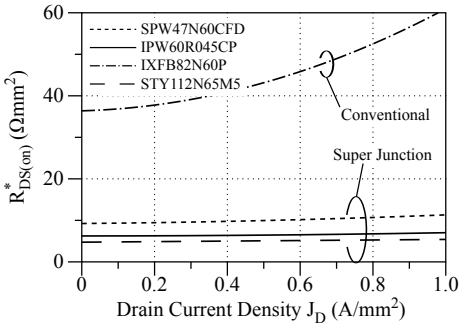


Fig. 5. Specific on-resistance of several 600 V MOSFETs in dependence of J_{D}, at $T_{\mathrm{j}} = 150°\mathrm{C}$.

TABLE III
SEMICONDUCTOR DEVICE PARAMETERS

MOSFET Parameters				
Device	U_{DSS} V	A_{Si} mm²	$R^*_{\mathrm{DS,on}}$ Ωmm²	Q^*_{G} nC/mm²
SPW47N60CFD	600	69.33	9.75	4.48
IPW60R045CP	600	69.16	6.77	2.70
IXFB82N60P	600	193	36.31	1.27
STY112N65M5	600	123	4.94	2.92

$R^*_{\mathrm{DS,on}}$ at $J^*_{\mathrm{D}} = 0.5\mathrm{A/mm}^2$ and $T_{\mathrm{j}} = 150°\mathrm{C}$

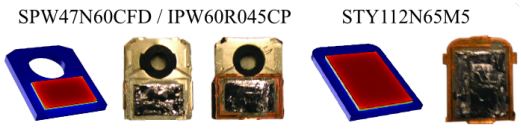


Fig. 6. Package interiors and FEM models, showing respectively the chip sizes and the temperature distribution for several of the semiconductor devices listed in Table III.

B. Semiconductor Volume

The volume occupied by each semiconductor device, V_{sem}, can be related to its losses when the relation between the thermal resistance $R_{\text{th,j-b}}$ and the dimensions of the transistor-cold plate assembly is known. The same transistor cooling concept is assumed for all topologies, consisting of an aluminium cold plate with a thickness of $h_{\text{CP}} = 8\text{mm}$ and constant bottom temperature $T_{\text{b}} = 80°\text{C}$, combined with a thermal pad, and the semiconductor packages (Fig. 7). A thickness of $h_{\text{pkg}} = 8\text{mm}$ is taken for the semiconductor package, including mounting with a screw, clamp or plate. The surface area of the coldplate is calculated from the Si area, taking into account the overhead caused by the packaging of the Si chips, the connection pins, and the space that is needed between two transistors when mounting them on a PCB. Therefore, when scaling the semiconductor area with a factor f_{Si}, each dimension is scaled with a factor $\sqrt{f_{\text{Si}}}$, allowing to determine the total area occopied by a semiconductor - cold plate assembly. By multiplying this area with the height ($h_{\text{CP}} + h_{\text{pkg}}$) of the assembly, the volume V_{sem} can be calculated.

Fig. 8 shows a simplified steady state thermal model of the semiconductor - cold plate assembly. The total thermal resistance between the MOSFET junction and the bottom of the cold plate consists of a series connection of the MOSFET junction-to-case thermal resistance $R_{\text{th,j-c}}$, the thermal resistance of the thermal pad $R_{\text{th,pad}} = {}^{h_{\text{pad}}}/_{k_{\text{pad}} A_{\text{pad}}}$, and the thermal resistance of the coldplate $R_{\text{th,t-b}} = {}^{h_{\text{CP}}}/_{k_{\text{CP}} A_{\text{CP}}}$. For each MOSFET type listed in Table III, the relation between $R_{\text{th,j-c}}$ and the Si area A_{Si} was detemined by detailed modeling of the package and FEM simulation, resulting in the relations depicted in Fig. 9. All analytical thermal models were validated through FEM simulations.

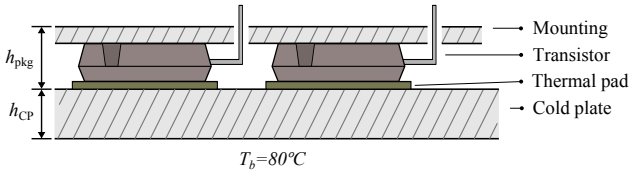


Fig. 7. Semiconductor-cold plate assembly. The packages are mounted onto an aluminium cold plate with isothermal bottom surface at 80°C.

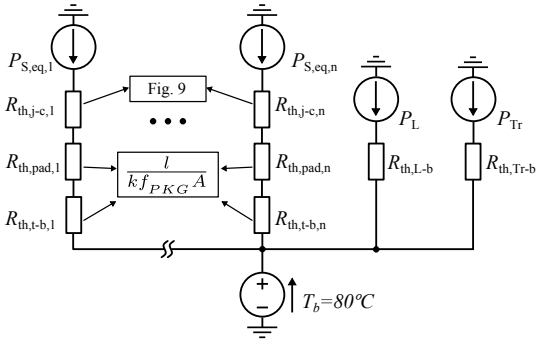


Fig. 8. Thermal network of the cold-plate assembly.

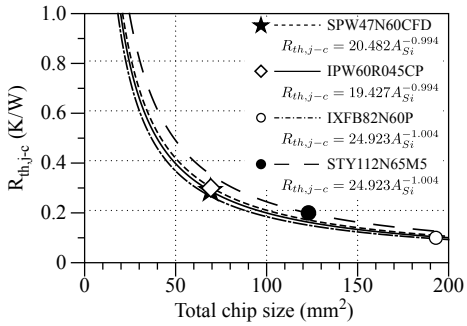


Fig. 9. Junction to case thermal resistance in dependence of the chip size for different 600 V MOSFETs. The relations are derived via modeling of the packages and FEM simulation. The datasheet values are indicated by marks.

C. Inductors and Transformers

Losses in inductors and transformers depend on the geometry and the arrangement of the windings, the type of wire, the core type, and the geometry and material of the core. The resulting (boxed) volume is mainly determined by the core geometry. In the scope of this paper, an optimization algorithm was developed to optimize each of the possible combinations. This allows to map a multi-dimensional design space into a multi-dimensional performance space for each inductor/transformer. The boundary of the feasible performance space indicates the best possible compromise with respect to different performance indices (i.e. efficiency (losses) and power density (volume)). For the optimization, planar cores are considered because of their advantageous properties with respect to high power density and excellent electromagnetic and thermal characteristics. All possible EELP and EILP core combinations from FERROXCUBE (core material: 3F3) and EPCOS (core material: N49, N87, and N92) in the dimensions range from ELP32 up to ELP64 were considered. The number of cores was limited by setting a maximum of 15cm to the total core length. Litz wires are chosen to reduce eddy current losses in the windings. All commercially available Litz wires from the RUPALIT Classic product range of PACK-FEINDRAHTE were taken into consideration. Four possible arrangements are investigated, including split, concentric, hexagonal and orthogonal type windings.

For each iteration, in a *first step* of the optimization algorithm the reluctance model R_{m} is calculated in order to meet the inductance values (L, L_{M}, $L_{1\text{-}3}$) depicted in Table II (the inductance is controlled with the air gap length l_{g}), while guaranteeing that the peak induction B_{pk} and air gap length l_{g} do not exceed a maximum value. This introduces an upper and lower limit for the number of turns (transformer primary side: n_1, inductor: N):

$$\frac{(V \cdot s)_{\text{prim,max}}}{2 B_{\text{pk,max}} A_{\text{c}}} \leqslant n_1 \leqslant \sqrt{L_{\text{M}} \left(R_{\text{m,core}} + R_{\text{m,air,max}} \,|_{l_{\text{g}}=l_{\text{g,max}}} \right)} \tag{10}$$

$$\frac{L I_{\text{L,pk}}}{B_{\text{pk,max}} A_{\text{c}}} \leqslant N \leqslant \sqrt{L \left(R_{\text{m,core}} + R_{\text{m,air,max}} \,|_{l_{\text{g}}=l_{\text{g,max}}} \right)} \tag{11}$$

The upper boundary of the maximum operating flux $B_{\text{pk,max}}$ is set by the core material saturation flux B_{sat}, applying a 20% safety margin to achieve low core losses and to avoid operation close to saturation. $(V \cdot s)_{\text{prim,max}}$ is the maximum Volt-seconds product (primary side of the transformer), A_{c} is the effective core cross section, and $I_{\text{L,pk}}$ the peak inductor current. The air gap reluctance $R_{\text{m,air}}$ is calculated using the 3D method proposed in [13]. In a *second step* the objective function is calculated (i.e. the total inductor/transformer losses), requiring detailed models of the winding losses and core losses. For each iteration the objective function is minimized within the design constraints such as the available window area. The *ohmic losses* in the Litz wires can be separated into skin effect losses $P_{\text{Litz,S}}$ from self-induced eddy currents inside the conductor, external proximity effect losses $P_{\text{Litz,P,e}}$ from eddy currents due to the external magnetic field H_{e} (originated in the air gap fringing field and the magnetic field from neighboring conductors), and internal proximity effect losses $P_{\text{Litz,P,i}}$ from eddy currents due to the internal magnetic field H_{i} (produced by the wire itself). The winding losses per unit length (index "l") can be calculated with [14]:

$$P_{\text{Litz,S,l}} = n_{\text{s}} \cdot R_{\text{DC}} \cdot F_{\text{R}}(f) \cdot \left(\frac{\hat{I}}{n_{\text{s}}} \right)^2 \tag{12}$$

$$P_{\text{Litz,P,l}} = P_{\text{Litz,P,e,l}} + P_{\text{Litz,P,i,l}} \tag{13}$$

$$P_{\text{Litz,P,l}} = n_{\text{s}} \cdot R_{\text{DC}} \cdot G_{\text{R}}(f) \cdot \left(\hat{H_e}^2 + \frac{\hat{I}^2}{2\pi^2 d_{\text{b}}^2} \right) \tag{14}$$

Here, R_{DC} is the per unit length DC resistance of a single strand of the Litz bundle, n_{s} the number of strands in the bundle, d_{b} the diameter of the bundle, and $\hat{I}$ the Fourier amplitude coefficients of the current time function $i_{\text{bundle}}(t)$. $F_{\text{R}}(f)$ and $G_{\text{R}}(f)$ are factors that model the frequency dependence of the losses and are given in [14], which also provides the 2D method used for calculating the external field H_{e}. The *Core losses* per unit volume (index "V") are calculated with the Steinmetz parameters k, α, β using the improved Generalized Steinmetz Equation (iGSE) [15]:

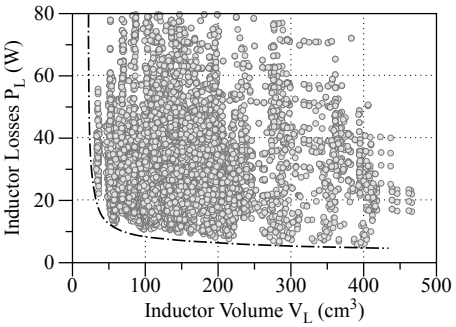
$$P_{\text{core,V}} = \frac{1}{T} \int_0^T k_{\text{i}} \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} (\Delta B)^{\beta - \alpha} \, \mathrm{d}t \tag{15}$$

The performance space for the SSHF inductor is depicted in Fig. 10(a). An overview of the boundaries of the performance spaces of all inductors/transformers is shown in Fig. 10(b). The designs that were chosen (marked) were thermally verified using a 2D nodal network (represented by $R_{\text{L-b}}$ and $R_{\text{Tr-b}}$ in Fig. 8), using the same coldplate as in Section III and assuming a maximum inner temperature of 120°C.

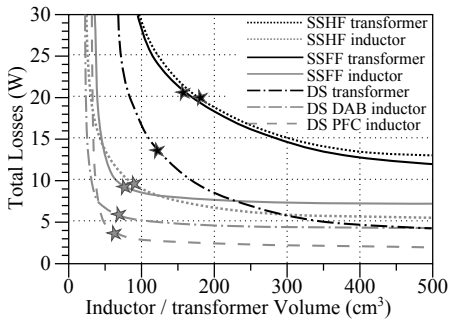
D. DC-Link Capacitors

The capacitance values required for keeping the 100Hz ripple amplitude $\hat{\tilde{u}}_{\text{st}}$ of the DC-link voltages within its limit ($\hat{\tilde{u}}_{\text{st,max}} = 0.05 \cdot V_{\text{DC,nom}}$) are calculated using:

$$C_{\text{st}} = \frac{Q_{\text{st}}}{2\hat{\tilde{u}}_{\text{st,max}}} \tag{16}$$



(a) Performance space of the SSHF DAB inductor.



(b) Boundaries of the performance spaces of all inductors/transformers. The chosen designs are marked.

Fig. 10. Results of the inductor/transformer optimization.

where the charge difference Q_{st} is determined by:

$$Q_{\text{st}} = \frac{1}{2} \int_0^{10ms} |i_{\text{C,st}}(t)| \, \mathrm{d}t \tag{17}$$

The capacitor current $i_{\text{C,st}}(t)$ is the difference between the incoming and outgoing current, $i_{\text{C,st}}(t) = i_{\text{C,st(in)}}(t) - i_{\text{C,st(out)}}(t)$. Given the operating range, the value of $C_{\text{st}} = 962.5\mu\text{F}$ is the same for each converter concept. For the capacitor volume calculations, electrolytic capacitors are chosen above film capacitors because of their lower volume/capacitance ratio, as can be seen from Fig. 11. For a given rated voltage the volume of EPCOS high density electrolytic B4345x 550V DC-link capacitors scales linearly with the capacitance, $V_{\text{C}} = k_{\text{C1}} + k_{\text{C2}} C = 88.8\ \text{cm}^3 + 0.1969\ \text{cm}^3/\mu\text{F} \cdot C$. In practice, the bulky 100Hz DC-link capacitors are often accompanied by small high-frequency capacitors, which can be polypropylene (PP) film type capacitors. However, they only account for a small portion of the total capacitor volume and are therefore not taken into account. The same remark can be made for the other high-frequency capacitors. The losses in the capacitors are neglected in this comparison.

E. EMI filters and Auxiliary Circuits

Typically, the losses in the EMI filters and auxiliary circuits only account for a very small portion of the total converter losses and are therefore neglected. Moreover, since it was not the intention of this paper to perform a detailed design of the EMI filter and auxiliary circuits for each topology, the volume occupied by these components is estimated based on the real prototype converters shown in Fig. 15.

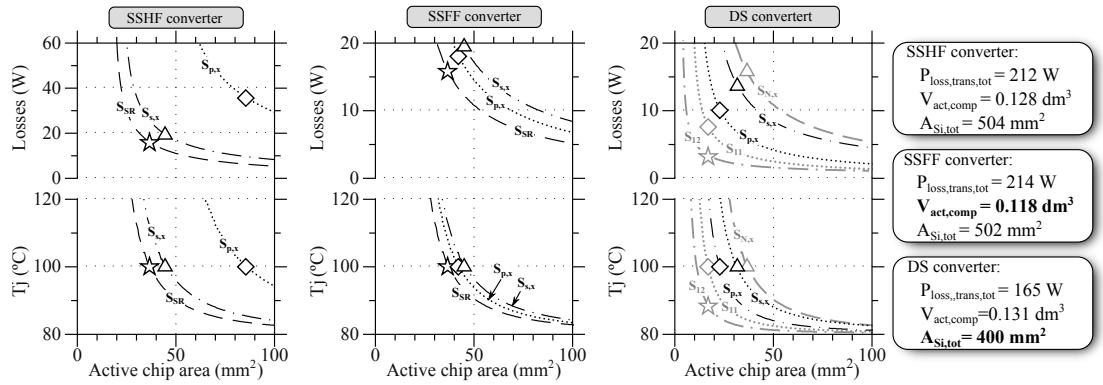


Fig. 12. Junction temperature and semiconductor losses (conduction + gate losses) in function of the active chip area, for the separate switches in each topology (IPW60R045CP MOSFETs, nominal operating conditions). For each switch, $A_{\mathrm{Si,act}}$ for $T_{\mathrm{j}} = 100°\mathrm{C}$ is marked.

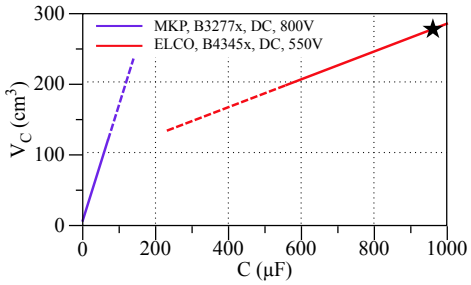


Fig. 11. Volume versus capacitance for Aluminium electrolytic and PolyPropylene DC-link capacitors (B4345x respectively B3277x, EPCOS).

IV. Topology Comparison

A. Semiconductor Chip Area Based Converter Comparison (SAC^2)

In order to allow for a fair comparison between the different topologies, the total chip area needed to not exceed a junction temperature T_{j} of 100°C in all semiconductor devices and at nominal operating conditions is used as a first comparison criterion. Therefore, the models described in Section III-A, correlating the thermal and electrical characteristics of the semiconductor devices to the chip area, are used. Fig. 12 shows the results of the SAC^2 for the IPW60R045CP MOSFET. The lowest total chip size was achieved with the DS converter, while the lowest volume (cold plate assembly + gate drivers) is for the SSFF topology. The SSHF has the worst chip area utilization.

B. Efficiency

Under the considerations of Section III, the converter efficiency is calculated from:

$$\eta = \frac{P_{\mathrm{AC,in}} - (P_{\mathrm{S,cond}} + P_{\mathrm{S,sw}} + \sum (P_{\mathrm{Litz}} + P_{\mathrm{core}})_{\mathrm{ind.,\ transf.}})}{P_{\mathrm{AC,in}}} \tag{18}$$

As semiconductor losses strongly depend on the specific device parameters and the chip area per switch, and due to the varying number of semiconductors, they can only be compared among the converter concepts for the same total Si area $A_{\mathrm{Si},\Sigma}$. For each device a weight factor γ_{i} is introduced that indicates the percentage of $A_{\mathrm{Si},\Sigma}$ and is calculated in relation to the sum of all RMS currents ($\gamma_{\mathrm{i}} = I^2_{\mathrm{eq,rms,i}} / \sum I^2_{\mathrm{eq,rms,i}}$). The calculated efficiency of all converter concepts is depicted in Fig. 13. STY112N65M5 MOSFETs, having the lowest $R^*_{\mathrm{DS,on}}$, are used in the synchronous rectifier of the single stage topologies (switches S_{SR}), as well as in the low-frequency leg of the TCM PFC (switches $S_{\mathrm{N,x}}$). In the DABs of all topologies (switches $S_{\mathrm{p,x}}$, $S_{\mathrm{s,x}}$), and in the high-frequency legs of the TCM PCF (switches $S_{\mathrm{x,x}}$), IPW60R045CP MOSFETs are used because of their better switching characteristics. The DS converter has the highest efficiency at nominal power, while the SSFF converter shows the best partial load performance. The SSHF converter has the worst efficiency, both at nominal power and at partial load.

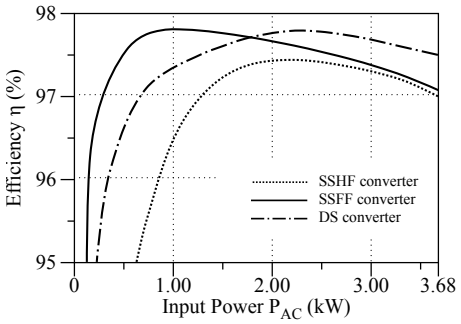


Fig. 13. Calculated efficiency of the SSHF, the SSFF, and the DS converters.

C. Power Density

Weight and volume limitations cause the power density to be an important performance index for the analyzed AC/DC converter concepts, especially in automotive applications, and can be estimated from:

$$\rho = \frac{P_{\mathrm{DC,out}}}{(1 + f_{\mathrm{pack}})(V_{\mathrm{sem}} + V_{\mathrm{GD}} + V_{\mathrm{Tr.}} + V_{\mathrm{Ind.}} + V_{\mathrm{C}} + V_{\mathrm{x}})} \tag{19}$$

where V_{GD} is the volume of the gate drivers, and V_{x} the volume of the auxiliary circuits, EMI filter and control board. In the

following, V_x is estimated based on the existing prototypes shown in Fig. 15. A factor $f_{pack} = 30\%$ accounts for the increase in volume due to non-ideal packing, interconnection of the components, and not considered small components (e.g. the high-frequency capcitors). As the correlation between converter losses and volume is conflicting, a comparison of ρ is only meaningfull in consideration of the same efficiency. Therefore a total inductor and transformer loss of 35W is aasumed, and the total Si area $A_{Si,\Sigma}$ is determined to obtain an efficiency of $\eta = 97.2\%$ at nominal operating conditions. The converter volumes for the different converter concepts are given in Fig. 14. The calculations predict the lowest volumes (highest power density) for the single stage converter concepts.

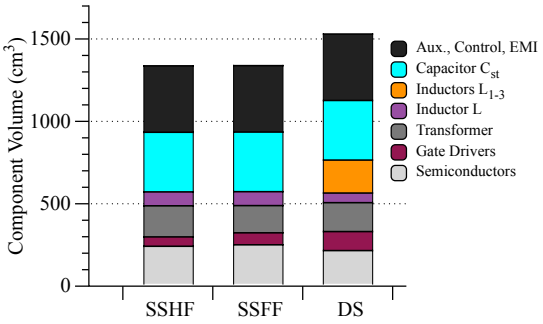


Fig. 14. Converter volumes for obtaining a nominal load efficiency of $\eta = 97.2\%$. $A_{Si,SSHF} = 1357mm^2$, $A_{Si,SSFF} = 1346mm^2$, $A_{Si,DS} = 889mm^2$.

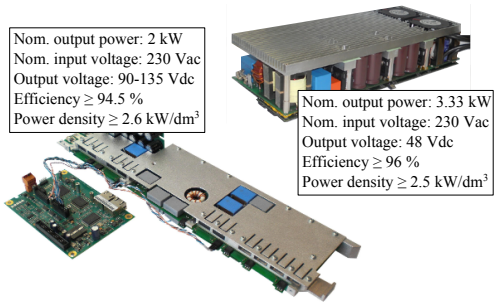


Fig. 15. Experimental prototypes of the SSHF (left) and DS (right), bidirectional, isolated AC/DC converters.

V. Conclusion

A comparative evaluation of three soft-switching, bidirectional, isolated AC/DC converter concepts is presented. A chip area based comparison (SAC^2) shows an advantage for the conventional DS converter concept since the semiconductor area is better utilized. This reflects in the highest efficiency in nominal operating conditions. In partial load the SSFF outperformes the DS converter as the variable frequency TCM PFC suffers from high RMS currents during low load (switching frequency limit). The SSHF has the worst semiconductor utilisation, resulting in the lowest overall efficiency. Concerning component count and power density, the single-stage concepts are advantageous as they use less active components and show a lower volume for the passive components, being also a cost and reliability advantage. The volume benefit of the single-stage concepts becomes even bigger when being used in a three-phase configuration, as the bulky 100Hz capacitor can be ommited. Disadvantageous for the dual-stage converter is also the variable switching frequency operation of the TCM PFC, while the single-stage converters cannot assure a flat output-bus DC voltage in a single-phase configuration. Experimental prototypes of the SSHF and DS validate the conclusions of the theoretical analysis.

References

[1] A. Stupar, T. Friedli, J. Miniböck, M. Schweizer, and J. W. Kolar, "Towards a 99% Efficient Three-Phase Buck-Type PFC Rectifier for 400 V DC Distribution Systems," in *IEEE 26th Applied Power Electronics Conference and Exposition (APEC 2011)*, March 2011, pp. 505–512.

[2] A. Matsumoto, A. Fukui, T. Takeda, and M. Yamasaki, "Development of 400-Vdc Output Rectifier for 400-Vdc Power Distribution System in Telecom Sites and Data Centers," in *32nd International Telecommunications Energy Conference (INTELEC 2010)*, June 2010, pp. 1–6.

[3] A. Emadi, S. S. Williamson, and A. Khaligh, "Power Electronics Intensive Solutions for Advanced Electric, Hybrid Electric, and Fuel Cell Vehicular Power Systems," *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 567–577, May 2006.

[4] K. Clement-Nyns, E. Haesen, and J. Driesen, "The Impact of Vehicle-to-Grid on the Distribution Grid," *Electric Power Systems Research*, vol. 81, no. 1, pp. 185–192, 2011. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0378779610002063

[5] Directorate-General for Research and Innovation, European Commission. (2005) Towards Smart Power Networks, Lessons Learned from European Research FP5 Projects. [Online]. Available: http://ec.europa.eu/research/energy/eu/publications/index_en.cfm

[6] J. Everts, J. Van den Keybus, and J. Driesen, "Switching Control Strategy to Extend the ZVS Operating Range of a Dual Active Bridge AC/DC Converter," in *IEEE Energy Conversion Congress and Exposition (ECCE 2011)*, Sept. 2011, pp. 4107–4114.

[7] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J. W. Kolar, "Switching Control Strategy for Full ZVS Soft-Switching Operation of a Dual Active Bridge AC/DC Converter," in *IEEE 27th Applied Power Electronics Conference and Exposition (APEC 2012)*, Feb. 2012.

[8] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) Resonant Transition, Single Phase PFC Rectifier with High Efficiency and High Power Density," in *International Power Electronics Conference (IPEC 2010)*, June 2010, pp. 1725–1732.

[9] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching Control Strategy to Minimize Dual Active Bridge Converter Losses," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1826–1838, July 2009.

[10] F. Krismer and J. W. Kolar, "Accurate Power Loss Model Derivation of a High-Current Dual Active Bridge Converter for an Automotive Application," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 881–891, March 2010.

[11] S. Waffler and J. W. Kolar, "Comparative Evaluation of Soft-Switching Concepts for Bi-Directional Buck+Boost DC-DC Converters," in *International Power Electronics Conference (IPEC 2010)*, June 2010, pp. 1856–1865.

[12] T. Friedli and J. W. Kolar, "A Semiconductor Area Based Assessment of AC Motor Drive Converter Topologies," in *IEEE 24th Applied Power Electronics Conference and Exposition (APEC 2009)*, Feb. 2009, pp. 336–342.

[13] J. Muhlethaler, J. W. Kolar, and A. Ecklebe, "A Novel Approach for 3D Air Gap Reluctance Calculations," in *IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE ECCE 2011)*, June 2011, pp. 446–452.

[14] ——, "Loss Modeling of Inductive Components Employed in Power Electronic Systems," in *IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE ECCE 2011)*, June 2011, pp. 945–952.

[15] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate Prediction of Ferrite Core Loss with Nonsinusoidal Waveforms Using only Steinmetz Parameters," in *IEEE Workshop on Computers in Power Electronics*, June 2002, pp. 36–41.