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Optimal Design of *LCL* Harmonic Filters for Three-Phase PFC Rectifiers

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***Abstract*—Inductive components such as line filter inductors or transformers occupy a significant amount of space in today's power electronic systems, and furthermore, considerable losses occur in these components. A main application of inductive components is EMI filters, as, e.g., employed for the attenuation of switching frequency harmonics of power factor correction (PFC) rectifier systems. In this paper, a design procedure for the mains side *LCL* filter of an active three-phase rectifier is introduced. The procedure is based on a generic optimization approach, which guarantees a low volume and/or low losses. Different designs are calculated to show the tradeoff between filter volume and filter losses. The design procedure is verified by experimental measurements. Furthermore, an overall system optimization, i.e., an optimization of the complete three-phase PFC rectifier, is given.**

***Index Terms*—*LCL* filter, magnetic components, optimization.**

I. Introduction

THE trend in power electronics research is toward higher efficiency and higher power density of converter systems. This trend is driven by cost considerations (e.g., material economies), space limitations, (e.g., for automotive applications), and increasing efficiency requirements (e.g., for telecom applications). The increase of the power density often affects the efficiency, i.e., a tradeoff between these two quality indices exists [1].

Inductive components occupy a significant amount of space in today's power electronic systems, and furthermore, considerable losses occur in these components. In order to increase the power density and/or efficiency of power electronic systems, losses in inductive components must be reduced, and/or new cooling concepts need to be investigated.

At the Power Electronic Systems Laboratory at ETH Zurich, a project has been initiated with the goal to establish comprehensive models of inductive power components which can be adapted to various geometric properties, operating conditions, and cooling conditions. These models will form the basis for the optimization of inductive components employed in key power electronics applications.

Numerous papers have been written about how to find optimal designs of power electronic systems, whereas the goal of the according optimization task can be minimum costs, volume, losses, etc. Some papers investigated parts of a system, some others tried to model and optimize the overall system. For instance, in [2], an overall optimization of a two-FET forward converter is presented. For it, a two-stage optimization method to optimize the efficiency from light load to full load is proposed. Another approach to conduct an overall optimization is given in [3], where a flyback converter has been optimized. In [4], an overall optimization of a boost power factor correction (PFC) converter including the input electromagnetic interference filter is conducted. Examples of papers in which the focus is put only on parts of a system are, e.g., given in [5] and [6]. In [5], it is shown on the example of a buck converter, how the capacitors of a dc-link capacitor tank are selected optimally. In [6], a design methodology that finds the volumetric optimized inductors employed in single-phase PFC boost converters is given, whereas the corresponding optimum switching frequency and input current ripple is found.

The aim of this paper is to use the recently established comprehensive models of inductive power components to optimally design *LCL* input filters for a three-phase PFC rectifier. The focus of the paper at hand is put on the optimal design of the *LCL* harmonic filters. LCL input filters are an attractive solution to attenuate switching frequency current harmonics of active voltage source rectifiers [7], [8]. In this paper, a design procedure for *LCL* filters based on a generic optimization approach is introduced guaranteeing low volume and/or low losses. Different designs are calculated showing the tradeoff between filter volume and filter losses. Furthermore, it is shown at the end of this paper how an overall system optimization, i.e., an optimization of the complete three-phase PFC rectifier (not only the filter), could be conducted. It is important to consider the complete system, since there are parameters that bring advantages for one subsystem but bring disadvantages for another. For instance, in the selected example of an *LCL* input filter, a higher switching frequency leads to lower volume, or, when keeping the volume constant, to lower losses of the inductive components. However, higher semiconductor switching losses are expected in the case of higher switching frequencies.

In Section II, the three-phase PFC rectifier is introduced; in Section III, the applied models of the *LCL* filter components are discussed; and in Section IV, the optimization algorithm for the *LCL* filter is described. Simulation and experimental results

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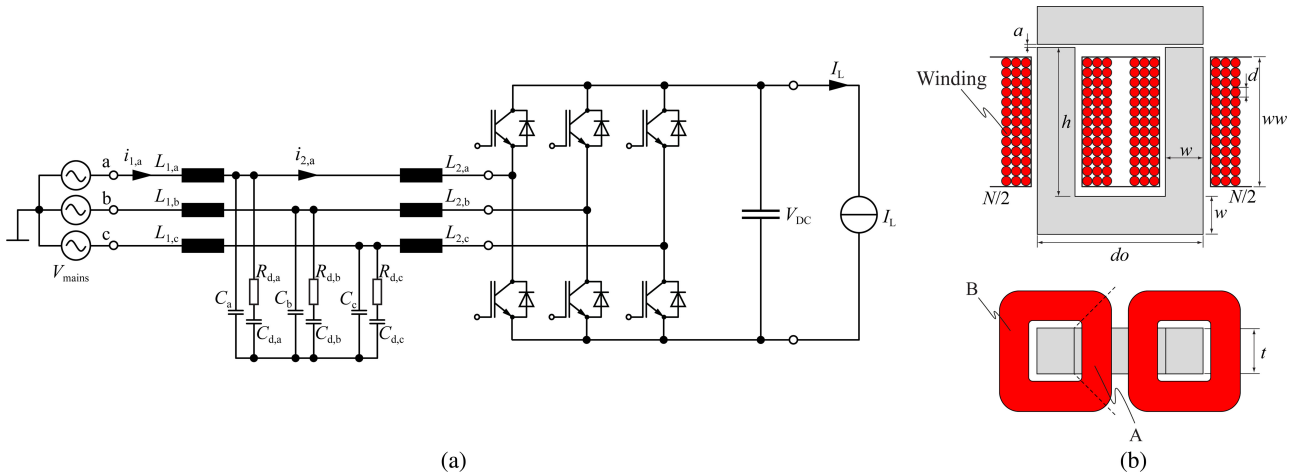

Fig. 1. (a) Three-phase PFC rectifier with *LCL* input filter. (b) Cross sections of inductors employed in the input filter.

TABLE I
SPECIFICATION OF THE THREE-PHASE PFC RECTIFIER

Parameter	Variable	Value	
Input Voltage AC	V_{mains}	230	V
Mains Frequency	f_{mains}	50	Hz
DC-Voltage	V_{DC}	650	V
Load Current	I_{L} (nominal)	15.4	A
Switching Frequency	f_{sw}	8	kHz

are given in Sections V and VI, respectively. In Section VII, the converter volume and losses are taken into consideration, i.e., an overall system optimization is performed.

II. Three-Phase PFC Rectifier With Input Filter

The three-phase PFC rectifier investigated in this paper is shown in Fig. 1. The rectifier comprises in each phase a boost inductor L_2, a damped *LC* filter $L_1/C/C_d/R_d$, and a pair of switches with free-wheeling diodes. The load is assumed to be a dc current source. The considered operating point of the PFC rectifier is described in Table I. A space vector modulation (SVM) scheme with loss-optimal clamping has been implemented to have a fundamental displacement factor of $\cos\phi = 1$. In the applied SVM scheme with loss-optimal clamping, a switching of the phase with the highest current is omitted; hence, the switching losses are reduced accordingly. The functionality and the detailed control of the used SVM scheme are described in [9]. The three-phase PFC rectifier with input filter has been simulated in MATLAB/Simulink, where the nonlinearity of the core material of the inductors, i.e., the change of the inductance value with changing current, is taken into account.

The three inductors $L_{1,a}$, $L_{1,b}$, and $L_{1,c}$, and the three capacitors C_a, C_b, and C_c in star arrangement, together with the three boost inductors $L_{2,a}$, $L_{2,b}$, and $L_{2,c}$, result in a third-order *LCL* low-pass filter between the mains and the switching stage. The capacitor/resistor branches $C_{d,a}/R_{d,a}$, $C_{d,b}/R_{d,b}$, and $C_{d,c}/R_{d,c}$ are necessary to damp the resonance of the *LC* input filter. All inductors are assumed to have the same geometry, which is illustrated in Fig. 1(b). The cores are made of grain-oriented steel (M165-35S, lamination thickness 0.35 mm). Solid copper wire is taken for the conductors. The windings are divided into two halves arranged on the two legs which lead to a more distributed winding structure. A more distributed winding structure has advantages such as better heat dissipation capabilities, lower inductor volume, etc.

III. Modeling of Input Filter Components

The loss modeling is based on the framework introduced in [10], where a high level of accuracy has been achieved by combining the best state-of-the-art approaches and by embedding newly developed approaches into a novel loss calculation framework. In [10], the impact of the peak-to-peak flux density ΔB, frequency f, dc premagnetization H_{DC}, temperature T, core shape, minor and major BH-loops, flux waveform, and material on the core loss calculation has been considered. In order to calculate the winding losses, formulas for round conductors and litz wires, each considering skin and proximity effects and also considering the influence of an air gap fringing field have been included. In the following, a discussion about the implemented models for the employed inductors [cf., Fig. 1(b)] is given.

A. Calculation of the Inductance

The inductance of an inductive component with N winding turns and a total magnetic reluctance $\mathcal{R}_{\mathrm{m,tot}}$ is calculated as

$$L = \frac{N^2}{\mathcal{R}_{\mathrm{m,tot}}}. \tag{1}$$

Accordingly, the reluctance of each section of the flux path has to be derived first in order to calculate $\mathcal{R}_{\mathrm{m,tot}}$. The total reluctance for a general inductor is calculated as a function of the core reluctances and air gap reluctances. The core and air gap reluctances can be determined applying the methods described in [11]. The reluctances of the core depend on the relative permeability μ_{r} which is defined by the nonlinear BH-relation of the core material; hence, the reluctance is described as a function of the flux. Therefore, as the flux depends on the core reluctance and the reluctance depends on the flux, the system

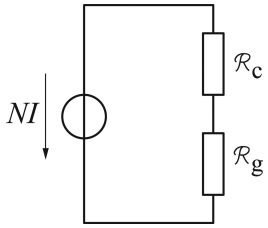

Fig. 2. Reluctance model of the inductor shown in Fig. 1(b). It consists of one voltage source (representing the two separated windings), one air gap reluctance $\mathcal{R}_g$ (representing the two air gaps), and one core reluctance $\mathcal{R}_c$.

can only be solved iteratively by using a numerical method. In the case at hand, the problem has been solved by applying the Newton approach.

The reluctance model of the inductor shown in Fig. 1(b) is illustrated in Fig. 2. It consists of one voltage source (representing the two separated windings), one air gap reluctance $\mathcal{R}_g$ (representing the two air gaps), and one core reluctance $\mathcal{R}_c$. The fact that the flux density in core parts very close to the air gap is (slightly) reduced as the flux lines already left the core has been neglected.

B. Core Losses

The applied core loss approach is described in [10] in detail and can be seen as a hybrid of the *improved–improved Generalized Steinmetz Equation* i²GSE [12] and a loss map approach: a loss map is experimentally determined and the interpolation and extrapolation for operating points in between the measured values is then made with the i²GSE.

The flux density waveform for which the losses have to be calculated is, e.g., simulated in a circuit simulator, where the magnetic part is modeled as a reluctance model. This simulated waveform is then divided into its fundamental flux waveform and into piecewise linear flux waveform segments. The loss energy is then derived for the fundamental and all piecewise linear segments, summed up and divided by the fundamental period length in order to determine the average core loss. The dc flux level of each piecewise linear flux segment is considered, as this influences the core losses [13]. Furthermore, the relaxation term of the i²GSE is evaluated for each transition from one piecewise linear flux segment to another.

Another aspect to be considered in the core loss calculation is the effect of the core shape/size. By introducing a reluctance model of the core, the flux density can be calculated. Subsequently, for each core section with (approximately) homogenous flux density, the losses can be determined. In the case at hand, the core has been divided into four straight core sections and four corner sections. The core losses of the sections are then summed up to obtain the total core losses.

C. Winding Losses

The second source of losses in inductive components is the ohmic losses in the windings. The resistance of a conductor increases with increasing frequency due to eddy currents. Self-induced eddy currents inside a conductor lead to the skin effect.

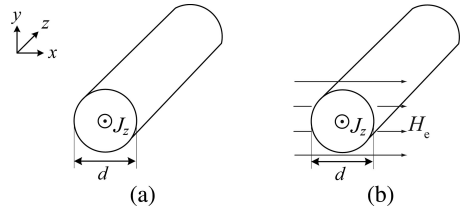

Fig. 3. Cross section of the round conductor considered with a current in z-direction. The conductor is infinitely large in z-direction.

Eddy currents due to an external alternating magnetic field, e.g., the air gap fringing field or the magnetic field from other conductors, lead to the proximity effect.

The sum of the dc losses and the skin effect losses per unit length in round conductors [cf., Fig. 3(a)] can be calculated as [14]

$$P_S = R_{\mathrm{DC}} \cdot F_R(f) \cdot \hat{I}^2 \tag{2}$$

and[1]

$$F_R(f) = \frac{\xi}{4\sqrt{2}}\left(\frac{\mathrm{ber}_0(\xi)\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} - \frac{\mathrm{bei}_0(\xi)\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2}\right) \tag{3}$$

with $\delta = \frac{1}{\sqrt{\pi\mu_0\sigma f}}, \xi = \frac{d}{\sqrt{2}\delta}, R_{\mathrm{DC}} = \frac{4}{\sigma\pi d^2}$; δ is commonly named the skin depth, f is the frequency, d is the conductor diameter, and σ is the electric conductivity of the conductor material.

The proximity effect losses in round conductors [cf., Fig. 3(b)] per unit length can be calculated as [14]

$$P_P = R_{\mathrm{DC}} \cdot G_R(f) \cdot \hat{H}_e^2 \tag{4}$$

and

$$G_R(f) = -\frac{\xi\pi^2 d^2}{2\sqrt{2}}\left(\frac{\mathrm{ber}_2(\xi)\mathrm{ber}_1(\xi) + \mathrm{ber}_2(\xi)\mathrm{bei}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} + \frac{\mathrm{bei}_2(\xi)\mathrm{bei}_1(\xi) - \mathrm{bei}_2(\xi)\mathrm{ber}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2}\right). \tag{5}$$

R_{DC} is the resistance per unit length; hence, the losses P_S and P_P are losses per unit length as well. The external magnetic field strength H_e of every conductor has to be known when calculating the proximity losses. In the case of an ungapped core and windings that are fully enclosed by core material, 1-D approximations to derive the magnetic field exist. The most popular method is the Dowell method [16]. However, in the case of gapped cores, such 1-D approximations are not applicable as the fringing field of the air gap cannot be described in a 1-D manner. For the employed gapped cores, another approach has to be selected. The applied approach is a 2-D approach and is

[1]The solution for F_R (and G_R) is based on a *Bessel differential equation* that has the form $x^2y'' + xy' + (k^2x^2 - v^2)y = 0$. With the general solution $y = C_1\mathbb{J}_v(kx) + C_2\mathbb{Y}_v(kx)$, whereas $\mathbb{J}_v(kx)$ is known as *Bessel function of the first kind* and order v and $\mathbb{Y}_v(kx)$ is known as *Bessel function of the second kind* and order v [15]. Furthermore, to resolve $\mathbb{J}_v(kx)$ into its real and imaginary part, the *Kelvin functions* can be used: $\mathbb{J}_v(\mathrm{j}^{\frac{3}{2}}x) = \mathrm{ber}_v x + \mathrm{j}\,\mathrm{bei}_v x$.

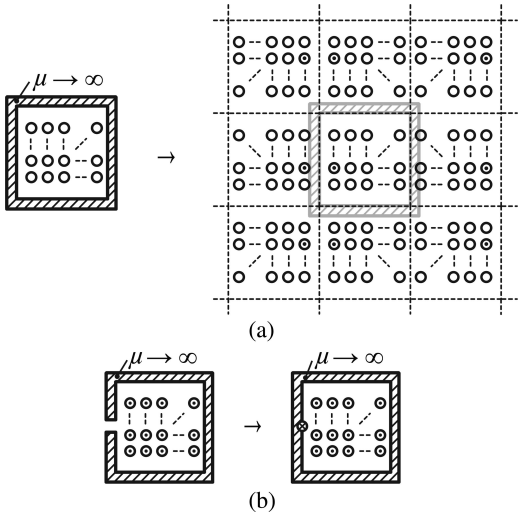

Fig. 4. (a) Illustration of the *method of images* (mirroring). (b) Illustration of modeling an air gap as a fictitious conductor.

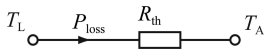

Fig. 5. Thermal model with only one thermal resistance.

described in detail in [10], where it has been implemented based on a previously presented work [17].

The magnetic field at any position can be derived as the superposition of the fields of each of the conductors. The impact of a magnetic conducting material can further be modeled with the *method of images*, where additional currents that are the mirrored version of the original currents are added to replace the magnetic material [17]. In case of windings that are fully enclosed by magnetic material (i.e., in the core window), a new wall is created at each mirroring step as the walls have to be mirrored as well. The mirroring can be continued to pushing the walls away. This is illustrated in Fig. 4(a). For this study, the mirroring has been stopped after the material was replaced by conductors three times in each direction. The presence of an air gap can be modeled as a fictitious conductor without eddy currents equal to the magneto-motive force across the air gap [17] as illustrated in Fig. 4(b).

According to the previous discussion, the winding losses have to be calculated differently for the sections A and B illustrated in Fig. 1(b), as the mirroring leads to different magnetic fields.

D. Thermal Modeling

A thermal model is important when minimizing the filter volume, as the maximum temperature allowed is the limiting factor when reducing volume. The model used in this paper consists of only one thermal resistance $R_{\rm th}$ and is illustrated in Fig. 5. The inductor temperature T_L is assumed to be homogenous; it can be calculated as

$$T_L = T_A + P_{\rm loss} R_{\rm th} \tag{6}$$

where $P_{\rm loss}$ are the total losses occurring in the inductor, consisting of core and winding losses, and T_A is the ambient temperature. The ambient temperature T_A is assumed to be constant at $25\,^{\circ}$C.

The heat transfer due to convection is described with

$$P = \alpha A (T_L - T_A) \tag{7}$$

where P is the heat flow, A the surface area, T_L the body surface temperature (i.e., inductor temperature), and T_A the fluid (i.e., ambient air) temperature. α is a coefficient that is determined by a set of characteristic dimensionless numbers, the Nusselt, Grashof, Prandtl, and Rayleigh numbers. Radiation has to be considered as a second important heat transfer mechanism and is described by the Stefan–Boltzmann law. Details about thermal modeling are not given here; the interested reader is referred to [18], from where the formulas used in this paper have been taken.

E. Capacitor Modeling

The filter and damping capacitors are selected from the EPCOS X2 MKP film capacitors series, which have a rated voltage of 305 V. The dissipation factor is specified as $\tan\delta \leq 1$ W/kvar (at 1 kHz) [19], which enables the capacitor loss calculation. The capacitance density to calculate the capacitors volume can be approximated with $0.18\,\mu$F/cm^3. The capacitance density has been approximated by dividing the capacitance value of several components by the according component volume.

F. Damping Branch

An *LC* filter is added between the boost inductor and the mains to meet a total harmonic distortion (THD) constraint. The additional *LC* filter changes the dynamics of the converter and may even increase the current ripple at the filter resonant frequency. Therefore, a C_d/R_d damping branch has been added for damping. In [20] and [21], it is described how to optimally choose C_d and R_d. Basically, there is a tradeoff between the size of damping capacitor C_d and the damping achieved. For this study, $C_d = C$ has been selected as it showed to be a good compromise between additional volume needed and a reasonable damping achieved. Hence, the volume of the damping capacitor is the same as the volume of the filter capacitor. The value of the damping resistance that leads to optimal damping is then [20], [21]

$$R_d = \sqrt{2.1 \frac{L_1}{C}}. \tag{8}$$

The C_d/R_d damping branch increases the reactive power consumption of the PFC rectifier system. Therefore, often other damping structures, such as the R_f-L_b series damping structure, are selected [21]. For this study, however, the C_d/R_d damping branch has been favored as its practical realization is easier and lower losses are expected. Furthermore, as will be seen in Section V, the reactive power consumption of the PFC rectifier system including the damped *LC* input filter is in the case at hand rather small, and, if necessary, it could be actively compensated by the rectifier.

The losses in the damping branch, which occur mainly in the resistors, are calculated and taken into consideration in the optimization procedure as well.

IV. Optimization of the Input Filter

The aim is to optimally design a harmonic filter of the introduced three-phase PFC rectifier. For the evaluation of different filter structures, a cost function is defined that weights the filter losses and filter volume according to the designer needs. In the following, the steps toward an optimal design are described. All steps are illustrated in Fig. 6. The optimization constraints are discussed first.

A. Optimization Constraints and Conditions

The high-frequency ripple in the current $i_{2,a/b/c}$ is limited to the value $I_{\mathrm{HF,pp,max}}$, which is important as a too high $I_{\mathrm{HF,pp,max}}$, e.g., impairs controllability (for instance, an accurate current measurement becomes more difficult). Furthermore, the THD of the mains current is limited. In industry, a typical value for the THD that is required at the rated operating point is 5 % [22]. In the design at hand, a THD limit of 4 % is selected in order to have some safety margin. Two other design constraints are the maximum temperature $T_{\max}$ and the maximum volume $V_{\max}$ the filter is allowed to have. A fixed switching frequency f_{sw} is assumed. The dc-link voltage V_{DC} and the load current I_L of the converter are also assumed to be given and constant. All constraints/condition values for the current system are given in Fig. 6.

B. Calculation of $L_{2,\min}$

The minimum value of the inductance $L_{2,\min}$ can be calculated based on the constraint $I_{\mathrm{HF,pp,max}}$ as

$$L_{2,\min} = \delta_{(100)} \cdot \frac{\frac{2}{3}V_{\mathrm{DC}} - \sqrt{2}V_{\mathrm{mains}}}{I_{\mathrm{HF,pp,max}} \cdot f_{\mathrm{sw}}} \tag{9}$$

with $\delta_{(100)} = \frac{\sqrt{3}M}{2}\cos(\pi/6)$ the relative turn-on time of the space vector (100) when the current of phase a peaks. Equation (9) is based on the fact that, in case of a fundamental displacement factor of $\cos\phi = 1$, the maximum current ripple $I_{\mathrm{HF,pp,max}}$ occurs when the current reaches the peak value $\hat{I}_{\mathrm{LF}}$ of the fundamental (at this instant, the voltage $\frac{2}{3}V_{\mathrm{DC}} - \sqrt{2}V_{\mathrm{mains}}$ is across the inductor). With $M = \frac{2\sqrt{2}V_{\mathrm{mains}}}{V_{\mathrm{DC}}}$, (9) becomes

$$L_{2,\min} = \frac{\sqrt{3}\sqrt{2}|V_{\mathrm{mains}}|}{V_{\mathrm{DC}}}\cos(\pi/6) \cdot \frac{\frac{2}{3}V_{\mathrm{DC}} - \sqrt{2}V_{\mathrm{mains}}}{I_{\mathrm{HF,pp,max}} \cdot f_{\mathrm{sw}}}. \tag{10}$$

C. Loss Calculation of Filter Components

In the foregoing sections, it has been shown how an accurate loss modeling based on simulated current and voltage waveforms is possible. However, such a calculation based on simulated waveforms is time consuming and therefore, for an efficient optimization, simplifications have to be made. In Fig. 7, idealized current waveforms for each filter component of a phase are

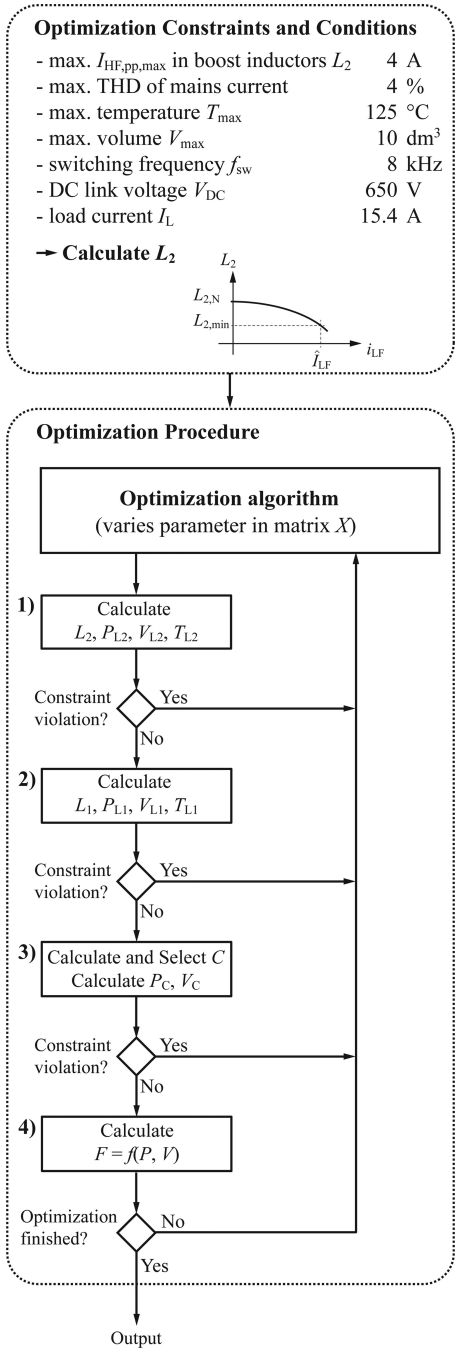

Fig. 6. Design procedure for three-phase *LCL* filters based on a generic optimization approach.

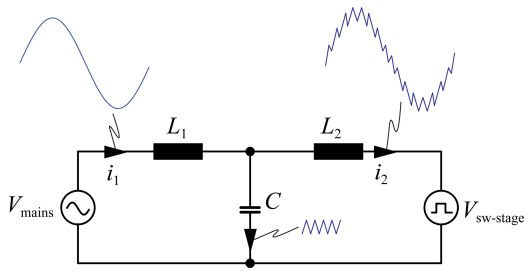

Fig. 7. Idealized current waveforms for each filter component.

illustrated. The current in L_1 is approximated as purely sinusoidal with a peak value of

$$\hat{I} = \frac{2}{3}\frac{I_{\mathrm{L}} V_{\mathrm{DC}}}{\sqrt{2} V_{\mathrm{mains}}} \tag{11}$$

where V_{mains} is the RMS value of the mains-phase voltage. A possible reactive current is rather small and has been neglected. With the mains frequency $f_{\mathrm{mains}} = 50\,\mathrm{Hz}$, losses, volume, and temperature of L_1 can be calculated.

The current in L_2 has a fundamental (sinusoidal) component, with an amplitude as calculated in (11) and a fundamental frequency of $f_{\mathrm{mains}} = 50\,\mathrm{Hz}$, and a superimposed ripple current. The ripple current is, for the purpose of simplification, in a first step considered to be sinusoidal with constant amplitude $I_{\mathrm{HF,pp,max}}$ over the mains period. The losses for the fundamental and the high-frequency ripple are calculated independently, and then summed up. By doing this, it is neglected that core losses depend on the dc bias condition.

The ripple current is assumed to be fully absorbed by the filter capacitor C, hence, with the given dissipation factor $\tan\delta$, the losses in the capacitor can be calculated as well.

How the aforementioned simplifications affect the modeling accuracy will be discussed in Section V.

D. Optimization Procedure

After the optimization constraints and the simplifications chosen for the loss calculation have been described, the optimization procedure itself will be explained next.

A filter design is defined by

$$\mathbf{X} = \begin{pmatrix} a_{L_1} & a_{L_2} \\ w_{L_1} & w_{L_2} \\ N_{L_1} & N_{L_2} \\ do_{L_1} & do_{L_2} \\ h_{L_1} & h_{L_2} \\ t_{L_1} & t_{L_2} \\ ww_{L_1} & ww_{L_2} \\ d_{L_1} & d_{L_2} \end{pmatrix} \tag{12}$$

where all inductor parameters are defined as in Fig. 1(b). The subscripts L_1 and L_2 describe to which inductor each parameter corresponds. The capacitance value of the filter capacitor is calculated based on the L_1 value to guarantee that the THD constraint is met. The parameters in X are varied by an optimization algorithm to obtain the optimal design. The optimization is based on the MATLAB function `fminsearch()` that applies the downhill simplex approach of Nelder and Mead [23].

The optimization algorithm determines the optimal parameter values in X. A design is optimal when the cost function

$$F = k_{\mathrm{Loss}} \cdot q_{\mathrm{Loss}} \cdot P + k_{\mathrm{Volume}} \cdot q_{\mathrm{Volume}} \cdot V \tag{13}$$

is minimized. k_{Loss} and k_{Volume} are weighting factors, q_{Loss} and q_{Volume} are proportionality factors, and P and V are the filter losses and filter volume, respectively. The proportionality factors are chosen such that, for a "comparable performance," $q_{\mathrm{Loss}} \cdot P$ and $q_{\mathrm{Volume}} \cdot V$ are in the same range.[2] In the case at hand, this was achieved with $q_{\mathrm{Loss}} = 1/\mathrm{W}$ and $q_{\mathrm{Volume}} = 3 \cdot 10^4/\mathrm{m}^3$ (these values differ a lot from case to case and, accordingly, are valid for the case at hand only).

In order to calculate the volumes V_{L1} and V_{L2} of the inductors, their boxed volumes are calculated based on the parameters in X.

The following steps are conducted to calculate the filter losses P and the filter volume V of (13) (cf., Fig. 6).

1) Calculate the inductance value L_2 as a function of the current. Furthermore, the losses P_{L_2}, the volume V_{L_2}, and temperature T_{L_2} of the boost inductors L_2 are calculated. In case a constraint cannot be met, the calculation is aborted and the design is discarded and a new design will be evaluated.
2) Calculate the inductance value L_1 as a function of the current. Furthermore, the losses P_{L_1}, the volume V_{L_1}, and temperature T_{L_1} of the filter inductors L_1 are calculated. In case a constraint cannot be met, the calculation is aborted and the design is discarded and a new design will be evaluated.
3) For the purpose of simplification, the THD without filter is approximated with $\mathrm{THD} = I_{\mathrm{HF,pp,max}}/I_{(1),\mathrm{pp}}$, where $I_{(1),\mathrm{pp}}$ is the fundamental peak-to-peak value of the mains current.[3] Furthermore, it is assumed that the dominant harmonic content appears at f_{sw} (this assumption is motivated by simulation results). The *LC* filter has then to attenuate the ripple current by
$$A = 20\log_{10}\left(I_{(1),\mathrm{pp}}\mathrm{THD}_{\mathrm{max}}/I_{\mathrm{HF,pp,max}}\right) \tag{14}$$
(in dB) at a frequency of f_{sw}. Therewith, C is calculated as
$$C = \frac{1}{L_1\omega_0^2} = \frac{1}{L_1(2\pi f_{\mathrm{sw}} \cdot 10^{\frac{A}{40\,\mathrm{dB}}})^2} \tag{15}$$
where ω_0 is the filter cutoff frequency. The losses and the volume of the capacitors and damping resistors can then be calculated. In case a constraint cannot be met, the calculation is aborted and the design is discarded and a new design will be evaluated.
4) The volume, temperature, and losses are now known and the cost function (13) can be evaluated.

The optimal matrix X is found by varying the matrix parameters, evaluating these matrixes by repeating previous steps, and minimizing the cost function (13). After the optimal design is found, the algorithm quits the loop of Fig. 6.

[2]The filter losses are in the range of approximately $100\,\mathrm{W} \ldots 250\,\mathrm{W}$, whereas the filter volumes are in the range of approximately $0.001\,\mathrm{m}^3 \ldots 0.01\,\mathrm{m}^3$. With $q_{\mathrm{Loss}} = 1/\mathrm{W}$ and $q_{\mathrm{Volume}} = 3 \cdot 10^4/\mathrm{m}^3$, the volume range is lifted to $30 \ldots 300$ and therewith becomes comparable to the losses.

[3]The THD is defined as $\mathrm{THD} = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \ldots + I_n^2}}{I_1}$, where I_n is the RMS value of the nth harmonic and I_1 is the RMS value of the fundamental current. Under the assumption that only the dominant harmonic content $I_{\mathrm{HF,pp,max}}$ (which, for the purpose of simplification, is assumed to appear at one frequency) leads to a harmonic distortion, the THD becomes $I_{\mathrm{HF,pp,max}}/I_{(1),\mathrm{pp}}$, consequently.

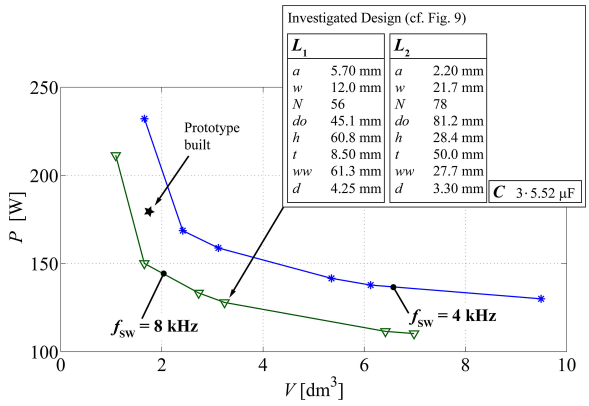

Fig. 8. P–V Pareto front showing filter volumes V and filter losses P of different optimal designs.

V. Optimization Outcomes

The optimization procedure leads to different filter designs depending on the chosen weighting factors k_1 and k_2 in (13), i.e., depending whether the aim of the optimization is more on reducing the volume V or more on reducing the losses P. Limiting factors are the maximum temperature $T_{\max}$ (limits the volume from being too low) and a maximum volume $V_{\max}$ (limits the efficiency from being too high). Different designs are shown by a P–V plot, i.e., a P–V Pareto front in Fig. 8; the tradeoff between losses and volume can be clearly identified.

One design of Fig. 8 has been selected for further investigations. Particularly, a comparison between the (for the optimization procedure) simplified and the more elaborate calculation based on voltage/current waveforms from a circuit simulator has been made. The filter parameters of the selected design are detailed in Fig. 8. The circuit of the three-phase PFC rectifier with the selected input filter has been simulated in MATLAB/Simulink, and the simulated current and voltage waveforms have been taken to calculate the losses according to Section III. The results are given in Fig. 9. The THD constraint is met and the current $I_{\mathrm{HF,pp,max}}$ is only insignificantly higher. The simplified loss calculation used for the optimization leads to an overestimation of the boost inductor losses. This is due to the fact that the maximum ripple current has been assumed to be constant over the mains period. The losses in the filter inductors, on the other hand, have been underestimated as any high-frequency ripple in the current through L_1 has been neglected in the simplified calculations. One could try to improve/change the simplifications made for the optimization and therewith improve the simplified loss calculation. However, the difference between the two calculation approaches has been considered as acceptable for this study.

Another important design criteria is the achieved power factor. The reactive power consumption of the PFC rectifier system, including the damped *LC* input filter, is in the case at hand rather small (power factor = [real power]/[apparent power] = 0.998).

So far, all results are based on simulations and calculations. The models have to be verified experimentally to prove the validity of the optimization procedure. In the following section, experimental results are shown.

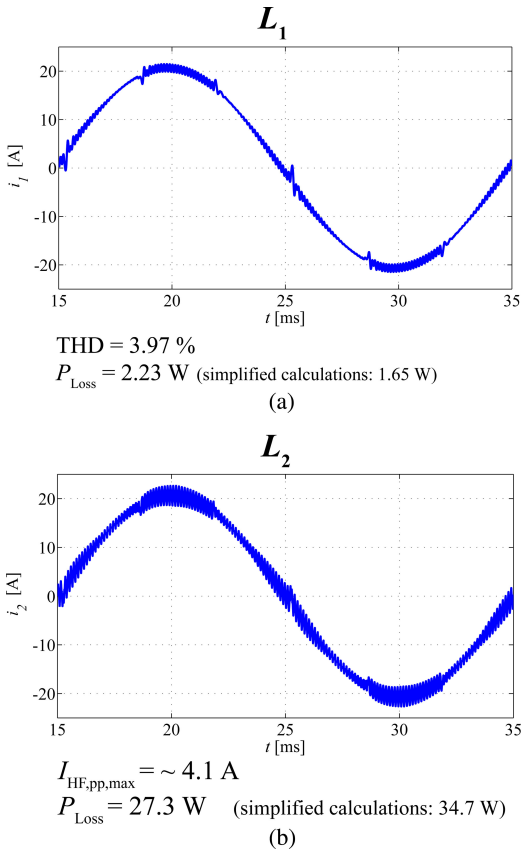

Fig. 9. Simulations and calculations to one selected design (cf., Fig. 8). (a) Filter inductor $L_{1,a}$. (b) Boost inductor $L_{2,a}$.

VI. Experimental Results

Experimental measurements have been conducted to show that the previous introduced calculations are valid. The filter prototype built in the course of this study has been assembled of laminated sheets and coil formers of standard sizes, in order to keep the cost low. This avoids an exact implementation of an optimum as can be seen in Fig. 8 (the prototype built is not on the 8 kHz-line). However, this does not impair the significance of the measurement results. Specifications, dimensions, and photos of the *LCL* filter built are given in Fig. 10. All measurements have been carried out with a Yokogawa WT3000 Precision Power Analyzer.

The measurements have been conducted with the T-type converter introduced in [24]. In Fig. 11, a photo of the converter is given. The T-type converter is a three-level converter; however, a two-level operation is possible as well. A two-level operation with the same modulation scheme (optimal-loss clamping modulation scheme) as in the MATLAB simulation has been implemented.

The results of the comparative measurements and simulations are given in Figs. 12 and 13. As can be seen, the calculated and measured loss values are very close to each other. The maximum current ripple in the actual system is (slightly) higher than in the simulation. This can be explained by the fact that in the simulation the inductance of the boost inductor is assumed to be constant over the full frequency range. However, in reality, the

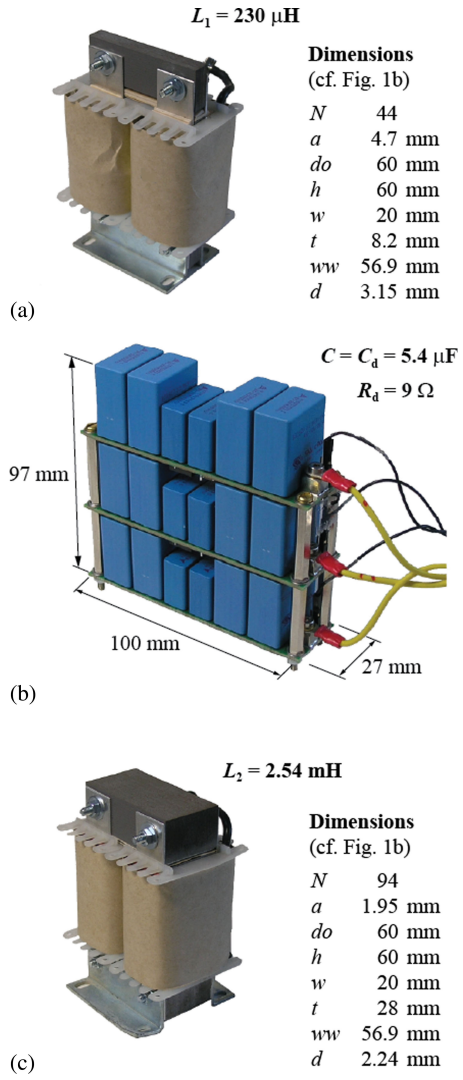

Fig. 10. Specifications, dimensions and photos of (a) one filter inductor L_1, (b) all filter and damping capacitors/resistors C, C_d, and R_d, and (c) one boost inductor L_2.

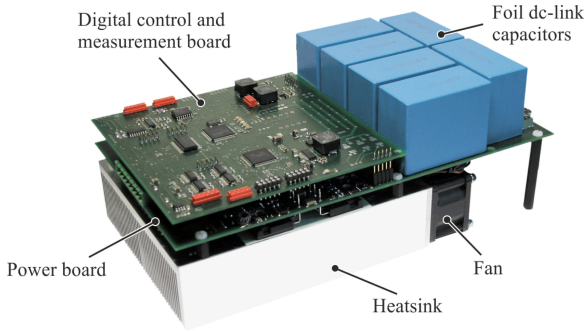

Fig. 11. Photo of the PFC converter.

effective inductance decreases with increasing frequency due to inductor losses and parasitic capacitances. The higher THD value can also be explained with the same effect since the filter inductance decreases with increasing frequency as well. The frequency behavior could be modeled analytically by representing the inductors as *RLC* networks.

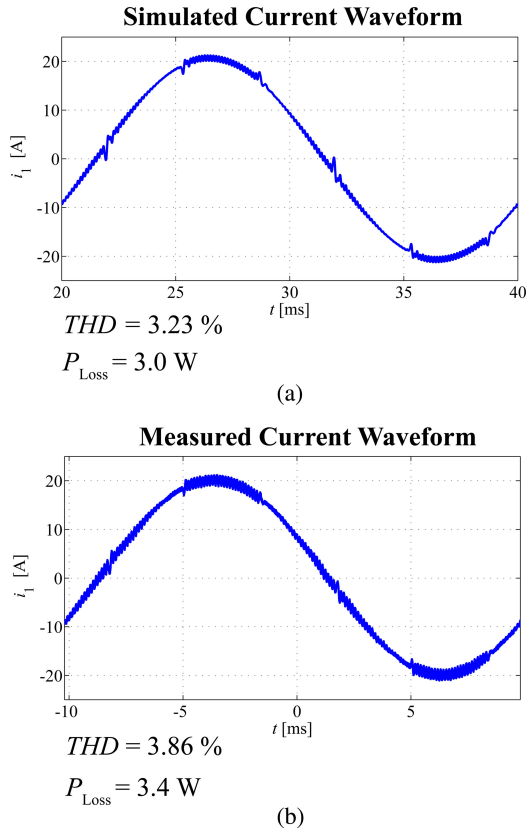

Fig. 12. (a) Simulations and (b) measurements on one of the filter inductors L_1 of the implemented design.

VII. Overall Rectifier Optimization

As can be seen in Fig. 8, an increase in switching frequency leads to lower filter losses and lower filter volumes. However, in return, an increase in switching frequency leads to higher switching losses in the converter semiconductors. In other words, it is important to consider the system as a whole in order to achieve a truly optimal design. In the following, first, a model for the converter is derived, which allows to determine a P–V Pareto front of the converter. Later, the tradeoff in the switching frequency is illustrated and the optimal frequency for the overall system is determined.

A. Overall Optimized Designs

The Infineon Trench and Field Stop 1200 V IGBT4 series has been selected to determine the P–V pareto front of the converter. These semiconductors are the same as the ones employed in the converter of Fig. 11. A converter model has been set up, which determines the junction temperature of the transistors $T_{j,T}$, the junction temperature of the diodes $T_{j,D}$, the volume of the converter V, and the losses of the converter P. As input variables, it needs the transistor chip area A_T, the diode chip area A_D, the cooling system volume V_{CS}, and the operating point defined by the switching frequency f_{sw}, and peak-to-peak fundamental current $I_{(1),\mathrm{pp}}$. The high-frequency ripple current $I_{\mathrm{HF,pp}}$ has, as long as $I_{\mathrm{HF,pp}} \ll I_{(1),\mathrm{pp}}$, only a negligible impact on the losses and is therewith not taken into consideration.

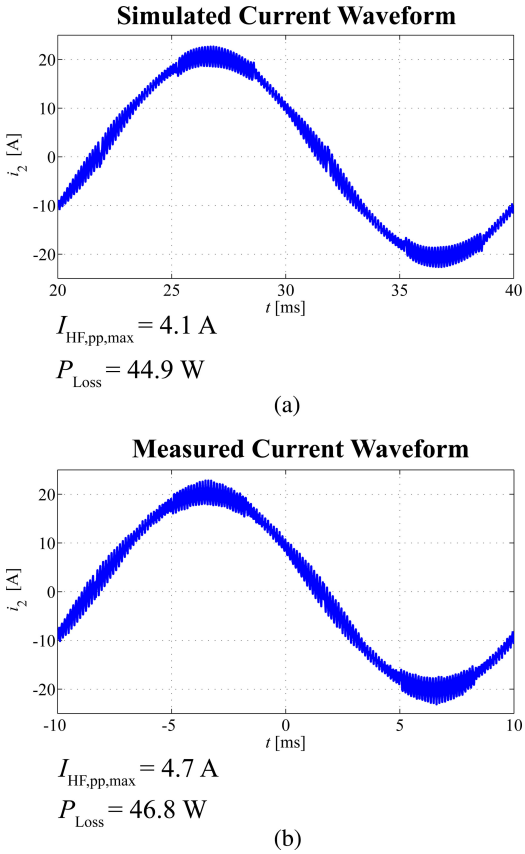

Fig. 13. (a) Simulations and (b) measurements on one of the boost inductors L_2 of the implemented design.

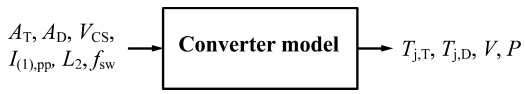

Fig. 14. Illustration of a converter model.

TABLE II
CONSTRAINTS AND CONDITIONS FOR CONVERTER OPTIMIZATION

Parameter	Variable	Value	
Max. junction temp.	$T_{j,max}$	125	°C
Max. cooling system vol.	$V_{CS,max}$	0.8	dm^3
Heatsink height		4	cm
Max. area per chip	$A_{T,max}/A_{D,max}$	1	cm^2
DC link voltage	V_{DC}	650	V
max. DC link voltage overshoot	ΔV_{DC}	50	V
Fund. peak-peak current	$I_{(1),pp}$	20.5	A

The inputs and outputs of the converter model are illustrated in Fig. 14 and all optimization constraints and conditions are listed in Table II. This optimization based on the semiconductor chip area is motivated by previously presented works [25], [26].

The thermal resistance of the cooling system, i.e., the heat sink surface to ambient thermal resistance $R_{th,sa}$, has been modeled with the cooling system performance index (CSPI) [27]; the $R_{th,sa}$ is then calculated as

$$R_{\mathrm{th,sa}} = \frac{1}{\mathrm{CSPI} \cdot V_{\mathrm{CS}}} \tag{16}$$

where CSPI $= 15\,\mathrm{W/(K \cdot L)}$ can be approximated to be constant for a given cooling concept. The value $15\,\mathrm{W/(K \cdot L)}$ has been calculated for the cooling concept of the converter shown in Fig. 11 according to [27]. According to [25], for the selected insulated-gate bipolar transistor (IGBT) series, the junction to sink surface thermal resistance $R_{\mathrm{th,js}}$ can be approximated as a function of the chip area as

$$R_{\mathrm{th,js}} = 23.94\,\frac{\mathrm{K}}{\mathrm{W \cdot mm^2}} \cdot A^{-0.88}. \tag{17}$$

The switching and conduction losses per chip area have been extracted from data sheets. Different IGBTs with different current ratings, but from the same IGBT series have been analyzed. To determine the losses as a function of the chip area, the IGBT and diode chip area as a function of the nominal chip current I_N has to be known. This chip area-current dependency has been taken from [25] and is for the transistor

$$A_{\mathrm{T}} = 0.95\,\frac{\mathrm{mm^2}}{\mathrm{A}} \cdot I_{\mathrm{N}} + 3.2\,\mathrm{mm^2} \tag{18}$$

and for the diode

$$A_{\mathrm{D}} = 0.47\,\frac{\mathrm{mm^2}}{\mathrm{A}} \cdot I_{\mathrm{N}} + 3.6\,\mathrm{mm^2}. \tag{19}$$

The switching losses scaled to the same current do not vary much with the chip size in the considered range, as a comparison of different data sheets of the selected IGBT series has shown; therefore, for this study, the switching loss energies have been considered as independent of the chip area. The switching loss energies have been extracted at two junction temperatures (25 °C and 150 °C) and, for intermediate temperatures, a linear interpolation has been made. These, from the data sheet extracted and interpolated, switching loss energies are then assigned to each switching instant in order to determine the switching losses.

In return, the conduction losses depend substantially on the chip size area. This has been modeled as in [26], but with taking the impact of the temperature into consideration. The following equation describes the conduction losses

$$P_{\mathrm{cond}}(A, i, T_{j,T/D}) = V_f \cdot i + \frac{R_{\mathrm{on,N}}(T_{j,T/D}) \cdot A_N}{A} \cdot i^2 \tag{20}$$

where V_f is the forward voltage drop, $R_{\mathrm{on,N}}(T_{j,T/D})$ is the nominal on-resistance, A_N is the nominal chip size area (to which $R_{\mathrm{on,N}}(T_{j,T/D})$ is taken from the data sheet), i is the current through the transistor, and A is the actual chip size area. The on-resistance has been extracted at two junction temperatures (25 °C and 150 °C) and, for intermediate on-resistance values, a linear interpolation has been made. The current i has been calculated for the chosen modulation scheme. Equation (20) is evaluated with different values for V_f and $R_{\mathrm{on,N}}$, depending whether the conduction losses of the transistor or the diode are calculated.

The converter volume is the sum of the cooling system volume, the dc-link capacitor volume, and the volume of the switching devices. The switching device volume has been calculated by multiplying the chip areas by a depth of 1 cm in order to approximate the transistor volume. The cooling system volume is known as it is a model input parameter. The dc-link capacitor

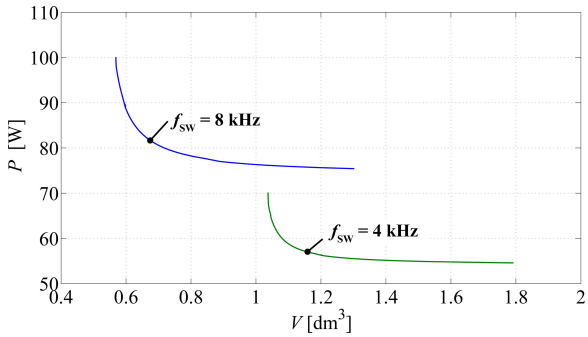

Fig. 15. P–V Pareto front showing converter volumes V and converter losses P of different optimal designs.

C_{DC} has been selected such that the dc-link voltage in case of an abrupt load drop from nominal load to zero load does not exceed a predefined value. The maximum dc-link voltage increase ΔV_{DC} after the load drop can then be approximated as

$$\Delta V_{\mathrm{DC}} = \frac{1}{C_{\mathrm{DC}}} \frac{3}{2} \frac{\sqrt{2} V_{\mathrm{mains}}}{V_{\mathrm{DC}}} \cdot \left(\frac{\hat{I}_2}{f_{\mathrm{sw}}} + \frac{1}{2} \hat{I}_2 t_{\max} \right)$$

where $\hat{I}_2$ is the peak value of the phase current through the boost inductor L_2 and $t_{\max}$ is the time difference between the moment where the system sampled the load drop (i.e., latest $1/f_{\mathrm{sw}}$ after the load drop occurred, since the sampling interval is $1/f_{\mathrm{sw}}$) and the moment where the dc-link voltage peaks (i.e., $V_{\mathrm{DC}} + \Delta V_{\mathrm{DC}}$ is reached). The chosen value for the maximum voltage overshoot is $\Delta V_{\mathrm{DC}} = 50$ V. The dc-link capacitors have been selected from the EPCOS MKP dc-link film capacitors series, which have a rated voltage of 800 V. The capacitor losses are low and, therewith, have been neglected. The capacitance density to calculate the capacitors volume can be approximated with $0.6\,\mu\mathrm{F/cm}^3$.

The losses and volumes of other system parts, such as the DSP, auxiliary supply, gate driver, etc., have not been considered.

An optimization algorithm has been set up similar to that of the filter. A design is characterized by the parameters A_T, A_D, and V_{CS}. The optimization algorithm varies these parameter in order to find optimal designs. The optimization procedure leads to different designs depending whether the aim of the optimization is more on reducing the volume V or more on reducing the losses P. Different designs are shown by a P–V plot, i.e., a P–V Pareto front in Fig. 15; the tradeoff between losses and volume can be clearly identified. It becomes clear that a higher switching frequency leads to higher losses; therefore, there must exist an overall optimal switching frequency at which the system losses are minimized.

Basically, one can combine the results from the filter and from the converter and, therewith, determine the overall system performance. The losses of loss optimized designs for different frequencies have been calculated and are shown in Fig. 16(a). In the case at hand, the optimal switching frequency is at approximately 5–6 kHz. In Fig. 16(b), the losses of a volumetric optimized designs are given for different frequencies; it can be seen that the optimal switching frequency is in the same range.

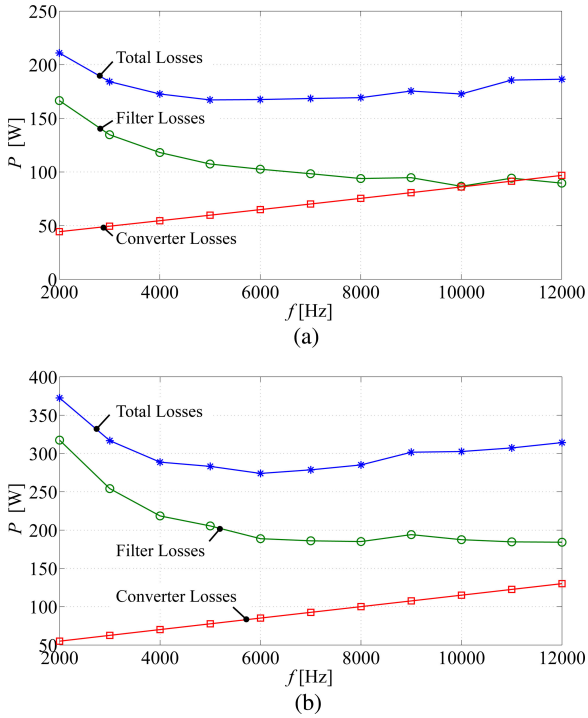

Fig. 16. (a) Losses of loss optimized designs for different frequencies. (b) Losses of volumetric optimized designs for different frequencies.

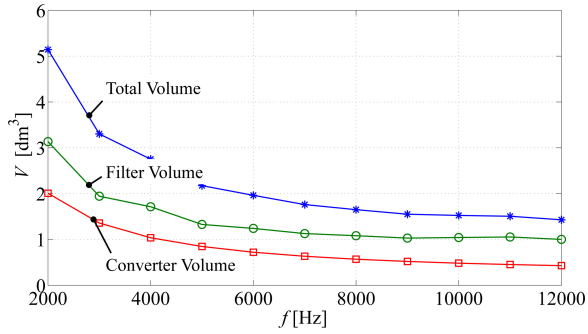

Fig. 17. Volume of volumetric optimized designs for different frequencies.

In case of loss-optimized designs, the major volume part comes from the filter volume. This becomes clear when Fig. 8 is compared with Fig. 15: the maximum filter volume is much higher than the maximum converter volume. This has to do with the selected constraints; however, a further increase of the converter volume would not have a big impact in further decreasing the losses; therefore, it can be concluded that the constraints have been selected well.

In Fig. 17, the volume of volumetric optimized designs for different frequencies is plotted. As both, the filter size and the converter size, decrease with increasing frequencies, a high frequency is favorable with respect to system size. The converter size decreases with increasing frequency because the dc-link capacitance reduces with increasing frequency. The fact that the volume decreases with increasing switching frequency is only true in a limited frequency range; above this frequency range, the losses become very high and the size of the components

increases again so that the heat can be dissipated. This effect is not visible here.

VIII. Conclusion and Future Work

A design procedure for three-phase *LCL* filters based on a generic optimization approach is introduced guaranteeing low volume and/or low losses. The cost function, which characterizes a given filter design, allows a weighting of the filter losses and of the filter volume according to the designer's need. Different designs have been calculated to show the tradeoff between filter volume and filter losses. Experimental results have shown that a very high loss accuracy has been achieved. To improve the THD and current ripple accuracy, the frequency behavior of the inductors could be modeled as well.

As can be seen in Fig. 8, a higher switching frequency leads to lower filter volume, or, when keeping the volume constant, to lower filter losses. However, higher switching losses are expected in case of higher switching frequencies. Therefore, an overall system optimization, i.e., an optimization of the complete three-phase PFC rectifier including the filter, has been performed. Generally, it is important to consider the system to be optimized as a whole, since there are parameters that bring advantages for one subsystem while deteriorating another subsystem.

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