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U. Badstübner
A. Stupar
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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U. Badstuebner, A. Stupar and J.W. Kolar
Power Electronic Systems Laboratory
ETH Zurich, Switzerland
Email: badstuebner@lem.ee.ethz.ch; www.pes.ee.ethz.ch

***Abstract*—Efficient power conversion is one of the fundamental research drivers for modern power supplies. In order to achieve and design on the edge of the system performance space, automatic optimization procedures based on comprehensive analytical converter operation and loss models have to be employed.**

In this paper, a 5 kW, 400 V to 46-56 V phase-shift dc-dc converter with LC output filter is optimized for the highest possible full-load efficiency. The system performance is discussed and compared for full-load, half-load and part-load optimization. Furthermore, the complexity of the first applied comprehensive analytical models is reduced step by step and the resulting values of the design parameters and the system performance are compared in detail with the reference system optimized with the comprehensive models. The sensitivity of the optimization to the level of detail of the modeling as well as the possibilities of the model-complexity reduction is explained. It is shown that certain complex components of the system model can be omitted without noticeably affecting the resulting efficiency.

I. Introduction

Over the past few years the focus of research on power supply units (PSUs) for data centers and telecom applications has shifted from being primarily focused on maximizing the power density [1] to being more concerned with maximizing efficiency while maintaining power density at a high level. Additional design parameters like cost and weight lead to multi-objective design goals for the development engineer [2].

In order to save energy and resources and to increase product competitiveness the developed systems must be at the edge of the feasible performance space, i.e. the systems have to be simultaneously optimized for several performance indices, e.g. as presented in [3], [4]. This kind of optimization is based on comprehensive analytical models of the thermal, electric and magnetic behavior of a converter system. Deriving and applying these models requires a broad, multidisciplinary knowledge base. Such models have been used to optimize dc-dc converters for efficiency [5] or for power density [6] and are characterized by high complexity, detailed loss calculations, a large number of free design parameters, and total computation times ranging from several hours to days. Furthermore, combining them to perform a multi-objective optimization would further increase the number of design variables and/or the dimensions of the design space to be explored and therefore the computation time. For these reasons, it is of interest to explore how much such modeling of power converters for optimization purposes could be simplified, while still obtaining high performance converters with respect to the design goals.

This paper evaluates the influence of the models dependency of the resulting optimized system performance, i.e. the sensitivity of the optimization to the level of detail of the modeling. The evaluation is based on an efficiency-optimized phase-shift PWM dc-dc converter with LC-output filter as presented in [5], [7]. There, the analytical models have been validated by comprehensive simulations and measurement results. The system and the applied models are summarized in **Section II**.

By applying an automatic efficiency optimization based on the accurate models a dc-dc converter with specifications given in table I is optimized with respect to full-load efficiency. The resulting design parameter values and the system performance are discussed in **Section III**.

Depending on the optimization goal the system performance and design parameter values will be different. Aside from the full-load-optimization the converter system can be optimized e.g. with respect to half-load or for several load points as presented in [5], [7], where the part-load efficiency over a load range from 10 % to 100 % could be considered as proposed in the Energy Star® requirements for computer servers [8]. In **Section IV** the influence of such optimization goals on the resulting converter design and its performance is discussed.

In **Section V** the influence of the level of detail of the modeling on resulting optimized converter design parameter values and the system performance is evaluated. The model complexity is reduced step by step and the differences of the resulting optimized designs are discussed. Moreover, the resulting design parameter values of the reduced-model-optimized systems are applied in the calculation loop based on the accurate / comprehensive models and the resulting system performance is compared to the reference system from section III.

II. Converter Modeling

Many different topologies can be found in literature applicable to power supply units for telecom applications and data centers. In order to achieve highly efficient power conversion and to satisfy the specifications given in table I the converter topology should fulfill the following demands: galvanic isolation, soft switching (ZVS and/or ZCS), high power transfer (full bridge), low topology-complexity, small RMS currents and synchronous rectification.

There are basically two converter types which fulfill these demands: resonant and phase-shift PWM converters. If the

Table I
Specifications for the DC-DC converter system.

Input voltage	V_{in}	400 V
Output voltage	V_{out}	46-56 V
	nominal	50 V
Output power	P_{out}	5 kW
Output ripple voltage	V_{ripple}	300 mV_{pp}

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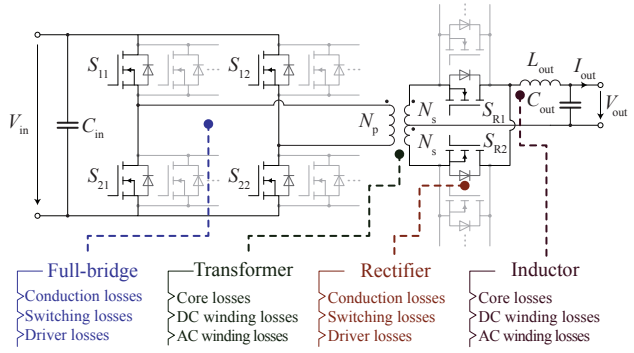

Figure 1. Schematic of the phase-shift PWM converter with LC-output filter. V_{in} = 400 V, V_{out} = 46-56 V, P_{out} = 5 kW. The different loss components calculated for the switches and the magnetic components are shown. Additional losses occur in the auxiliary supply for the system control and the output capacitors.

converter types are optimized with the same goal the resulting performance of the system will be approximately the same even though the advantages and/or disadvantages of the representatives of the topologies will differ. One topology which fulfills the above listed minimum demands and is additionally characterized by a low complexity is the phase-shift PWM converter with LC-output filter which is depicted in Fig. 1 and has been selected for evaluation in this paper in order to determine the performance limit of the standard system approach as reference of further optimizations of systems of higher complexity. The topology consists of a full-bridge on the high-voltage side, a center-tapped transformer, two synchronous rectifier switches and an LC-output filter.

Even though a low-complexity, standard topology is applied the design of the converter system has numerous degrees of freedom. The main design parameters, which values have to be determined during the development process, are the selection and number of parallel MOSFETs of the full-bridge and synchronous rectifier, the core material, core geometry, winding arrangement and wire type (solid, litz or foil), number of turns, inductances, air gap of the transformer and output inductor, as well as the switching frequency.

As these design parameters are to some degree interdependent, the entire system rather than a single component must be considered and the component values cannot be determined independently. For instance, the switching frequency has major influence on the geometry of the magnetic components because of the frequency-dependent flux density and winding design considerations. An optimum transformer with respect to minimum losses might however not result in minimum overall converter losses as current waveforms being optimal for magnetic components and thus could increase the losses in the semiconductors. Additionally, the switching frequency directly determines switching losses especially in the synchronous rectifier and the gate driver losses.

With an automatic optimization procedure based on comprehensive analytical models as presented e.g. in [5] it is possible to find the optimum design of the converter system. The summary of the optimization routine and (cf. Fig. 2) the applied models is given in the following paragraphs.

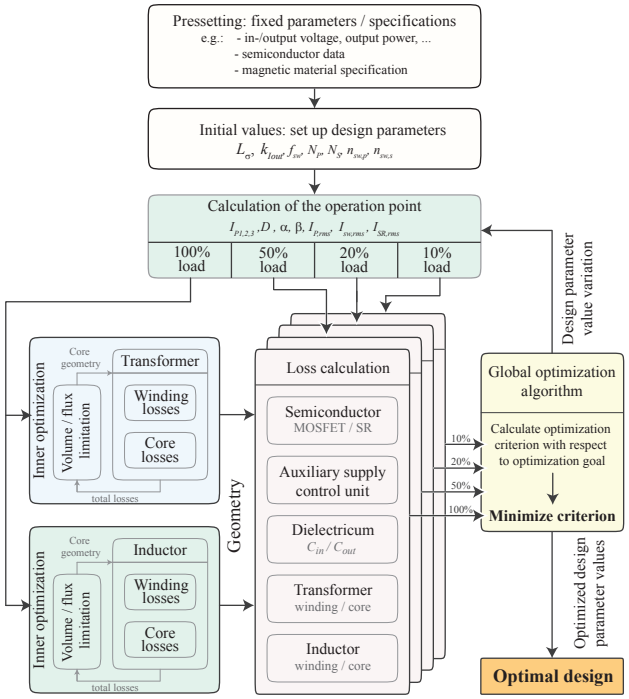

Figure 2. A representation of the converter optimization procedure. The design parameters are varied in a loop and the operating point determined and efficiency calculated for each iteration.

a) Operation point: The corner stone of the optimization routine is the calculation of the operation point based on a coupled inductor model of the center-tapped transformer (cf. Fig. 3). By developing and solving the piecewise current and power equations as presented in [5] the current and voltage waveforms can be determined which enables e.g. the calculation of the RMS values and the harmonics of the currents in the windings of the magnetic components and the switching devices. These values are important for the following loss calculations.

b) Losses in the full-bridge: The conduction losses in the full-bridge MOSFETs can be determined with the on-resistance, RMS current and the number of parallel switches. As the converter operates with zero-voltage switching by inserting an interlock-delay between the switching states in a bridge-leg, the switching losses are negligible during nominal operation. However, especially at light-load condition, the current might not be sufficient for the total dis-/re-charge of the MOSFET parasitic output capacitor and under such conditions the MOSFETs are partly, or in the worst case fully, hard switched. With the calculated residual drain-source voltage and the voltage-dependent energy extracted from the data sheet the switching losses are determined [5]. Additionally, the losses of the gate-driver are calculated with the gate charge and the applied gate-source voltage [5].

c) Losses in the synchronous rectifier: The conduction and gate drive losses in the synchronous rectifier switches are calculated in the same manner as for the full bridge switches. As the rectifier MOSFETs are turned-on during the free-wheeling phase, where the voltage is approximately zero over the switches, the turn-on losses are negligible. However,

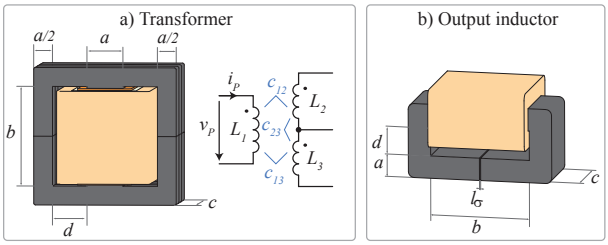

Figure 3. Geometry model of transformer and output inductor. In addition, the coupled inductance model of the transformer is presented.

the switches are turned off hard since the current commutation of the body diodes is forced when a voltage is reapplied to the transformer primary side after the free-wheeling phase. The switching losses are caused by the parasitic elements of the commutation circuit, i.e. the parasitic output capacitor of the synchronous rectifier MOSFET and the commutation-path inductance (consisting of the leakage inductance of the secondary winding, PCB inductance, pin inductances, etc.). When the rectifier MOSFET is turned off, the current is first commutated to the anti-parallel body-diode of the switch. A diffusion charge is then built up until the point where the current becomes zero. This charge and the parasitic output capacitor charge determine the reverse current peak which can be obtained with the approach presented in [9]. The electrical energy stored in the commutation-path inductance at this point is mainly dissipated in the ohmic resistances of the commutation-path as the output-filter impedance is too high to allow a power transfer to the load.

d) Losses in the transformer: The geometric parameters of the magnetic components are calculated in the inner optimization loop, where the values are varied systematically in order to obtain minimum losses, with the maximum allowed flux density and allowed component volume (bounding box) as constraints, since the losses decrease continuously for higher volumes as explained in [5]. For the transformer assembly foil windings are considered, where the optimal foil thickness is calculated with the approach presented in [10]. The transformer configuration is shown in Fig. 3(a). The core losses are calculated with the extended Steinmetz formula [11]. The HF winding losses due to the skin and proximity effect are determined based on a one-dimensional approach [12].

e) Losses in the output inductor: The core and winding losses in the output inductor are calculated with the same methods applied for determining the transformer losses. Output inductor geometry is shown in Fig. 3(b).

f) Additional losses: Ceramic capacitors are considered for the output filter of the converter. The dielectric losses are determined with the given loss factor of the applied capacitors, the specified voltage ripple (cf. table I), which determines the necessary capacitance value, and the current ripple in the output inductor with the assumption that the ac-current is completely filtered by the capacitor. The losses in the auxiliary supply and control unit are considered to be constant over the entire load range and set to 2 W.

The different loss components considered for each part of the converter are summarized in Fig. 1.

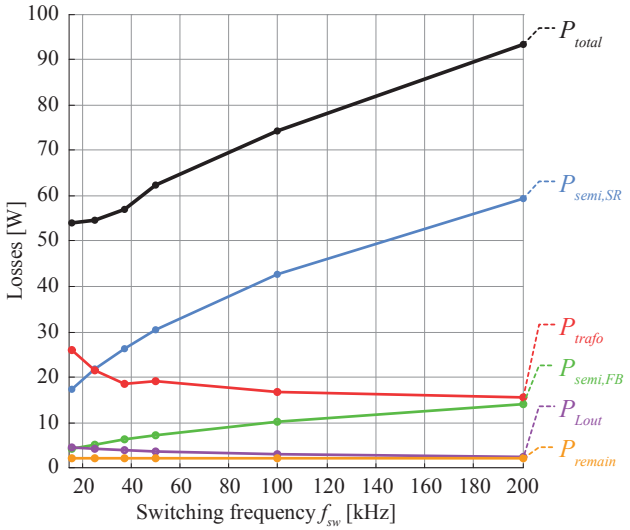

Figure 4. Losses of the full-load-optimized systems in dependency of the switching frequency.

The optimization procedure is illustrated in Fig. 2. In every loop iteration the losses are calculated for different output power points related to the defined optimization goal. For example, the goal could be to optimize full-load efficiency, half-load efficiency, or to satisfy a certain defined minimum efficiency for several different load points. This is discussed in detail in **Section IV**.

The optimization loop is iterated over several thousand times while varying the design parameter values as described above until the maximum efficiency design is found. The results of the optimization process are presented in the next section.

III. Optimized (Reference) System

The dc-dc converter shown in Fig. 1 was optimized according to the procedure and models described in the previous section for peak efficiency at 100 % load. The design was constrained by the specifications shown in table I. The choice of switching frequency is explained by examining Fig. 4, which shows the optimized total converter losses and the losses of the converter components at full load at different switching frequencies.

The transformer volume was limited to 0.5 liter (31 in^3). The transformer design is further constrained by a maximum allowed flux density of the applied ferrite material (B_{max} = 0.3 mT). As transformer losses always decrease with increasing volume [5], the optimization procedure always results in a transformer fully utilizing the allowed volume. At low frequency, due the volume and flux density limitation, the minimum number of turns rises, which results in higher winding losses. Also at lower frequency the flux density is higher leading to higher core losses [5]. Therefore, up to approximately 200 kHz, transformer losses decrease with frequency for the relatively large allowed volume. At higher switching frequencies beyond 200 kHz, transformer losses

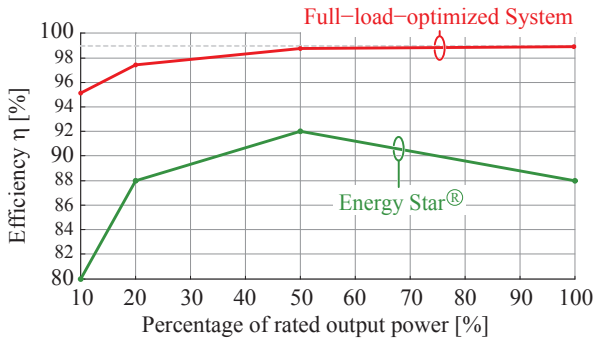

Figure 5. Part-load-efficiency of the optimized system related to the Energy Star® requirements of computer servers.

increase, as HF-winding losses become higher and more significant. Note that if the volume allowed for the transformer were to be further reduced, the frequency at which transformer losses are at a minimum would increase [5].

The above similarly applies to the output inductor, where however the HF-winding losses are almost negligible and where core losses are relatively small since the maximum peak-to-peak inductor current ripple is limited to 10 % of the dc output current, leaving the winding dc-resistance losses the dominant component. The volume of the inductor was limited to 0.3 liter (18 in^3).

The full-bridge switches are soft-switched, and therefore have negligible switching losses over a wide load-range, but driving losses are frequency-dependent causing the overall full-bridge losses to increase slowly with increasing frequency. The synchronous rectifier switches however are hard-switched, and switching losses are significant. As a result losses in the rectifier increase sharply with increasing frequency so that, at higher frequency, the rectifier losses become dominant. The remaining losses are almost constant over the frequency range as they are mostly caused by the auxiliary supply for the control, since the output capacitor losses are very small. Since the rectifier losses become so dominant at higher frequencies, the total converter losses at full load always increase with increasing frequency, as shown in Fig. 4. Therefore, the minimum losses and highest efficiency are achieved at the lowest switching frequency. For this reason, for the optimized system the switching frequency results in 16 kHz, at the limit of the audible range. The resulting converter design parameter values are summarized in table II.

Fig. 5 shows the efficiency of the full-load optimized system at 10 %, 20 %, 50 % and 100 % load. A peak efficiency of 98.9 % is achieved at full load. At half-load, efficiency is 98.8 %. The minimum efficiency is 95.1 % at 10 % load. As can be seen from Fig. 5, the optimized system efficiency over the entire load range far exceeds the Energy Star® requirement for computer servers. (Note, that in the proposed Energy Star® standard the complete power supply unit (PSU) is considered, i.e. ac-dc and dc-dc converter.)

A breakdown of losses by converter component and for different load levels of the full-load optimized system is given in Fig. 6. At all loads the synchronous rectifier switches and

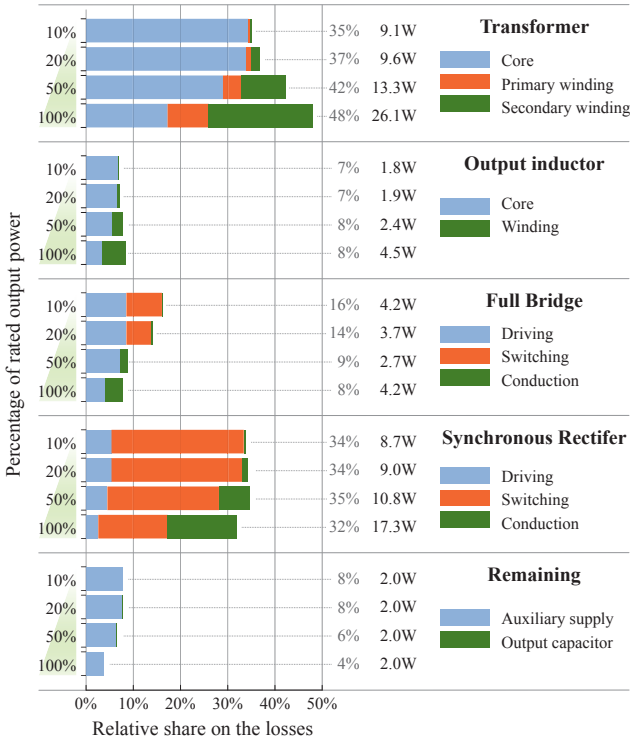

Figure 6. Losses distribution in the full-load-optimized (reference) system.

the transformer together account for the largest loss fraction, being approx. 70-80 % of the total losses across the entire load range. Note that this largest fraction of losses is also more or less equally split between the rectifier and the transformer across the different load points. At full load, which the converter is optimized for, for all components the frequency dependent losses (e.g. core losses, driving losses, switching losses) are almost equal to the non-frequency dependent losses (e.g. conduction losses). Although this results in the nearly 99 % efficiency at full load, at lower loads the frequency-dependent losses result in a significantly lower efficiency, especially below 50 % load. In the magnetic components, core losses remain large at lower loads even as winding losses greatly decrease.

To minimize the semiconductor conduction losses at full load, a large number of transistors is paralleled: 7 for each full-bridge switch, and 15 for each rectifier switch. As a result zero-voltage-switching (ZVS) no longer occurs below 50 % load as the conducted current is too low and this results in significant switching losses, which combined with the driver losses cause the total full-bridge losses to be the same at 10 % load as at 100 % load. From 100 % to 10 % load the share of the full-bridge losses doubles, consequently efficiency is decreasing. Similarly in the rectifier switches at low loads the losses are completely unbalanced, i.e. the switching losses greatly exceed the conduction losses. The remaining losses, mostly caused by the auxiliary supply, are essentially constant over the entire load range, what results in a more severe impact on the efficiency at low loads than at higher loads.

Table II
COMPARISON OF RESULTING DESIGN PARAMETER VALUES

	Optimization goal		
Design parameter	Ⓐ full-load	Ⓑ half-load	Ⓒ part-load
Switching frequency	16.0 kHz	16.0 kHz	16.0 kHz
Parallel full-bridge switches	7	3	3
Parallel sync. rectifier switches	15	8	6
Transformer turns ratio $N_p : N_s$	32 : 5	32 : 5	32 : 5
Leakage inductance L_σ	6.0 μH	6.0 μH	6.0 μH
Leg thickness a (cf. Fig. 3)	22 mm	22 mm	22 mm
Window width b (cf. Fig. 3)	105 mm	105 mm	105 mm
Core thickness c (cf. Fig. 3)	42 mm	42 mm	42 mm
Primary winding foil thickness	60 μm	59 μm	59 μm
Secondary winding foil thickness	179 μm	178 μm	178 μm
Output inductor turns N_L	8	7	7
Inductance L_{out}	31 μH	52 μH	62 μH
Leg thickness a (cf. Fig. 3)	16 mm	19 mm	19 mm
Window width b (cf. Fig. 3)	140 mm	95 mm	83 mm
Core thickness c (cf. Fig. 3)	24 mm	34 mm	38 mm
Winding foil thickness	500 μm	500 μm	500 μm
Air gap length l_σ (cf. Fig. 3)	1.03 mm	0.79 mm	0.82 mm

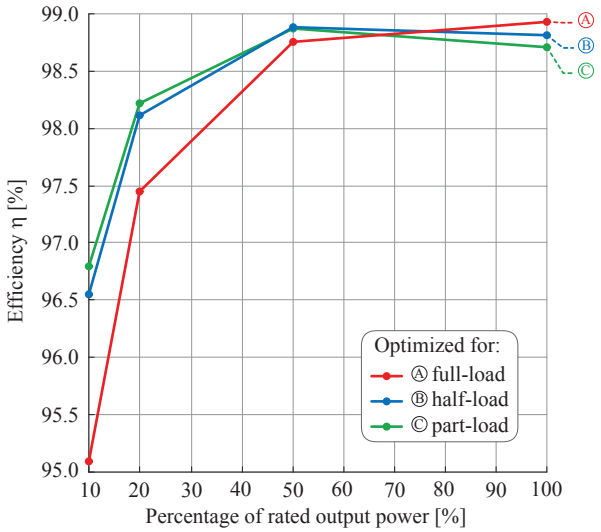

Figure 7. Efficiency as function of the output power for full-load-optimized Ⓐ, half-load-optimized Ⓑ and part-load-optimized Ⓒ converter system.

IV. Optimization Goals

Depending on the design requirements, the converter may be required to have peak efficiency at a load point other than 100 %, e.g. the converter might be required to operate mainly at 50 % load, and should therefore have the maximum efficiency at this load point. Alternatively, a required minimum efficiency may be specified for several load points, e.g. as proposed by the Energy Star® specification for computer servers shown in Fig. 5. Therefore, the influence of the optimization goal on the converter design must be analyzed. Three systems are compared: system Ⓐ is the full-load optimized system described in the previous section; system Ⓑ is a converter optimized for peak efficiency at half-load; and system Ⓒ is a converter optimized for part-load efficiency. For system Ⓒ, a reference efficiency curve was created by shifting up the Energy Star® limit shown in Fig. 5 so that the required peak efficiency, at 50 % load, is 99 %. The optimization criterion, which is minimized in the optimization process, is determined by comparing the calculated efficiency at each load point to the reference curve using a penalty function [7]. The resulting system with the minimum penalty value represents the part-load optimized system. It should also be noted that the inner optimization loop for the transformer and inductor (cf. Fig. 2) always considers full load only in order to reduce computation time and to meet the full-load constraints (e.g. maximum flux density). For this reason the transformer parameters in the three systems are nearly identical. The three different resulting designs are compared in table II.

The efficiencies of the three different converter designs are compared in Fig. 7. Naturally, system Ⓐ has the highest efficiency at 100 % load, 98.9 %, compared to 98.8 % for Ⓑ and 98.7 % for Ⓒ. At 50 % load, systems Ⓑ and Ⓒ achieve 98.9 % efficiency, while system Ⓐ is slightly lower at 98.8 %. At lower loads, as expected Ⓒ has a slightly higher efficiency than Ⓑ, while the efficiency of Ⓐ is significantly lower: 95.1 % at 10 % load compared to 96.6 % for Ⓑ and 96.8 % for Ⓒ, and 97.5 % at 20 % load compared to 98.1 % for Ⓑ and 98.2 % for Ⓒ. The similar behaviour of systems Ⓑ and Ⓒ can be explained by the fact that the part-load reference used for Ⓒ places the peak efficiency at 50 % load, making it similar to a half-load optimized system.

The distribution of the losses for the three designs at 100 % load and 10 % load is shown in Fig. 8. The loss distribution of the part-load and half-load optimized systems is very similar, in correspondence with the two resulting designs shown in table II. As the transformer is nearly identical in each case, also the transformer losses in each system are very similar, but their share of the total losses differs primarily due to the different number of paralleled switches used in each system. Compared to system Ⓐ, system Ⓑ and Ⓒ both have approximately half as many switches paralleled in the full bridge and synchronous rectifier. For the half-load and part-load optimized systems, the conduction and switching losses are balanced at a lower load point, where the conduction losses are lower, meaning of course that high conduction losses occur at full load, in contrast to the full-load optimized system. On the other hand, switching and driving losses are noticeably lower in systems Ⓑ and Ⓒ than in system Ⓐ.

In the inductor, winding dc-losses, dependent on the output current, and core losses, dependent on the current ripple, dominate. The core losses dominate at lower loads, and for this reason the part- and half-load optimizations minimize the current ripple to favor reducing core losses more than winding losses. At full load, the winding losses are larger than the core losses, so the full-load optimization allows a larger inductor current ripple, resulting in the smaller inductance given in table II. In correspondence, the inductor losses are smaller at full load for the full-load optimized system compared to the other two systems, but larger at lower loads (cf. Fig. 8).

The choice of optimization goal has a significant impact on the resulting design and its loss distribution. Nevertheless, the simplest design goal - peak efficiency at full load - still

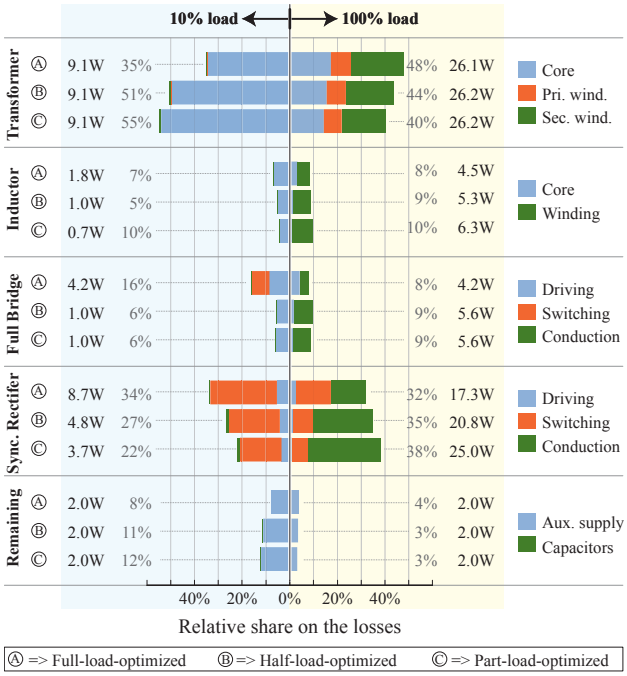

Figure 8. Losses distribution for full-load-optimized Ⓐ, half-load-optimized Ⓑ and part-load-optimized Ⓒ converter system.

delivers high efficiency (>95 %) over the entire load range. Therefore and for the sake of clarity, in the remainder of this discussion only the full-load optimization goal is considered.

V. Model Complexity Reduction

The reference system in this section is the full-load-optimized system from section III calculated based on comprehensive / detailed converter and component models. In order to gain insight into the robustness of the optimization process, i.e. to understand which level of detail of modeling is required for achieving (nearly) correct optimal design parameter values, the model complexity was reduced step by step and the optimization process was run with the simplified models. With the resulting optimized design parameter values, such as core geometry of the magnetic components and number of parallel semiconductors, the calculation-loop was re-run with the comprehensive models as illustrated in Fig. 9. The re-calculated performance of the systems optimized using different model complexity reduction levels (MCRL) is compared with the system performance of the reference system. This is done for each MCRL in order to determine the difference in the performance space and identify the potential for model simplification.

In table III the overview of the MCRL is presented. For every MCRL one of the loss models as described in section II was simplified and/or omitted. In the following subsections the discussion for each level is given based on the performance comparison with respect to the reference system from section III. For clarity the efficiency and loss values given in the following correspond to the full-load operation if not stated differently.

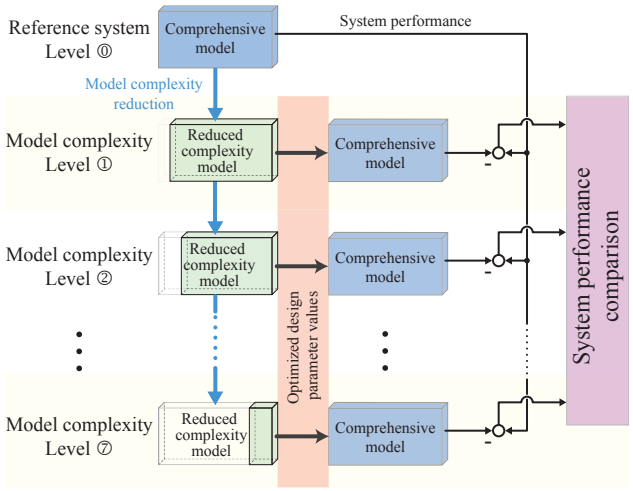

Figure 9. Illustration of the model reduction procedure, showing the optimization performed with reduced models, accurate calculation of the losses of the resulting systems with the comprehensive models, and comparison of the resulting performance.

A. Model Complexity Reduction Level (MCRL) ①

In the reference system (⓪ in table III), up to the 30th harmonic of the currents in the primary and secondary windings were considered in order to accurately determine the high-frequency (HF) winding losses. In the first MCRL (①) only the first harmonic is considered. The relative deviation of the primary and secondary winding losses between the reference system and the optimized MCRL ① system is 18 % and 13 %, respectively. However, the design parameter values of the transformer change only marginally, e.g. the core geometry parameters change only by ±2-4 % and thus the resulting performance of the reduced-model-complexity-optimized system ① is almost the same - the absolute total converter losses increase by less than 200 mW.

B. MCRL ②

Calculating only the first harmonic does not result in a significant decrease of computation effort compared to calculating several harmonics, since a Fourier analysis must be

Table III
Model complexity reduction Levels (MCRL)

	Model complexity reduction Level							
Loss-model	⓪	①	②	③	④	⑤	⑥	⑦
Transformer HF-winding	•							
1st harmonic winding	•	•						
DC-winding	•	•	•	•	•	•	•	•
Accurate core losses	•	•	•					
Inductor HF-winding	•	•	•	•				
DC-winding	•	•	•	•	•	•	•	•
Accurate core losses	•	•	•	•	•			
Full-bridge Driving	•	•	•	•	•	•	•	•
Conduction	•	•	•	•	•	•	•	•
Switching	•	•	•	•	•	•		
Sync. Rectifier Driving	•	•	•	•	•	•	•	•
Conduction	•	•	•	•	•	•	•	•
Switching	•	•	•	•	•	•	•	

performed in either case. Moreover, considering only the first harmonic results in principle in a relatively high error for this topology which operates with an almost rectangular primary current waveform. In the second complexity reduction step, i.e. MCRL ②, only the RMS value of the current and the dc-resistance are considered.

The calculated total converter losses are just 4 % lower (for MCRL ① modeling 7 %) and so the influence on the design parameter values is also low (±1-3 %, cf. Fig. 10). Furthermore, compared to the reference system, the reduced-model-complexity-optimized system again results in a negligible performance decline - less than 100 mW of additional losses.

C. MCRL ③

The transformer core losses are calculated with the extended Steinmetz formula for non-sinusoidal waveforms as proposed in [11]. In MCRL ③ only the simple Steinmetz formula is considered for calculating the core-losses per volume

$$P_{core,vol} = k f^{\alpha} \hat{B}^{\beta} \tag{1}$$

with the Steinmetz parameters k, α and β found by curve fitting, the switching frequency f and the maximum flux density $\hat{B}$.

Compared to MCRL ② the calculated core losses almost do not change (approx. -0.5 %) and conversely the resulting design parameter values and converter system performance do not change either.

D. MCRL ④

Similar to the transformer-MCRL ② only dc-losses are considered in the inductor windings in MCRL ④. Even though the HF-component of the output inductor current is small compared to the dc-component and the share of the winding losses in the total losses is only 5 % (cf. Fig. 6) the resulting design parameter values of the converter change. As presented in Fig. 10 the inductor geometry parameter values change by ±3-4 % and the calculated optimal output inductance is 11 % higher. The interdependency of the design parameters can be pointed out at this MCRL as well, as the number of parallel switches used is reduced from 7 to 6 on the primary side and from 15 to 14 on the secondary side due to the decreased RMS value of the currents in the devices.

The decline in the actual system efficiency for the MCRL ④ is again negligible compared to the reference system.

E. MCRL ⑤

The core losses in the inductor are small (less than 3 W at full load) as the flux ripple is small. In MCRL ⑤ the core losses are calculated with the simple Steinmetz formula (1) for sinusoidal current waveforms, neglecting the dc-offset of the flux. The relative error of the calculated core losses is high (approx. 54 %,) but the absolute error is less than 1 W. The resulting optimized design parameter values however are changed again: the optimum inductance is almost the same as for the reference system and the cross-sectional

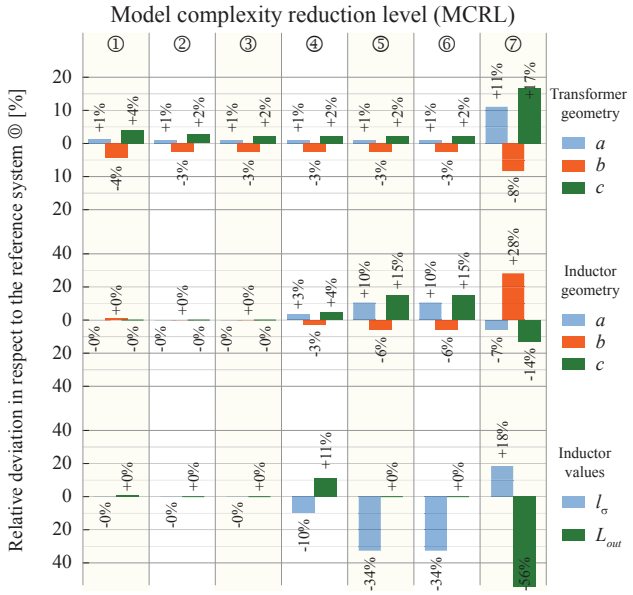

Figure 10. Relative deviation of the design parameter values resulting from the reduced-model-complexity-optimization in respect to the design parameter values of the reference system.

area determined by the core geometry parameters a and c is increased as shown in Fig. 10.

Again, the resulting system performance is only minimally worse, even though the core losses are increased by ≈ 5 %.

F. MCRL ⑥

The switching losses of the full-bridge switches in the converter are negligible at full-load as there is enough energy to fulfill the zero voltage switching condition. Thus, for a full-load optimization the resulting system performance doesn't change if the calculation of the full-bridge switching losses is omitted as done in MCRL ⑥. The number of parallel switches is limited because of the driving losses at full load. Thus, the driving losses cannot be neglected because the number of parallel switches would be unlimited as the effective on-resistance and therefore total conduction loss decreases with every switch added in parallel.

Note that the resulting system performance for part-load optimization would be much more affected by this model complexity reduction as the number of switches would be increased resulting in high switching losses at part-load as explained in section IV.

G. MCRL ⑦

Unlike the full-bridge switches, the synchronous rectifier MOSFETs are switched hard at any load condition. Neglecting the switching losses of the rectifier switches as is done in MCRL ⑦ not only has a big influence on the accuracy of the loss calculation but also on the system performance.

The frequency dependence of these switching losses results in the low switching frequency (16 kHz) of the optimized system. By omitting these switching losses the resulting optimal switching frequency is higher (37.5 kHz) since the core losses in the magnetic components are lower at higher

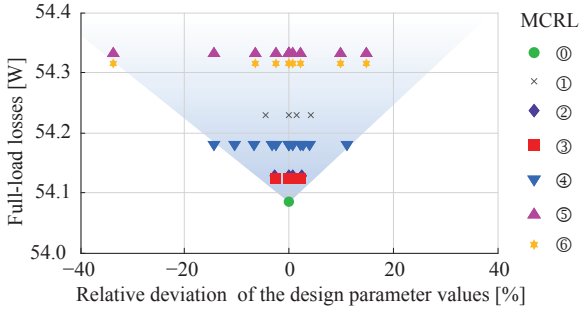

Figure 11. Influence of the deviation of the design parameter values resulting from the model complexity reduction. (Note that MCRL ⑦ is omitted for the sake of clarity as the deviation and the resulting loss is much higher. The principal trend of deviation vs. system performance shown here holds also for MCRL ⑦.)

frequencies as shown in Fig. 4. Due to the interdependency of the design parameter values the geometry parameters are changed by ±8-17 % for the transformer and ±7-28 % for the output inductor; the inductance is reduced by more than 55 %.

The number of parallel full-bridge switches is reduced from 7 to 4 because of the increased driving losses due to the higher switching frequency. This results in increased conduction losses. In contrast to that the number of paralleled synchronous rectifier MOSFETs is now only limited by the driving losses and thus results in an increase from 15 to the unrealistic value of 23. The absolute deviation of the calculated total losses due to the reduced model is more than 18 W (a decrease of approx. 34 % in calculated losses).

Compared to the reference system the system performance of the reduced-model-complexity-optimized system is much lower. The resulting total losses are increased from 54 W to 68 W (25 % higher) and the efficiency is decreased from 98.9 % to 98.6 %. Even more pronounced is the decrease of the efficiency at 10 % load, from 95.1 % to 91.9 %, i.e. the converter losses increase by more than 70 %. A further model complexity reduction for the synchronous rectifier, e.g. neglecting driving and/or conduction losses, would prevent a reasonable optimization process.

In Fig. 11 the resulting full-load losses with respect to the design parameter values resulting from the reduced-model-complexity-optimizations are illustrated. Every point in the figure presents a design parameter value such as a core geometry parameter, number of parallel semiconductors or switching frequency. In principle, the higher the variation of the values of the design parameters the higher the distance from the reference system optimum (MCRL ⓪ in Fig. 11). The absolute deviation of the losses for the MCRL ① - ⑥ is small as presented before. A drastic change occurs when rectifier switching losses are neglected in MCRL ⑦ which has been omitted in the figure because of the large loss and parameter deviation.

VI. Conclusion

High efficiency is one of the most important requirements for modern power supplies. An optimization based on comprehensive and validated analytical models results in optimal design parameter values for the converter system with respect to the optimization goal. The goal takes significant influence on the values of the design parameters determined by the optimization process, and on the resulting system performance, as shown for full-load, half-load and part-load optimization.

Reducing the model complexity results in partially high deviations of the calculated losses compared to the losses given for the system optimized with the most comprehensive model. However, as has been shown, neglecting HF-winding losses of the transformer and inductor results in a negligibly lower total efficiency at full load. Furthermore, even if the core losses of the transformer and inductor are calculated only with the simple Steinmetz formula, the resulting losses, re-calculated with the comprehensive model, are still only marginally higher.

A drastic change of the free design parameters and system performance results however when neglecting the switching losses of the synchronous rectifier for the evaluated full-load optimization. Therefore the calculation of the semiconductor losses cannot be neglected. However the calculation effort for the losses of magnetic components can be significantly reduced compared to the comprehensive system model while still achieving in a nearly optimal converter design.

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