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Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier

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***Abstract*—This paper presents the analysis and realization of a topology suitable to realize a power factor correction (PFC) rectifier with a thickness of only a few millimeters. The low height of the converter requires all components to be integrated into the printed circuit board (PCB). Still reasonable dimensions of the converter PCB are feasible (221 mm × 157 mm for a 200 W PFC rectifier), since PCB-integrated inductors and capacitors allow for high energy densities due to their large surface area which facilitates a low thermal resistance to ambient. A multicell totem-pole PFC rectifier employing a soft-switching modulation scheme over the complete mains period is identified as an adequate topology. The mode of operation is entitled *triangular current mode* (TCM) due to the triangular-shaped inductor currents. The modulation technique requires a reliable description of the switching transition of a half-bridge in order to provide accurate timing parameters. For this purpose, a simplified model of the nonlinear MOSFETs' output capacitances facilitates closed-form analytical expressions for duty cycle and switching frequency. Furthermore, this paper details the control of three interleaved converter cells which yields a reduction of the input current ripple. A 200 W TCM PFC rectifier with a low height of 5 mm has been realized and measurement results are provided in order to validate the theoretical considerations. The presented TCM PFC rectifier achieves an efficiency of 94.6% and a power factor of 99.3% at nominal power.**

***Index Terms*—Single-phase power factor correction (PFC) rectifier, power sheet, printed circuit board (PCB)-integration, triangular current mode (TCM).**

I. Introduction

OVER the past decades, the evolution of power electronic systems has shown a trend toward higher power densities, either due to limited space requirements [1] or indirectly driven by cost and/or weight reductions (aircraft applications [2], [3], server farms [4]). In the systems presented in [1]–[4], the increase of power density is accompanied by an increase of efficiency as the reduced volume provides less surface area for power loss dissipation.

Over the past years, rising energy cost and increasing environmental awareness have shifted the focus toward high-efficient power systems. Converter systems with ultrahigh efficiency, however, are large and expensive [5]. For that reason, the economic realization requires a tradeoff between power density ρ and efficiency η of a converter system for which the ρ-η-Pareto front, e.g., presented in [6], is a vivid representation. The analysis in [4]–[6], however, is based on cubical-shaped converters and needs to be modified for flat converters, since most of its components, e.g., inductors and capacitors, are subject to particular limitations [7].

TABLE I
Specifications of the PFC Rectifier of the *Power Sheet* With a Thickness of 1 mm

Input voltage	$v_{\mathrm{n}} = 230$ V	Output power	$P_{\mathrm{out}} = 200$ W
Output voltage	$V_{\mathrm{out}} = 400$ V	Amb. temperature	$T_{\mathrm{amb}} = 45$ °C

Cubical-shaped power converters applied to specific future applications, as, e.g., flat screens [8], [9] or OLED lighting panels [10]–[12], would determine the outline of the entire system, and therefore, ultraflat power converters are highly demanded. The thicknesses of the respective converter systems, which are composed of a power factor correction (PFC) rectifier and a series-connected dc–dc converter providing an output power of up to 200 W, are typically limited to $1, \ldots, 2$ cm [13].

In order to meet the demand of ultraflat power supplies, topologies suitable to realize converter systems with a thickness of only 1 mm and an output power of 200 W (cf., Table I) are under investigation. The respective research project, entitled the *Power Sheet* [7], analyzes the implications of the extreme height limitation on the converter's efficiency and its power density, i.e., its ρ-η-Pareto front, and compares it to conventional cubical-shaped converter systems.

The extremely low thickness can only be achieved if each component is integrated into the printed circuit board (PCB). As a consequence, the dissipated heat has to be transferred to the ambient through the PCB which can be beneficially achieved with a multicell configuration as the power dissipation is divided into several converter cells.

In order to facilitate reasonable dimensions of the converter PCB, ultraflat converter systems employ a topology which facilitates comparably low magnetic and electric energy storage requirements, i.e., small inductors and capacitors. Low energy storage requirements are effectively achieved by increasing the switching frequency. In a conventional hard switching topology, however, an increased switching frequency causes increased switching losses and the requirements put on the cooling system increase [4]. Thus, a soft-switching topology is proposed in

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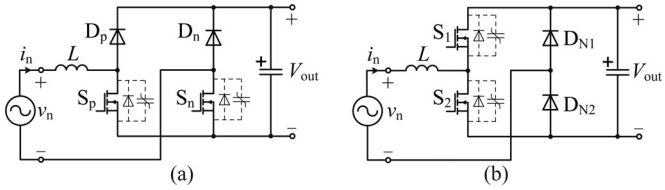

Fig. 1. (a) Bridgeless PFC rectifier with parasitic output capacitances of the MOSFETs. D_p and S_p shape i_n for $v_n > 0$ whereas D_n and S_n shape i_n for $v_n < 0$ [16]. (b) Totem-pole bridgeless PFC boost rectifier [16].

order to realize a high switching frequency and low losses due to the switching operation. Furthermore, the converter topology needs to be selected with respect to the electromagnetic interference (EMI) filter requirements, since the EMI filter typically allocates one third of the overall converter volume [6].

A comparison of several PFC rectifier topologies presented in [14] renders the bridgeless PFC rectifier [see Fig. 1(a)] to be promising regarding high efficiency and high power density, as the number of semiconductors in the conduction path is reduced compared to conventional boost-type rectifiers which employ a diode bridge in the input [15], [16]. The bridgeless topology, however, suffers from considerable common-mode (CM) noise as the output rails are floating during the negative mains half-wave. As a consequence, arrangements with either capacitors or diodes as CM return path have to be employed which cause additional losses and increased circuit complexity [6], [16], [17], [18].

A modification of the bridgeless PFC rectifier is the totem-pole bridgeless PFC rectifier depicted in Fig. 1(b) and presented in [16]. Compared to the basic bridgeless topology, a diode and a switch are interchanged which allows the output bars to be connected to the mains for the complete mains period through one of the diodes. Thus, the CM noise is considerably reduced. In continuous conduction mode (CCM) of operation, however, the bridge-leg that is composed of the switches suffers from significant reverse recovery losses. Low switching losses can only be achieved operating in critical conduction mode (CrCM) or in discontinuous conduction mode (DCM) which allow for a resonant switching transition and thus reduced switching losses.

With the modulation technique proposed in [19], the operating range for soft-switching, i.e., zero-voltage switching (ZVS), is limited to $|v_n| \leq V_{\rm out}/2$; for larger input voltages, valley-switching has to be employed to reduce the switching losses. Full-range ZVS over the entire mains period can be achieved with an advanced modulation technique [20], [21], entitled *triangular current mode* (TCM) due to the triangular-shaped inductor currents, which require elaborate numerical calculations [20] or measurement results [21] to determine the timing parameters needed to operate the converter. The conduction losses of the converter can be reduced by replacing the diodes D_{N1} and D_{N2} by switches. The resulting circuit, depicted in Fig. 2(a), even enables bidirectional power flow.

A drawback of the totem-pole PFC rectifier is the large input current ripple which requires for a large differential-mode (DM) EMI filter. Since the proposed converter is operated with

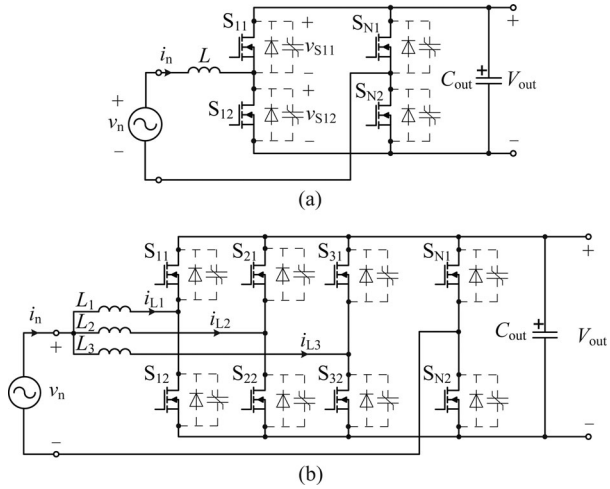

Fig. 2. (a) Single-cell and (b) three-cell configuration of a TCM PFC rectifier system employing ZVS over the entire mains period.

a switching frequency greater than 150 kHz, an interleaved arrangement of n converter cells facilitates a reduced filter size, e.g., the setup with three interleaved converter cells depicted in Fig. 2(b) cancels the first and the second harmonic component of the inductor current i_{L1} in the input current i_n. A two-cell configuration of this converter is discussed in [22]; however, the interleaving control is not detailed and the applied modulation does not allow for ZVS within the complete mains period. Thus, a detailed analysis of the interleaving of three cells [cf., Fig. 2(b)] is shown in this paper.

The interleaved three-cell TCM PFC rectifier depicted in Fig. 2(b) is considered to be the most appropriate topology appropriate regarding the ultraflat converter system as it has the following features:

1) low conduction loss due to synchronous rectification;
2) ZVS over the complete mains period;
3) distributed losses due to the multicell configuration;
4) a reduced DM EMI filter effort due to interleaved inductor currents;
5) low CM noise, and
6) bidirectional operation.

This paper presents a novel accurate and analytical description of the three-cell TCM PFC rectifier. Section II details the full-range ZVS modulation scheme. In particular, the nonlinear characteristic of the MOSFETs' output capacitances has a strong impact on the inductor current and, subsequently, on the timing parameters needed to operate the PFC rectifier. Therefore, Section III proposes a simple analytical model of the nonlinear MOSFET capacitances facilitating the derivation of closed-form analytical expressions that directly enable the calculation of the timing parameters needed to operate the converter and to achieve full-range ZVS. Section IV discusses the control of the complete converter system, i.e., the interleaving control of all inductor currents, an input current control, and an output voltage control. Finally, Section V presents measurement results obtained from a low-height 200 W TCM PFC rectifier prototype.

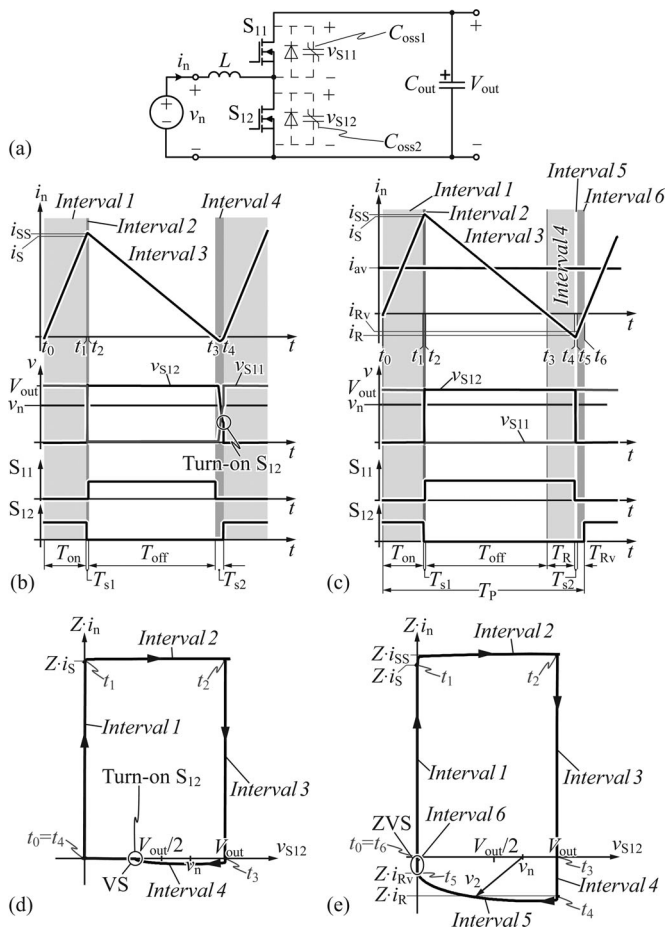

Fig. 3. (a) Single-cell configuration during the positive half-line cycle. (b) Current and voltage waveforms for valley switching. (c) Current and voltage waveforms for the proposed ZVS strategy. A detailed view of the switching transition in *intervals* 4 and 5 is given in Fig. 6. (d) *V–Zi* plot for valley switching. (e) *V–Zi* plot employing ZVS.

II. Basic Operation

This section presents the basic principle of the operation of a TCM PFC rectifier and points out the difference between valley switching and the proposed triangular mode modulation technique which allows for ZVS during the complete mains period.

Fig. 2(a) depicts the PFC rectifier circuit. There, for positive input voltages v_n, S_{N2} is turned ON and S_{N1} is turned OFF. The resulting simplified circuit is given in Fig. 3(a) and the converter operation is explained based on this circuit. The explanation, however, is similar for negative input voltages. There, only the roles of the upper switch S_{11} and the lower switch S_{12} are interchanged.

A typical input current waveform for critical conduction mode is depicted in Fig. 3(b) [19]. The switching period is split into two main intervals and two short resonant transitions. The initial conditions are

$$i_n(t_0) = 0, \qquad v_{S12}(t_0) = 0. \tag{1}$$

Interval 1 $[t_0, \ldots, t_1]$: During *interval* 1, the switch S_{12} is closed, v_n is applied to the inductor L, and the inductor current i_n increases linearly. As soon as the current i_S is reached or the on-time of S_{12}, $T_{\rm on}$, defined by the controller (cf., Section IV) has passed S_{12} is turned OFF

$$i_n(t_1) = i_S, \qquad v_{S12}(t_1) = 0. \tag{2}$$

Interval 2 $[t_1, \ldots, t_2]$: During this interval, a switching transition takes place in which the nonlinear MOSFET output capacitance $C_{\rm oss2}$ is charged and $C_{\rm oss1}$ is discharged. The voltages applied to the switches v_{S11} and v_{S12} follow according to the characteristic of the nonlinear capacitances. The switch voltages and currents during this interval can only be evaluated using numerical and iterative methods. Since i_n is large, however, the switching transition is very fast, and *interval* 2 can usually be neglected

$$i_n(t_2) = i_{\rm SS} \approx i_S, \qquad v_{S12}(t_2) = V_{\rm out}. \tag{3}$$

Interval 3 $[t_2, \ldots, t_3]$: When $C_{\rm oss2}$ is fully charged, the body diode of S_{11} starts to conduct the inductor current i_n and *interval* 3 starts. After an interlocking delay time (cf., Section IV), S_{11} is turned ON at zero voltage. During *interval* 3, the voltage applied to the inductor is negative and i_n decreases.

$$i_n(t_3) = 0, \qquad v_{S12}(t_3) = V_{\rm out}. \tag{4}$$

Interval 4 $[t_3, \ldots, t_4]$: Once i_n reaches zero, S_{11} is turned OFF and *interval* 4 begins. L, $C_{\rm oss1}$, and $C_{\rm oss2}$ form a resonant circuit which starts to oscillate. The behavior of the oscillation depends on the input to output voltage ratio $v_n/V_{\rm out}$. For $v_n/V_{\rm out} < 1/2$, v_{S11} rises to $V_{\rm out}$ and v_{S12} declines to zero and ZVS is achieved [19].

If $v_n/V_{\rm out}$ exceeds $1/2$, the instantaneous switch voltage $v_{S12}(t)$ does not reach 0 and ZVS cannot be achieved. Instead, the turn-on instant has to coincide with the instant when v_{S12} is minimal in order to minimize the switching losses [cf., Figs. 3(b) and 4(a)]. This is pointed out in the *V–Zi* plot in Fig. 3(d). The *V–Zi* plot shows a state graph of v_{S12} and i_n which are the state variables of the system. If the system trajectory reaches the ordinate after a switching cycle, ZVS can be achieved. Thus, the *V–Zi* plot clearly shows whether or not ZVS can be achieved [cf., Fig. 3(d)]

$$i_n(t_4) = 0 \tag{5}$$

$$v_{S12}(t_4) = \begin{cases} 0, & \text{if } v_n/V_{\rm out} < 1/2 \\ 2\,v_n - V_{\rm out}, & \text{else.}^1 \end{cases} \tag{6}$$

To overcome the drawback of losing ZVS during the mains period, a modified modulation technique can be applied. Considering the current waveform shown in Fig. 3(c), it is obvious that *intervals* 1–3 are similar to the waveforms depicted in Fig. 3(b). However, S_{11} is kept turned ON at the zero crossing of i_n and the current keeps decreasing linearly [cf., *interval* 4 in Fig. 3 (c)]

$$i_n(t_4) = i_{\rm R}, \qquad v_{S12}(t_4) = V_{\rm out}. \tag{7}$$

[1] Equation (6) assumes that the output capacitance is linear. An analytical expression that includes the nonlinearity of the capacitance is not feasible.

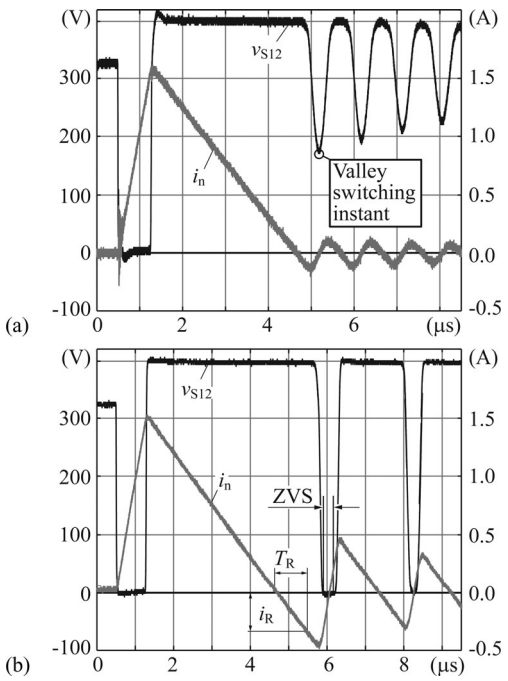

Fig. 4. Measurement results of a boost cell (a) without and (b) with an extended reverse conduction time $T_{\rm R}$ [cf., Fig. 3(b) and (c)]. In order to minimize the switching losses, (a) valley switching can be applied, whereas the extension of $T_{\rm R}$ allows for (b) ZVS over the complete mains period. (Parameters: $v_n = 328\,{\rm V}$, $V_{\rm out} = 400\,{\rm V}$, and $T_{\rm on} = 750\,{\rm ns}$).

Interval 5 $[t_4, \ldots, t_5]$*:*. As soon as a defined current $i_{\rm R}$ is reached or a given reverse conduction time $T_{\rm R}$ has passed (cf., Section IV) S_{11} is turned OFF and an oscillation starts (*interval* 5). Different to the previous situation shown in Fig. 3(b), the energy stored in the inductor now is large enough to completely charge $C_{\rm oss1}$ and discharge $C_{\rm oss2}$. Thus, v_{S12} reaches 0 during *interval* 5. The negative current $i_{\rm R}$ enlarges the elliptic oscillation trajectory [cf., v_2 in the *V–Zi* diagram of Fig. 3(e)] so that v_{S12} is able to decrease to 0. Consequently, ZVS can be achieved over the complete mains period by controlling the on-time of S_{11} and thus controlling the reverse current $i_{\rm R}$ in the inductor L

$$i_n(t_5) = i_{\rm Rv}, \qquad v_{S12}(t_5) = 0. \tag{8}$$

Interval 6 $[t_5 \ldots t_6]$: During *interval* 6, i_n commutates to the body diode of S_{12} and increases linearly. During this interval, S_{12} can be turned ON at zero voltage

$$i_n(t_6) = 0, \qquad v_{S12}(t_6) = 0. \tag{9}$$

Fig. 4 presents measurement results which illustrate the difference between valley switching and the proposed TCM. As can be clearly seen, applying an additional reverse current $i_{\rm R}$ allows for ZVS, which is particularly important for high switching frequencies.

A. Converter design

A PFC rectifier shapes the input current i_n to be proportional to the input voltage v_n. The average current $i_{\rm av}$ over a switching period [cf., Fig. 3(c)] has thus to be controlled by adjusting the on-time $T_{\rm on}$ and the reverse conduction time $T_{\rm R}$ during each switching cycle. Knowing these timing parameters allows for the determination of the switching frequency, the duty cycle, all converter currents, and the losses of the converter.

From Fig. 3(c) it can be concluded that there is an infinite set of combinations $\{T_{\rm on}, T_{\rm R}\}$ which lead to a required average current $i_{\rm av}$ since an increase of $T_{\rm on}$ can be compensated by a respective increase of $T_{\rm R}$ so that the average value of the input current $i_{\rm av}$ over the switching period keeps constant. The infinite set of applicable parameters $\{T_{\rm on}, T_{\rm R}\}$ can be used to adjust the switching period, $T_{\rm P}$. This can be beneficially used to interleave several boost cells (cf., Section IV). Large values of i_S and $i_{\rm R}$, however, result in an increased rms value of i_n and in a higher flux density swing in the boost inductor which increases copper and core losses, respectively. As a consequence, it is beneficial to keep the switching period as short as possible.

The average current $i_{\rm av}$ can be calculated numerically by integrating the inductor current [cf., Fig. 3(c)] over a switching period for a given input voltage $v_n(t)$ ($v_n(t) \approx$ constant is assumed during a single switching period)

$$i_{\rm av} = \frac{1}{T_{\rm P}} \sum_{j=1}^{6} \int_{t_{j-1}}^{t_j} i_n(t)\, dt. \tag{10}$$

Due to the nonlinearity of the MOSFETs' output capacitances *intervals* 2 and 5 can only be described by solving a nonlinear differential equation of the charge $q(t)$ in the capacitances

$$L \cdot \frac{d^2 q(t)}{dt^2} + v_{\rm C}(q(t)) = v_n \tag{11}$$

where $v_{\rm C}(q(t))$ represents the voltage applied to the parallel connection of the output capacitances $C_{\rm oss1}$ and $C_{\rm oss2}$.

This results in a considerable calculation effort as (11) can only be solved iteratively [20]. In order to simplify the calculation, an adequate model of the capacitance during the switching transition is detailed in the next section.

III. Closed-Form Analytical Converter Model

In order to obtain a sinusoidal input current of the TCM PFC rectifier i_n, it is crucial to determine the average current over a switching period [cf., (10)]. However, a switching period consists of switching transitions which depend on the nonlinear output capacitances of the applied MOSFETs. The respective current waveforms can only be solved numerically with iterative methods. This section presents a simple and accurate model that allows for closed-form solutions of the inductor current within a switching period in a TCM PFC rectifier. These closed-form expressions enable the calculation of the timing parameters needed for the control and the converter design, i.e., the loss evaluation of each component.

The derivation of the timing parameters has to be carried out for two cases: the first case considers $v_n > V_{\rm out}/2$ where an additional time $T_{\rm R}$ is required to achieve ZVS. In the second case, $v_n \leq V_{\rm out}/2$, $T_{\rm R}$ is not required to achieve ZVS but the oscillation needs to be modeled accurately in order to determine the timing values needed for the design and the control. For the

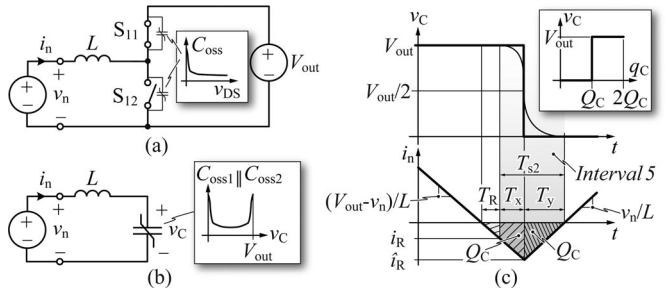

Fig. 5. (a) Bridge-leg for positive input voltage v_n during *interval* 4 [cf., Fig. 3(c)]. The output capacitance of S_{11} is discharged, whereas the capacitance of S_{12} is charged to the output voltage $V_{\rm out}$. (b) During the switching transition [*interval* 5 in Fig. 3(c)], both capacitors are connected in parallel. (c) Proposed model of the parallel connected nonlinear output capacitances of the switches for $v_n > V_{\rm out}/2$ which assumes a triangular-shaped current waveform. The peak current $\hat{i}_{\rm R}$ is assumed to occur when the output voltage $v_{\rm C}$ decreased to half of the initial value.

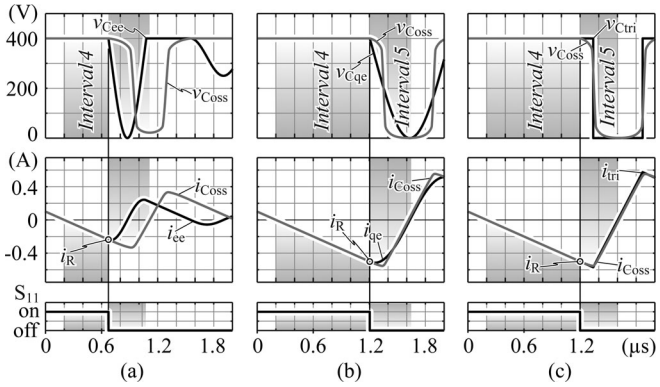

Fig. 6. Comparison between different capacitor models used to describe the nonlinear output capacitances of the MOSFETs. In simulations, each model is compared to the nonlinear capacitance given in the datasheet of the switch. (a) Energy equivalent linear capacitance, (b) charge equivalent linear capacitance, and (c) proposed charge model (13) of the capacitance. For each model, the corresponding current value $i_{\rm R}$ is calculated in order to achieve ZVS.

sake of brevity, only the first case is discussed in the following. However, the second case is derived analogously [23].

Considering a positive input voltage v_n and starting at *interval* 4 in Fig. 3(c), the equivalent circuit shown in Fig. 5(a) is obtained. There, the inductor current i_n is decreasing, $C_{\rm oss1}$ is discharged, and $C_{\rm oss2}$ is charged. Fig. 5(a) shows the typical characteristic of the MOSFET's output capacitance.

As soon as S_{11} is turned OFF, $C_{\rm oss1}$ and $C_{\rm oss2}$ are connected in parallel and the equivalent circuit illustrated in Fig. 5(b) is obtained. In order to discharge $C_{\rm oss2}$, the charge $Q_{\rm C}$

$$Q_{\rm C} = q_{\rm C}(V_{\rm out}) = \int_0^{V_{\rm out}} C_{\rm oss2}(v_{\rm C})\, dv_{\rm C} \tag{12}$$

has to be removed and, assuming identical switches, the same charge $Q_{\rm C}$ is needed to charge $C_{\rm oss1}$ to $V_{\rm out}$. Consequently, as soon as the time integral of the current i_n during *interval* 5 exceeds $2\,Q_{\rm C}$, ZVS can be achieved as $v_{\rm C}$ declines to zero.

The most simple capacitance model reduces the voltage $v_{\rm C}$ applied to the parallel connected capacitances $C_{\rm oss1}\|C_{\rm oss2}$ to

$$v_{\rm C}(q_{\rm C}) = \begin{cases} V_{\rm out}, & \text{if } q_{\rm C} > Q_{\rm C} \\ 0, & \text{else} \end{cases} \tag{13}$$

where as $q_{\rm C}$ is the charge in the capacitance $C_{\rm oss1}\|C_{\rm oss2}$. Fig. 5(c) illustrates the waveforms obtained with the proposed model and it can be seen that a triangular-shaped current i_n results and the derivation of an analytical expression becomes feasible. The proposed model (13) is based on the condition that

$$\int_{\rm Interval5} |i_n(t)|\, dt \geq 2 \cdot Q_{\rm C} \tag{14}$$

which can be assured by controlling the reverse current $i_{\rm R}$.

A simulation is used to validate the model and to compare it to other conventionally used models for nonlinear output capacitances, i.e., the (linear) energy-equivalent capacitance $C_{\rm ee}$ and the (linear) charge-equivalent capacitance $C_{\rm qe}$ [24]

$$C_{\rm ee}(V_{\rm out}) = \frac{2}{V_{\rm out}^2} \int_0^{V_{\rm out}} C_{\rm oss}(v_{\rm DS})\, v_{\rm DS}\, dv_{\rm DS} \tag{15}$$

$$C_{\rm qe}(V_{\rm out}) = \frac{1}{V_{\rm out}} \int_0^{V_{\rm out}} C_{\rm oss}(v_{\rm DS})\, dv_{\rm DS}. \tag{16}$$

Fig. 6 presents the simulation results. For each model, the required negative current $i_{\rm R}$ is calculated in order to achieve ZVS and compared to the nonlinear capacitance model specified in the datasheet of the applied MOSFET. Fig. 6(a) shows that the energy-equivalent model yields a poor approximation of the inductor current, the model even fails to predict whether ZVS can be achieved. The charge-equivalent model achieves a better approximation [cf., Fig. 6(b)]; however, resonant states need to be considered during *intervals* 2 and 5. The proposed model, finally, achieves a very good approximation of the inductor current without the need for resonant states [cf., Fig. 6(c)], which renders this model most suitable with respect to an analytical investigation of the TCM PFC rectifier.

The required negative current $i_{\rm R}$ is independent of the output power but only depends on $V_{\rm out}$, v_n, and the selected switch which defines $Q_{\rm C}$. Considering Fig. 5(c), $\hat{i}_{\rm R}$ can be calculated with

$$Q_{\rm C} = \frac{-\hat{i}_{\rm R}\, T_y}{2} \quad \Rightarrow \quad \hat{i}_{\rm R} = -\sqrt{\frac{2\,Q_{\rm C}}{L}\, v_n} \tag{17}$$

where as $L\, di/dt = L\,(-\hat{i}_{\rm R})/T_y = v_n$ has been substituted. With (17), $i_{\rm R}$ can be calculated with the same approach which yields

$$i_{\rm R} = \begin{cases} -\sqrt{\dfrac{2\,Q_{\rm C}}{L}\,(2\,v_n - V_{\rm out})}, & \text{if } v_n > V_{\rm out}/2 \\ 0, & \text{else} \end{cases} \tag{18}$$

i.e., no additional reverse current $i_{\rm R}$ is required for $v_n < V_{\rm out}/2$.

Applying the presented model of the nonlinear capacitances to *interval* 5 allows for the analytical description of each interval and a closed-form converter model is obtained. As already mentioned, *interval* 2 is also determined by a switching transition including nonlinear MOSFET capacitances but due to the large inductor current i_n, the switching transition is very fast and *interval* 2 can be neglected.

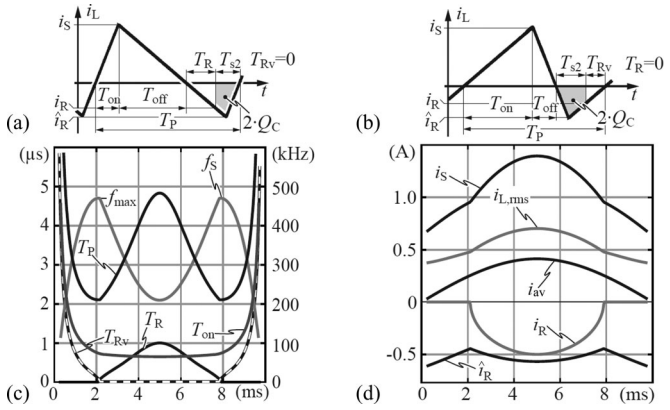

Fig. 7. (a) Inductor current waveform for $v_n > V_{\rm out}/2$ and (b) for $v_n \leq V_{\rm out}/2$. (c) Resulting switching timings and the switching frequency $f_{\rm S}$ over a half mains period. (d) Current values whereas $i_{\rm L,rms}$ is the local rms value and $i_{\rm av}$ is the local average value of the inductor current. Parameters: $V_n = 230\,{\rm V}$, $V_{\rm out} = 400\,{\rm V}$, $L = 150\,\mu{\rm H}$, $Q_{\rm C} = 75.2\,{\rm nC}$, and $P_{\rm out} = 200\,{\rm W}/3$. The output power is divided because three converter cells are considered.

Considering Fig. 7(a), the average current in the inductor over a switching period is

$$i_{\rm av} = \frac{1}{T_{\rm P}}\left(\frac{i_S \cdot T_{\rm on}}{2} + \frac{i_S \cdot T_{\rm off}}{2} + \frac{i_{\rm R} \cdot T_{\rm R}}{2} - 2 \cdot Q_{\rm C}\right). \tag{19}$$

The relation between inductor current and inductor voltage applied to each interval results in

$$i_S = \frac{v_n}{L} \cdot T_{\rm on}, \quad T_{\rm off} = \frac{L \cdot i_S}{V_{\rm out} - v_n}, \quad T_{\rm R} = \frac{L \cdot (-i_{\rm R})}{V_{\rm out} - v_n}. \tag{20}$$

The switching period is defined by

$$T_{\rm P} = T_{\rm on} + T_{\rm off} + T_{\rm R} + T_{s2} \tag{21}$$

with

$$T_{s2} = L \cdot \frac{-(\hat{i}_{\rm R} - i_{\rm R})}{V_{\rm out} - v_n} + L \cdot \frac{-\hat{i}_{\rm R}}{v_n}. \tag{22}$$

Substitution of (20)–(22) into (19) and solving for a desired average current $i_{\rm av}$ yields the on-time $T_{\rm on}$ [cf., (23)] and consequently all timing and current values. Fig. 7(c) presents the timing values and the switching frequency over a half mains period for the parameters listed in Fig. 7(b). Fig. 7(d) shows the respective current values. As can be seen, the required $i_{\rm R}$ is very high compared to i_S which is particularly pronounced for low power converters as the required input current is inherently small. For high power converters, this ratio decreases so that the additional rms current caused by the modulation has almost no impact [25] (23), as shown at the bottom of the page.

The determination of the required negative current $i_{\rm R}$ can also be easily implemented in a DSP which is needed for the rectifier's control presented in the following section.

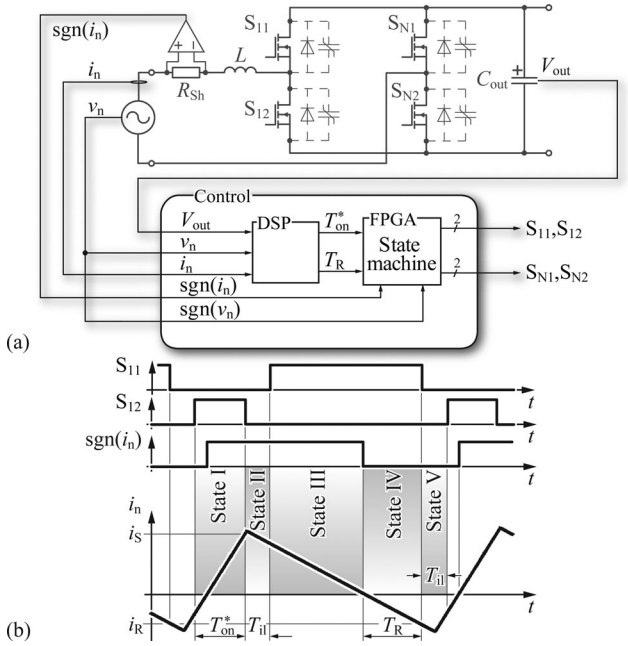

Fig. 8. (a) Schematic and simplified control structure of a single-cell TCM PFC rectifier which shows all required measurements. (b) State machine goes through each stage. It requires $T^*_{\rm on}$ and $T_{\rm R}$ which are determined in the DSP and the zero-crossing signal of the inductor current. A constant interlock delay $T_{\rm il}$ is considered.

IV. Control of the TCM PFC Rectifier

Based on the switching cycle discussed in Section II and the simplified model of the switching transition detailed in Section III, the converter control is described in this section. Contrary to control presented in [20], the proposed control does not need any lookup tables or interpolations which simplifies the implementation considerably. Fig. 8(a) depicts a single-cell TCM rectifier including a simplified control structure. The input quantities required for the control are the input voltage, the output voltage, the input current, and the sign of the inductor current which is determined using a shunt resistor and a high-speed comparator in each inductor path [20]. For high-power converters (up to several kilowatts), a current transformer with saturable core may be employed to reduce the conduction losses [25].

The DSP calculates the required on-time $T_{\rm on}$ and the reverse conduction time $T_{\rm R}$ according to the current values of v_n, $V_{\rm out}$, and i_n. With $T_{\rm on}$, $T_{\rm R}$, and the sign of the inductor current being known, a state machine residing in an field-programmable gate array (FPGA) generates the switching pattern illustrated in Fig. 8(b). The transitions between the five states are determined by either the specified timing value (States I, II, IV, and V) or the zero-crossing detection (State III → State IV). A constant interlocking delay time $T_{\rm il}$ is assumed for States II and V ($T_{\rm il} = 400\,{\rm ns}$ for the realized prototype).

$$T_{\rm on} = \frac{L \cdot i_{\rm av}}{v_n} + \sqrt{\frac{L}{V_{\rm out} \cdot v_n^2} \cdot \left(L\, i_{\rm av}^2\, V_{\rm out} + L\, i_{\rm R}^2\, v_n + 4\, v_n V_{\rm out} Q_{\rm C} - 4\, v_n^2\, Q_{\rm C} + 2\, i_{\rm av}\, V_{\rm out} \sqrt{L\, v_n Q_{\rm C}}\right)} \tag{23}$$

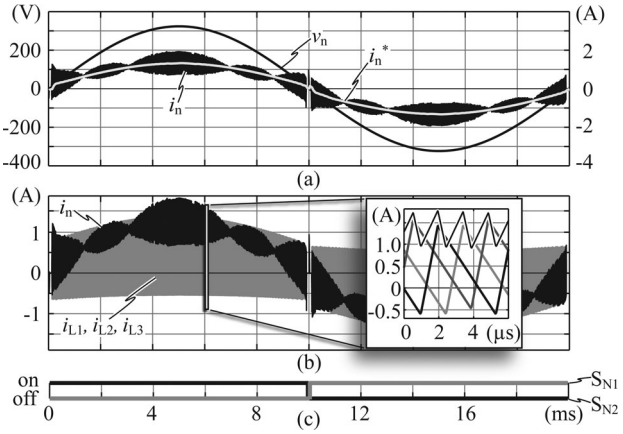

Fig. 9. Simulation results for a 200 W three-cell PFC rectifier system [cf., Fig. 2(b)]. (a) Mains voltage v_n, input current i_n, and first-order low-pass filtered input current i_n^* ($f_c = 16$ kHz). (b) Inductor currents including a magnified view which shows the smoothing effect of the superposition on the input current i_n. (c) Gate signals of the low frequency switching bridge-leg.

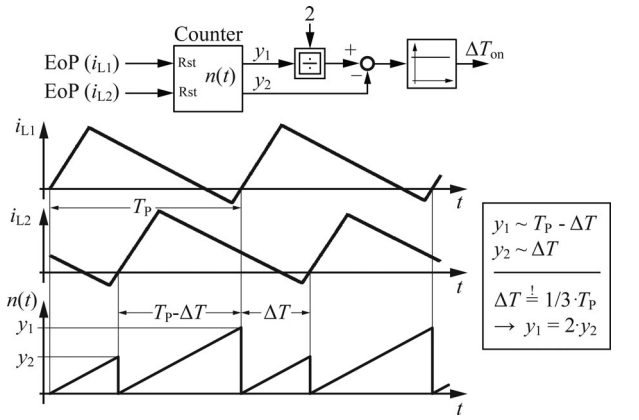

Fig. 10. Evaluation of the control signal for the interleaving control which is based on the EoP signals of each inductor current i_{L1}–i_{L3}. A counter is reset at EoP of each current and the values are then compared to each other.

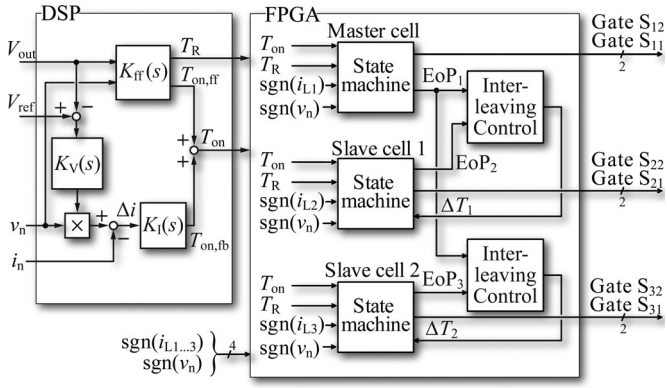

Fig. 11. Schematic of the control structure of the converter system which is subdivided into the state machine of each HF bridge-leg and the interleaving control of the inductor currents which are implemented in an FPGA and a superimposed input current and output voltage control realized in a DSP.

Contrary to the analysis of Section II, State I starts before the zero crossing of the i_n [cf., Fig. 8(b)] as the triggering of State I using the zero-current signal would be slightly time delayed and S_{12} would be turned ON without ZVS. Therefore, State I follows directly State V, while i_n is still negative and the parameter $T_{\rm on}^*$ has to be calculated including this additional time before the zero crossing of i_n which has been implemented in a feed-forward control $K_{\rm ff}$ of the current controller. The time delay of the zero-crossing signal triggering State IV is not critical as there is no switching transition involved which could lose ZVS.

A drawback of the presented topology in Fig. 8(a) is the large ripple of the inductor current i_n which results in a reduced power factor PF, a large total harmonic distortion (THD) value, and hence a large DM EMI filter size. In order to obtain a smooth input current, a multicell configuration can be applied [cf., Fig. 2(b)] where the superposition of several inductor currents results in a smooth input current i_n.

Fig. 9 depicts the simulation results of a 200 W three-cell TCM PFC rectifier system. The magnified part shows the input current i_n and the three inductor currents $i_{L1,\ldots,L3}$ and illustrates the input current ripple reduction achieved by means of interleaving the inductor currents. Applying a first-order low-pass filter with a cutoff frequency of $f_{\rm c} = 16$ kHz, the input current i_n^* can be achieved which has a THD value of 6.9% and a power factor of PF $=$ 99.6% ($v_n = 230$ V, $V_{\rm out} = 400$ V, $P_{\rm out} = 200$ W).

Fig. 10 presents the basic idea of the implemented interleaving control for two boost cells with the corresponding inductor currents i_{L1} and i_{L2}. There, the boost cell conducting i_{L1} is considered as master cell to which several other cells are synchronized. The only required input signal is the zero-crossing signal of each inductor current. For each boost cell, the end of a period (EoP) is characterized with a zero-crossing signal which changes from negative to positive.[2] A counter is reset on every EoP signal no matter from which cell it is generated. The resulting counter values y_1 and y_2 are thus proportional to $T_{\rm P} - \Delta T$ and to ΔT, respectively, and the desired delay between the two phases can be adjusted by selecting the ratio between y_1 and y_2. For example, a delay of $T_{\rm P}/3$ requires y_1 to be twice the value of y_2. Any deviation from this ratio is used as control parameter $\Delta T_{\rm on}$, and added to the slave cell as an extension or a reduction of its on-time. The input current can be kept constant by compensating $\Delta T_{\rm on}$ with a corresponding $\Delta T_{\rm R}$ as explained in Section II. Other interleaving control techniques can be found in [26]–[28].

The interleaving control and the state machines for each boost cell are implemented in an FPGA. Fig. 11 presents the implemented control of the multicell TCM PFC rectifier. The sign of the input voltage sgn(v_n) defines which switch of a bridge-leg is considered as boost switch and which is the free-wheeling switch. For example, for positive v_n, S_{x1} is the free-wheeling switch and S_{x2} is the boost switch where x corresponds to the bridge-legs $x = 1, \ldots, 3$.

The bridge-leg composed of S_{N1} and S_{N2} switches synchronously to the mains frequency [cf., Fig. 9(c)]. For positive input voltages v_n, S_{N1} is OFF, while S_{N2} is turned ON and

[2] This is valid for positive input voltages v_n. For negative input voltages, the sign changes accordingly.

TABLE II
CIRCUIT PARAMETERS OF THE 200 W TCM PFC RECTIFIER

Size: 221 mm × 157 mm × 5 mm			
Inductors EIR 23/5/13 [30]		**DSP and FPGA**	
L	150 µH	DSP	TMS320C2808 [31]
N	20	FPGA	LCMX02280C [32]
$I_{\rm sat}$	1.85 A		
Material	N49		
MOSFETs IPR60R385CP [33]		**Output capacitor [34]**	
$R_{\rm DS(on)}$	385 mΩ @ 25 °C	C	220 nF
$V_{\rm DS}$	650 V	$V_{\rm max}$	630 V
$Q_{\rm g,typ}$	17 nC	Package	2220
Package	D^2PAK	230 in parallel	

vice versa. This bridge-leg is hard-switched and considerable charging currents occur during the switching transitions which are detrimental for the THD value of the mains current. In order to prevent high peak currents during the switching operation of S_{N1} and S_{N2}, the switching speed of the low-frequency (LF) bridge-leg is decreased by selecting a very high gate resistance of several kiloohms. Since the modulation of the converter system is only active if the input voltage is larger than a threshold voltage ($|v_n| \geq 22$ V for the realized prototype), the slow switching speed of the LF bridge-leg has no effect on the converter operation if the LF bridge-leg is switched during the zero-crossing of v_n. With this modification, the current spikes reported in [22] are avoided and a smooth zero-voltage crossing is achieved without the need for a special gate signal pattern applied to the high-frequency (HF) bridge-legs as proposed in [21].

The control structure resides in the DSP and is composed of a feed-forward controller $K_{\rm ff}(s)$, a current controller $K_I(s)$, and a superimposed output voltage controller $K_V(s)$. The current controller and the output voltage controller are conventionally designed PI-controllers (e.g., [29]). The feed-forward controller $K_{\rm ff}$ calculates $T_{\rm on,ff}$ and $T_{\rm R}$ according to (18). As already mentioned, $T_{\rm on,ff}$ is determined in order to consider the difference between $T_{\rm on}$ and $T^*_{\rm on}$, [cf., Figs. 3(c) and 8(b), respectively).

V. LABORATORY SETUP

In order to validate the proposed model and the simulation results, a 200 W TCM PFC rectifier has been designed and realized. The design of the prototype aims for an ultraflat shape of the converter outline, and therefore, all components are selected with respect to a low thickness.

Table II lists the circuit parameters of the prototype featuring an overall thickness of 5 mm and Fig. 12(a) and (b) presents the measured inductor currents and the switch voltage v_{S12} for the prototype being operated as dc–dc converter at two different operating points. Obviously, v_{S12} declines to 0 V and ZVS is achieved. Furthermore, the interleaving control of the inductor currents works properly. The negative current $i_{\rm R}$ is slightly less than the calculated value ($i_{\rm R,calc} = -570$ mA, $i_{\rm R,meas} = -750$ mA at $v_n = 325$ V) due to the time delay imposed by the zero-current detection, the signal processing in the FPGA, and the turn-off delay of the switch.

Fig. 12 further depicts the measured efficiencies for both dc–dc operating points, and Table III lists the calculated loss contribution of each component. As can be seen, the core losses of the boost inductor determine the overall efficiency, and hence, the core losses have to be reduced for a further efficiency improvement. It is interesting to note that the core losses at $v_n = 230$ V are higher than at 325 V because the switching frequency is higher at 230 V, whereas the flux density swing in the core remains approximately constant ($f_S = 325$ kHz, $\Delta B = 266$mT at 230 V, $f_S = 178$kHz, and $\Delta B = 300$mT at 325 V).

For PFC rectifier operation, the prototype achieves an efficiency of $\eta = 94.6\%$ and a power factor PF $= 99.3\%$ at full load of $P_{\rm out} = 200$ W (measured with a Precision Power Analyzer WT3000 [35]). Fig. 13(a) presents the measurement result of input voltage v_n and input current i_n and Fig. 13(b) illustrates the

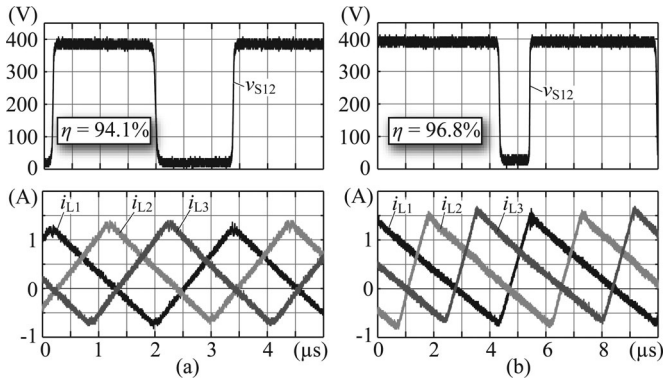

Fig. 12. Measurement results of converter system operating in dc–dc mode. The figure shows that each bridge-leg operates in ZVS mode and that the interleaving of the inductor currents is properly achieved with the presented interleaving control method. (a) $v_n = 230$ V, $V_{\rm out} = 400$ V, and $P_{\rm out} = 200$ W. (b) $v_n = 325$ V, $V_{\rm out} = 400$ V, and $P_{\rm out} = 400$ W.

TABLE III
CALCULATED LOSS DISTRIBUTION OF THE PROTOTYPE OPERATED IN DC–DC MODE

	$v_{\rm n} = 230$ V, $P_{\rm out} = 200$ W	$v_{\rm n} = 325$ V, $P_{\rm out} = 400$ W
$P_{\rm core}$	7.7 W	5.3 W
$P_{\rm wind}$	1.5 W	2.2 W
$P_{\rm cond}$	0.7 W	0.9 W
$P_{\rm gate}$	0.5 W	0.3 W
$P_{\rm aux}$	2.0 W	2.0 W
$P_{\rm tot}$	12.4 W	10.7 W
$\eta_{\rm calc}$	94.2 %	97.4 %
$\eta_{\rm meas}$	94.1 %	96.8 %

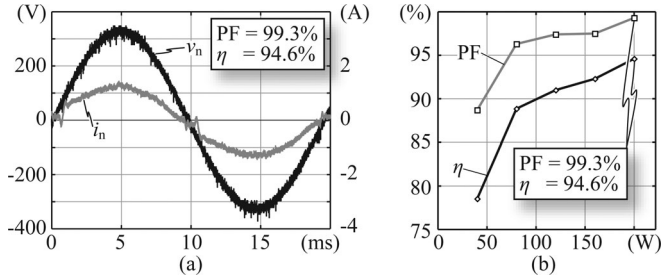

Fig. 13. (a) Input voltage v_n and input current i_n of the TCM PFC rectifier ($V_n = 230$ V, $V_{\rm out} = 400$ V, $P_{\rm out} = 200$ W). (b) Efficiency η and power factor PF as a function of the output power $P_{\rm out}$.

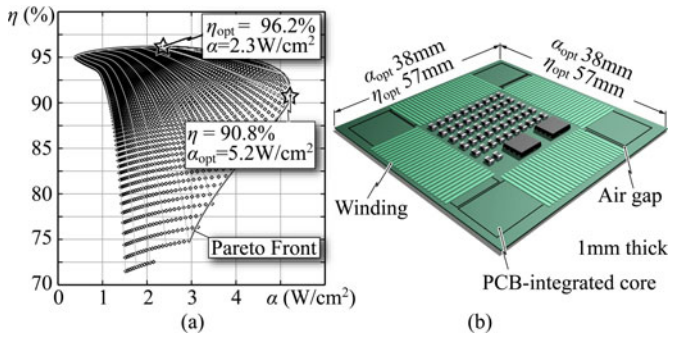

Fig. 14. (a) α-η-Pareto front of a PCB-integrated boost inductor, which allows for an ultraflat realization of the converter system. A detailed description of the design procedure is given in [37]. (b)Three-dimensional sketch of a PCB-integrated boost inductor. The dimensions are given with respect to the two optima indicated in (a). Due to the large winding window, several components could be placed within the boost inductor in order to increase the power density α.

measured efficiency η and power factor PF as a function of the load. In order to analyze the benefit of the TCM modulation over the conventional valley switching, the switching losses of valley switching have been calculated which results in $P_{\mathrm{V}} = 2\,\mathrm{W}$ per switch. All six HF switches would thus cause 12W additional losses and the overall converter losses would double. Therefore, the TCM modulation achieves a considerably benefit over conventional employed modulation methods.

The presented topology is also applicable to higher power levels, e.g., [36] reports a 3.3 kW TCM PFC rectifier which achieves an efficiency of more than 99% over the entire load range at a power density of 1.1 kW/dm^3.

All components of the realized 200 W prototype are surface mounted in order to simplify the manufacturing, tests, and measurements which results in a converter height of 5 mm. A converter thickness of 1 mm would be feasible with all components being integrated into the PCB. It becomes apparent in [37] that the main challenge is the realization of PCB-integrated magnetic components, and thus, a comprehensive design procedure for PCB-integrated magnetic components is presented there. Applying this design procedure to the boost inductor of the TCM PFC rectifier yields the α-η-Pareto front presented in Fig. 14(a) which depicts several inductor designs. The Pareto front, indicated in Fig. 14(a), shows the tradeoff between inductor efficiency η and its area-related power density α. The optimal designs with respect to η or α are indicated in the figure and an illustration of the PCB-integrated inductor with magnetic core and with the windings realized as tracks and vias is shown in Fig. 14(b); there, the dimensions for both optima are given.

VI. Conclusion

This paper presented the analysis and the modeling of a single-phase multicell TCM PFC rectifier and discussed the implications on the design of an extremely thin converter with a targeted thickness of 1 mm. In order to achieve this low height, all components have to be integrated into the PCB. Due to the resulting stringent converter requirements, a modified multicell totem-pole PFC rectifier is considered to be most appropriate for the specified ultraflat PFC rectifier, since this topology enables low conduction losses, low switching losses, and reduced EMI filter requirements. It is shown that full-range ZVS can be achieved with a specific modulation technique entitled TCM. However, the nonlinear output capacitances of the MOSFETs need to be considered, since they have a strong impact on the inductor current waveform and on the timing parameters. The proposed simplified capacitance model facilitated the derivation of closed-form expressions which allows for a straightforward design of each component and an accurate loss estimation. Furthermore, it is implemented in a DSP to calculate the timing values which would not be possible with a more complex model due to the required calculation effort. This paper further detailed the implemented control structure including interleaving control, input current control, and output voltage control. All theoretical considerations were validated using measurement results on a prototype of a 200 W three-cell TCM PFC rectifier. The realized PFC rectifier achieved an efficiency of $\eta = 94.6\%$ and a power factor of PF $= 99.3\%$ at a footprint size of 221 mm $\times$ 157 mm and a thickness of $h = 5$ mm.

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