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# Three-Phase High Power Factor Mains Interface Concepts for Electric Vehicle Battery Charging Systems

T. Soeiro,
T. Friedli,
J. W. Kolar



Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

# Three-Phase High Power Factor Mains Interface Concepts for Electric Vehicle Battery Charging Systems

T. Soeiro, T. Friedli and J. W. Kolar
Power Electronic Systems Laboratory
ETH Zurich, Switzerland
Email: soeiro@lem.ee.ethz.ch

***Abstract*— This paper discusses novel three-phase high power factor mains interfaces appropriate for Electric Vehicle (EV) battery charging systems. Initially, a highly efficient two-stage ac-dc system, consisting of a three-phase line-commuted rectifier combined with a three-phase shunt connected Active Power Filter (APF) and a group of interleaved dc-dc buck converters operating in Triangular Current Mode (TCM), is presented. In order to replace the costly APF circuit of the front-end converter, while maintaining PFC capability at the input and allowing similar operating conditions for the back-end dc-dc converter, a rectifier topology employing an active third harmonic current injection circuit is proposed. In addition, a novel three-phase buck-type PFC rectifier is introduced for EV charging systems. The characteristics of the presented EV systems, including the principle of operation, modulation strategy, suitable control structures, and dimensioning equations, are described in detail. Finally, a comprehensive comparison of the studied converters rated to 12 kW is shown.**

## I. Introduction

Charging of Electric Vehicle (EV) batteries inherently requires conversion of energy from the ac mains into dc-quantities. Several charging voltage and power levels have been defined by different standardization organizations (IEC 61851, IEC62196, SAE J1772). Single-phase Power Factor Corrector (PFC) mains interfaces are commonly employed for low charging power levels (e.g. $P < 5$ kW), whereas for higher charging power levels, three-phase PFC mains interfaces have to be employed [1]. The EV charger, typically implemented as a two-stage system, i.e. comprising a PFC rectifier input stage followed by a dc-dc converter, can be either integrated into the car (on-board chargers) or accommodated in specially designed EV charging stations (off-board chargers) [2]. Basic requirements for such systems are controlled output voltage, high power factor, and high efficiency. If the power electronics has to be accommodated on-board the EV, a low weight and high power density are also desirable [1]-[4]. Finally, if isolation of the PFC output from the dc-bus is necessary due to safety reasons, this could be provided by an isolated dc-dc converter. Possible Power Electronics (PE) configurations for charging of EVs are given in **Fig. 1**.

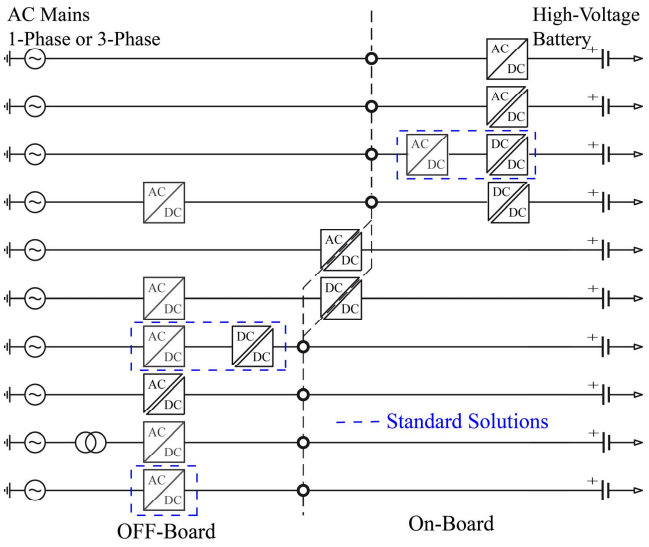



**Fig. 1:** Power electronic converter topologies for EV charging systems.

With respect to public high power charging infrastructures, also called semi- or ultra-fast chargers, the nearly empty battery should be re-charged in the shortest time possible. These EV chargers, supplied from three-phase ac lines at 110 / 230 V (*rms*) and 50 / 60 Hz, typically require a peak power ranging from 10 kW to 150 kW in order to inject direct current into the battery sets at variable voltage levels according to the vehicle (50 V to 600 V) [5]. Buck-type three-phase PFC rectifiers, also known as Current Source Rectifiers (CSRs), are appropriate for these high power chargers as a direct connection to the dc-bus could be used. Compared to the boost-type systems, buck-type topologies provide a wider output voltage control range, while maintaining PFC capability at the input and can potentially enable direct start-up, while allowing for dynamic current limitation [3]-[7]. In addition, three-phase boost-type rectifiers generate an output voltage which is too high to directly feed the dc-bus (typ. 700 V to 800 V), requiring a step-down dc-dc converter at their output.

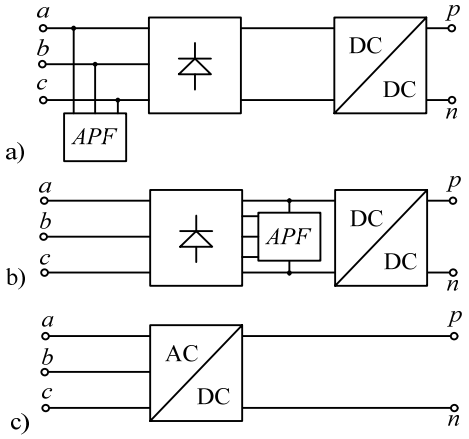



**Fig. 2:** EV battery charger concepts employing **a)** a three-phase active power filter and dc-dc converter, **b)** active 3rd harmonic current injection rectifier as front-end converter and a dc-dc converter, and **c)** a single-stage ac-dc converter.

In order to be compliant with IEC harmonic injection standards and also achieve high power factor operation, non-isolated three-phase mains interface concepts well suitable for semi- or ultra-fast chargers are analysed and/or proposed in this paper (cf. **Fig. 2**). A remarkable two-stage ac-dc system, consisting of a three-phase full-bridge line-commuted rectifier combined with a three-phase shunt connected Active Power Filter (APF) and a group of interleaved dc-dc buck-type converters performing the charging process, is analyzed in **Section II** [cf. **Fig. 2(a)** and **Fig. 3**]. Additionally, to facilitate the selection of a Voltage Source Converter (VSC) for the APF of the proposed EV charger, an efficiency comparison between two- and three-level VSC topologies is presented. The analyses are performed for 12 kVAr, 3x400 V / 50 Hz converters in the switching frequency range of 5 kHz to 48 kHz and with a dc-link voltage level of $U_{DC}$ = 800 V. The analyses show that for a highly efficient 12 kVAr / 48 kHz APF system the three-level neutral-point-clamped (NPC) converter represents the natural solution for implementation. In **Section III,** a hybrid 3rd harmonic injection PFC rectifier circuit built by the combination of an active-filter-type 3rd harmonic injection rectifier and a series connected dc-dc buck-type converter is proposed for EV applications [cf. **Fig. 2(b)**]. The buck stage to be controlled as a current supply with controllable dynamic current limitation can be assembled with single or interleaved dc-dc converters. The implementation with a single dc-dc buck-type converter is shown in **Fig. 4**. **Section IV** introduces a single-stage EV charger [cf. **Fig. 2(c)**] employing the novel three-phase buck-type PFC rectifier topology shown in **Fig. 5**, known as SWISS Rectifier. The characteristics of this new topology, suitable control stage, and methods for calculating losses of all components are also given. Finally, in **Section V**, the proposed EV systems, rated to 12 kW and fully designed for employing commercial components, are systematically compared.

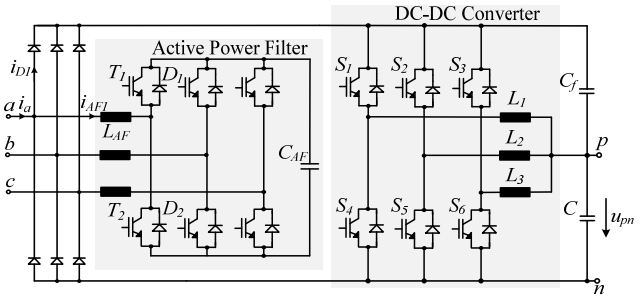



**Fig. 3:** EV battery charger employing a three-phase two-level active power filter and interleaved dc-dc buck converters.

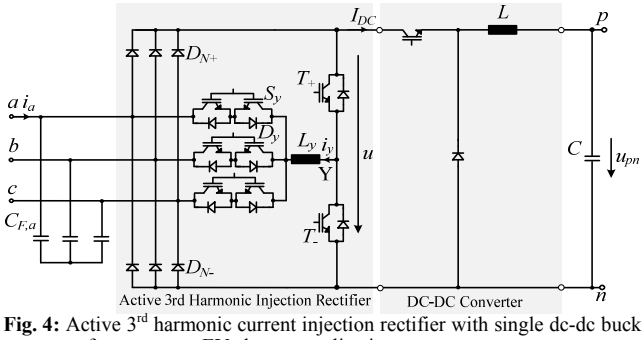



**Fig. 4:** Active 3rd harmonic current injection rectifier with single dc-dc buck converter for two-stage EV charger applications.

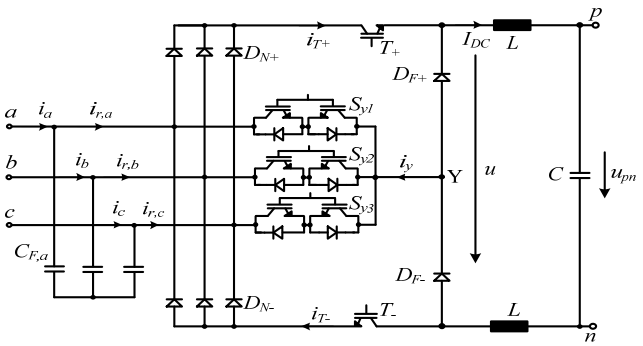



**Fig. 5:** Circuit topology of the buck-type SWISS Rectifier.

## II. TWO-STAGE EV BATTERY CHARGING EMPLOYING ACTIVE POWER FILTERS

**Fig. 3** shows a highly efficient two-stage ac-dc converter appropriate for EV charging applications. This system consists of a three-phase full-bridge line-commuted rectifier combined with a three-phase two-level shunt connected APF and a group of interleaved dc-dc buck converters. One advantage of this approach is the relatively small power rating of the APF, which remains approximately 40% of the charging power demanded by the battery [6]. Additionally, the system can fully benefit from the high reliability of the line-commuted rectifier, as in case of an APF failure, the EV charger could remain in operation, but without power factor correction capability.

In **Fig. 6**, suitable shunt active filters, derived from the three-phase three-level T-type and three-level I-type (NPC) VSCs, are presented. For low grid voltage levels, i.e. for a *rms* line-to-line voltage between 320 V to 530 V, the three-level topologies are not wide spread because of the intrinsically large number of components and consequently the high costs. On the other hand, a three-level APF built with

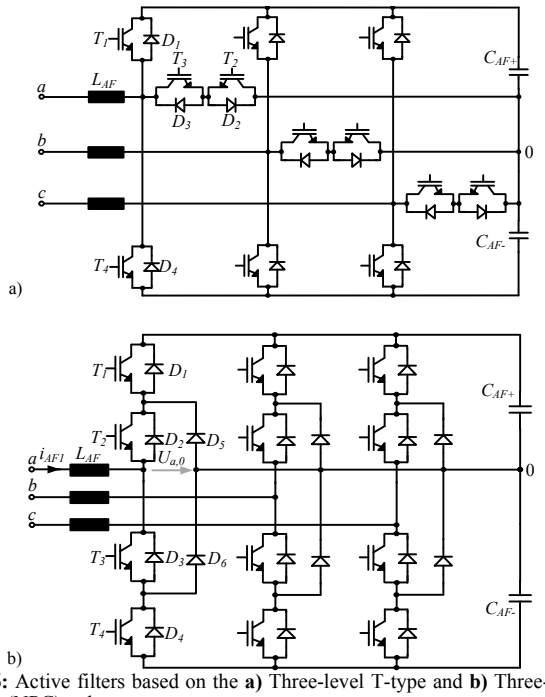



**Fig. 6:** Active filters based on the **a)** Three-level T-type and **b)** Three-level I-type (NPC) voltage source converter.

600 V semiconductors can achieve lower losses than a two-level system built with 1200 V devices if the considered switching frequency is high enough (typ. > 10 kHz) [7]. Consequently, 3-level APFs constitute interesting solutions for applications which aim for outstanding efficiency at low weight/volume.

An efficiency comparison between APFs derived from the two- and three-level topologies for 12 kVAr power capability is shown in **Fig. 7**. The analyses are performed for converter operation in the switching frequency range of 5 kHz to 48 kHz, 400 V line-to-line *rms* grid voltage, and 800 V dc-link voltage level. The 600 V IGBTs IKW30N60T and the 1200 V IGBTs IKW25T120 from Infineon are selected for the assessment and their loss characteristics are determined with a test set-up [cf. **Fig. 7(a)**]. A Space Vector Modulation (SVM) scheme incorporating an optimal clamping of the phase is selected for analysis. When compared to a simple carrier-based sinusoidal pulse-width modulation (SPWM), even for low switching frequencies, the SVM strategy demonstrates better efficiency and loss distribution features (cf. [8]).

Due to the fact that the 1200 V devices in the T-type active filter are mostly commuted at 400 V (half of the dc-link voltage) instead of 800 V compared to the two-level VSC, the switching losses are considerably reduced. Therefore, for low switching frequency values, the three-level T-type active filter already shows superior performance than the conventional two-level VSC. Compared to the three-level I-type VSC, the T-type system has lower conduction losses, but higher switching losses. For the considered APF specification, the efficiency of the T-type converter is the best for switching frequencies up to $f_P = 30$ kHz. On the other hand, for higher switching frequencies, the three-level I-type APF is superior. Therefore, for a highly efficient 12 kVAr / 48 kHz APF, the three-level I-type converter is the natural solution for implementation.

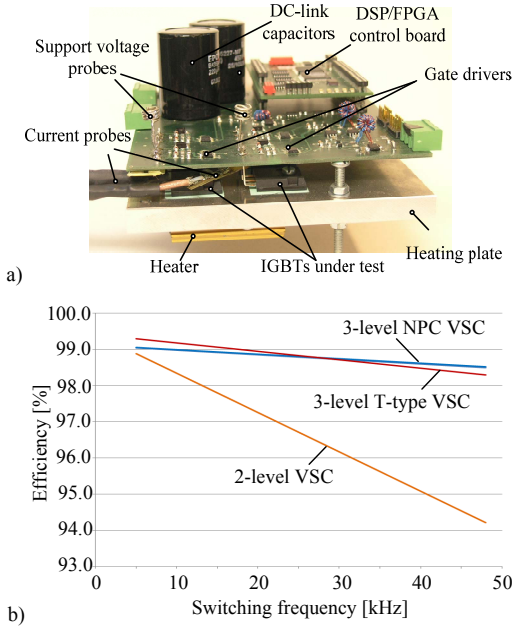



**Fig. 7: a)** Switching loss measurement set-up and **b)** efficiency comparison between the different topologies of 12 kVAr APFs employing commercial semiconductors.

**Fig. 8(a)** shows a designed 12 kVAr / 48 kHz three-phase three-level NPC APF prototype. It uses custom three-level bridge-leg modules employing SiC Schottky diodes to enable highly efficient operation [diodes $D_1$, $D_4$, $D_5$, and $D_6$ in **Fig. 6(b)**]. A digital signal processing board with a TI DSP and a Lattice FPGA is used to implement a "dq-frame" control strategy and a SVM using clamping of the phase conducting the highest current. The power density of this APF is 3.65 kVAr/dm$^3$. The performance of the EV charger employing the designed APF is shown in **Fig. 8(b)**. As can be noted, the system can efficiently compensate the current harmonics of the load as the line currents have a sinusoidal shape ($THD_I \approx 4\%$). The results attest the feasibility of this solution.

In order to simultaneously achieve high power density as well as high efficiency, while the EV charger output current ripple is kept small, a modular configuration of interleaved dc-dc converters is presented in this paper. For a 12 kW EV charger specification, two paralleled 6 kW ultra-efficient (≈ 99%) multi-cell converters are designed, each consisting of three interleaved buck stages operating in Triangular Current Mode (TCM), which features zero voltage switching (ZVS) for the employed power MOSFETs (cf. **Fig. 9**). The high TCM inductor current ripple is not transferred to the EV battery set as the superposition of all buck cells currents, $i_{L1,2,3}$, results in a smooth output current waveform $i_L$, with relatively low ripple. Additionally, the reverse-recovery behavior of the MOSFET body diode becomes irrelevant, and consequently very low switching losses are achieved.

**Fig. 9** shows the basic configuration of the proposed modular dc-dc converter, including the control strategy used for a single buck sub-cell. Note that the ZVS switching can be achieved because the inductor current declines to zero and a subsequent oscillation between inductor and parasitic

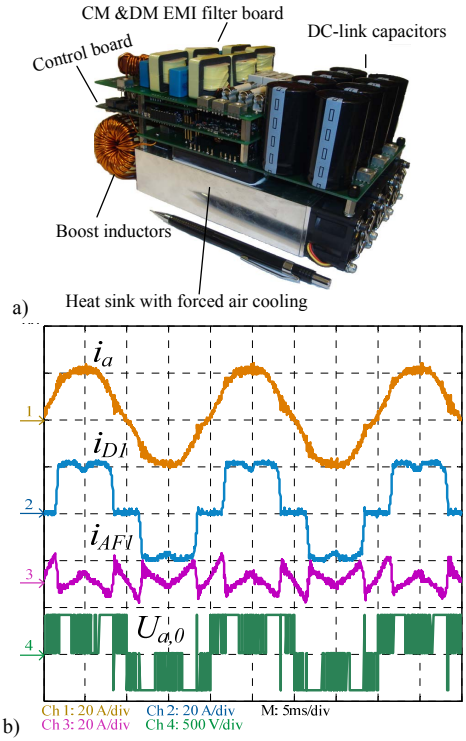



**Fig. 8: a)** Three-level APF prototype and **b)** main experimental waveforms.

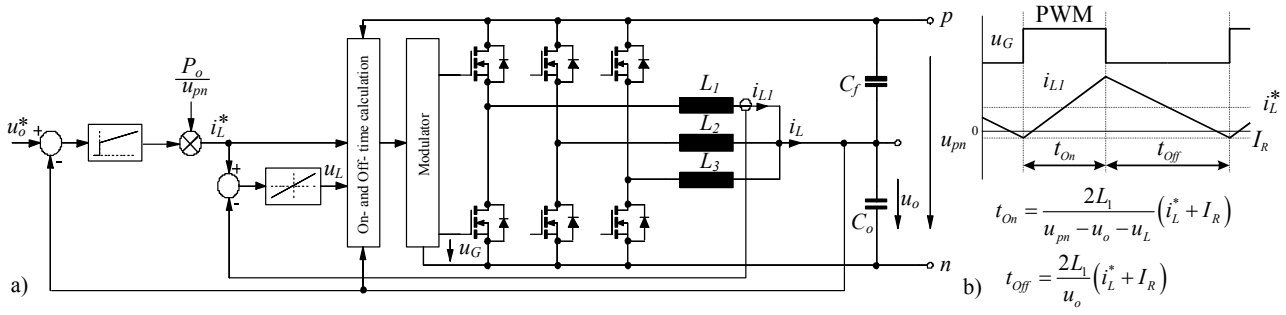



**Fig. 9: a)** Three interleaved dc-dc buck-type converters and **b)** proposed control scheme.

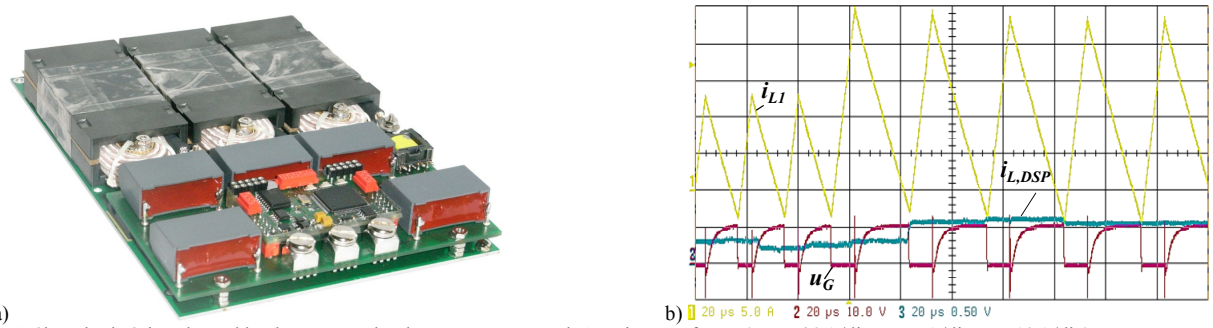



**Fig. 10: a)** 6 kW dc-dc 3-interleaved buck converter hardware prototype and **b)** main waveforms ($i_{L,DSP}$: 30 A/div, $i_{L1}$: 5 A/div, $u_G$: 10 A/div).

MOSFET capacitors starts in which the voltage across the power semiconductors of the bridge-leg drops and increases to 0 and $u_{pn}$, respectively. In order to avoid a Valley Switching (VS) condition, where the parasitic capacitors are not fully charged/discharged (loss of ZVS switching), the inductor current is actively decreased below zero until it reaches a specified value $I_R$, which sustains ZVS switching. For more details about the TCM operation of interleaved converters, see [9].

In order to validate the presented control method and calculations for the output stage of the rectifier, a 6 kW ultra-efficient (≈ 99%) high-power density (10 kW/dm$^3$) dc-dc converter prototype, as depicted in **Fig. 10(a)**, has been built. In **Fig. 10(b)**, measurement results for operation at 200 V output voltage and a load step are shown, which includes the total interleaved output current calculated by the DSP $i_{L,DSP}$ (30 A/div), the TCM operation with ZVS switching for a single buck sub-cell $i_{L1}$ (5 A/div), and gate signal $u_G$ (10 V/div). The results confirm the proper operation of the designed converter, as even during load transients, a smooth continuous total output current with low ripple could be achieved, while ZVS switching for the MOSFETs is preserved.

## III. Two-Stage EV Battery Charging Employing Active 3rd Harmonic Injection Rectifier

**Fig. 4** shows the basic configuration of a three-phase high power factor active third harmonic injection rectifier and a series connected dc-dc buck-type converter appropriate for EV charging mains interfaces. The front-end converter consists of a three-phase high-efficiency electrolytic capacitor-less line-commuted rectifier combined with an active current injection circuit (cf. [10]). The latter circuit can effectively replace the APF system of the front-end converter depicted in **Fig. 3**, because it allows to sinusoidally shape the input current of the line- commuted system. The current injection circuit is formed only by a single fast-commuted half-bridge-leg, an inductor, and three low frequency bidirectional switches. Advantageously, the negative output voltage terminal is always connected to the mains via a diode of the lower half bridge of the diode rectifier. Therefore, no output CM voltage with switching frequency is generated.

The third harmonic injection rectifier of the proposed EV charger shows a relatively low implementation effort, however, at the expense of a missing output voltage control. The output voltage is now determined directly by the diode bridge rectifier and hence exhibits a six-pulse shape. Therefore, a series connected dc-dc converter is necessary to provide the charging requirements of the EV battery. If the back-end converter, i.e. a group of interleaved dc-dc buck-type converters, is controlled to demand constant power, currents varying in opposite phase to the six-pulse rectifier voltage will be impressed at the input of the rectifier. As shown in **Fig. 11**, this leads to a sinusoidal shape of all mains phase currents after overlaying with a 3rd harmonic controlled injection current $i_y$.

A suitable feedback control structure and the main converter dimensioning equations, which include the average and *rms* current values of the power semiconductors, are given in **Fig. 11(a)**. The modulation of the current injection circuit is performed at low frequency following the rectifier input voltages $u_{a,b,c}$ in such a way that the active current injection always occurs into only one mains phase as presented in **Tab. I** (cf. **Fig. 12**).

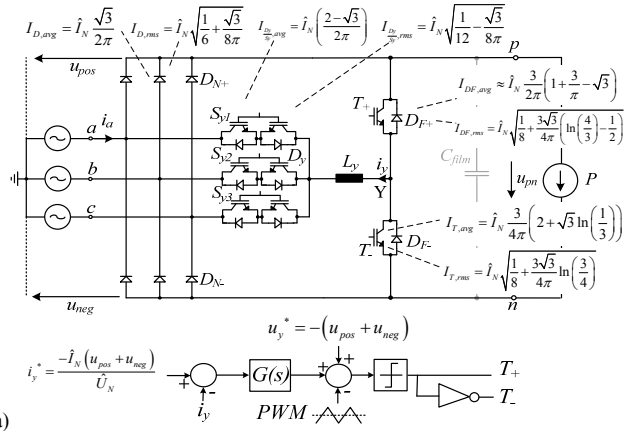
For proof of the sinusoidal controllability of the mains currents, the equivalent circuit of the proposed EV charger for the mains interval $[0, \pi/3]$ ($u_a > u_b > u_c$), which is depicted in **Fig. 11(b)**, is considered for analysis. Ideally, the rectifier system operates as a symmetric three-phase load of (fundamental) phase conductance $G$ to the mains, therefore,

the value of the current to be injected into phase *b* may be written as

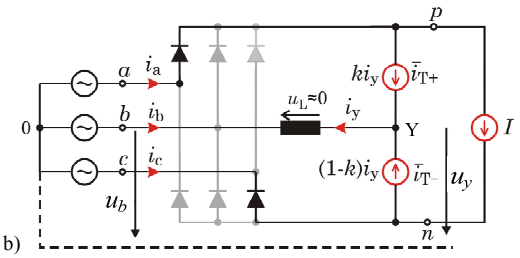
$$i_y = -i_b = -Gu_b \tag{1}$$

The mains frequency voltage drop across the inductor of the current injection circuit can in a first approximation be neglected for the formation of $i_y$,

$$u_L = 0\,. \tag{2}$$




a)

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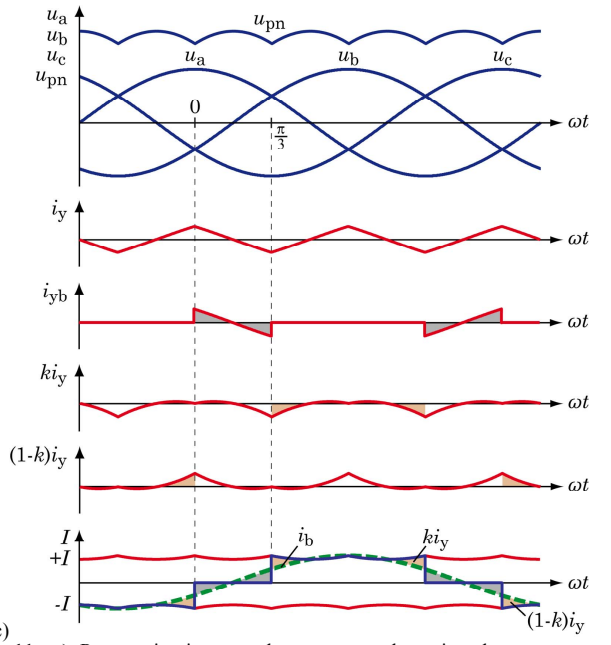


c)

**Fig. 11: a)** Power circuit, control structure and semiconductors current stresses of the active-filter-type 3rd harmonic current injection rectifier; **b)** equivalent circuit of the rectifier for $u_a > u_b > u_c$. **c)** Main waveforms of the EV charger front-end converter for constant output power consumption *P* of the back-end converter. $\hat{U}_N$ and $\hat{I}_N$ are the amplitude of the phase voltage and current, respectively.

Accordingly, the voltage formed at the output of the bridge-leg will be given by

$$u_y = u_b\,. \tag{3}$$

If the voltage at the terminal *Y* is formed according the relative on-time of the transistor $T_+$ as *k* and $T_-$ as (1-*k*), it will result in

$$u_L = ku_a + (1-k)u_c = ku_{ac} + u_c\,. \tag{4}$$

For the duty cycle *k* given by

$$k = \frac{u_{bc}}{u_{ac}}\,, \tag{5}$$

the current in $T_+$ can be calculated as

$$\overline{i}_{T+} = ki_y = -ki_b = -kGu_b = -Gu_b\frac{u_{bc}}{u_{ac}}\,. \tag{6}$$

Considering the fundamental input currents that have to be generated at the input

$$i_a = Gu_a\,;\; i_b = Gu_b \;\text{ and }\; i_c = Gu_c\,, \tag{7}$$

the current consumption of the constant power load can be calculated via

$$I = \frac{P}{u_{ac}} = \frac{i_a u_{ac} + i_b u_{bc}}{u_{ac}} = G\frac{u_a u_{ac} + u_b u_{bc}}{u_{ac}}\,. \tag{8}$$

Accordingly, the resultant low frequency current drawn from phase *a* is proportional to the mains voltage

$$i_a = I + \overline{i}_{T+} = Gu_a\,. \tag{9}$$

Additionally, the low frequency current for phase *c* can be determined using (1), (9), $i_a + i_b + i_c = 0$ and $u_a + u_b + u_c = 0$ as

$$i_c = Gu_c\,. \tag{10}$$

With this, the sinusoidal shape of all phase currents has been proved.

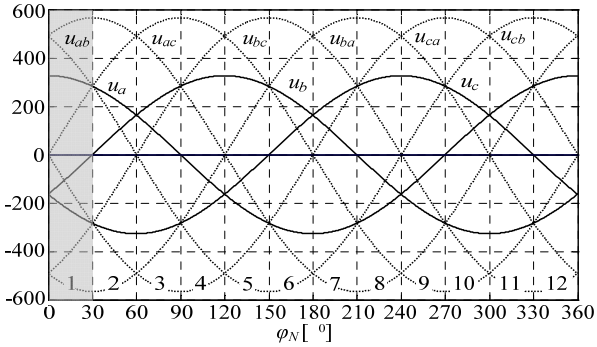


**Fig. 12:** Mains sectors 1 to 12 defined by the different relations of the instantaneous values of the mains phase voltages $u_{a,b,c}$.

**TABLE I:** Modulation of the current injection circuit (cf. **Fig. 12**).

| Sector | $S_{y1}$ | $S_{y2}$ | $S_{y3}$ | Sector | $S_{y1}$ | $S_{y2}$ | $S_{y3}$ |
|---|---|---|---|---|---|---|---|
| 0°-30° | 0 | 1 | 0 | 180°-210° | 0 | 1 | 0 |
| 30°-60° | 0 | 1 | 0 | 210°-240° | 0 | 1 | 0 |
| 60°-90° | 1 | 0 | 0 | 240°-270° | 1 | 0 | 0 |
| 90°-120° | 1 | 0 | 0 | 270°-300° | 1 | 0 | 0 |
| 120°-150° | 0 | 0 | 1 | 300°-330° | 0 | 0 | 1 |
| 150°-180° | 0 | 0 | 1 | 330°-360° | 0 | 0 | 1 |

**Fig. 13** presents a 7.5 kW hardware implementation of the proposed EV charger depicted in **Fig. 4**. This system was designed to enable operation as the EV charger depicted in **Fig. 5** (SWISS Rectifier) by only performing small changes in the prototype circuit. The overall dimensions of the system are 210 mm x 132 mm x 92 mm, hence giving a power density of 2.94 kW/dm$^3$.

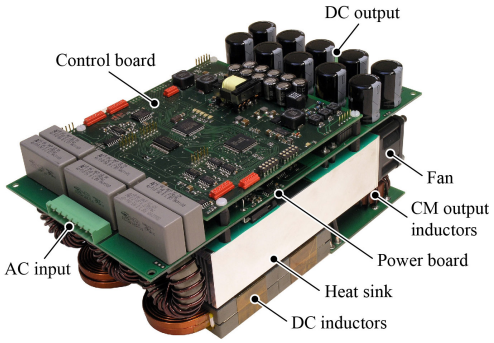


**Fig. 13:** 7.5 kW active-filter-type 3rd harmonic current injection rectifier hardware prototype to operate as converter according to **Fig. 4** or **Fig. 5**.

## IV. SINGLE-STAGE EV BATTERY CHARGER EMPLOYING ACTIVE 3RD HARMONIC INJECTION RECTIFIER

A novel three-phase PFC rectifier solution combining buck dc-dc converters and an active 3rd harmonic injection rectifier circuit, named here as the SWISS Rectifier, is shown in **Fig. 5**. With this new topology and a relatively low complexity control stage, not only a controlled output voltage can be achieved, but also high power factor operation [11].

The new rectifier system allows the local average values of currents in the positive and negative active switches, $i_{T+}$ and $i_{T-}$, to be formed proportionally to the input voltages involved in the formation of the output voltage of the diode bridge. If the difference between $i_{T+}$ and $i_{T-}$ is fed back into the mains phase with the currently smallest absolute voltage value via a current injection network, formed by three four-quadrant switches commanded at twice the line frequency, a sinusoidal input current shape can be assured for all mains phases while the dc-dc converter guarantees the output voltage regulation.

The modulation of the current injection circuit is performed at low frequency following the rectifier input voltages $u_{C,a,b,c}$ in such a way that the active current injection occurs always into only one mains phase as presented in **Tab. I** [cf. **Fig. 12**]. Accordingly, in each one of the 30°-wide sectors of the mains period, four different conduction states can be defined by the switches $T_+$ and $T_-$ within a pulse period $T_P$, where the dc current $I_{DC}$, impressed by the dc inductors, is distributed to two of the input phases or is kept in a freewheeling state.

**Fig. 14(a)** presents the four conduction states of the SWISS Rectifier for the interval $\varphi_N \in [0, 30°]$. For the switching state $j = (\text{ON}, \text{ON})$, where $j = (T_+, T_-)$ indicates a combination of the switching functions of the two fast switches ($T_+$ and $T_-$) and ON means that the respective switch is turned on, while OFF indicates an off-state of the switch, the rectifier input currents are $i_{r,a} = I_{DC}$, $i_{r,b} = 0$, and $i_{r,c} = -I_{DC}$, therefore, the rectifier input current space vector for this switching state results in

$$\underline{i}_{r,(ON,ON)} = \frac{2}{\sqrt{3}} I_{DC} e^{j\pi/6}. \tag{11}$$

Analogously, the three remaining space vectors can be calculated as

$$\underline{i}_{r,(ON,OFF)} = \frac{2}{\sqrt{3}} I_{DC} e^{-j\pi/6}, \tag{12}$$

$$\underline{i}_{r,(OFF,ON)} = \frac{2}{\sqrt{3}} I_{DC} e^{j\pi/2}, \tag{13}$$

$$\underline{i}_{r,(OFF,OFF)} = 0. \tag{14}$$

With these four space vectors, a resulting input current space vector $\underline{i}^*_r$ can be formed [cf. **Fig. 14(b)**] so that it is in phase with the mains voltage vector $\underline{u}$ and has the required amplitude according to the actual power demand.

Proper selection of the sequences of the switching states allows control over the current ripples across the inductor $L$ and the phase injection current $i_y$. Accordingly, the converter can be modulated in order to minimize the current ripple of $i_y$, or that of the dc current $I_{DC}$.

For the first mains sector ($0° < \varphi_N < 30°$), the SWISS Rectifier can operate with minimal $i_y$ current ripple and consequently lower ripple values of the input capacitor voltages $u_{CF,a,b,c}$ if a vector modulation with the switching

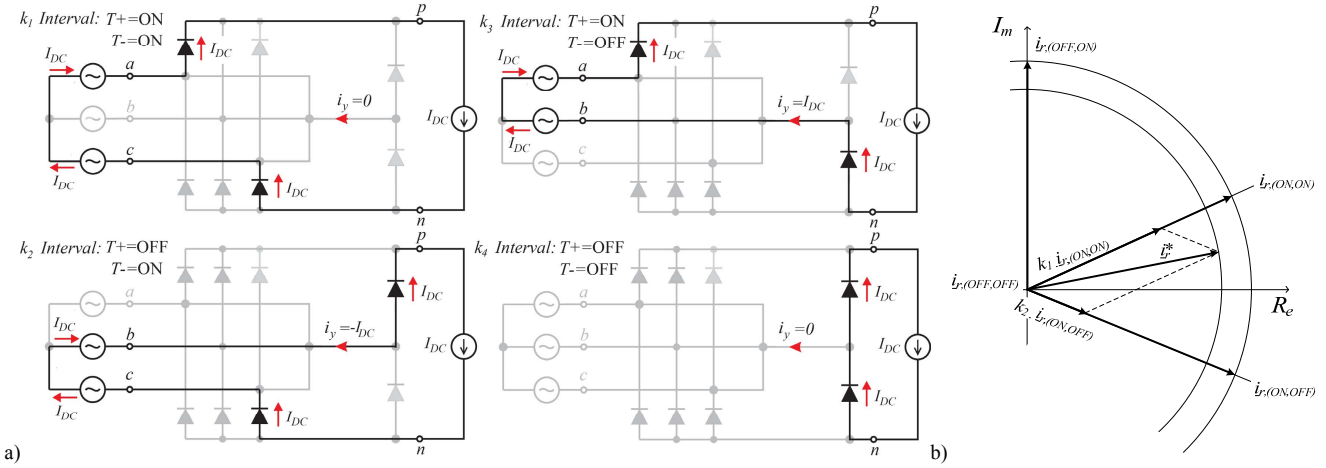


**Fig. 14: a)** Conduction states and **b)** input current space vector diagram of the SWISS Rectifier for $\varphi_N \in [0, 30°]$.

sequence (ON, ON) - (ON, OFF) - (OFF, OFF) - (ON, OFF) - (ON, ON), arranged symmetrically around the middle of the pulse interval, is applied. Therefore, the input phase currents are formed by the dc current $I_{DC}$ and the relative on-times of the current space vectors $k_i$

$$i_{r,a} = I_{DC}\left(k_1 + k_2\right);\; i_{r,b} = -I_{DC}k_2;\; i_{r,c} = -I_{DC}k_1. \quad (15)$$

The output voltage $u_{pn}$ is formed by the line-to-line voltages $u_{ab}$ and $u_{ac}$, rated by the relative on-time of the respective current vectors as

$$u_{pn} = k_1 u_{ac} + k_2 u_{ab}. \quad (16)$$

Note that the output voltage range is limited by the minimal value of the six-pulse diode bridge output voltage

$$u_{pn} < \sqrt{\frac{3}{2}} u_{N,l-l,rms}. \quad (17)$$

Finally, PFC operation in the first mains sector can be achieved with relative on-times $k_i$, dependent on the modulation index $M$, the instantaneous values of $u_{a,b,c}$, and the amplitude of the mains phase voltages $\hat{U}_N$ given by

$$M = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N}, \quad (18)$$

$$k_1 = -M\frac{u_c}{\hat{U}_N},\;\; k_2 = -M\frac{u_b}{\hat{U}_N},\;\text{and}\;\; k_4 = 1 - M\frac{u_a}{\hat{U}_N}. \quad (19)$$

Note that the switch duty cycles $\alpha_+$ and $\alpha_-$ for symmetric mains ($u_a + u_b + u_c = 0$) are defined as follows

$$\alpha_+ = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_a = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}\left(-u_b - u_c\right) = k_1 + k_2, \quad (20)$$

$$\alpha_- = -\frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_c = k_1. \quad (21)$$

Alternatively, for the first mains sector ($0° < \varphi_N < 30°$), the SWISS Rectifier can operate with minimized dc current ripple $\Delta i_{DC}$ ripple and consequently reduced ripple values of the output low-pass filtering if a vector modulation with the switching sequence (ON, OFF) - (ON, ON) -(OFF, ON) - (ON, ON) - (ON, OFF), arranged symmetrically around the middle of the pulse interval, is applied. The input phase currents formed by the dc current $I_{DC}$ and the relative on-times of the current space vectors $k_i$ result as

$$i_{r,a} = I_{DC}\left(k_1 + k_2\right);\; i_{r,b} = I_{DC}\left(k_3 - k_2\right);\; i_{r,c} = -I_{DC}\left(k_1 + k_3\right). \quad (22)$$

The output voltage $u_{pn}$ is formed by the line-to-line voltages $u_{ab}$, $u_{bc}$, and $u_{ac}$ rated by the relative on-time of the respective current vectors

$$u_{pn} = k_1 u_{ac} + k_2 u_{ab} + k_3 u_{bc}. \quad (23)$$

Finally, PFC operation in the first mains sector can be achieved with relative on-times $k_i$, dependent on the modulation index $M$, instantaneous values $u_{a,b,c}$ and the amplitude of the phase voltages $\hat{U}_N$ given by

$$k_2 = 1 + M\frac{u_c}{\hat{U}_N},\; k_3 = 1 - M\frac{u_a}{\hat{U}_N},\; k_1 = 1 - k_2 - k_3 = M\frac{u_a - u_c}{\hat{U}_N} - 1. \quad (24)$$

A possible implementation of a control circuit for the SWISS Rectifier and the main converter dimensioning equations, including the average and *rms* current values of the power semiconductors, are given in **Fig. 15**. This feedback PWM control structure comprises a superimposed output voltage controller $R(s)$ and a subordinate output current controller $G(s)$. A feed-forward loop adds the normalized modulation functions defined by the positive and negative diode bridge output voltage and the system output voltage reference value $u^*_{pn}$ to the dc current controllers in order to directly generate the input current forming voltage $u$.

In the proposed feedback control, by setting the PWM modulator for $T_+$ and $T_-$ to operate with in-phase carriers, the current ripple $\Delta i_y$ is reduced while the dc current ripple $\Delta i_{DC}$ is maximized. For interleaved operation of these carriers, the opposite will occur.

A complete description of the characteristics of the SWISS Rectifier, including the principles of operation, modulation strategy, control structure analysis, EMI modelling and dimensioning equations, is given in [12].

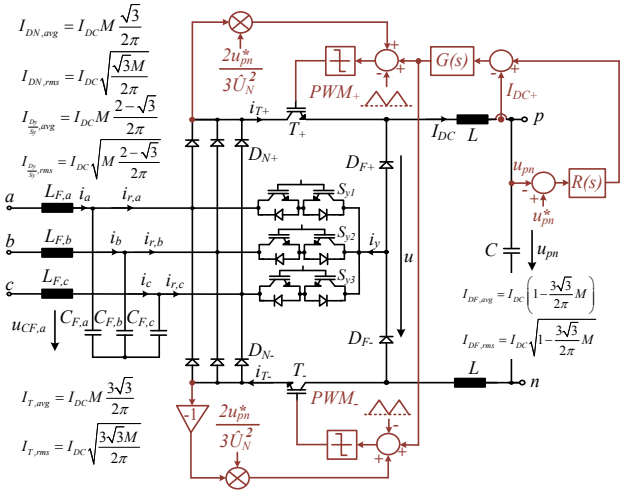


**Fig. 15:** Control structure and semiconductors current stresses for the SWISS Rectifier (buck-type PFC rectifier).

## V. COMPARATIVE EVALUATION

In order to evaluate and compare the new three-phase high-power-factor mains interface concepts for EV charging applications discussed in this paper, several normalized performance indices are defined. The main comparison features are: the power factor $\lambda$, the total current harmonic distortion $THD_I$, the relative total switching losses $\tau_S$ for transistors and diodes ($\delta_S$), the relative total conduction losses $\tau_C$ for transistors and diodes ($\delta_C$), the magnetic rated power $P_L$ (current ripple $\Delta i_{L,pp,max}$ is limited to 25% of $I_{DC}$), and the capacitors current stress $I_{C,rms}$. For any system, these characteristics can give information about size/volume, cost of the components, and the ability to meet power quality standards. Based on these performance metrics, a comparison of the proposed systems is performed graphically, as illustrated in **Fig. 16**. An advantageous system would preferably cover a small area in the graphical representation.

The comparison results for the 12 kW/3x400 V/48 kHz two-stage systems, described in Section II and III employing in total six interleaved buck-type dc-dc converters, are depicted in **Fig. 16(a)**. The requirement for small dc-link capacitors and the fact that only a single inductor is necessary

to shape the line currents make the active-filter-type 3rd harmonic injection converter advantageous in terms of size, weight and cost of hardware over the solution employing a dedicated APF. The possibility of using film dc-bus capacitors over electrolytic capacitors is beneficial for the system reliability. Nevertheless, this system allows a sinusoidal regulation of the mains currents only in the case that the back-end converter is demanding constant power and no smoothing capacitor (of higher capacitance) is connected to the dc-bus. Load variations are thus passed on directly to the mains. Additionally, the absence of energy storage at the input of the dc-dc converter makes it difficult to supply power to the battery during short input voltage interruption.

Advantageously, the EV system employing an APF can fully benefit from the high reliability of the line-commuted rectifier, as in case of an APF failure the EV charger could remain in operation, but without PFC capability.

The comparison results for the 12 kW / 3x400 V / 36 kHz SWISS Rectifier and active-filter-type 3rd harmonic current injection rectifier with a single dc-dc buck converter connected in series are compiled in **Fig. 16(b)**. The main advantages of the active-filter-type 3rd harmonic current injection rectifier with a single dc-dc buck converter over the SWISS Rectifier is that only one transistor is lying in the main current path, i.e. in particular at high output voltages with a relatively short freewheeling interval, low conduction losses occur. In addition, the negative output voltage terminal is always connected to the mains via a diode of the lower half bridge of the diode rectifier. Therefore, no output CM voltage with switching frequency is generated. The main advantages of the SWISS Rectifier are the better line power quality and that the system can basically be controlled like a dc-dc converter. Accordingly, basic knowledge of the function of a passive diode rectifier at the input stage of the system is sufficient to implement a three-phase PFC rectifier with sinusoidal input current and controlled output voltage.

Finally, among the studied systems the SWISS Rectifier is the solution combining the best features for an EV charger, and provides a good compromise between reliability, simplicity, and relatively low cost, volume, and weight.

## VI. CONCLUSION

This paper proposes three-phase high power factor mains interfaces appropriate not only for high power EV battery charging systems, but also for power supplies for telecommunication, future more electric aircraft, variable speed ac drivers, and high power lighting systems.

The requirements for power converters in EV battery charging applications have been described. Furthermore, the characteristics of the presented EV systems, including the principles of operation, modulation strategy, suitable control structures, and dimensioning equations, have been summarized. Finally, a comparison of the studied converters rated for an output power of 12 kW has been shown, which identify the SWISS Rectifier and the active-filter-type 3rd harmonic injection rectifier with series connected buck converters as most advantageous solutions.

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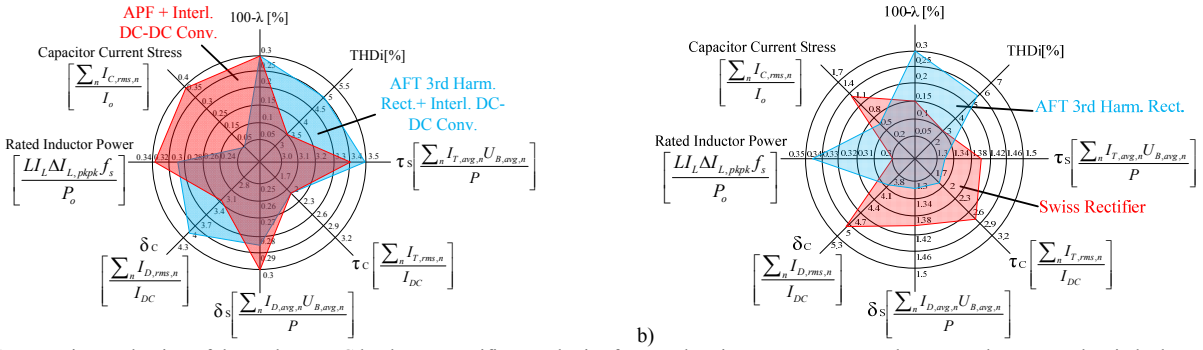


**Fig. 16:** Comparative evaluation of three-phase PFC buck-type rectifier topologies for EV charging systems. $I_{T,avg}$ and $I_{D,avg}$ are the averaged switched current and $U_{B,avg}$ is the averaged switched voltage across the power semiconductors. $I_{T,rms}$, $I_{D,rms}$, $I_L$ and $I_{C,rms}$ are the *rms* current value of the specific component.