Extending Winding Capacitance Cancellation to Three-Phase EMC Input Filter Networks

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***Abstract*—Techniques have been presented in the literature for canceling stray capacitances for inductors in single-phase power filters. With the same aim, the flexibility of three-phase networks is here explored. A thorough theoretical analysis is presented, where pros and cons of parasitic cancellation networks are highlighted and improvements are proposed. A systematic mathematical procedure to evaluate impedances for different noise modes in three-phase circuits is presented. The influence of parasitic effects is accessed and asymmetrical capacitance cancellation is proposed, facilitating applications in switched power circuits. Experimental results are presented, which prove the feasibility of the presented techniques.**

Keywords-parasitic capacittance cancellation; three-phase power line filters; three-phase networks.

I. INTRODUCTION

Moved by cost reduction demands, Power Electronics as a research field has been having its focus in the miniaturization of power converters. This means that the same functionality must be guaranteed for electronic systems built within ever smaller spaces, thus requesting electronic components with very much different characteristics to cohabit in tightly confined areas [1]. The situation gets more complex because switching and digital clock frequencies are steadily increasing, thus higher frequency components are prone to be observed in the electromagnetic field spectra generated in the power systems. The results achieved in the last decades have pushed the limits of available circuit topologies, materials, components, modulation schemes and control strategies [2]. These results have also compelled design engineers to achieve a better understanding around the measures to be taken in order to assure the electromagnetic compatibility (EMC) of such a system within its electrical environment and inside the system itself (self-compatibility) [3]. As power electronics systems are know to be very efficient conducted emissions (CE) sources, efforts in research are being done in reducing these emissions in their source, but also in the line filters, the interfaces between power grid and converters [3]–[5]. For high performance power converter systems, these power filters are mostly low-pass circuits designed based on inductors and capacitors along with resistors providing passive damping [5]–[6]. Although active filters circuits have been lately also researched [7]–[10] and some practical applications have been reported [10], most of power filters is still based on passive elements, where inductors play a major role in increasing series impedance for both, differential (DM) and common mode (CM) emissions.

Inductors are heavy/bulky components, but are especially useful in reducing CM currents once the utilization of capacitors between lines and protective earth (PE) is limited due to earth leakage current limitations given in electric equipment safety standards (e.g. EN 60950 series). Inductors to be used in filters have been studied and theoretical models have been proposed [11]–[14] and what all models have in common is the connection of a capacitor in parallel with the inductor, thus providing capacitive impedance beyond the so-called self-resonance frequency (cf. **Fig.1**). The observed capacitance is a consequence of the physical disposition of the wires/turns (conductors) and isolation paint/layers (dielectric). This capacitive behavior is a highly undesirable effect since it might greatly reduce the attenuation provided by a filter at high frequencies. This effect gets worst if multiple winding layers are used in the construction of the inductor [4], [12] and as a result inductor designs shall be limited to one or at most two layers, thus increasing the required total core material volume. If a planar design is used the capacitive effect is even more pronounced due to the wider conductive area in contrast with thinner dielectric distances between layers [15].

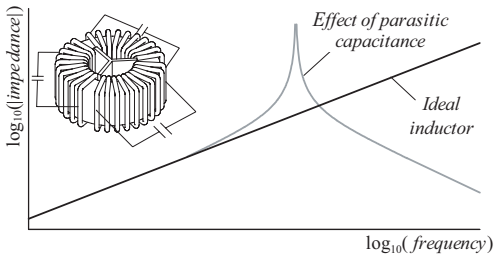

Fig.1: Three-phase CM inductor illustration with an impedance curve showing the parallel capacitance effect on the impedance magnitude for high frequencies.

To overcome the challenge imposed by parasitic elements in the construction of inductors, thorough research is being done to improve magnetic materials [2] and, lately, in the research of methods to reduce parasitic elements through the use of different circuit topologies in the filtering networks [15]–[18]. A term called capacitance cancellation has been created to address these techniques, which have the practical outcome of eliminating the parasitic capacitance effects observed from a perspective of CM, DM or both in a filter for a feasible frequency range. Since CE are, in general, regulated up to 30 MHz, both in Europe (EN) and USA (FCC), this is the upper bound frequency, for which a designed inductor should behave as ideal as possible.

This work aims on analyzing the possibility of application of some capacitance cancellation networks to three-phase power line filters, since previous literature on this subject is limited to single phase topologies, but the utility and costs of three-phase power converters are prone to justify the utilization of extra components in the filters. Due to the lack of existing tools for the analysis of three-phase networks, a procedure is presented (cf. Section II), which uses the parameters of the networks admittance matrices (Y) and evaluates relevant impedances for CM and DM. The derived equations are also used in the search for suitable capacitance cancellation networks, where some of the presented results can be extended to single-phase

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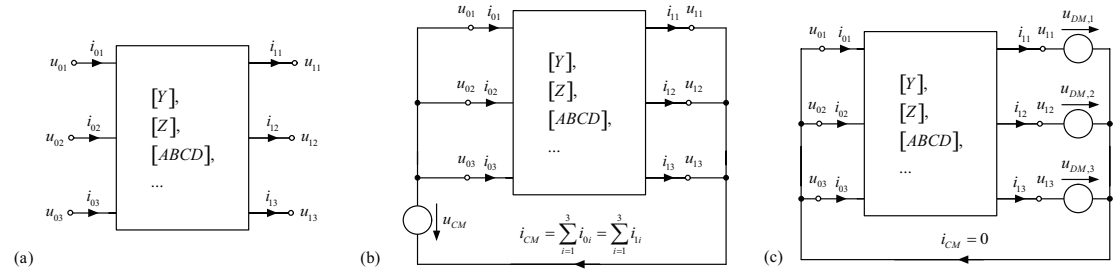

Fig.2: Network configurations used in the derivation of the relevant matrices: (a) General three-phase network; (b) Configuration used for the definition of CM impedance, and; (c) Used for the DM impedance definition.

networks. Cancellation networks are proposed (cf. Section III) for three-phase inductive networks, where the impact for CM and DM, of the introduced components, is evaluated and the flexibility provided by three-phase networks is exploited. A basic study proposing the possibility of asymmetrical capacitance cancellation is presented in Section IV. Extra measures are taken to improve the performance of such networks in the higher frequencies of the spectrum. These are based on the study of the influence of other parasitic effects, such as non-ideal coupling factors and winding resistances, which is done theoretically (cf. Section V) and experimentally as shown in the experimental results presented in Section VI.

II. The Use of Admittance Matrices to Analyze Three-Phase Networks for EMC

A three-phase network consisting of linear and time invariant elements, as displayed in **Fig.2(a)**, is completely defined by one of its characteristic impedances (*Y*, *Z*, *T*, *h*, *s*, etc). The admittance matrix *Y* is especially useful if networks are to be connected in parallel, because the resulting matrix (Y_{res}) of the parallel connection of two networks defined by Y_1 and Y_2 is the direct sum of them, $Y_{res}=Y_1+Y_2$. Some of the capacitance cancellation networks can be placed directly in parallel with the network of inductors and for this reason the admittance matrix is thought of being well suited for the present analysis, even though any other form could be used.

The objective of this analysis is to search for equations to evaluate impedances, which are relevant for the EMC assessment in three-phase circuit networks. That is here achieved by deriving equivalent impedances from two perspectives, CM and DM, which are based on the admittance matrix of the three-phase network of interest.

A. Derivation of an Ideal CM Impedance

The circuit configuration presented in Fig.2(b) is used to define the total CM impedance (Z_{CM}) presented by the network for an ideal case, where the impedances outside the network are balanced with respect to the reference ground. From the inspection of the circuit,

$$\begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \\ i_{11} \\ i_{12} \\ i_{13} \end{bmatrix} = \begin{bmatrix} [Y_{11}] & [Y_{12}] \\ [Y_{21}] & [Y_{22}] \end{bmatrix} \cdot \begin{bmatrix} u_{CM} \\ u_{CM} \\ u_{CM} \\ 0 \\ 0 \\ 0 \end{bmatrix} \Rightarrow \begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \end{bmatrix} = [Y_{11}] \cdot \begin{bmatrix} u_{CM} \\ u_{CM} \\ u_{CM} \end{bmatrix}, \tag{1}$$

where, Y_{11}, Y_{12}, Y_{21} and Y_{22} are the square sub-matrices of *Y*. From equation (1) the individual currents are defined by

$$i_{0i} = u_{CM} \cdot \sum_{m=1}^{3} y_{m,i} \ . \tag{2}$$

If the network is symmetric, considering the polarities presented in Fig.2(b), then $Y_{12} = -Y_{21}$ and $Y_{11} = -Y_{22}$ and the equivalent CM impedance Z_{CM} presented by the network can be evaluated through the sum of all elements of the sub-matrix Y_{11},

$$Z_{CM} = \frac{u_{CM}}{i_{CM}} = \frac{u_{CM}}{\sum_{i=1}^{3} i_{0i}} = \frac{u_{CM}}{\sum_{i=1}^{3} \left(u_{CM} \cdot \sum_{m=1}^{3} y_{m,i} \right)} = \frac{1}{\sum_{i=1}^{3} \left(\sum_{m=1}^{3} y_{m,i} \right)} . \tag{3}$$

B. Derivation of the Ideal Series DM Impedances

Again, for the derivation of ideal DM impedances for the three-phase network, the impedances outside the network are considered balanced. The circuit for this derivation is shown in Fig.2(c), thus

$$\begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \\ i_{11} \\ i_{12} \\ i_{13} \end{bmatrix} = \begin{bmatrix} [Y_{11}] & [Y_{12}] \\ [Y_{21}] & [Y_{22}] \end{bmatrix} \cdot \begin{bmatrix} 0 \\ 0 \\ 0 \\ u_{DM,1} \\ u_{DM,2} \\ u_{DM,3} \end{bmatrix} \Rightarrow \begin{bmatrix} i_{01} \\ i_{02} \\ i_{03} \end{bmatrix} = [Y_{12}] \cdot \begin{bmatrix} u_{DM,1} \\ u_{DM,2} \\ u_{DM,3} \end{bmatrix} . \tag{4}$$

From the definition of differential mode voltages, their sum must equal zero,

$$\sum_{i=1}^{3} u_{DM,i} = 0 \ . \tag{5}$$

There can be infinity possibilities for this sum to hold true. A general case is here assumed, where

$$\begin{cases} u_{DM,1} = U_1 \cdot e^{j\alpha} \\ u_{DM,2} = U_2 \cdot e^{j\beta} \\ u_{DM,3} = -\left(U_1 \cdot e^{j\alpha} + U_2 \cdot e^{j\beta} \right) \end{cases} . \tag{6}$$

Three DM impedances $Z_{DM,i}$ are defined,

$$Z_{DM,i} = \frac{u_{DM,i}}{i_{0i}} \text{ , where } i = 1..3 \ . \tag{7}$$

The general solution for the three DM impedances is

$$Z_{DM,i} = \frac{u_{DM,i}}{\sum_{m=4}^{6} \left(y_{i,m} \cdot u_{DM,m-3} \right)} . \tag{8}$$

If the network under consideration is symmetric, it follows that $y_{1,4}=y_{2,5}=y_{3,6}$ and $y_{1,5}=y_{1,6}=y_{2,4}=y_{2,6}=y_{3,4}=y_{3,5}$. Therefore, the DM impedances are:

$$Z_{DM,1} = Z_{DM,2} = Z_{DM,3} = \frac{1}{y_{1,4} - y_{1,5}} = Z_{DM} \ . \tag{9}$$

III. Capacitance Cancellation for Three-Phase Inductive Networks

The results and analyses presented on this section are based on some simplifications in the models for the inductors, namely: (*i*) a first order approximation is adopted that is valid in most situations up to 30 MHz; (*ii*) the parallel resistance is omitted since it pays neglectable role in the capacitance cancellation; (*iii*) the influence of the series

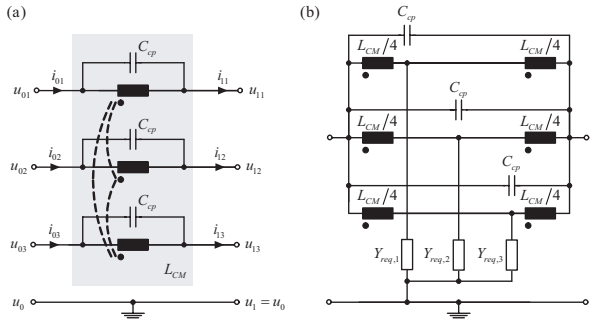

Fig.3: Three-phase CM inductor networks: (a) model of a three-phase CM inductor, and; (b) equivalent CM network aiming for finding impedances $Y_{req,i}$ (i= 1…3) that effectively cancel the effects of the parallel capacitors C_{cp}.

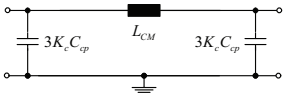

Fig.4: Desired final equivalent network for CM.

resistances is here neglected; (*iv*) a perfect coupling factor k = 1 is assumed; (*v*) the lead inductances are disregarded because they can be seen in series with the remaining networks, thus their connection can be done in a second step, and; (*vi*) the networks have balanced impedances. The influence of the series resistance and the reduction of the coupling factors are studied in Section V. These simplifications are important in reducing the complexity of the equations and providing useful insight about the involved phenomena. The principles presented in [17] are here used and extended to three-phase networks.

A. Capacitance Cancellation for Three-phase CM Inductors

A three-phase CM inductor can be modeled as the six-port network shown in **Fig.3**(a) and for a CM analysis the three inputs can be shortened as well as the output ports, thus the six-port device is simplified to a two-port one (cf. Fig.3(b)). The final aim for the capacitance cancellation is that the parallel capacitors C_{cp} disappear and an equivalent network as in **Fig.4** results.

The admittance matrix Y_{des} of the circuit of Fig.4 is

$$Y_{des} = \begin{bmatrix} \frac{3sK_cC_{cp}}{2} + \frac{1}{sL_{CM}} & -\frac{1}{sL_{CM}} \\ -\frac{1}{sL_{CM}} & \frac{3sK_cC_{cp}}{2} + \frac{1}{sL_{CM}} \end{bmatrix}. \tag{10}$$

The remaining analysis considers no magnetic coupling among the different windings. This assumption does not strongly influence the results, since the inter-winding magnetic coupling is reduced for high frequencies due to lowering permeability of any employed core material. This consideration is on the safe side since the higher the coupling amongst the different windings the better for the capacitance cancellation. An ideal magnetic coupling k_{cm} = 1 between the halves of the windings is considered in order to simplify the equations, but the influence of a non-ideal coupling is studied in Section V.

For a symmetric cancellation network, $Y_{req,1} = Y_{req,2} = Y_{req,3} = Y_{req}$ and the admittance matrix Y_{canc} for the circuit of Fig.3(b) is defined by:

$$Y_{canc} = \begin{bmatrix} y_\alpha & -y_\beta \\ -y_\beta & y_\alpha \end{bmatrix}, \tag{11}$$

where $$y_\alpha = \frac{9s^3C_{cp}L_{CM}{}^2Y_{req} + 12s^2C_{cp}L_{CM} + 6sL_{CM}Y_{req} + 4}{sL\left(4 + 3sL_{CM}Y_{req}\right)} \tag{12}$$

and $$y_\beta = \frac{9s^3C_{cp}L_{CM}{}^2Y_{req} + 12s^2C_{cp}L_{CM} + 4}{sL\left(4 + 3sL_{CM}Y_{req}\right)}. \tag{13}$$

The capacitance cancellation is achieved when $Y_{canc} = Y_{des}$, from where:

$$\begin{cases} Y_{des\,1,1} = Y_{canc\,1,1} = y_\alpha \\ Y_{des\,2,1} = Y_{canc\,2,1} = -y_\beta \end{cases}. \tag{14}$$

Solving (14) for Y_{req} leads to

$$\begin{cases} K_c = 4 \\ \frac{1}{Y_{req}} = \frac{1}{4sC_{cp}} - \frac{3sL_{CM}}{4} \end{cases}. \tag{15}$$

This shows that the cancellation network can be achieved with the series connection of a negative inductance with a value of ¾L_{CM} with a capacitor of 4C_{cp}. The final circuit is illustrated in **Fig.5**, where $C_{cc,i}$ = 4C_{cp} and k_{CM} = 1. This is a very useful result, since it shows that the inclusion of only three capacitors (of usually small value) is able to cancel the negative effect of the parallel capacitances.

For the case that one of the admittances $Y_{req,i}$ is set to zero, for instance only $Y_{req,3}$ = 0, then two capacitors of 6C_{cp} suffice for canceling C_{cp} as shown in (16).

$$\begin{cases} K_c = 4 \\ \frac{1}{Y_{req,1}} = \frac{1}{Y_{req,2}} = \frac{1}{6sC_{cp}} - \frac{3sL_{CM}}{4} \end{cases}. \tag{16}$$

If two admittances are set to zero, for instance only $Y_{req,1} \neq 0$, then a single capacitors of 12C_{cp} suffices:

$$\begin{cases} K_c = 4 \\ \frac{1}{Y_{req,1}} = \frac{1}{12sC_{cp}} - \frac{3sL_{CM}}{4} \end{cases}. \tag{17}$$

This shows that for the CM capacitance cancellation of an ideal three-winding CM inductor it is not required that the network cancellation is done symmetrically, thus a single capacitor connected to the center of one winding (cf. **Fig.6**(a)) might be enough. This effect can also be explained by inspecting Fig.6(b), where, for CM currents, the voltage is the same in all three windings, and if a perfect coupling is assumed, the voltage at the center point of any winding should be the exactly the same, therefore the connection of capacitors between any of these points and the electric ground (PE) shall provide the same effect as long as the coupling factors are high and the external impedances (connected in series with the inductors) are approximately symmetrical and balanced. This might prove useful for manufacturing reasons, since only one center point must be accessed, but attention must be paid if mixed mode is pronounced in the circuit

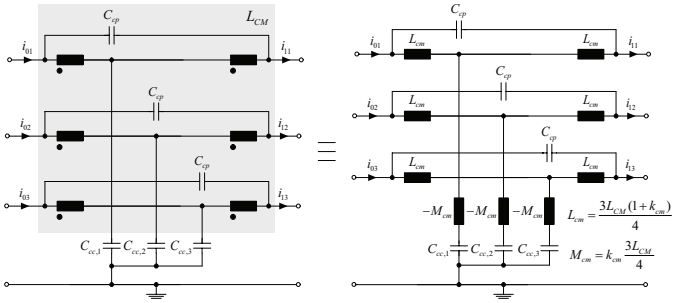

Fig.5: Networks that achieve the capacitance cancellation for a three-phase CM inductor (for the equivalence of these networks refer to Appendix I).

and if the coupling among the windings is low.

B. Capacitance Cancellation for Three-phase DM Inductors

A network composed of three DM inductors is an important building block for three-phase power filters and, unless some special winding technique is used, three non-coupled inductors are applied. The simplified model for the six-port network is shown in **Fig.7**. Two ways of achieving capacitance cancellation for this network are presented in the following.

1) First Approach – No magnetic coupling required

As the capacitors and inductors are connected in parallel in the model of Fig.7, the inductances can be removed (the final network is the sum of the admittances of both circuits) and the remaining network is built with the connection of capacitors C_{dp}, as displayed in **Fig.8**(a). The admittance matrix of this network Y_{con} is

$$Y_{con}=\begin{bmatrix} sC_{dp} & 0 & 0 & -sC_{dp} & 0 & 0 \\ 0 & sC_{dp} & 0 & 0 & -sC_{dp} & 0 \\ 0 & 0 & sC_{dp} & 0 & 0 & -sC_{dp} \\ sC_{dp} & 0 & 0 & -sC_{dp} & 0 & 0 \\ 0 & sC_{dp} & 0 & 0 & -sC_{dp} & 0 \\ 0 & 0 & sC_{dp} & 0 & 0 & -sC_{dp} \end{bmatrix}. \tag{18}$$

If the network of Fig.8(b) is used for capacitance cancellation, it is left to know the value of capacitors C_{dc}. The admittance matrix Y_X of this network is

$$Y_X=\begin{bmatrix} 2sC_{dc} & 0 & 0 & 0 & -sC_{dc} & -sC_{dc} \\ 0 & 2sC_{dc} & 0 & -sC_{dc} & 0 & -sC_{dc} \\ 0 & 0 & 2sC_{dc} & -sC_{dc} & -sC_{dc} & 0 \\ 0 & sC_{dc} & sC_{dc} & -2sC_{dc} & 0 & 0 \\ sC_{dc} & 0 & sC_{dc} & 0 & -2sC_{dc} & 0 \\ sC_{dc} & sC_{dc} & 0 & 0 & 0 & -2sC_{dc} \end{bmatrix}. \tag{19}$$

And the final admittance matrix $Y_{DM,final}$ is the sum of both $Y_{DM,final}=Y_{con}+Y_X$. As the networks are symmetric, the DM impedances $Z_{DM,i}$ can be evaluated from (9) and it follows that

$$Z_{DM,i}=\frac{1}{y_{1,4}-y_{1,6}}=\frac{1}{s\left(-C_{dp}+C_{dc}\right)}, \text{ where } i=1..3. \tag{20}$$

The aim of the capacitance cancellation in this case is to achieve infinite DM impedance. This is fulfilled, by inspecting (20), if

$$C_{dp}=C_{dc}\Rightarrow Z_{DM,final,i}\to\infty. \tag{21}$$

An important parameter for the evaluation of the final network is the impedance observed from CM, since the DM inductors have an impact on CM currents as well. The serial CM impedance can be calculated with (3) leading to

$$Z_{CM,final}=\frac{1}{\sum_{j,k=1}^{3}y_{k,j}}=\frac{1}{3\left(2sC_{dc}+sC_{dp}\right)}=\frac{1}{9sC_{dp}}. \tag{22}$$

From (21) and (22) it is seen that, with the inclusion of the six capacitors C_{dc}, the parallel capacitance C_{dp} is cancelled for DM currents, whereas for CM the final capacitance is increased three times in value. This is clear from the inspection of **Fig.9**, where the CM analysis can be done by connecting input and output ports respectively together and the equivalent capacitance is the sum of all capacitors.

2) Second Approach – Relying on magnetic couplings

If the inductors L_{DM} of **Fig.10** are split in two, the same principle used in the CM cancellation section can be used (cf. Fig.5) and the admittances $Y_{req,i}$ shall be derived.

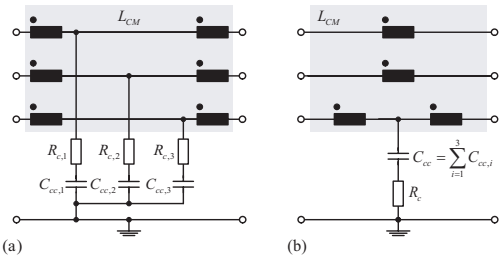

Fig.6: Networks that provide parasitic capacitance cancellation in a three-phase CM inductor: (a) symmetrical network, where $C_{cc,i}=4C_{cp}$, and; (b) single capacitor network.

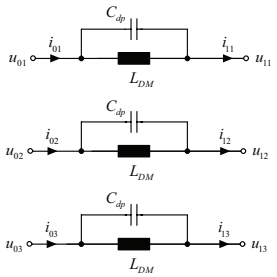

Fig.7: Model applied for the analysis of three DM inductors.

The admittance matrix of the network of Fig.10 is given by,

$$Y_{d,canc}=\begin{bmatrix} y_A & -y_B & -y_B & -y_A & -y_B & -y_B \\ -y_B & y_A & -y_B & -y_B & -y_A & -y_B \\ -y_B & -y_B & y_A & -y_B & -y_B & -y_A \\ y_A & y_B & y_B & -y_A & y_B & y_B \\ y_B & y_A & y_B & y_B & -y_A & y_B \\ y_B & y_B & y_A & y_B & y_B & -y_A \end{bmatrix}, \tag{23}$$

where:

$$\begin{cases} y_A=\dfrac{3s^3C_{dp}L_{DM}{}^2Y_{req,d}+12s^2C_{dp}L_{DM}+5sL_{DM}Y_{req,d}+12}{3sL_{DM}\left(4+sL_{DM}Y_{req,d}\right)} \\ y_B=\dfrac{Y_{req,d}}{3\left(4+sL_{DM}Y_{req,d}\right)} \end{cases}, \tag{24}$$

The only element that is desirable for the DM currents is the inductance L_{DM}, therefore the desired DM impedance $Z_{DM,canc,i}$, evaluated through (9) and (23), is

$$Z_{DM,canc,j}=\frac{1}{y_{1,4}-y_{1,6}}=\frac{1}{-y_A-y_B}=-\frac{1}{sL_{DM}}, \tag{25}$$

Solving the system of equations formed by (23), (24) and (25) it follows that

$$Z_{DM,canc,i}\to-\frac{1}{sL_{DM}}\Rightarrow Y_{req,i}=\frac{1}{\dfrac{1}{4sC_p}-\dfrac{sL_{DM}}{4}}. \tag{26}$$

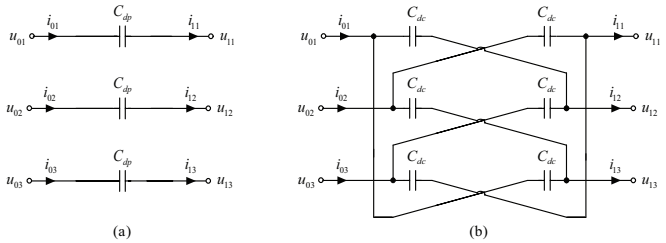

Fig.8: Capacitive networks: (a) parallel capacitances, and; (b) DM capacitive cancellation network.

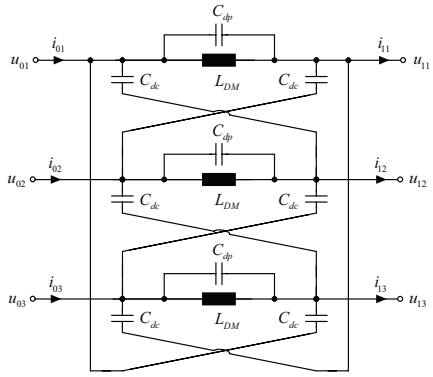

Fig.9: Final network for DM capacitance cancellation. The connection of capacitors C_{dc} effectively cancels the effect of C_{dp} for DM currents, not relying on magnetic couplings. For CM currents the final capacitance is increased, being, therefore, a drawback of this type of network.

The idea of using a network similar to the one used for the CM capacitance cancellation also works here. That means that if a symmetrical cancellation network (with three capacitors) is used for the CM inductor, then the parallel capacitance is cancelled for both modes. The final network is presented in **Fig.11**, where the capacitors $C_{dy,i}$ are added for canceling the effects of C_{dp}.

What is left is the calculation of the impedance observed by CM currents. This is calculated using (23) and (24) into (3), leading to

$$Z_{CM,canc} = \frac{1}{\sum_{i,k=1}^{3} y_{k,i}} = \frac{sL_{DM}}{\left(s^2 C_{dp} L_{DM} + 1\right)}, \tag{27}$$

which is the same impedance seen without the inclusion of the capacitance cancellation network, therefore this approach does not decrease the final CM impedance.

IV. Short Discussion on Asymmetrical Cancellation

The networks presented in the previous section and in the literature [15]–[17] have as a characteristic that the final equivalent circuit is symmetric, since the connection of the canceling networks is symmetric as in **Fig.12**(a). For the case where the inductor is used directly at the input of a switching cell (cf. Fig.12(b)), the switches S_1 and S_2 will present switching losses which are approximately proportional to the parallel capacitance C_p, thus this capacitance is completely unwanted. If the symmetrical capacitance cancellation networks are used, the effective parallel capacitance is increased. In fact it is doubled for the circuit in Fig.12(a), what means that the switching losses due to C_p would be twice as much. This would require special attention of design engineers in the use of the cancellation techniques and leads to the question: is it possible to implement a cancellation network (asymmetric), which does not increase the capacitance to be switched?

To start with, the networks presented in **Fig.13** are used, where the parameters L_1, L_2 and K are left undefined and a mutual inductance with unitary magnetic coupling factor is considered $M=(L_1 L_2)^{1/2}$. The admittance matrices of the networks are used to derive the values.

The admittance matrix for the circuit in Fig.13(a) Y_C is

$$Y_C = \begin{bmatrix} y_{\alpha,C} & -y_{\beta,C} \\ -y_{\chi,C} & y_{\delta,C} \end{bmatrix}, \tag{28}$$

where $$y_{\alpha,C} = \frac{\left(L_1 + L_2 + 2M\right) C_p s^2 + Y_{req} L_2 s + 1}{s\left(L_1 + L_2 + 2M\right)}, \tag{29}$$

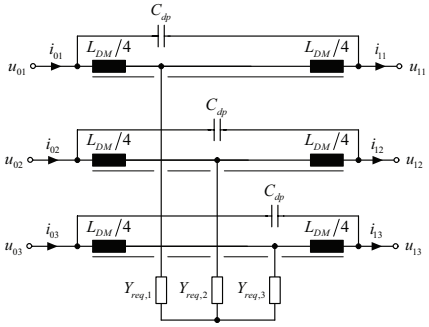

Fig.10: Network used to find a suitable circuit to implement capacitance cancellation for DM inductors.

$$y_{\beta,C} = y_{\chi,C} = \frac{\left(L_1 + L_2 + 2M\right) C_p s^2 + Y_{req} M s + 1}{s\left(L_1 + L_2 + 2M\right)} \tag{30}$$

and $$y_{\delta,C} = \frac{\left(L_1 + L_2 + 2M\right) C_p s^2 + Y_{req} L_1 s + 1}{s\left(L_1 + L_2 + 2M\right)}. \tag{31}$$

The admittance matrix for the circuit in Fig.13(b) Y_D is

$$Y_D = \begin{bmatrix} y_{\alpha,D} & -y_{\beta,D} \\ -y_{\beta,D} & y_{\alpha,D} \end{bmatrix}, \tag{32}$$

where $$y_{\alpha,D} = \frac{\left(L_1 + L_2 + 2M\right) K_1 C_p s}{L_1 + L_2 + 2M} + \frac{1}{s\left(L_1 + L_2 + 2M\right)}, \tag{33}$$

$$y_{\beta,D} = y_{\chi,D} = \frac{-1}{s\left(L_1 + L_2 + 2M\right)} \tag{34}$$

and $$y_{\delta,D} = \frac{\left(L_1 + L_2 + 2M\right) K_2 C_p s}{L_1 + L_2 + 2M} + \frac{1}{s\left(L_1 + L_2 + 2M\right)}. \tag{35}$$

The capacitance cancellation is achieved when $Y_C = Y_D$, resulting in a four linearly independent equations. Solving this system leads to

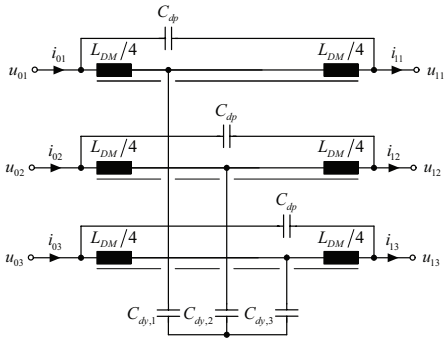

Fig.11: Network to achieve capacitance cancellation for DM inductors used in three-phase filters based on the magnetic coupling among two halves of each of inductors.

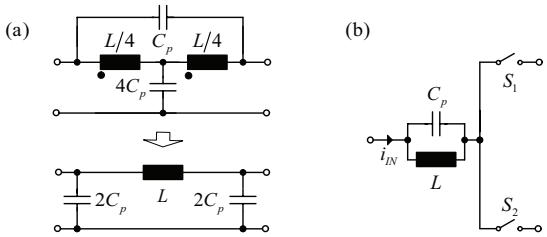

Fig.12: (a) Basic principle for symmetric capacitance cancellation and its equivalent circuit. (b) Inductor applied at the input of a switching cell, where its parasitic parallel capacitance increases switching losses in the cell.

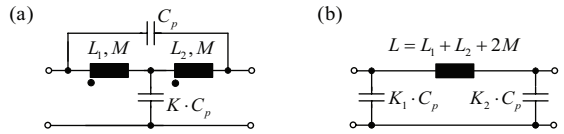

Fig.13: Networks used to analyze the possibility of asymmetric parasitic capacitance cancellation: (a) proposed cancellation network, and; (b) desired equivalent circuit.

$$\begin{cases} K = \dfrac{K_2^{\,2}}{K_2 - 1} \\ K_1 = \dfrac{K_2}{K_2 - 1} \end{cases} \text{ and,} \tag{36}$$

$$\begin{cases} L_1 = (K_2 - 1)M \\ L_2 = \dfrac{1}{K_2 - 1}M \end{cases} . \tag{37}$$

After a value is chosen for K_2 the other parameters follow, but there is a theoretical lower boundary for K_2, given by $K_2 \geq 1$. This limit, in practice, means that the original parallel capacitance C_p can not be downsized from a perspective of switching losses. The total amount of capacitance KC_p used in the circuit has its minimum at $K_2 = 2$ (cf. **Fig.14**), which is the case of symmetric cancellation. This means that for an asymmetric cancellation more capacitance must be used, but it brings the advantage that the input capacitance K_1C_p is large, thus providing more effective filtering.

The implementation of such a technique is more involved, since the splitting of the inductor is not done at its center point, but depends strongly in the chosen ratio K_2. **Fig.15** illustrates how the inductance must be divided in order to achieve capacitance cancellation, where it becomes clear that if a small K_2 is desirable, the inductor shall be divided in uneven parts, which might be difficult to control.

V. Study on the Influence of Parasitic Elements

The previous sections have assumed close to ideal equivalent circuits, but as the high frequency behavior of the components is paramount for EMC, the influence of the main parasitic effects must be considered. For that, the circuit of **Fig.16** is used, where the stray resistances of the windings R_σ, a non-ideal magnetic coupling k_{cm} and the stray inductance L_σ are considered.

The calculation of the CM impedance is done with equation (3) and of the DM impedance with equation (9), both applied to the admittance matrix of the network of Fig.16, which is not displayed due to space constraints. The surfaces plotted in **Fig.17** provide insight into the influence of the non-ideal parameters. Fig.17(a) shows the CM impedance as a function of frequency and the coupling factor k_{cm}, from where it is seen that the resonance frequency gets lower for low values of coupling and is infinite for unitary coupling. The influence of the series resistances R_σ has the same type of effect as lowering the magnetic coupling (cf. Fig.17(b)).

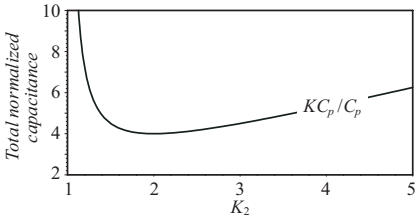

Fig.14: Normalized total capacitance required for the cancellation of C_p as a function of K_2.

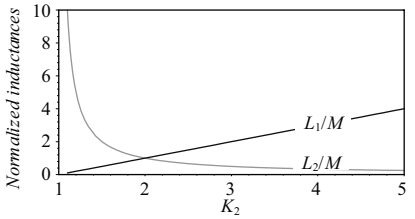

Fig.15: Normalized inductances required for the cancellation of C_p as a function of K_2.

The use of the capacitance cancellation network leads to the inclusion of L_σ, what creates resonances at frequencies higher than the self-resonance. It produces undesired resonances in both, CM and DM, impedances and if these resonances are under 30 MHz they might cause problems for conducted emissions, otherwise they affect radiated emissions. These resonances can be damped with the help of a damping resistance R_d as observed in Fig.17(c) and **Fig.18**.

A similar study can be performed for the DM capacitance

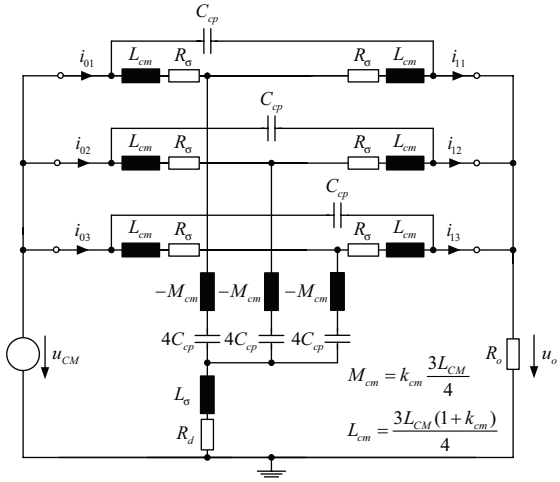

Fig.16: Circuit used for analyzing the influence of parasitic elements R_σ, L_σ and k_{cm} in the performance of the capacitance cancellation for a three-phase CM inductor. Damping resistors R_d are shown.

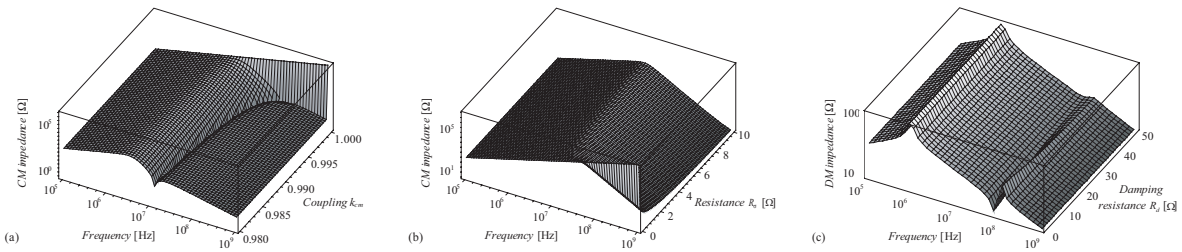

Fig.17: Influence of parasitic elements, where L_{CM}=500 µH and C_{cp}=10 pF; (a) CM impedance as a function of the coupling factor k_{cm} with R_σ=0 Ω and L_σ=0 H; (b) CM impedance as a function of the series resistance R_σ with k_{cm}=1 and L_σ=0 H, and; (c) DM impedance as a function of the damping resistance R_d with k_{cm}=1, R_σ=0 Ω and L_σ=100 nH.

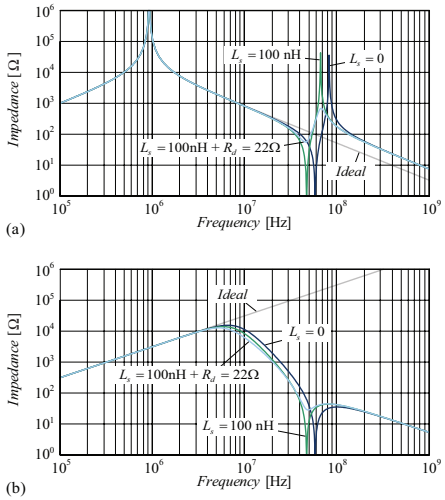

Fig.18: Influence of L_σ in the (a) DM and (b) CM impedances and the possibility of damping by inserting a resistor R_d in series.

cancellation techniques leading to similar results, but for the sake of brevity these are here omitted.

VI. Experimental Results

In order to verify the presented principles experiments are performed. A three-phase 6 kVA adjustable speed drive (ASD) prototype based on a highly compact indirect matrix converter (IMC) built with "state-of-the-art" reverse blocking IGBTs (RB-IGBT) [19] is employed as emissions source. An external filter board comprising DM and CM filters as shown in **Fig.19** is connected to the input of the converter. The filters are built in a way that the capacitors included for capacitance cancellation are easily removable, so that the effects of their inclusion are observed.

The first measurements were performed with an impedance analyzer in order to evaluate the total parallel capacitance for each of the inductors. The parallel capacitances were measured with the technique described in [20]. For the CM inductor L_{CM} the total measured parallel capacitance was 17.7 pF, while the capacitance for the DM inductors had an average of 52 pF within ±2 % margin.

A second set of experiments comprised measurements of insertion loss (cf. **Fig.20**) of the filter board with a two-port network analyzer. CM insertion loss measurements are performed with the first port connected between terminals *a*, *b* and *c* together and PE and the second port connected from *A*, *B* and *C* to PE. DM insertion loss is measured with the help of two insulation transformers (input and output) from terminals *a* and *b* to terminals *A* and *B*. Due to the limited commercially available capacitance values, only approximate values were used. This was relevant information also in order to evaluate the sensibility to the variation in capacitance.

Fig.20(a) shows the insertion loss for CM when applying capacitance cancellation networks which employ: (*i*) upper trace – no capacitance cancellation network; (*ii*) middle trace – a single 220 pF capacitor connected to the center of one of the windings as in equation (17), and; (*iii*) lower trace – three 68 pF capacitors as in equation (15), each connected to each one of the windings. The effectiveness of the capacitance cancellation networks is clearly observed since the resonance of the circuit without cancellation at approximately 2 MHz is no longer observed and an increasing gain in the insertion loss curves is seen up to 30 MHz, where a difference of more than 20 dB is seen from the configuration with three capacitors. The connection of a

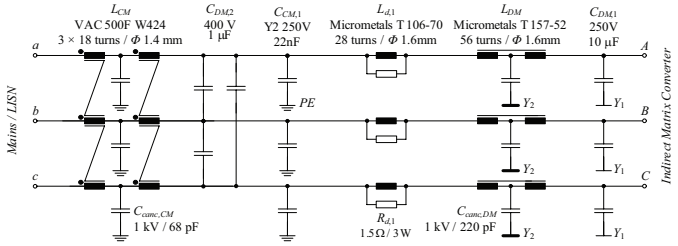

Fig.19: Input filter circuits employed in the testing of capacitance cancellation techniques.

single capacitor is less effective and an appreciable difference is noticed for frequencies higher than 15 MHz.

The insertion loss curves for the DM capacitance cancellation is presented in Fig.20(b) for a network as in Fig.11. It is observed that the results are not as expressive as in the CM case. A deeper analysis proves that, depending on the complete filter configuration, the cancellation of these capacitances might not improve the situation considerably. This is due to the relation between all impedances involved, for instance, in a resonance frequency. Despite that, the measurements with the DM capacitance cancellation show an improvement in very high frequencies and an appreciable reduction of the resonance peak at 4 MHz.

Conducted emission measurements with the filter and the IMC were performed with and without the inclusion of the discussed cancellation capacitors. The CE measurement results are displayed in **Fig.21**, where a three-phase CM/DM noise separator [21] is used in order to show the different contributions of the noise modes and the impact of the capacitance cancellation in each of them. The measured CM emissions are seen in **Fig.21**(a) for both versions of the filter, with and without the cancellation capacitors. Once the capacitance cancellation network is included, it is seen that the emission levels are appreciably reduced in the frequency ranges from 150 kHz to 500 kHz and from around 3 MHz to 30 MHz. However, the improvements are

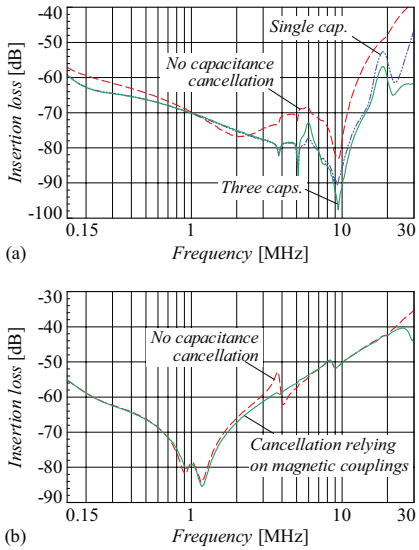

Fig.20: Insertion loss measurements showing the application of capacitance cancellation in the employed three-line power filter. (a) Filter CM insertion loss illustrating the application of capacitance cancellation to a three-phase CM choke. Shown are: measurement without capacitance cancellation; with three cancellation capacitors (68 pF per winding), and; with a single one (220 pF) connected to one of the windings. (b) DM insertion loss measurement with and without capacitance cancellation to three DM inductors (220 pF per inductor).

not as significant as in the insertion loss measurements. This is because the IMC's noise source impedance certainly presents an impedance value which is different from the impedance used for measuring the insertion loss (50 Ω). The DM emissions are depicted in **Fig.21**(b). From there it is observed that improvements are present in the frequency ranges from 4 MHz to 10 MHz and from around 20 MHz to 30 MHz. As for the CM case, the difference with the inclusion of canceling capacitors is not the same observed in the insertion loss. Finally, the total emission levels for one of the phases is shown in **Fig.21**(c), where it is seen that improvements are achieved with the inclusion of capacitance cancellation networks.

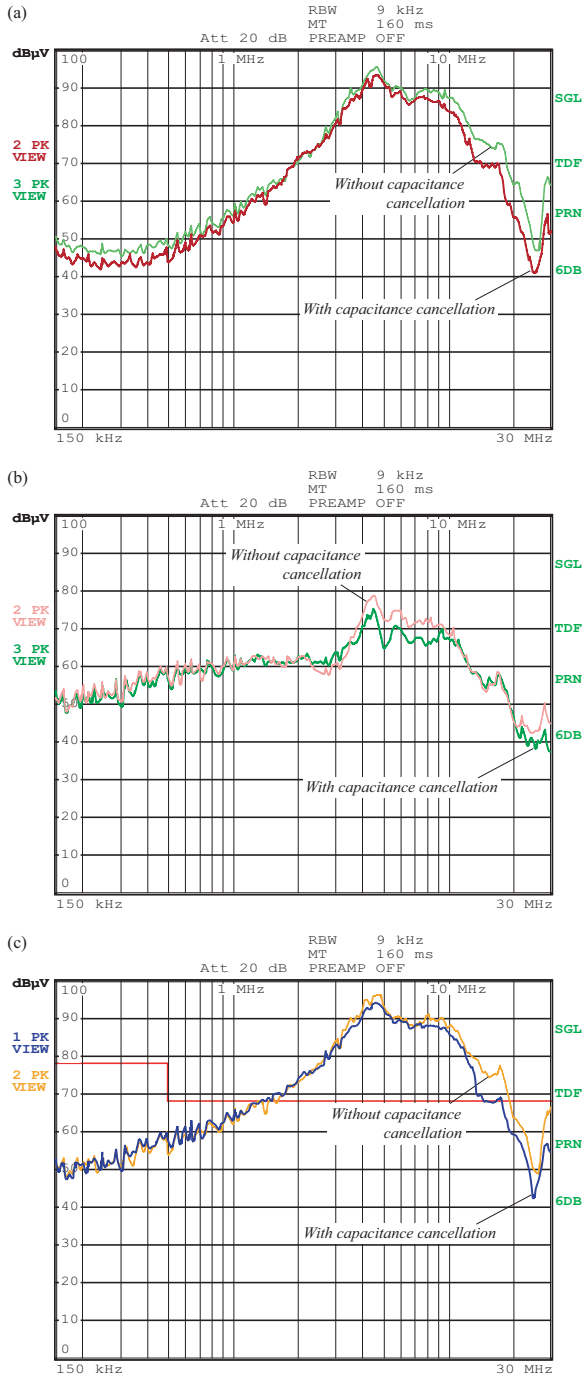

Fig.21: Conducted emission (CE) measurements performed in a three-phase 6 kVA ASD prototype built with an indirect matrix converter (IMC) based on RB-IGBTs [19].

VII. Conclusions

This work has presented a systematic way of evaluating impedances (CM and DM) in three-phase networks to be used in power line filtering. The flexibility of three-phase networks has been explored to achieve winding parasitic capacitance cancellation. Techniques have been presented for three-phase inductive networks along with a thorough theoretical analysis, where advantages and side-effects of the networks have been highlighted and possible improvements through damping resistances and use of different networks have been proposed. The influence of common parasitic effects was studied, from where the guidelines for a good design can be derived. The possibility of asymmetrical capacitance cancellation was proposed, which can improve the application of these techniques for switched mode power circuits. With the application of the proposed cancellation networks it is expected that cheaper inductors can be used, since the magnetic component designer is able to use a core with fully winded window. In order to prevent the elevation of the cost with capacitors it is proposed that the small capacitors are integrated into the printed circuit board. A set if experimental results attest the presented principles and prove that the analyzed techniques allow for improvements in the performance of a EMC filter. From the experimental analyses it is seen that the degree of improvement is dependent on the circuit structure, since different source and load impedances considerably change the influence of an inductor's parasitic capacitance. Good layout techniques, other parasitic impedance cancellation techniques and the reduction of capacitive and magnetic couplings are to be used along with the capacitance cancellation and shall allow for more compact, cheap and high performance filtering.

Acknowledgment

The authors would like to specially thank Thomas Friedli for the very helpful assistance during the CE tests.

Appendix I – Equivalence of 2-port networks

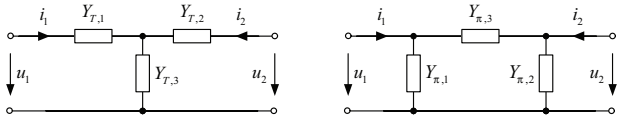

Fig.22: Considered networks.

The impedance matrices for the circuits of **Fig.22** are given by:

$$Z_T = \begin{bmatrix} \dfrac{Y_{T,1}+Y_{T,3}}{Y_{T,1}Y_{T,3}} & \dfrac{1}{Y_{T,3}} \\ \dfrac{1}{Y_{T,3}} & \dfrac{Y_{T,1}+Y_{T,3}}{Y_{T,1}Y_{T,3}} \end{bmatrix} \text{ for the } T\text{-network.} \quad (A.1)$$

And for the *Pi*-network by

$$Z_\pi = \begin{bmatrix} \dfrac{Y_{\pi,2}+Y_{\pi,3}}{Y_{\pi,1}Y_{\pi,2}+Y_{\pi,2}Y_{\pi,3}+Y_{\pi,3}Y_{\pi,1}} & \dfrac{Y_{\pi,3}}{Y_{\pi,1}Y_{\pi,2}+Y_{\pi,2}Y_{\pi,3}+Y_{\pi,3}Y_{\pi,1}} \\ \dfrac{Y_{\pi,3}}{Y_{\pi,1}Y_{\pi,2}+Y_{\pi,2}Y_{\pi,3}+Y_{\pi,3}Y_{\pi,1}} & \dfrac{Y_{\pi,1}+Y_{\pi,3}}{Y_{\pi,1}Y_{\pi,2}+Y_{\pi,2}Y_{\pi,3}+Y_{\pi,3}Y_{\pi,1}} \end{bmatrix} \quad (A.2)$$

If all elements of matrices Z_T and Z_π are the same, then the networks are equivalent.

Another equivalence of interest is given for the networks depicted in **Fig.23**. These are used in some of the capacitance cancellation

networks, inductance cancellation networks and on "zero"-ripple filters.

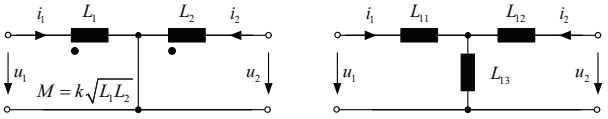

Fig.23: Equivalent circuits with magnetic coupling.

Considering the coupled inductor circuit, its impedance matrix is given by,

$$Z_{coupl} = \begin{bmatrix} sL_1 & -sM \\ -sM & sL_2 \end{bmatrix}. \quad \text{(A.3)}$$

The non-coupled network presents the matrix,

$$Z_{non-coupl} = \begin{bmatrix} s(L_{11} + L_{13}) & sL_{13} \\ sL_{13} & s(L_{12} + L_{13}) \end{bmatrix}. \quad \text{(A.4)}$$

Solving the equation given by $Z_{coupl} = Z_{non\text{-}coupl}$ in order to find equivalent networks results that,

$$\begin{aligned} L_{11} &= L_1 + M \\ L_{12} &= L_2 + M \\ L_{13} &= -M \end{aligned}. \quad \text{(A.5)}$$

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