Design Guidelines for Interleaved Single-Phase Boost PFC Circuits

Thomas Nussbaumer, *Member, IEEE*, Klaus Raggl, *Member, IEEE*, and Johann W. Kolar, *Senior Member, IEEE*

***Abstract*—This paper provides a comprehensive guideline for the design of a single-phase PFC targeting for minimal volume, as it is highly relevant for ultracompact integrated systems. It is shown, how different operation modes (continuous, boundary, and discontinuous conduction mode) may influence the design and consequently the achieved power density. Furthermore, the effect of interleaving of several boost stages is analyzed as a measure for compactness increase. Finally, the selection of the appropriate switching frequency in order to achieve an overall optimized system is discussed. In this way, the design of the crucial components is carried out, namely, the boost inductor, including a volume optimization through a thermal connection to the heat sink; the output capacitor considering the rms current stress; and the input filter, which is designed for compliance with high-frequency electromagnetic compatibility standards, taking into account the quasi-peak detection measurement of the test receiver equipment.**

***Index Terms*—Electromagnetic compatibility (EMC), interleaved converters, power density, power factor correction (PFC), single-phase boost converter.**

I. Introduction

In THE DESIGN process of mains-connected power electronic systems, always the question of compliance with harmonic standards both in the low- and high-frequency range arises. In particular, this fact has led to the development of boost power factor correction (PFC) circuits [1] ensuring sinusoidally shaped input currents (achieving a power factor close to unity) in connection with electromagnetic compatibility (EMC) input filters, which are preventing high-frequency noise from being transmitted from the converter to the mains.

The design of a PFC for power supply units is normally aiming for high efficiency and high power density at the same time, whereby these targets are typically contradicting (with the switching frequency as parameter), and for a specific application, a compromise has to be accepted. However, for integrated systems, such as pumps, fans, handheld tools, drilling machines, etc., the PFC design is usually more focused on high compactness than on high efficiency. First, space is typically the absolute limiting factor in these applications. Second, the efficiency is of minor importance, since the efficiency of the mechanical and/or hydraulic part of the motors and pumps is normally significantly lower than of the power electronics part. In addition, last, in many applications, effective cooling (such as water cooling or the presence of a cold plate) is present, making the power electronics losses less relevant. Therefore, the design of a PFC for such integrated systems aims for highest level of compactness, while keeping the efficiency in a reasonable range. Although this definition is quite vague, it will be shown in this paper that it leads to specific design rules.

In this paper, the focus shall be put on the conventional boost PFC topology (cf., Fig. 1), where the effects of interleaving of various parallel boost cells are investigated as a potential measure to increase power density. Alternative topologies, as, e.g., the bridgeless PFC circuit [2]–[4], where slightly higher efficiency potential [3], [5], but also increased common mode (CM) noise issues [2], [5], [6] have been reported, shall not be investigated here.

The operation modes of the boost PFC can be roughly classified into three categories depending on the waveform of the boost-inductor current, namely, the continuous conduction mode (CCM), the boundary conduction mode (BCM),[1] and the discontinuous conduction mode (DCM) operation. Typical boost-inductor current waveforms for these three operation modes are shown in Fig. 2, and a good basic overview about theses operating modes is given in [7].

In the past years, the conventional CCM operation has been replaced in many designs by BCM or DCM operation mainly due to three facts: First, the measurement of the boost-inductor current, which has to be very accurate for the CCM operation, is no longer required for BCM and DCM. For BCM operation, only the current zero crossing has to be detected by an additional sensing winding on the boost-inductor coil, and for DCM operation, it can be omitted completely [7]. Second, the boost inductor can be designed more compactly for the BCM and DCM operation, since a larger ripple is allowed. However, it has to be considered that, in turn, a larger input filter is required for BCM and DCM operation due to the increased current ripple noise [8]. Finally, lower switching losses appear for BCM and DCM, since no turn-on losses occur [7], [9] in the semiconductors due to zero current switch-on [cf., Fig. 2(b) and (c)]. However, for the design, it has to be taken into account that higher current stresses occur in both active and passive components, which are leading again to higher losses. In particular, for BCM, the switching frequency has to be strictly limited around the

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T. Nussbaumer was with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH), 8092 Zürich, Switzerland. He is now with Levitronix GmbH, 8005 Zürich, Switzerland.

K. Raggl was with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH), 8092 Zürich, Switzerland. He is now with Hilti AG, 9494 Schaan, Liechtenstein (e-mail: klaus.raggl@hilti.com).

J. W. Kolar is with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH), 8092 Zürich, Switzerland.

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[1]This mode is often also called "critical conduction mode;" however, due to the identical abbreviation of the CCM, the denomination "BCM" is preferred.

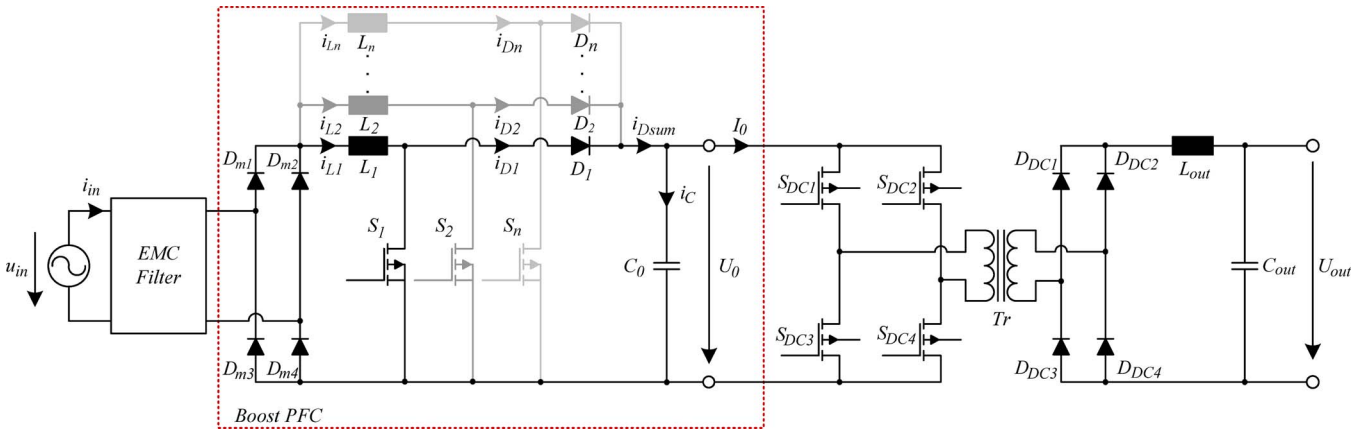

Fig. 1. Topology of a input PFC converter with n interleaved boost cells and an output full-bridge dc–dc converter.

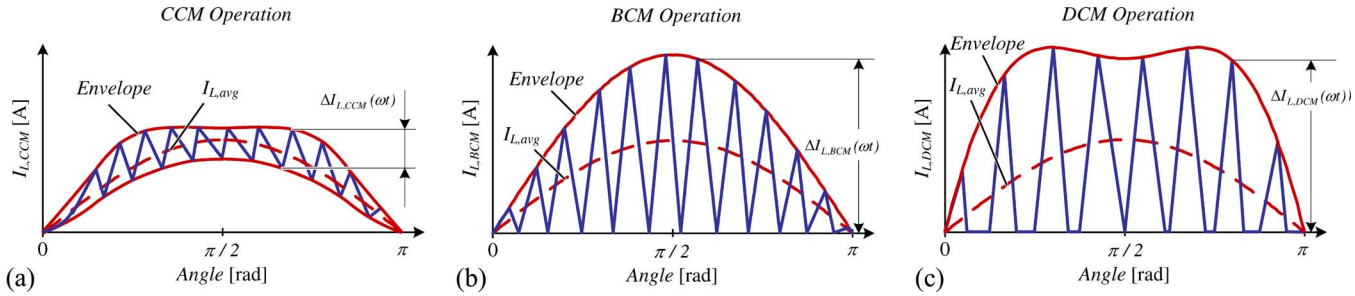

Fig. 2. Time behavior of the boost-inductor current for different operating modes. (a) CCM. (b) BCM. (c) DCM.

current zero crossings in order to avoid high switching losses in that area [7], which, in consequence, leads to a lower total harmonic distortion (THD) of this operation mode [8]. Recently, new semiconductor devices have made the CCM operation again more attractive. In particular, the employment of SiC (silicon carbide) Schottky diodes can effectively eliminate turn-on losses due to the fact that they show virtually no reverse recovery behavior [10], [11].

In the literature, several of these aspects have been investigated separately, such as the optimal design of the inductor [12]–[14] and capacitor [15], and the sensing and controlling of the inductor current (average current mode control [7], [16], hysteresis control [7], [17], [18]), the effect of interleaving of several boost stages [19]–[21], the efficiency improvement by employment of SiC [11], together with the appropriate selection of the switching frequency. However, no comprehensive work has been done until now, where all the aforementioned issues are included and an overall optimization is presented. It will be shown in this paper that the selection of the switching frequency, the operation mode, and the number of interleaved boost cells only leads to maximum power density, if all important power components are considered. Therefore, the dependence of the volume and the losses of the main power components on these three parameters is shown in a general manner by analytic formulas. Apart from serving as a tutorial design guideline, this paper also proposes some novel ways how to increase the power density of PFCs.

1) In Section II, where the boost-inductor design is discussed, particularly the effect of a thermal connection of the inductor with the heat sink is analyzed. Two thermal connection alternatives, i.e., via cooling pin and via cooling tube, are proposed, appropriate thermal models are developed and the improvement compared to a conventional inductor design is shown. Based on this, the effect of the operation mode, switching frequency, and number of interleaved stages on the boost-inductor size is analyzed under consideration of thermal constraints.
2) In Section III, where the output capacitor design is treated, parameter-based formulas for the capacitor current ripple are developed. With this, a designer may calculate the capacitor current stress both for the continuous and discontinuous current conduction mode and for different number of interleaved stages for any given load condition, since the formulas only depend on the voltage transfer ratio and the output current.
3) In Section IV, where the design of the input filter both in terms of CM and differential mode (DM) is discussed, a method to minimize the filter size while ensuring the fulfillment of noise emission standards is presented. In particular, the optimum number of filter stages and the selection of optimum component values in order to achieve a minimum total filter volume are discussed.

While this paper shall serve as a guideline for the design of a boost PFC with maximum power density and is valid for any power rate, in [22], a PFC is designed for a specific power range of 300 W in order to exemplify the considerations given in this paper.

All considerations in this paper are carried out both for the CCM and for the DCM. Although BCM operation has the advantage that commercial integrated circuits are available

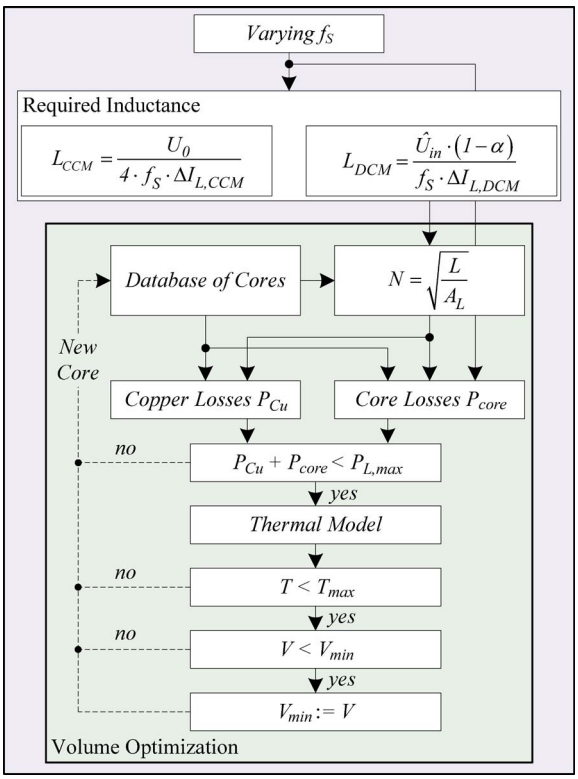

Fig. 3. Flowchart for the boost-inductor optimization.

[23], [24] (even for dual interleaved operation [25]), it results in higher losses and/or lower THD compared to DCM operation as discussed before. Furthermore, DCM can be operated completely without any current sensing device. With this, the most promising operation modes to achieve the targeted ultrahigh power density are CCM and DCM, which will be discussed in the following.

II. Boost-Inductor Design

The design of the boost inductor is one of the main challenges in the PFC design, wherefore it has been discussed extensively in literature [12], [15], [17], [26]–[28]. Typically, the design process starts with a certain inductance that is required in order to guarantee proper PFC operation. Since inductors may show strong saturation behavior, this inductance value has to be ensured until the maximum appearing inductor current. Then, a core material and size have to be selected in order to satisfy the following design criteria.

1) The number of turns that are needed in combination with a certain core type have to fit into the provided space, i.e., for toroidal inductor cores the inside area.
2) The temperature rise due to the copper losses in the windings and the core losses have to remain below a certain maximum allowed value.

These issues lead to an optimization including electrical, magnetic, and thermal design aspects. Fig. 3 shows the optimization routine, which is based on a certain required inductance value and a database of inductor core values. The needed inductance value is depending on the operating mode as will be shown in the following section as well as on the switching frequency and on the operating point. The inductor core database has to include core specific parameters such as the A_L value (inductance per square-turns), geometric data and core loss data. With this, for each core the required number of turns N, the occurring copper losses P_{Cu} and core losses P_{core}, being in total lower than a certain maximum allowed value $P_{L,\max}$, can be calculated. Applying the thermal model, described in Section II-C, the actual temperature T of the inductor can be derived and compared to the maximum allowed temperature $T_{\max}$. Finally, the inductor volume for a specific core can be calculated and the cores featuring minimal volume can be identified for a specific switching frequency f_{S}.

In these calculations, for the case of interleaving equal inductance values in the parallel boost cells will be assumed. As a matter of fact, different inductance values due to tolerances lead to an unequal current distribution and, consequently, to generation of subharmonics and different losses appearing in the boost stages. In order to ensure a proper current sharing, control strategies can be employed both for CCM [29] and BCM/DCM [30], [31]. In any case, an unequal current distribution also leads to slightly higher values of the input current ripple [30]. However, for the subsequent design considerations, these facts will be neglected in order to focus on the essentials.

In the following, first, the required inductance values and the appearing losses for the CCM and the DCM operation will be calculated. Subsequently, a thermal model of the inductor will be developed, where it will be shown that the amount of allowed losses and the total volume can be improved significantly by a thermal connection of the inductor with the heat sink via a cooling pin and a cooling tube, respectively.

A. Selection of Inductance Value

The boost-inductor design for CCM [12], [15], [17], [27] and DCM [26], [28] operation has been already discussed in literature. Therefore, for the sake of simplicity, only the most important equations will be mentioned in this section.

1) CCM Operation: For CCM, the required inductor value L_{CCM} is given by

$$L_{\mathrm{CCM}} = \frac{U_0}{4 \cdot f_{\mathrm{S}} \cdot \Delta I_{L,\mathrm{CCM,pk\text{-}pk,max}}} \tag{1}$$

with the dc-link voltage U_0, the switching frequency $f_{\mathrm{S}} = 1/T_{\mathrm{S}}$, and the maximum allowed peak-to-peak current ripple $\Delta I_{L,\mathrm{CCM,pk\text{-}pk,max}}$, which is set in relation to the amplitude of the local average inductor current $\hat{I}_{L,\mathrm{CCM,avg}}$

$$\Delta I_{L,\mathrm{CCM,pk\text{-}pk,max}} = k_{\mathrm{ripple}} \cdot \hat{I}_{L,\mathrm{CCM,avg}} \tag{2}$$

where the local average inductor current is given by

$$\hat{I}_{L,\mathrm{CCM,avg}} = \frac{\hat{I}_{\mathrm{in}}}{n} \tag{3}$$

with n being the number of interleaved boost cells and $\hat{I}_{\mathrm{in}}$ being the mains current amplitude. This maximum current ripple occurs when $\hat{U}_{\mathrm{in}}$ equals $U_0/2$.

In principle, the selection of the ripple factor k_{ripple} will have an influence on the appearing losses, the electromagnetic

interference (EMI) filter requirements and the inductance volume and should therefore be carefully selected for CCM operation. In [32], an optimization of k_{ripple} regarding the inductance volume has been presented for the case of natural convection via the inductor surface. There, it has been shown that an optimal value of k_{ripple} regarding minimal inductor volume can be found for a specific switching frequency.

However, if the converter efficiency is not of major importance and the losses can be transferred effectively to the heat sink (as will be proposed in Section II-C), the main tradeoff in the selection of k_{ripple} appears between the inductor volume and the input-filter volume. As shown in [22], it is advisable to chose a ripple factor of at least $k_{\mathrm{ripple}} \geq 0.4$ in order to achieve minimum total volume.

For a higher number of boost cells n, the current through each inductor decreases with $\hat{I}_{L,\mathrm{CCM,avg}} \propto 1/n$ according to (3). Hence, for the same inductor value the ripple factor k_{ripple} increases with n, wherefore discontinuous operation may occur around the zero crossings particularly at light load conditions. This leads to the fact that a designer may have to choose even bigger inductance values for a higher number of boost cells in order to ensure proper CCM operation. Thus, for keeping k_{ripple} constant, the inductance value of each stage is increased linearly with n. In this case, the total inductor volume stays theoretically constant according to the general scaling law $V_L \propto n \cdot L \cdot I_L^2 \propto \mathrm{const}$. The validity of this fact will be discussed in [22]. As will be shown there, this scaling law is not perfectly true if only a limited number of cores is available.

2) DCM Operation: For DCM, the inductor value L_{DCM} is selected in such way that the sum of the turn-on and the turn-off time of the boost switch exactly equals the pulse period $T_{\mathrm{S}} = 1/f_{\mathrm{S}}$ at the middle of the mains period ($\omega t = \pi/2$)

$$L_{\mathrm{DCM}} = \frac{\hat{U}_{\mathrm{in}} \cdot (1-\alpha)}{f_{\mathrm{S}} \cdot \Delta I_{L,\mathrm{DCM}}(\omega t = \pi/2)} \tag{4}$$

with the input–output voltage ratio $\alpha = \hat{U}_{\mathrm{in}}/U_0$ and the maximum allowed peak-to-peak current ripple

$$\Delta I_{L,\mathrm{DCM}}(\omega t = \pi/2) = \frac{2}{n} \cdot \hat{I}_{\mathrm{in}}. \tag{5}$$

With this, the inductor current stays discontinuous during the whole mains period. For practical applications, it is recommended to choose a boost-inductor value being lower than given in (4) in order to guarantee discontinuous operation in all boost cells also for the case of unequal current distribution due to inductance tolerances as mentioned before.

Equation (5) indicates that the inductor ripple is decreasing and consequently the inductor value is increasing with higher number of interleaved cells $L_{\mathrm{DCM}} \propto n$. Thus, the DCM inductor volume is also theoretically independent of the number of boost cells $V_{L,\mathrm{DCM}} \propto n \cdot L_{\mathrm{DCM}} \cdot I_L^2 \propto \mathrm{const}$, since the current is again divided up to n stages $I_{L,\mathrm{DCM}} \propto 1/n$. Again, variations from this scaling law may occur in the case of a limited number of cores as will be discussed in [22].

B. Inductor Core Losses

Based on the core-dependent A_L value given in datasheets [33], [34] the needed winding number N can now be calculated as

$$N = \sqrt{\frac{L}{A_L(I_L = I_{L,\max})}} \tag{6}$$

where the dependence of the A_L factor (and hence the inductance) on the current has to be considered in order to guarantee the needed inductance over the whole current range. Thereunto, in [33], some useful design guidelines can be found. The next step for the inductor design is to calculate the appearing power losses. The inductor losses can be separated into copper losses P_{Cu} given by

$$P_{\mathrm{Cu}} = I_{L,\mathrm{rms}}^2 \cdot R_{\mathrm{Cu}} \tag{7}$$

with

$$R_{\mathrm{Cu}} = \frac{\rho_{\mathrm{Cu}} \cdot l_{\mathrm{Cu}}}{A_{\mathrm{Cu}}} \tag{8}$$

where ρ_{Cu} is the electrical resistivity, l_{Cu} is the length, and A_{Cu} the cross-sectional area of the copper winding; and the core losses P_{core}, which can be calculated based on the Steinmetz equation [35]

$$P_{\mathrm{core}} = k \cdot f^a \cdot \hat{B}^b \tag{9}$$

where the parameters k, a, and b can be found in the datasheets. However, (9) is only valid for sinusoidal currents, which is not the case here, particularly for the DCM operation. For piecewise linear current curves, the Steinmetz equation can be adapted according to [36] to

$$P_{\mathrm{core}} = k_i \cdot f_{\mathrm{S}} \cdot \Delta B^{b-a} \sum_j \left(\frac{U_j}{N \cdot A_{\mathrm{c}}} \right)^a \cdot \Delta t_j. \tag{10}$$

Here, A_{c} stands for the cross-sectional area of the core, and the same factors a and b of the datasheets can be utilized as for (9). U_j means the voltage which is applied to the coil during a time interval Δt_j and which leads to a linear current waveform during this time interval. The parameter k_i has to be adapted according to [36] to

$$k_i = \frac{k}{2^{b+1} \cdot \pi^{a-1} \cdot \left(0.2761 + \frac{1.7061}{a+1.354}\right)}. \tag{11}$$

Decreasing the inductor volume generally leads to an unacceptable temperature rise ΔT due to the appearing losses and reduced surface for heat dissipation. To achieve highest power density, the losses have to be transferred to the heat sink through a thermal connection. Thus, in the following section, the thermal model of a toroidal inductor core, which is the most common inductor core type, is developed, and a guideline for the design of two alternative cooling concepts for achieving highest power density is given.

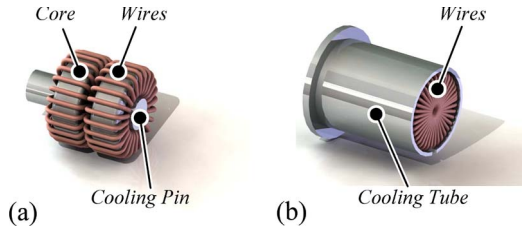

Fig. 4. Passive cooling methods for an inductor with a toroidal core.

C. Inductor Optimization Through Thermal Connection

Since the inductor design may result in a high volume due to the restriction of the maximum temperature rise ΔT, a method for dissipating the heat has to be found. In the following, two passive cooling methods to connect the inductor to a cold plate will be discussed, whereby exemplarily, a toroidal core geometry will be considered:

1) passive cooling by a pin in the inductor inside [cf., Fig. 4(a)];
2) passive cooling by a tube connected to the outer inductor surface [cf., Fig. 4(b)].

In the following sections, a thermal model will be developed, and the resulting core temperatures will be calculated analytically. Subsequently, it will be shown that both cooling methods lead to an enormous reduction of the total inductor volume.

1) Cooling Pin: An equivalent diagram for the thermal model is shown in Fig. 5(a), where the loss sources, thermal resistances, and temperature drops are drawn in analogy to electrical circuits. In the following, the thermal resistances will be derived for one of the n coils, which shows the largest distance to the heat sink connection. This coil will have the highest coil temperature drop and is therefore most relevant for the design. For the development of the thermal model, the following assumptions are made.

1) The heat dissipation to the ambiance is neglected due to the good thermal connection via the cooling pin.
2) The inductor core is assumed to be at a constant temperature level.
3) In addition, the copper windings are assumed to be at the same temperature level.
4) The heat is flowing uniformly in radial direction. No eddy current losses are considered. This assumption is valid for moderate switching frequencies in combination with electrically conductive material [37], [38]. Alternatively, a material with very low electrical conductivity and good thermal conductivity [39] can be employed.

The thermal resistors according to Fig. 5(a) are defined as follows.

$R_{\mathrm{th},1}$ Connection resistance between the core and the windings in radial direction. For reasons of producibility and proper thermal connection, this area is assumed to be filled out with filling material, such as epoxy resin.

$R_{\mathrm{th},2}$ Connection resistance between the windings and the cooling pin in radial direction. Again, this area is assumed to be filled out with filling material.

$R_{\mathrm{th},3}$ Conduction resistance of the connection pin in longitudinal direction.

The three resistances can be calculated based on the general formula [40]

$$R_{\mathrm{th}} = \frac{l}{\lambda \cdot A} \tag{12}$$

where λ is the thermal conductivity, l is the length (or thickness, respectively), and A is the cross-sectional area of the material of which the heat is flowing through.

For $R_{\mathrm{th},1}$, the heat is now flowing uniformly outwards in radial direction through the thickness of the filling material d_{fill},which has the shape of a tube [cf., Fig. 5(b)]. The cross-sectional area is now the average surface of the tube, which is given by

$$A = \pi \cdot (r_{a,\mathrm{core}} + r_{i,\mathrm{core}}) \cdot \left[2(h_{\mathrm{core}} + d_{\mathrm{fill}}) + 2(r_{a,\mathrm{core}} - r_{i,\mathrm{core}} + d_{\mathrm{fill}})\right]. \tag{13}$$

With this, the thermal resistance $R_{\mathrm{th},1}$ can be calculated as

$$R_{\mathrm{th},1} = \frac{d_{\mathrm{fill}}}{\lambda_{\mathrm{fill}} \cdot 2\pi \cdot (r_{a,\mathrm{core}} + r_{i,\mathrm{core}})} \cdot \frac{1}{(r_{a,\mathrm{core}} - r_{i,\mathrm{core}} + h_{\mathrm{core}} + 2d_{\mathrm{fill}})}. \tag{14}$$

In a similar manner, the thermal resistance $R_{\mathrm{th},2}$ can be derived, whereas the heat is now flowing radially inwards through the filling material thickness d_{fill} to the cooling pin. Here, the cross-sectional area is given by

$$A = \pi \cdot (2r_{\mathrm{pin}} + d_{\mathrm{fill}}) \cdot h_{\mathrm{coil}} \tag{15}$$

with

$$h_{\mathrm{coil}} = h_{\mathrm{core}} + 2d_{\mathrm{fill}} + 2h_{\mathrm{Cu}} \tag{16}$$

where h_{Cu} is the height of the windings, which may consist of several layers. This results in a thermal resistance

$$R_{\mathrm{th},2} = \frac{d_{\mathrm{fill}}}{\lambda_{\mathrm{fill}} \cdot \pi \cdot (2r_{\mathrm{pin}} + d_{\mathrm{fill}}) \cdot h_{\mathrm{coil}}}. \tag{17}$$

As for the thermal resistance $R_{\mathrm{th},3}$, the heat is now flowing in longitudinal direction toward the heat sink. For the design, only the core with the highest temperature rise has to be considered, which is appearing for the core being located at the other end of the connection between pin and heat sink. For this core, the thermal resistance is given by

$$R_{\mathrm{th},3} = \left(n - \frac{1}{2}\right) \cdot \frac{h_{\mathrm{coil}}}{\lambda_{\mathrm{pin}} \cdot \pi \cdot r_{\mathrm{pin}}^2}. \tag{18}$$

Due to the same losses P_{core} and P_{Cu}, the same thermal resistances $R_{\mathrm{th},1}$ and $R_{\mathrm{th},2}$ and the closer connection to the heat sink the other core values will show lower temperature rises and are therefore not relevant for the design. Knowing the thermal resistances and the losses, the temperature T_{core} of

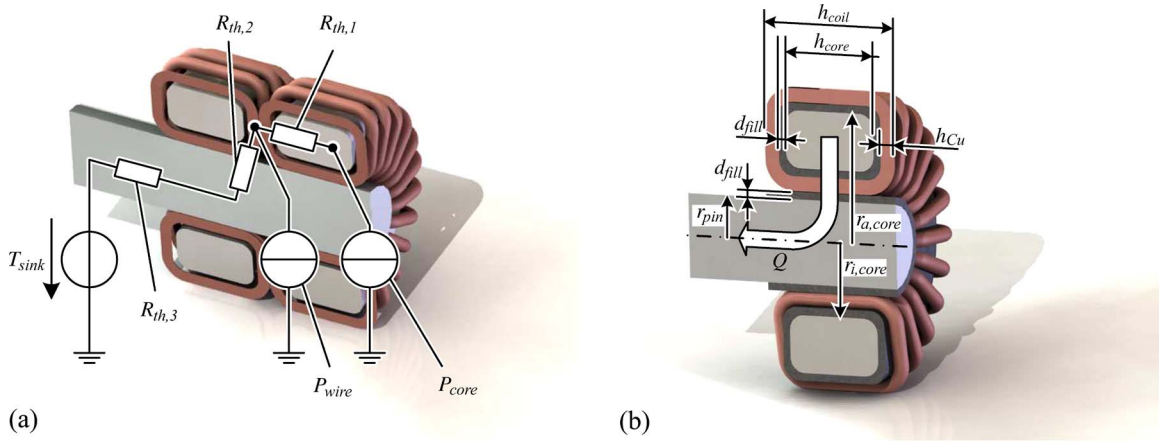

Fig. 5. Thermal connection of the boost inductor with the heat sink via cooling pin. (a) Simplified thermal model for one of the n interleaved boost inductors (exemplarily two inductors are shown). (b) Definition of the geometric variables of the inductor.

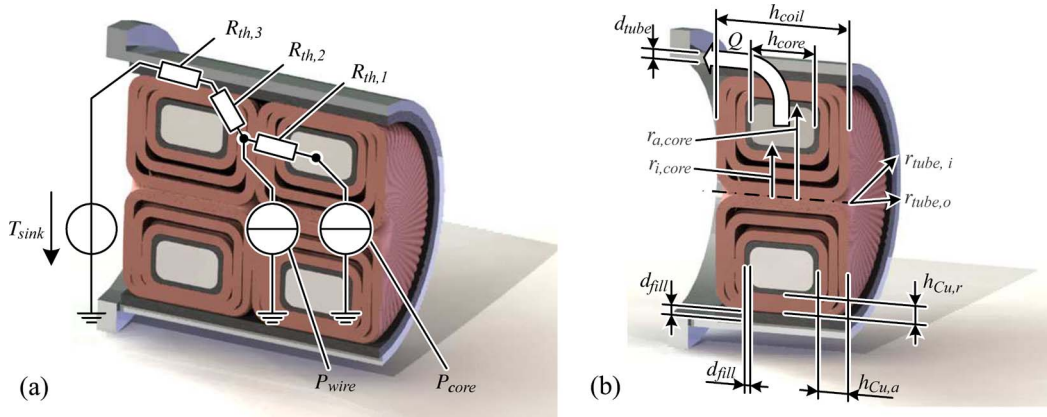

Fig. 6. Thermal connection of the boost inductor with the heat sink via a cooling tube. (a) Simplified thermal model for one of the n interleaved boost inductors (exemplarily two inductors are shown). (b) Definition of the geometric variables of the inductor.

the considered core compared to the heat sink temperature is calculated through

$$T_{\mathrm{core}} = T_{\mathrm{sink}} + P_{\mathrm{core}} \cdot R_{\mathrm{th},1} + (P_{\mathrm{core}} + P_{\mathrm{Cu}}) \cdot (R_{\mathrm{th},2} + R_{\mathrm{th},3}). \quad (19)$$

Based on this, a core with minimal volume fulfilling the condition $T_{\mathrm{core}} \leq T_{\max}$ can be selected, where for each core an optimal partition between copper volume and cooling pin volume can be found, i.e., a larger cross-sectional area of the copper decreases the copper losses, whereas a larger pin volume amends the heat transfer to the heat sink.

2) Cooling Tube: The thermal model for this cooling method is shown in Fig. 6(a) For the sake of brevity, only the formulas will be given in the following. $R_{\mathrm{th},1}$ is calculated in the same manner as in case of a cooling pin, cf., (14), whereas $R_{\mathrm{th},2}$ and $R_{\mathrm{th},3}$ are ascertained by

$$R_{\mathrm{th},2} = \frac{d_{\mathrm{fill}}}{\lambda_{\mathrm{fill}} \cdot \pi \cdot (2r_{a,\mathrm{core}} + 2h_{\mathrm{Cu,r}} + 3d_{\mathrm{fill}}) \cdot h_{\mathrm{coil}}} \quad (20)$$

$$R_{\mathrm{th},3} = \left(n - \frac{1}{2}\right) \cdot \frac{h_{\mathrm{coil}}}{\lambda_{\mathrm{tube}} \cdot \pi \cdot \left(r_{a,\mathrm{tube}}^2 - r_{i,\mathrm{tube}}^2\right)} \quad (21)$$

respectively, whereby the according geometric variables are shown in Fig. 6(b). If the inner core area is completely filled with windings, the outside radial height $h_{\mathrm{Cu,r}}$ of the windings is given by

$$h_{\mathrm{Cu,r}} = -r_{a,\mathrm{core}} + \sqrt{r_{a,\mathrm{core}}^2 + r_{i,\mathrm{core}}^2}. \quad (22)$$

The resulting temperature drop between the inductor core and the cold plate can be determined again by solving (19), and an optimal core with minimal volume can be found in a similar manner as for the cooling pin. Due to the good thermal conductivity of the tube material, usually already a thin wall thickness will lead to a good thermal connection with the heat sink and, therefore, to a minimal total volume. Hence, for small inductor cores, the manufacturability of the tube has to be taken into account as a limiting factor for the design.

3) Improvement Through Thermal Connection: In order to give an idea of the volume reduction potential of the proposed heat dissipation alternatives in comparison to a conventional boost-inductor design without thermal connection, the results for a specific design will be given in this section exemplarily. A more detailed analysis will be given in Part II [22] of this paper.

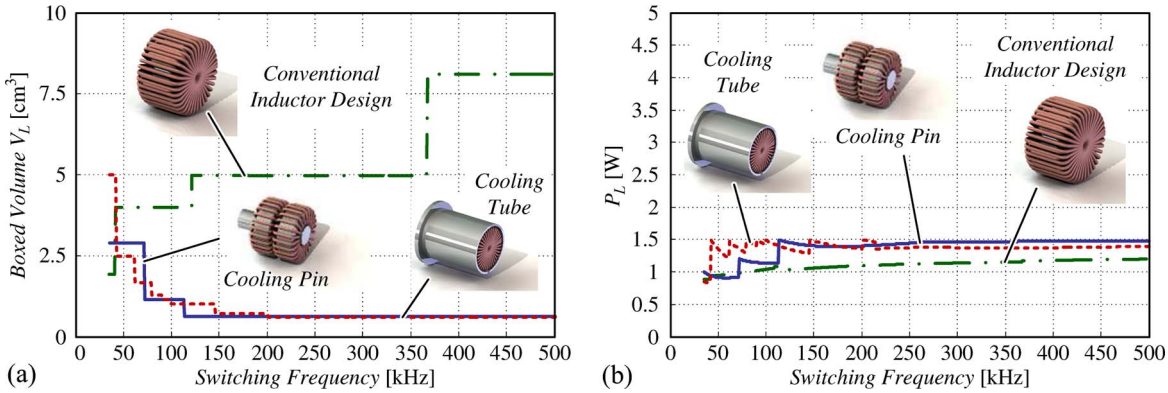

Fig. 7. Effect of thermal connection via cooling pin and cooling tube in terms of total boxed (a) inductor volume and (b) power losses as compared to a conventional inductor design without thermal connection. The comparison is carried out exemplarily for a 300-W PFC in two-cell interleaved DCM operation and for a maximum temperature rise of 30 °C between inductor core and heat sink.

In Fig. 7(a), the core volumes and, in Fig. 7(b), the core losses are depicted exemplarily for the boost inductors of a 300-W PFC in two-cell interleaved DCM operation in dependence of the employed switching frequencies. For the selection and dimensioning of the appropriate core for the cooling pin and cooling tube, the thermal model, which has been developed in the previous sections, has been utilized. For the calculation of the core temperature of the inductor without heat sink connection, an empirical formula (containing convection and thermal radiation) according to [33] has been used

$$T_{\mathrm{core}} = T_{\mathrm{ambient}} + \left(\frac{(P_{\mathrm{core}} + P_{\mathrm{Cu}})\ [\mathrm{mW}]}{A_{\mathrm{inductor}}\ [\mathrm{cm}^2]} \right)^{0.833} \tag{23}$$

where A_{inductor} is the total surface area of the inductor including core and windings. The steps in the volume curves in Fig. 7(a) occur due to the limited number of available cores [33]. For the case at hand, a temperature increase of 30 °C of the core with respect to the heat sink and ambient temperature, respectively, has been assumed.

It can be seen that the thermal connection to the heat sink effectuates a huge volume decrease for both alternatives. Without thermal connection, the inductor volume strongly increases with higher switching frequencies, since higher core losses occur and bigger core sizes have to be selected in order not to exceed the maximum allowed temperature. For this specific case, the volume of the cooling tube is slightly smaller than of the cooling pin for most of the switching frequencies [cf., Fig. 7(a)]. However, the cooling pin can be preferable from a practical point of view due to its advantage of better manufacturability. In both cases, the volume reduction leads to an increase of the occurring losses, which, however, is not of major importance in that case.

III. Output Capacitor Design

A. Capacitor Voltage Ripple

In this section, the output capacitor, which is also determining the power density of the PFC considerably, will be designed. Since the dc-link voltage $u_0 = U_0 \pm \Delta u_0$ shows a voltage ripple depending on the capacitor value C_0 and the output power P_0, and the angular mains frequency ω according to

$$\Delta u_0 = \frac{P_0}{2\omega \cdot C_0 \cdot U_0} \tag{24}$$

it has to be ensured that it always remains within the following limits:

1) $u_0 > \hat{U}_{\mathrm{in,max}}$ on the lower side to ensure a proper boost and PFC functionality;
2) $u_0 < U_{\mathrm{C,max}}$, $u_0 < U_{\mathrm{T,max}}$, and $u_0 < U_{\mathrm{D,max}}$ on the upper side to avoid a component damage.

This defines the minimum required capacitance value and voltage rating.

B. Capacitor rms Current Stress

Another important selection criterion for the needed dc-link capacitor is the maximum allowed capacitor current ripple. For switching frequencies being sufficiently higher than the mains frequency, the appearing global rms current [41], which is relevant for the capacitor design, can generally be derived via the integration of the local rms value $i^2_{\mathrm{C,rms}}(\omega t)$, which is given by

$$i^2_{\mathrm{C,rms}}(\omega t) = \frac{1}{T_{\mathrm{S}}} \int_0^{T_{\mathrm{S}}} i^2_{\mathrm{C}}(t) dt \tag{25}$$

over the mains period

$$I^2_{\mathrm{C,rms}} = \frac{1}{2\pi} \int_0^{2\pi} i^2_{\mathrm{C,rms}}(\omega t) d\omega t. \tag{26}$$

Depending on the specific topology and operating mode, the evaluation of this formula can lead to very complex analytical calculations, particularly for the interleaved operation. For both CCM and DCM operation, the diode currents are inherently discontinuous. However, as shown in Fig. 8, exemplarily for

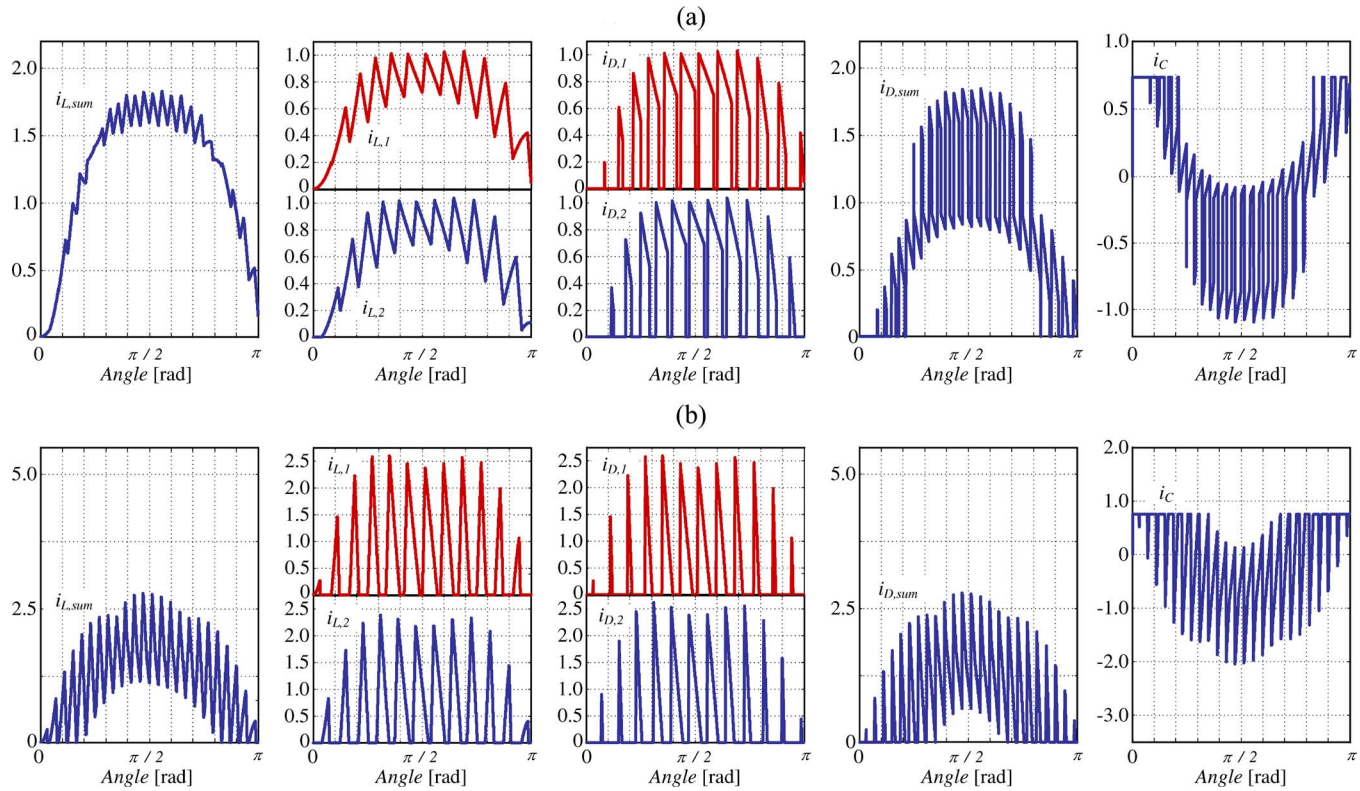

Fig. 8. Characteristic time behavior of relevant currents for dual interleaved (a) CCM operation and (b) DCM operation, whereby the switching frequency has been reduced to $f_S = 24 \cdot \omega/2\pi$ for reasons of better illustration.

dual interleaving $(n = 2)$, for the sum of the interleaved (and shifted by T_S/n) diode currents

$$i_{D,sum} = \sum_{i=1}^{n} i_{D,i} \tag{27}$$

overlapping occurs for a certain mains phase interval, which results in a partially continuous time behavior of $i_{D,sum}$. The calculation of the diode rms current $I_{D,sum,rms}$, which serves as a basis for the capacitor rms current $I_{C,rms}$ is thus afflicted with several difficulties.

1) First, the actual duty cycles $d = t_{on}/T_S$, which have to be known for the evaluation of (25), are varying over the mains period, i.e., for the CCM operation

$$d_{CCM} = 1 - \alpha \cdot \sin(\omega t) \tag{28}$$

and for the DCM operation

$$d_{DCM} = \sqrt{(1-\alpha) \cdot (1 - \alpha \cdot \sin(\omega t))} \tag{29}$$

with the voltage transfer ratio

$$\alpha = \frac{\hat{U}_{in}}{U_0}. \tag{30}$$

2) Second, also the current envelopes, which are used for the calculation of (25), vary over the mains period, i.e., for the CCM operation (neglecting the current ripple)

$$\Delta I_{CCM}(\omega t) = \frac{\hat{I}_{in}}{n} \cdot \sin(\omega t) \tag{31}$$

and for the DCM operation

$$\Delta I_{DCM}(\omega t) = \frac{2\hat{I}_{in}}{n} \cdot \sin(\omega t) \cdot \frac{\sqrt{1 - \alpha \cdot \sin(\omega t)}}{\sqrt{1-\alpha}}. \tag{32}$$

3) Finally, the major complication lies in the fact that the integral (25) for the capacitor rms current has to be partitioned into n intervals, where the integration borders ωt_i with $i = (1, \ldots, n)$ are given by

$$\omega t_i = \arcsin\left(\frac{i}{n \cdot \alpha}\right). \tag{33}$$

Thus, an analytical calculation leads to very complex formulas [42], which are not practical for a straightforward design and are, therefore, not presented in detail here. However, for both CCM and DCM operation, the capacitor rms current shows a basic dependence only on the output current I_0 and the voltage transfer ratio α according to

$$I_{C,rms} = I_0 \cdot f(\alpha). \tag{34}$$

Due to the linear dependence on the output current, the rated capacitor rms current $I_{C,rms}/I_0$ is a function of only the voltage transfer ratio $f(\alpha)$. Fig. 9 shows the analytically calculated dependence for the both operation modes and the

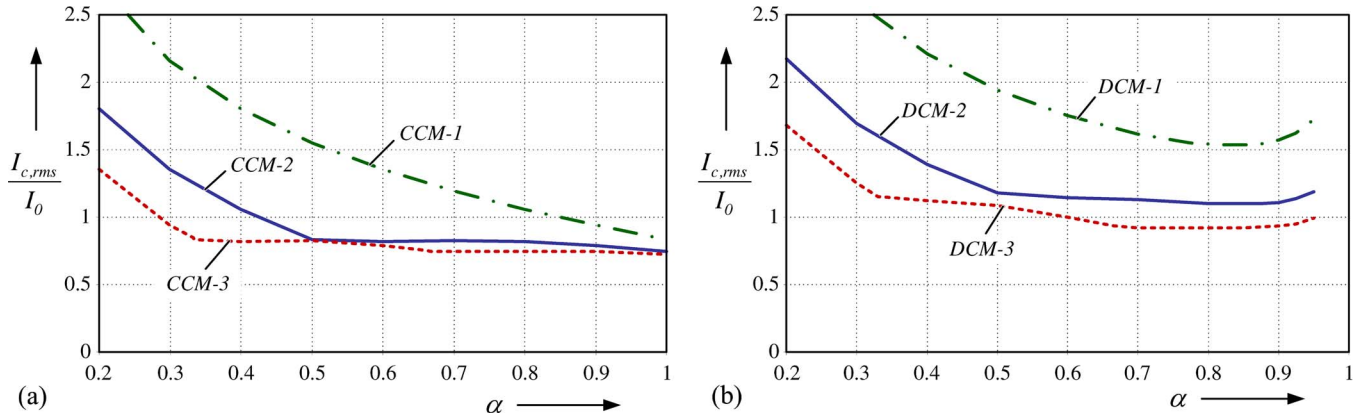

Fig. 9. Dependency of the rated rms capacitor current $I_{\mathrm{C,rms}}/I_0$ on the voltage transfer ratio α for $n = (1, \ldots, 3)$ for (a) CCM operation and (b) DCM operation, respectively.

TABLE I
PARAMETERS OF THE FUNCTIONS $f(\alpha)$ ACCORDING TO (35) FOR THE CALCULATION OF THE RATED CAPACITOR rms CURRENTS FOR DIFFERENT OPERATION MODES AND NUMBER OF INTERLEAVED STAGES

Operation Mode	Area of validity	k_0	k_1	k_2	k_3	k_4
CCM–1	$0 \le \alpha \le 1$	4.3	−9.7	10.7	−4.4	0
CCM–2	$0.0 \le \alpha \le 0.5$	3.5	−12.1	20.7	−14.3	0
	$0.5 \le \alpha \le 1.0$	0.67	0.55	−0.47	0	0
CCM–3	$0.00 \le \alpha \le 0.33$	2.7	−8.6	9.0	0	0
	$0.33 \le \alpha \le 0.66$	0.68	0.8	−1.0	0	0
	$0.66 \le \alpha \le 1.00$	0.49	0.67	−0.43	0	0
DCM–1	$0 \le \alpha \le 1$	6.1	−21.5	46.1	−49.3	20.6
DCM–2	$0.0 \le \alpha \le 0.5$	3.5	−8.1	6.8	0	0
	$0.5 \le \alpha \le 1.0$	−0.63	8.8	−13.9	7.0	0
DCM–3	$0.00 \le \alpha \le 0.33$	2.9	−7.5	6.5	0	0
	$0.33 \le \alpha \le 0.66$	1.06	0.72	−1.35	0	0
	$0.66 \le \alpha \le 1.00$	2.3	−3.56	2.29	0	0

practically interesting cases $n = (1, \ldots, 3)$, and in Table I, the parameters of the approximate functions of α are specified for the different cases. The functions $f(\alpha)$ have been fitted to the shown analytically calculated curves with least-square approximations of higher order type

$$f(\alpha) \approx k_0 + k_1 \cdot \alpha + k_2 \cdot \alpha^2 + k_3 \cdot \alpha^3 + k_4 \cdot \alpha^4 \qquad (35)$$

and have been verified by selected simulation data [22].

It is shown in Fig. 9 that for both CCM and DCM operation interleaving effectively decreases the capacitor rms current stress, particularly for lower voltage transfer ratios. Generally, the current levels lie higher for DCM operation. However, for $n = 2$ and $n = 3$, the current stresses for DCM operation are in a similar range as for CCM operation. Typically, a good selection of the voltage transfer ratio is in the range of $\alpha = 0.8$, which also makes sense from the viewpoint of effective utilization of the semiconductor components. With these results, it can be stated that DCM operation has no significant disadvantage in terms of capacitor current stress, if interleaving $(n \ge 2)$ is employed.

A further conclusion, which is important for the design, is that for both CCM and DCM operation the capacitor current is independent of the switching frequency, since, in both cases, the capacitor current originates from the discontinuous diode currents.[2]

IV. INPUT-FILTER DESIGN

While PFC circuits in proper operation already comply with the regulatory low-frequency harmonic standards (IEC 61000-3-2 [43]), a filter circuit has to be inserted at the input of the converter for compliance with the high-frequency EMC standards [44] in the range of 150 kHz–30 MHz. With this, high-frequency conducted emission (CE) noise occurring at multiples of the switching frequency shall be attenuated effectively and/or prevented from propagating toward the mains.[3]

The design of the input filter of the PFC converter is an important issue in the design process, since it has a strong impact on the achieved power density of the converter. As mentioned already before, a smaller volume of the boost inductors (e.g., by allowing a higher ripple value in the CCM operation or by operating the converter in DCM mode) may increase the amount of high-frequency harmonic noise [45], which will consequently increase the filtering requirements and lead to a larger filter size. Thus, the scaling of both the boost-inductor and the input-filter components with the switching frequency has to be considered for the design of an overall optimized system (as mentioned in the previous section, the capacitor volume does not scale with the switching frequency, but with the power and voltage specifications).

From this viewpoint, interleaving of several boost cells seems to be a very promising technique. While the inductor volume stays mainly constant (see Section II-A), but on the other hand, the harmonic noise is reduced in amplitude and shifted to higher frequencies [13], [18]–[20], [46] (e.g., this fact is shown in Fig. 8 by comparing ripple amplitudes and frequencies of $i_{L,\mathrm{sum}}$ and $i_{L,1}$), wherefore the filter size can be designed smaller. However, for the overall optimization, also the volumes

[2]For an exact calculation, also the switching frequency ripple of the boost inductor in CCM operation could be taken into account. However, for practical values of k_{ripple} in the range of $k_{\mathrm{ripple}} \le 0.4$, the switching frequency ripple has virtually no influence on the capacitor rms current.

[3]In this section, only conducted emissions are considered, since they are the determining factor for the filter volume.

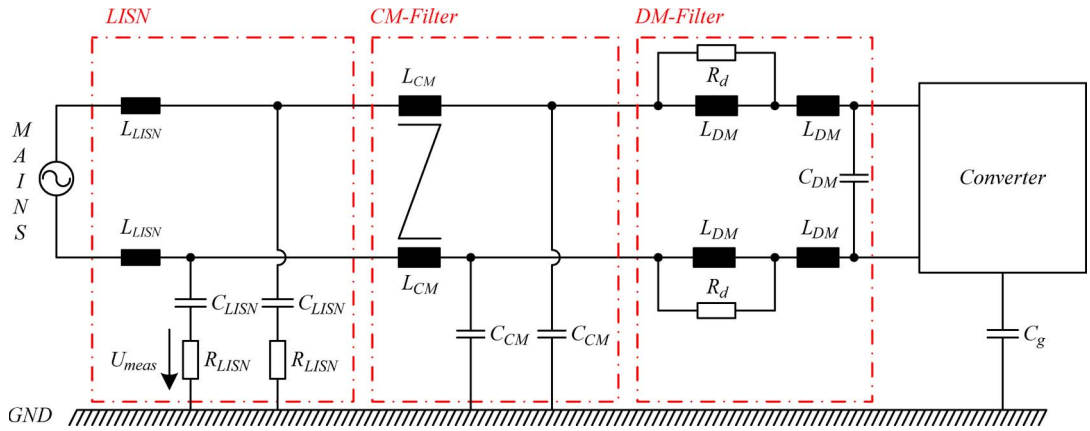

Fig. 10. DM and CM filter to attenuate high-frequency conducted noise emissions, which are measured at an LISN (for the sake of simplicity, only one DM and CM filter stage is shown and the LISN network is depicted in a simplified manner).

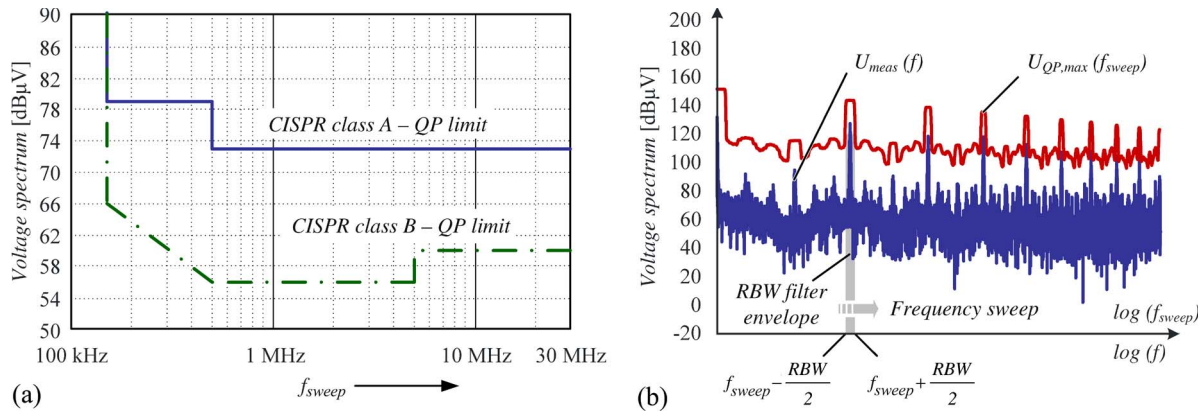

Fig. 11. (a) Limits for CE noise as defined in CISPR 22 [44] for QP detection. (b) Illustration of the QP measurement procedure.

of the boost switches and diodes have to be taken into account, which increase linearly with n. Thus, an optimal number of boost stages can be found for certain specifications, as will be illustrated in [22].

Generally, for the design of the input filter, it is important to distinguish between two different noise sources, namely, the DM and the CM noise [44], [47], [48]. Thus, also the filter design has to be split into these two steps. For converters with a diode bridge at the input, also so-called "mixed mode" (MM) noise occurs [49], [50], where CM current always flows only at one power line at a time due to the unidirectional behavior of the diode bridge and, consequently, appears partially as DM noise. Therefore, the DM filter inductances will be split and symmetrically arranged in both input lines, as shown in Fig. 10, in order to accommodate effectively the MM noise in combination with the DM capacitors [51], [52].

For the design of both filter parts, the EMC measurement equipment and procedure have to be taken into account. First, the high-frequency noise generated by the converter is measured at a line impedance stabilization network (LISN), which decouples the converter from the mains for high frequencies and defines the measurement impedance independently of the specific mains impedance. A simplified circuit of the LISN, which is connected to each input phase, is shown in Fig. 10. The voltage U_{meas} at the LISN resistance R_{LISN} is measured, filtered around a sweeping frequency [cf., Fig. 11(b)], and weighted by a quasi-peak (QP) detection network of an EMC test receiver. Details to the modeling of the measurement procedure can be found in [53]. A good worst case approximation for the measurement result [54], which appears in decibel microvolt and has to be compared with the limits given in the standards [cf., Fig. 11(a)], is given by

$$U_{\mathrm{QP,max}}(f_{\mathrm{sweep}})\ [\mathrm{dB}\mu\mathrm{V}] = 20 \cdot \log\left[\frac{1}{1\ \mu\mathrm{V}} \cdot \sum_{f=f_{\mathrm{sweep}}-\frac{\mathrm{RBW}}{2}}^{f=f_{\mathrm{sweep}}+\frac{\mathrm{RBW}}{2}} U_{\mathrm{meas}}(f)\right] \quad (36)$$

where f_{sweep} is the specific frequency of interest for a frequency sweep and RBW is the measurement band around f_{sweep}, which is defined in the standards [44] to be RBW = 9 kHz. This means that the sidebands of the switching frequency harmonics are also contributing to the measurement result. The fact that all frequency components are added linearly in (36) results in a worst case approximation of the result and therefore in a slightly overdimensioned filter. However, the exact modeling of the QP measurement process means a significantly larger mathematical effort [54].

The detected QP voltage depends on the converter topology, operation mode, operating point, and chosen switching frequency. For evaluation of (36) for a specific case, the voltage U_{meas} can be derived easily by a network simulation of the converter with the LISN and transferred into the frequency domain by Fourier analysis. Alternatively, if a converter prototype is already present, the QP detected voltage U_{QP} can be measured directly. In both cases, the result is compared with the noise limit $Limit(f_{\mathrm{sweep}})$ specified in the standards for the whole spectrum of f_{sweep} within 150 kHz–30 MHz [cf., Fig. 11(a)]. This results in an attenuation requirement

$$Att_{\mathrm{req}}(f_{\mathrm{sweep}})\ [\mathrm{dB}] = U_{\mathrm{QP,max}}(f_{\mathrm{sweep}})\ [\mathrm{dB}\mu\mathrm{V}] - Limit(f_{\mathrm{sweep}})\ [\mathrm{dB}\mu\mathrm{V}] + Margin\ [\mathrm{dB}] \quad (37)$$

which has to be provided by the inserted filter, including a margin to accommodate parameter tolerances and drift.

Based on this attenuation requirement, guidelines for the selection of the appropriate filter component values are given separately for the DM and the DM filter part in the following.

A. DM Input-Filter Design

Basically, the required filter attenuation $Att_{\mathrm{req,DM}}$ for a specific switching frequency f_{S} is achieved by an LC network of one or more stages, whereby the condition

$$Att_{LC}(f_{\mathrm{sweep}}) = (2\pi \cdot f_{\mathrm{sweep}})^{2n_{\mathrm{f}}} \cdot L_{\mathrm{DM}}^{n_{\mathrm{f}}} \cdot C_{\mathrm{DM}}^{n_{\mathrm{f}}} \quad (38)$$

with the number of filter stages n_{f} has to be fulfilled. As has been shown in [55], the selection of the same component values L_{DM} and C_{DM} for all filter stages leads to a minimal filter volume.

For converters with a constant switching frequency, it is sufficient to consider only the first multiple of the switching frequency (or the nth multiple for n interleaved boost cells) within the measurement range of 150 kHz–30 MHz as design point, while for variable switching frequency the highest attenuation requirement may appear at a different location and for the fulfillment of (38) the whole frequency range has to be considered.

The intentional variation of the switching frequency around its nominal value [47], [56]–[58] can lead to lower CEs typically in the range of about 10 dB [59]–[61] and, consequently, to a smaller filter volume. However, the frequency variation range has to be selected carefully, since very high frequencies may increase the power losses and low frequencies may coincide with the input-filter resonance frequency, which should be avoided by all means. Additionally, it has to be considered that the frequency variation also is associated with a higher control effort. Anyway, the following examinations are valid for both fixed and variable switching frequency, since only the attenuation requirement according to (37) is different and the subsequent volume optimization can be performed in the same manner.

It has to be stated that for very high switching frequencies ($f_{\mathrm{S}} > 500$ kHz), also the parasitics of L_{DM} and C_{DM} have to be taken into account, which is not done here for the sake of brevity [62].

In any case, (38) leads for a certain design point $f_{\mathrm{sweep}} = f_{\mathrm{D}}$ to

$$(2\pi \cdot f_{\mathrm{D}})^{2n_{\mathrm{f}}} \cdot L_{\mathrm{DM}}^{n_{\mathrm{f}}} \cdot C_{\mathrm{DM}}^{n_{\mathrm{f}}} = Att_{\mathrm{req,DM}}(f_{\mathrm{D}}). \quad (39)$$

For the DM-filter design, the relation between the filter inductances and capacitors is arbitrary as long as (39) is fulfilled. Therefore, a volume optimization utilizing volumetric parameters k_L, k_{L0}, k_C, and k_{C0} according to [22], [55] is possible and the total DM filter volume can be minimized

$$V_{\mathrm{DM}} = (n_{\mathrm{f}}+1) \cdot \left(k_L \cdot L_{\mathrm{DM}} \cdot \hat{I}_{\mathrm{in}}^2 + k_{L0}\right) + n_{\mathrm{f}} \cdot \left(k_{\mathrm{c}} \cdot C_{\mathrm{DM}} \cdot \hat{U}_{\mathrm{in}}^2 + k_{C0}\right) \rightarrow \min. \quad (40)$$

The term $(n_{\mathrm{f}}+1)$ for the number of inductors is due to a passive damping network, which is inserted for the filter stage at the converter input (cf., Fig. 10) and which is realized by the same inductor value as the filter inductors [55]. The damping resistor R_{d} can be selected in an optimal way according to [54]. The required inductance value L_{DM} is split into two equal parts to provide symmetrical conditions for the CM noise propagation. In order to achieve a realistic design, the volumetric parameters k_L and k_C should represent the boxed volumes of the components.

By combining (38) and (40), the component values of filters with minimal volume can be found for the design point, i.e., a certain frequency f_{sweep} [cf., Fig. 12(a)], in dependence on the specific operation mode, the switching frequency, and the number of filter stages n_{f}

$$L_{\mathrm{DM}} = \frac{\sqrt[2n_{\mathrm{f}}]{Att_{\mathrm{req,DM}}}}{2\pi \cdot f_{\mathrm{D}}} \cdot \sqrt{\frac{n_{\mathrm{f}} \cdot \left(k_{\mathrm{c}} \cdot \hat{U}_{\mathrm{in}}^2 + k_{C0}\right)}{(n_{\mathrm{f}}+1) \cdot \left(k_L \cdot \hat{I}_{\mathrm{in}}^2 + k_{L0}\right)}} \quad (41)$$

$$C_{\mathrm{DM}} = \frac{\sqrt[2n_{\mathrm{f}}]{Att_{\mathrm{req,DM}}}}{2\pi \cdot f_{\mathrm{D}}} \cdot \sqrt{\frac{(n_{\mathrm{f}}+1) \cdot \left(k_L \cdot \hat{I}_{\mathrm{in}}^2 + k_{L0}\right)}{n_{\mathrm{f}} \cdot \left(k_c \cdot \hat{U}_{\mathrm{in}}^2 + k_{C0}\right)}}. \quad (42)$$

This leads to the DM filter volume

$$V_{\mathrm{DM}} = \frac{\sqrt[2n_{\mathrm{f}}]{Att_{\mathrm{req,DM}}}}{\pi \cdot f_{\mathrm{D}}} \cdot \sqrt{(n_{\mathrm{f}}+1) \cdot \left(k_L \cdot \hat{I}_{\mathrm{in}}^2 + k_{L0}\right)} \cdot \sqrt{n_{\mathrm{f}} \cdot \left(k_c \cdot \hat{U}_{\mathrm{in}}^2 + k_{C0}\right)}. \quad (43)$$

In Fig. 12, the design procedure is shown for the boost converter at hand for dual-interleaved ($n = 2$) DCM operation (for $U_{\mathrm{in,rms}} = 230$ V, $U_0 = 400$ V, $P_0 = 300$ W). The attenuation requirement according to (37) is shown in Fig. 12(a)

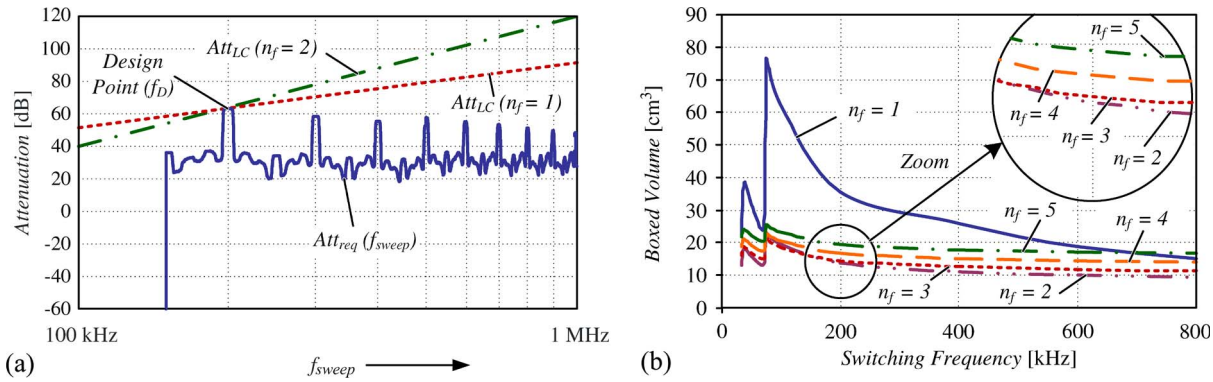

Fig. 12. Exemplary DM filter design curves for a 300 W boost converter in dual DCM operation. (a) Required filter attenuation curve $Att_{\mathrm{req,DM}}$ compared with the attenuation Att_{LC} provided by the LC filter with $f_{\mathrm{S}} = 50$ kHz. (b) DM filter boxed volume curves for different number of filter stages n_{f} in dependence on the switching frequency.

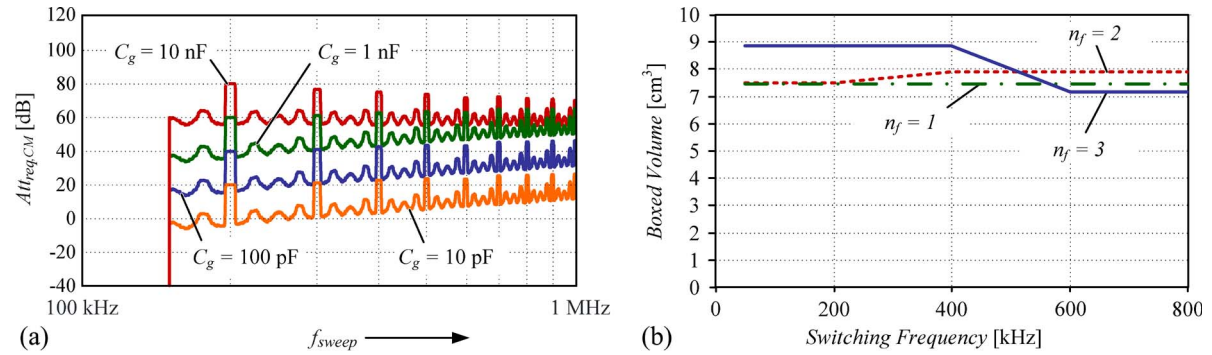

Fig. 13. Exemplary CM filter design curves for a 300-W boost converter in dual DCM operation. (a) Required filter attenuation curve $Att_{\mathrm{req,CM}}$ in dependence on the parasitic capacitance to ground with $f_{\mathrm{S}} = 50$ kHz. (b) CM filter boxed volume curves ($C_{\mathrm{g}} = 100$ pF) for different number of filter stages n_{f} in dependence on the switching frequency.

exemplarily for a switching frequency of $f_{\mathrm{S}} = 50$ kHz along with the attenuation curve, which is achieved by the inserted LC filter. With the optimal filter component values according to (41) and (42), the resulting volumes according to (43) in dependence of the switching frequency are shown in Fig. 12(b). It can be seen that a selection of only one filter stage results in a significantly higher total filter volume than for higher number of filter stages, whereby three or more filter stages generally no longer lead to a noticeable volume decrease (in fact, as the detailed zoom in Fig. 12(b) shows, the total volume typically even increases for $n_{\mathrm{f}} > 3$). The reason for this behavior lies in the inductor volume offset factor k_{L0}, which accounts for the fact that cores with smaller inductance are characterized by a larger volume-to-inductance ratio than larger cores [22], and the capacitor volume offset factor k_{C0}, which is typically of minor practical importance.

B. CM Input-Filter Design

For the design of the CM filter, there are two main differences as compared to the DM filter design.

1) First, a linearization and/or parameterization of the volume curves is not possible for most of the commercially available CM chokes.
2) Second, the maximum CM capacitance is limited by the maximum allowed total leakage current to ground $I_{\mathrm{GND,max,rms}} = 3.5$ mA [63] at 110% of the rated rms mains voltage. With the same capacitance values being employed for all filter stages n_{f} between both power lines to ground, the maximum CM capacitance value is generally given by

$$C_{\mathrm{CM}} \leq \frac{1}{2n_{\mathrm{f}}} \cdot \frac{I_{\mathrm{GND,max,rms}}}{1.1 \cdot U_{\mathrm{in,rms}} \cdot \omega}. \tag{44}$$

The CM filter inductance value is determined by the required attenuation $Att_{\mathrm{req,CM}}$, which can be evaluated in a similar manner as for the DM filter design. However, for the CM filter, the attenuation is mainly determined by the lumped parasitic capacitance of the converter components to ground C_{g} [cf., Figs. 10 and 13(a)], which depends on various parameters, such as mechanical assembling of the semiconductors, the heat sink and/or the cold plate, and the load. Since the assessment of the capacitance by electromagnetic finite element method simulations is associated with a very high modeling effort and uncertainties, a common approach is the impedance measurement on a test prototype. In combination with the CM noise voltage source, this parasitic capacitance leads to the required CM noise attenuation $Att_{\mathrm{req,CM}}$ [64]. The filter inductance is then given by

$$L_{\mathrm{CM}} = \frac{1}{(2\pi \cdot f_{\mathrm{D}})^2 \cdot C_{\mathrm{CM}}} \cdot \sqrt[n_{\mathrm{f}}]{Att_{\mathrm{req,CM}}}. \tag{45}$$

Preferably, the CM inductance L_{CM} should be built up with a single layer winding construction in order to reduce

the parasitic capacitances and to improve the high-frequency behavior of the CM choke [47], [65].

The total CM filter volume can be calculated in the same manner as for the DM filter by volumetric parameters [22], [55]. Exemplarily, again for the boost converter with dual-interleaved $(n = 2)$ DCM operation, the volume curves in dependence on the switching frequency are shown in Fig. 13(b) (for $U_{\mathrm{in,rms}} = 230$ V, $U_0 = 400$ V, $P_0 = 300$ W, $C_{\mathrm{g}} = 100$ pF). It can be seen that for practically the whole switching frequency range, a single-stage filter is sufficient and characterized by the smallest volume. The reason is that for this case already, the smallest available CM cores [66] provide a high inductance value and sufficient attenuation together with the CM capacitances, respectively. For cases of higher CM noise emissions and/or higher capacitance to ground, a multistage CM filter may eventually lead to a smaller volume.

V. Conclusion

In this paper, design guidelines for a single-phase PFC have been presented, whereby the focus has been put on a minimal total volume, as this is the main requirement for integrated systems, such as pumps, fans, handheld tools, and drilling machines. Thus, the design of the components, which are mainly determining the power density, has been discussed intensively, namely

1) the boost inductor(s);
2) the output capacitor;
3) and the EMI input filter.

For the design of these components, the operating mode of the converter is of crucial importance. Here, for achieving the targeted high compactness of the system, CCM and DCM have been selected as promising control concepts and evaluated comparatively. Furthermore, the effect of interleaving of two or more boost stages and the influence of the switching frequency on the volume of each PFC component have been analyzed in detail.

The presented design considerations indicate that only an overall optimization taking the all before-mentioned issues into account leads to a PFC with minimal volume. In a subsequent paper [22], a suchlike design will be carried out exemplarily for a 300-W PFC.

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Thomas Nussbaumer (S'02–M'06) was born in Vienna, Austria, in 1975. He received the M.Sc. degree (with honors) in electrical engineering from the University of Technology Vienna, Vienna, Austria, in 2001, and the Ph.D. degree from the Power Electronic Systems (PES) Laboratory, Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland, in 2004.

From 2001 to 2006, he was with the PES, where he conducted research on modeling, design, and control of three-phase rectifiers, power factor correction techniques, and electromagnetic compatibility. Since 2006, he has been with Levitronix GmbH, Zürich, Switzerland, where he is currently working on bearingless motors, magnetic levitation, and permanent-magnet motor drives for the semiconductor and biotechnology industry. His current research is focused on compact and high-performance mechatronic systems including novel power electronics topologies, control techniques, drive systems, sensor technologies, electromagnetic interference (EMI), and thermal aspects.

Klaus Raggl (M'06) was born in Zams, Austria, in 1980. He received the M.Sc. degree in mechatronics from Johannes Kepler University Linz, Linz, Austria, in 2005, and the Ph.D. degree from the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH), Zürich, Switzerland, in 2009. During his Ph.D. studies, he worked on bearingless pump systems with high power density in the Drive Technology and Magnetic Bearings Section.

Since April 2009, he has been with Hilti AG, Schaan, Liechtenstein, where he is currently working on high-performance drilling and demolition machines.

Johann W. Kolar (M'89–SM'04) received the Ph.D. degree (*summa cum laude/promotio sub auspiciis praesidentis rei publicae*) from the University of Technology Vienna, Austria.

Since 1984, he has been an Independent International Consultant in close collaboration with the Vienna University of Technology, in the fields of power electronics, industrial electronics, and high-performance drives. On February 1, 2001, he was appointed as a Professor and Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH), Zürich, Switzerland. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the VIENNA rectifier and the three-phase ac–ac sparse matrix converter. He has published over 300 scientific papers in international journals and conference proceedings. He is the holder of 75 patents. His current research is on ac–ac and ac–dc converter topologies with low effects on the mains, e.g., for power supply of telecommunication systems, more electric aircraft, and distributed power systems in connection with fuel cells. His other main areas of research include the realization of ultracompact intelligent converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multidomain/multiscale modeling and simulation, pulsed power, bearingless motors, and power MEMS.

Dr. Kolar is a member of the Institute of Electrical Engineers of Japan (IEEJ) and the technical program committees of numerous international conferences in the field (e.g., Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 to 2000, he served as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and since 2001, as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. Since 2002, he has been an Associate Editor for the *Journal of Power Electronics* of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ *Transactions on Electrical and Electronic Engineering*. He was the recipient of the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005 and an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003. In 2006, the European Power Supplies Manufacturers Association awarded the Power Electronics Systems Laboratory of ETH Zürich as the leading academic research institution in Europe.