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A 120 °C Ambient Temperature Forced Air-Cooled Normally-off SiC JFET Automotive Inverter System

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A 120 °C Ambient Temperature Forced Air-Cooled Normally-off SiC JFET Automotive Inverter System

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***Abstract*—The degree of integration of power electronic converters in current hybrid electric vehicles can be increased by mitigation of special requirements of these converters, especially those regarding ambient air and cooling fluid temperature levels. Today, converters have their own cooling circuit or are placed far away from hot spots caused by the internal combustion engine and its peripheral components. In this paper, it is shown, how the use of SiC power semiconductors operated at a junction temperature of 250 °C and active control electronics cooling employing a Peltier element can help to build an air-cooled inverter system for 120 °C ambient temperature.**

First, a detailed analysis of the operating temperature ranges of power semiconductors, thermal interface materials, capacitors and control electronics is conducted. Then, concepts for deriving a converter design that takes the electrical, mechanical and thermal requirements of the components and their interaction into account are shown. The inverter and the active Peltier cooling of the control electronics are dimensioned. Finally, a hardware prototype with discrete power semiconductor devices and thus with a junction temperature limit of 175 °C is shown to validate the theoretical considerations.

I. Introduction

Power electronic converters are used in Hybrid Electric Vehicles (HEVs) to drive the electrical machine in the vehicle's drive train or to supply electrical energy to loads on different voltage levels from a high voltage traction battery. Actual converters feature Silicon (Si) power semiconductors and thus their junction temperature is subjected to an upper temperature limit between 150 °C and 175 °C [1] due to the high intrinsic charge carrier concentration of Si [2].

In order to effectively remove the heat dissipated by the power semiconductor switches, a sufficiently large temperature difference between the semiconductor junction, where the switching and conduction losses of the switches occur, and the coolant, typically a glycol-water mixture, has to be maintained. That is, the temperature of the coolant for the power electronic converter has to be well below the temperature level of the cooling circuit of the internal combustion engine (ICE) which can be as high as 125 °C [3] and thus today two separate water-glycol circuits are needed. The previous and actual generations of the Toyota Hybrid Synergy Drive used for most of the Toyota and Lexus HEVs can be given as an industrial example of this concept [4]–[6].

With Silicon Carbide (SiC), a new material that can be used for power semiconductor switches has become available and SiC switches are capable of significantly higher operating temperatures above 400 °C [7]. Novel joining and bonding technologies such as low-temperature sintered silver die attachment and copper bonding instead of aluminium bonding are currently investigated and promise considerably improved reliability for thermal cycling with increased temperature swing [8], [9]. This makes the separation of the cooling circuits obsolete as the junction temperature can be increased beyond 175 °C and thus a significant temperature difference to the coolant at 125 °C can be established [10]. Furthermore, alternative cooling concepts such as pure air-cooling even in hot environments become feasible. Ambient-air-cooled converter systems can reduce the overall system complexity compared to water cooling as no pumps, water pipes, the water-glycol fluid itself and heat exchangers are needed. Hence, the flexibility in arranging the converters within the vehicle is increased, thus helping to develop novel car concepts.

Air-cooled power electronic converters can already be found in current HEVs, e. g. in the 2006 Honda Civic Hybrid model. As these drive inverters still feature Si power semiconductors, the ambient air used for cooling needs to be of low temperature. Hence, the gain in arrangement flexibility is not as high as with SiC as they cannot be placed, for example, in the engine compartment. (For the Honda Civic, it is placed behind the rear seat to make sure the ambient air level is low [11], [12] — in contrast to many other HEVs, such as the Toyota Prius or Lexus RX 400h Model, where the low-temperature-water-cooled converter is placed in the engine compartment.) Fig. 1 gives an overview over the different temperature levels in cars having an ICE.

Table I summarizes the specifications of the 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system.

TABLE I
Overview over inverter system specifications.

Dimension	Value	Unit
Maximum Inverter Output Power	10	kW
Maximum Ambient Temperature	120	°C
Maximum Power Semiconductor Junction Temp. (for first prototype with discrete devices)	175	°C
Maximum Power Semiconductor Junction Temp. (for design process)	250	°C
DC-Link Voltage	700	V
Switching Frequency	50	kHz

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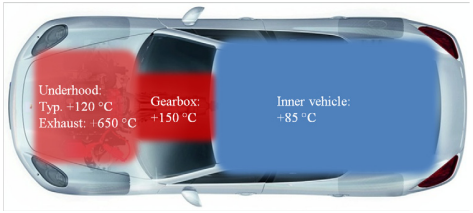

Fig. 1. Typical ambient temperature level specifications in vehicles with an internal combustion engine [13], [14].

In this paper, an ambient-air-cooled, high power density SiC inverter system for an ambient temperature of $120\,^{\circ}\mathrm{C}$ is analyzed. The employed power semiconductors are SemiSouth 1200 V 30 A SiC normally-off Junction-Field-Effect-Transistors (JFETs) with a very low on-resistance of $50\,\mathrm{m\Omega}$. Infineon 1200 V SiC diodes with a current rating of 15 A are connected antiparallel to the switches. In order to be able to fully utilize the semiconductors, the converter's construction is designed for a maximum junction temperature of $250\,^{\circ}\mathrm{C}$ [15]. To keep the output current and thus the chip size related costs low, the DC-link voltage is chosen to 700 V, which is similar to actual HEVs [1]. The optimized switching frequency of 50 kHz covers a broad range of possible industrial applications and output frequencies and keeps the volume and weight of passive filter components, such as common mode inductances, low.

Besides the SiC power semiconductors, a DC-link capacitor, a current, voltage and temperature measurement, control electronics, an auxiliary power supply and heat sinks with fans to cool the power semiconductors are the main critical components needed for the realization of the converter system. The main challenge in designing the inverter system for an ambient temperature of $120\,^{\circ}\mathrm{C}$ and a maximum junction temperature of $250\,^{\circ}\mathrm{C}$, addressed in this paper, is to make sure that the individual devices are operated within their specified temperature ranges by placing and, if necessary, active cooling of the components.

After a short overview over the allowed operating temperatures of the different components in Section II, the inverter system is designed in Section III and possible placing solutions of the power semiconductors, the heat sinks, the fans, the control electronics and the DC-link capacitors are analyzed with respect to power density and modularity. It is shown that in any case an active cooling of the control electronics is needed. The optimization of the design of the Peltier cooling with respect to volume and power consumption is shown in Section IV using a detailed thermal equivalent circuit diagram.

II. Allowable Operating Temperature Ranges of Inverter System Components

To consider different inverter designs and possible component placings, it has to be analyzed first, for which temperature levels the components needed are available. Fig. 2 gives an overview over the operating temperature ranges. Often, there are devices for specialized industries such as military, off-shore downhaul or aerospace applications available that

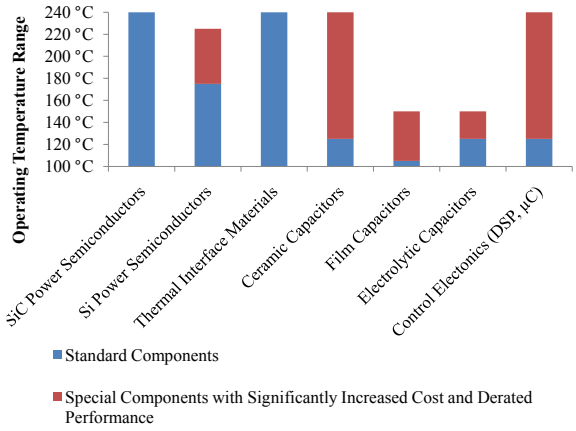

Fig. 2. Overview over operating temperature ranges of the main components of the investigated inverter system. The significantly derated performance of special components refers to the much higher on-resistance of Silicon-on-insulator-type Si power semiconductors, the much lower energy density of high temperature capacitors or the limited signal processing capability of high temperature DSPs.

have partially significantly extended operating temperature ranges at the expense of performance or functionality loss. The high temperature power FET technology by Honeywell can exemplify this: The n-channel FET is fabricated using a Silicon-On-Insulator (SOI) process in order to reduce the leakage currents at high temperatures. The device is rated up to $225\,^{\circ}\mathrm{C}$, i. e. the device shows significantly higher upper temperature limits than conventional Si power semiconductors (*cf.* Section I) [16]. Disadvantageous are the higher component costs and the derated performance of the device, e. g. in terms of the chip area specific on-resistance, which is with $43\,\mathrm{m\Omega cm^2}$ in the same range than the specific on-resistance of conventional Si power semiconductors, that have an order of magnitude higher blocking voltage (55 V compared to 650 V) [17]. Against the background of industrial practicability, no special components with derated performance will be chosen for this inverter system.

III. Design of Inverter System with Active Electronics Cooling

The first prototype of the inverter system is designed for and built with discrete power semiconductor devices with an upper junction temperature limit of $175\,^{\circ}\mathrm{C}$ in Section III-A. Therefore, the system will be operated either at the nominal ambient temperature of $120\,^{\circ}\mathrm{C}$ with reduced output power or at the nominal power level of 10 kW at reduced ambient temperature. The arrangement of the main components and the thermal design of the encapsulation of the control and gate drive electronics is conducted for power semiconductors with junction temperatures up to $250\,^{\circ}\mathrm{C}$, as will be shown in Section III-C. This makes it possible to replace the discrete power semiconductors with a customized power semiconductor module having a junction temperature limit of $250\,^{\circ}\mathrm{C}$ in a second step while maintaining the concepts developed in this paper. That converter will be shown to operate at both, nominal ambient temperature and power level.

A. Choice of Power Semiconductors

Currently, the main research and development focus concerning unipolar SiC devices is on Schottky Barrier Diodes (SBDs), Metal-Oxide-Semiconductor-FETs (MOSFETs) as well as normally-on and normally-off Junction-FETs (JFETs). While SiC Schottky diodes have already been commercially available for a few years (by Cree, Infineon and SemiSouth) and are now increasingly deployed in applications where the absence of any reverse recovery charge can significantly improve converter performance indices, SiC MOSFETs are not yet commercially available. The main issues are a low electron mobility at the channel surface and gate oxide reliability uncertainties [18], [19].

Considering the available SiC JFETs, in particular enhancement mode (EM) SiC JFETs are of interest. In contrast to normally-on JFETs, no safety concerns for voltage source converters occur because the EM SiC JFET is a truly normally-off device and blocks its nominal drain-source voltage at zero gate-source voltage. Nevertheless, it still features a pure SiC solution with all of its benefits (especially regarding high temperature operation capability) compared to cascode approaches using a Si MOSFET connected in series to the SiC JFET, which additionally brings up the question of matching the right MOSFET to the JFET [18]. Furthermore, the available normally-off device shows superior performance in terms of drain-source on-resistance per chip area ($2.8\,\mathrm{m\Omega cm^2}$ for a 1200 V device). The 1200 V 30 A normally-off JFET has been commercialized by SemiSouth Laboratories, Inc. in 2009 [20].

To be able to choose the power semiconductor switches and diodes employed in this inverter system, the requirements with respect to voltage and current ratings have to be analyzed.

For a specified DC-link voltage of 700 V, semiconductor devices with a maximum blocking voltage of 1200 V are chosen in order to include a safety margin in case of occurring overvoltages.

A significant advantage of employing unipolar switches is their ability to conduct currents in forward and reverse direction through their channel. SiC Schottky diodes have a large voltage drop of more than 1 V, i. e. the channel can be turned on during the freewheeling interval and the load current can flow through the channel of the switch. This avoids large currents and thus large power losses in the diode so that each diode is only used during the dead-time interval of the respective half-bridge.

The instantaneous value of the output phase current i_{ph} is the sum of the instantaneous current i_{DS} of the respective high- and low-side switch (*cf.* Fig. 3). During steady state converter operation, the rms values of the high- and low-side switches are the same for symmetric modulation schemes. Apart from currents charging the parasitic capacitances of the switches during the switching transients, the switches do not conduct currents at the same time and hence

$$I_{\mathrm{DS}} = \frac{I_{\mathrm{ph}}}{\sqrt{2}} \tag{1}$$

applies for the rms values.

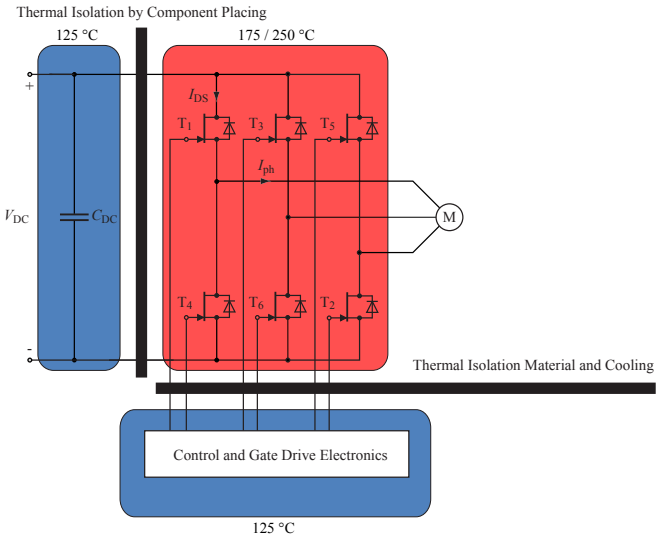

Fig. 3. Concept of thermal design of high temperature inverter system: The DC-Link capacitors with an upper temperature limit of 125 °C are thermally isolated from the hot power semiconductors (junction temperature up to 250 °C) by placing them below the heat sinks (distance: 45 mm). The control electronics need to be very close to the gate connections of the switches to allow fast switching and low switching losses. Thus, a special thermally isolating material is used to isolate the control electronics from the hot switches. Additionally, the electronics are actively cooled by a Peltier cooler.

The correlation between the real output power P of the 3-phase inverter and I_{ph} is

$$P = 3 \cdot U_{\mathrm{ph}} I_{\mathrm{ph}} \cos\varphi \tag{2}$$

where U_{ph} denotes the rms value of the output phase voltage and $\cos\varphi$ the phase shift between U_{ph} and I_{ph}.

PWM modulation with third order harmonic injection or space vector modulation leads to a maximum modulation index of $m = \frac{2}{\sqrt{3}}$ for sinusoidal output phase voltages and thus, the amplitude $\hat{U}_{\mathrm{ph}}$ of the phase voltage is

$$\hat{U}_{\mathrm{ph}} = m \cdot \frac{U_{\mathrm{DC}}}{2} = \frac{2}{\sqrt{3}} \frac{U_{\mathrm{DC}}}{2} \tag{3}$$

with U_{DC} being the DC-link voltage of the voltage source inverter. Hence, I_{ph} can be calculated according to

$$I_{\mathrm{ph}} = \frac{P}{\sqrt{3}\frac{U_{\mathrm{DC}}}{\sqrt{2}} \cos\varphi} \tag{4}$$

with (2) and (3). With (1) it follows for the load current of each switch

$$I_{\mathrm{DS}} = \frac{P}{\sqrt{3} U_{\mathrm{DC}} \cos\varphi} = 10.3\,\mathrm{A} \tag{5}$$

with an assumed phase shift factor of $\cos\varphi = 0.8$.

The normally-off JFET is available in a TO-247 discrete package with a single $4.5\,\mathrm{mm^2}$ die having a nominal on-resistance of $100\,\mathrm{m\Omega}$ at room temperature and two dies of the same size in parallel cutting also the on-resistance in half. For this design, the $50\,\mathrm{m\Omega}$ switch is chosen as this promises increased efficiency while keeping the package and thus volume constant.

The switches are operated at their maximum junction temperature of 175 °C. For a drain current of 10 A, the measured drain-source on-resistance of a switch with 37 mΩ at 25 °C and a gate current of 25 mA increases at 175 °C to 113 mΩ at a gate current of 100 mA [21]. As the maximum specified on-resistance of these switches is with 50 mΩ at room temperature 35% higher than for the measured switch, this additional margin has to be considered for the conduction loss calculation in order to make sure, that this calculation covers the highest possible on-resistance of the switch leading to $R_{\mathrm{DS,on}} = 153\,\mathrm{m\Omega}$. Hence, the conduction loss for one of the six switches in the inverter under full-load condition at 175 °C can be calculated to

$$P_{\mathrm{C}} = I_{\mathrm{DS}}^2 \cdot R_{\mathrm{DS,on}} = 16\,\mathrm{W}. \tag{6}$$

The total switching energy E_{S} for a switch in a half-bridge setup with an inductive load has been measured for different junction temperatures, DC-link voltages and load currents in [15]. For 175 °C, a current of 10 A and a switching frequency of $f_{\mathrm{S}} = 50\,\mathrm{kHz}$ the switching loss for a single switch is calculated to

$$P_{\mathrm{S}} = f_{\mathrm{S}} \cdot E_{\mathrm{S}} = 20\,\mathrm{W}. \tag{7}$$

B. DC-link Capacitor

Important characteristics of the DC-link capacitor for this inverter system include the DC voltage, current ripple and ambient temperature it can withstand as well as the capacitance needed.

A comprehensive study of the available capacitors (foil, ceramic and electrolytic capacitors) for 120 °C ambient temperature revealed, that film capacitors suffer from significantly derated withstand voltage (between $4\,\frac{\mathrm{V}}{\mathrm{K}}$ and $8\,\frac{\mathrm{V}}{\mathrm{K}}$) as soon as the temperature rises above 85 °C. If the voltage at high ambient temperature is half of the nominal voltage, four capacitors are needed to achieve the same capacitance as the capacitance is cut in half by a series connection of capacitors. Ceramic capacitors suffer from capacitance derating at high ambient temperatures and at high DC voltages. Furthermore, they have a low capacitance per device, leading to a high number of devices needed while the reliability of the devices is questioned due to cracks occurring at the caps. Therefore, electrolytic capacitors are considered for this inverter system.

The required DC voltage rating is given by the DC-link voltage of the inverter system (700 V) and the ambient temperature is 120 °C. The capacitance is given by the allowed DC-link voltage variation depending on capacitor current and switching frequency, by the duration of a supply failure that has to be compensated as well as the dynamic response of the supply to load variations and is chosen to 50 μF. The most essential parameter for choosing the right electrolytic capacitor is the rms value of the ripple current I_C, that can be calculated by

$$I_C = \frac{P}{\sqrt{3}\frac{V_{\mathrm{DC}}}{\sqrt{2}}\cos\varphi}\sqrt{2m\frac{\sqrt{3}}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{116}m\right)} = 8.4\,\mathrm{A} \tag{8}$$

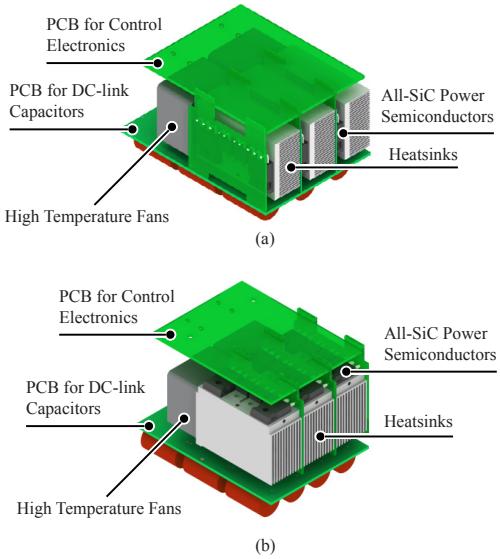

Fig. 4. Considered arrangement of SiC power semiconductors, heatsinks, fans, control and DC-link capacitor PCBs. The advantages of (a) are such that the hot power semiconductors are not placed close to the control electronics or DC-link capacitors. The disadvantage is the 10% higher thermal resistance of (a) compared to (b) for the same overall volume. Hence, the setup according to (b) is chosen for this inverter system.

for $\cos\varphi = 0.8$ and $m = 0.68$, which is the value where the maximum current ripple occurs for $\cos\varphi = 0.8$ [22]. The Epcos electrolytic capacitor B43693A2476 with 47 μF, a DC voltage of 250 V and a ripple current capability of 3.38 A at 125 °C is chosen: Three are connected in series and 4 in parallel, leading to a capacitance of 63 μF and 13.5 A ripple current capability. The volume consumed by the 12 capacitors is 0.19 l.

C. Arrangement of Main Components

The arrangement of the main components of the inverter system is subject to certain, partially conflicting, electrical and thermal constraints.

First, the setup is furthermore required to be symmetrical with respect to the gate drive inductances of the three half-bridge legs in order to facilitate equal switching times and hence equal switching losses. The air flow cooling the power semiconductors has also to be symmetrical to make sure that the thermal resistance of the power semiconductor switches and diodes, respectively, is equal.

Second, the connections between the power semiconductors and the control electronics including the gate driver as well as between the power semiconductors and the DC-link capacitors have to be of very low inductance in order to allow fast switching without excessive gate ringing [21] and low oscillations on the DC-link voltage.

Third, the main components operate at significantly different temperature levels, as can be seen from Fig. 2. The SiC power semiconductor switches and diodes have to be operated at junction temperatures up to 250 °C under full load conditions in order to fully utilize them at ambient temperatures of 120 °C [15]. The temperature of the power semiconductor package surfaces that are not aligned to the heatsink surfaces

(i. e. the top side and shoulders of the package) is very close to the junction temperature of the semiconductor as the thermal resistance from this surface to the surrounding air is significantly higher than from the junction to the surface. The upper temperature limit of the control electronics and DC-link capacitors that are available as standard components is 125 °C. Hence, it has to be made sure, that the required temperature drop of 125 °C from the power semiconductors to the control electronics and DC-link capacitors is maintained.

Fig. 4 shows two of the considered setups. In Fig. 4 (a) the power semiconductors are mounted vertically on heatsinks with horizontal fins, whereas in Fig. 4 (b) the switches and diodes are mounted horizontally on heatsinks with vertical fins. The dimensions of both concepts are given by the area of the power semiconductor packages and the height of the cooling fans. The semiconductors of a bridge leg are assembled adjacent to each other in a row, determining the length of the heatsink. Two Sanyo Denki San Ace 40 GV fans are selected due to their superior volume flow over static pressure characteristics and match with a width of 80 mm the width of the three bridge legs in Fig. 4 (b).

The PCBs for the control electronics and the DC-link capacitors are mounted on top and underneath the composite consisting of power semiconductors, heatsinks and fans. It is also possible to place both together either on top or underneath the heatsinks. They cannot be placed directly in front or behind the fans or heatsinks though, as they would then impede the air flow leading to a higher pressure for the fan and thus to a higher thermal resistance from the power semiconductor junction to the ambient. If they are placed at the sides of the heatsinks in parallel to the fins, a symmetrical connection to the three half-bridge legs will not be possible.

The advantage of the concept in Fig. 4 (a) over Fig. 4 (b) is the fact that the power semiconductor packages with surface temperatures close to 250 °C are not placed directly underneath the control electronics PCB. Furthermore, the air flow generated by the fans makes sure, that the surface of the packages as well as the pins are cooled so that only a negligible amount of heat is fed into the connecting PCB and thus to the gate driver and DC-link capacitors. Hence, the dissipated power is not directly induced into the control electronics PCB while the gate driver and DC-link parasitic inductances are the same for both concepts.

Finally, Fig. 4 (b) is chosen for this inverter system because of the 10% lower thermal resistance of this arrangement for equal volume. As can easily be seen, the length of the fins has to be decreased for version (a) and the baseplate area of the heatsinks is not fully utilized as it is so large (60 mm · 44 mm) compared to the area consumed by the power semiconductors ($4 \cdot 4.5\,\mathrm{mm}^2$ JFET area and $2 \cdot 8\,\mathrm{mm}^2$ diode area) that the outer fins of the heatsink do not contribute significantly to the cooling.

In the final concept of Fig. 4 (b), the DC-link capacitor board is placed underneath the heatsinks. The bottom end of the heatsinks has got a temperature of +10 °C to +20 °C (depending on whether the junction temperature is 175 °C or 250 °C) above ambient temperature level. PCBs with broad (60 mm) and close (distance between a pair of tracks only 0.5 mm) tracks make sure, that the connection has got a low parasitic inductance. The thermal management of the control electronics is described in the following chapter Section IV.

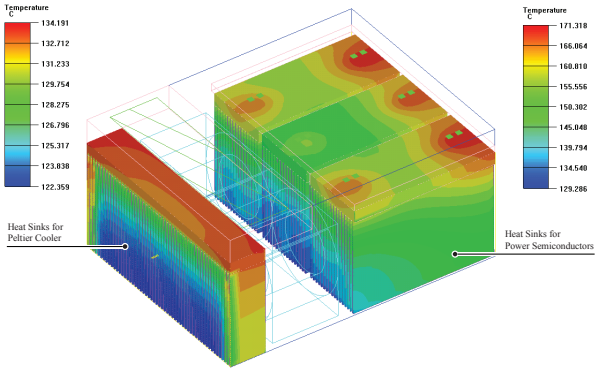

Fig. 5. Thermal simulations of the cooling of the power semiconductors and the Peltier element. The ambient temperature is 120 °C, the junction temperature of the power semiconductors is set to 250 °C (relevant operating point for the design of the electronics cooling) and the power dissipated by the Peltier element is 50 W.

D. Design of Power Semiconductor Heatsinks

An optimum fin geometry can be calculated for the physical dimensions of the heatsink derived in Section III-C and the chosen fan [23]. The results of this optimization for an aluminium heatsink with a width of 80 mm (thus matching the cross-section of two fans) and a length of 83 mm (62 mm for the heat sink of the power semiconductors and 21 mm for the heatsink of the Peltier element) are as follows: The minimum thermal resistance $0.14\,\frac{\mathrm{K}}{\mathrm{W}}$ can be achieved for 46 fins, that have got a thickness of 0.52 mm. Such thin fins can be manufactured by wire eroding. In this case, the heatsink are milled and thus the thickness is subject to a lower limit of 0.9 mm to avoid destruction of the fin during machining. The spacing is limited to values larger than 1.6 mm as due to the availability of saw blades with a thickness of larger or equal 1.6 mm and a diameter of more than 40 mm. This leads to a number of 30 fins and a thermal resistance for this heatsink of $0.15\,\frac{\mathrm{K}}{\mathrm{W}}$. Due to a rather flat optimum of the thermal resistance, the thermal resistance increases only by 10% even though the number of fins is reduced by a factor of more than 1.5. The thermal resistance of each of the three heatsinks for the power semiconductors depicted in Fig. 4 is then calculated to $3 \cdot \frac{83\,\mathrm{mm}}{62\,\mathrm{mm}} \cdot 0.15\,\frac{\mathrm{K}}{\mathrm{W}} = 0.6\,\frac{\mathrm{K}}{\mathrm{W}}$. The resulting temperature distribution for the heatsink of the Peltier element and the power semiconductor is simulated with Icepak and shown in Fig. 5.

IV. Electronics Cooling

A. Concept of Electronics Box

For the control electronics with an upper temperature limit of 125 °C, that are according to Fig. 4 (b) placed directly above the hot power semiconductors and heatsink baseplate, a thermal isolation concept is developed. The key ideas of this

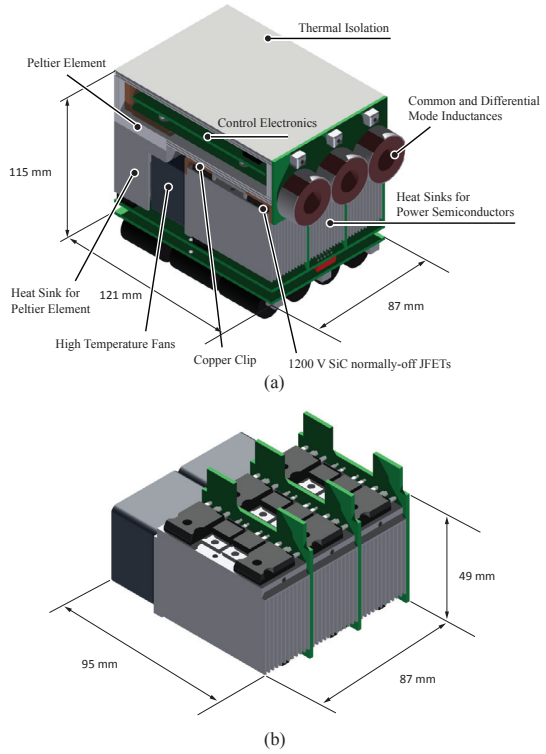

Fig. 6. (a) CAD representation of complete investigated inverter system. The overall volume including DC-link capacitors and active control electronics cooling is 1.2 l. (b) CAD representation of power part of the inverter system with a volume of 0.4 l.

concept are shown in Fig. 7. The hot surface of the power semiconductors as well as their gate and source connections cause a heat input into the control board. Additionally, heat is dissipated by the control electronics (e. g. by the DSP and the gate drivers delivering 100 mA at a voltage level of 3 V to each switch during its on-state). At the same time, it has to be assumed as a worst case scenario in the later arrangement within the HEV, that the converter is encapsulated such that the control electronics have got a very high thermal resistance to the 120 °C ambient. As the allowed temperature drop is only 5 °C, the power that could be conducted to the ambient is very limited compared to the heat input. Therefore, an active cooling of the control electronics is needed. For this purpose, the control electronics are encapsulated in a thermally isolating box and are cooled to a temperature level of 120 °C by a Peltier element. The heat dissipated by the Peltier element is fed into a heatsink. Ambient air (120 °C) is sucked through this heat sink for the Peltier element by the fan located in between the heat sinks for the Peltier element and the power semiconductors, respectively. Then, the air slightly heated up by the Peltier element heat sink is blown through the heat sinks of the power semiconductors.

To limit the electrical power that has to be fed into the Peltier element, the heat induced into the control board has to be minimized. For a detailed analysis of the different heat sources, an equivalent circuit model is shown in Fig. 8. A significant temperature reduction of the top sides of the power semiconductor packages can be achieved by means of copper

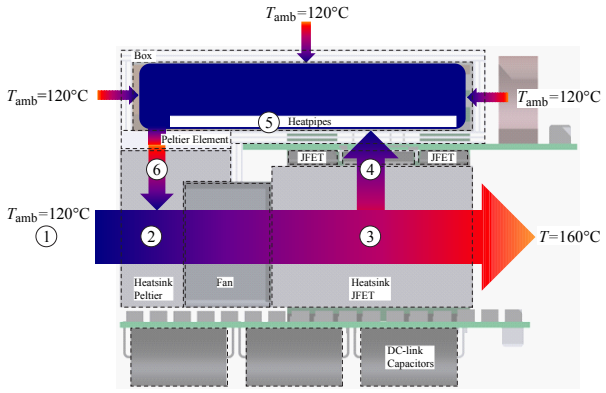

Fig. 7. Illustrated heat flow within the inverter system: Ambient air (120 °C) ① is sucked through the heat sink ② for the Peltier element by the fan located in between the heatsinks for the Peltier element and the power semiconductors, respectively. Then, the air slightly heated up by the Peltier Element heatsink is blown through the heat sinks ③ of the power semiconductors. The hot surface of the power semiconductors as well as their gate and source connections cause a heat input into the box ④ of the control electronics, that is transferred within the box by horizontal heat pipes ⑤. The heat is then removed by the Peltier element ⑥.

clips mounted on the packages and attached to the heat sink baseplate (*cf.* Fig. 6 (a)). These clips (thickness: 2 mm) cover the top sides and a poor contact area to the packages (e. g. by a rough copper surface or isolating film in between) together with a connection of low thermal impedance to the heatsink makes sure the temperature of the clip is on a comparable temperature level as the heatsink baseplate. The clips are represented in Fig. 8 by $R_{\mathrm{cu},1}$.

Furthermore, a thermal isolation material is mounted between the clips and the control electronics PCB (*cf.* Fig. 6 (a)). Frenzelit novaplan 02980 sheets with a thermal conductivity of $0.1\,\frac{\mathrm{W}}{\mathrm{mK}}$, a temperature limit of more than 1000 °C and a thickness of 0.8 mm are glued together with a distance of 0.8 mm to make use of the good thermal isolation capabilities of air (thermal conductivity: $0.026\,\frac{\mathrm{W}}{\mathrm{mK}}$). Loctite 5399 glue with a thermal conductivity of less than $0.3\,\frac{\mathrm{W}}{\mathrm{mK}}$ and a maximum specified temperature of 275 °C is used. This sandwich construction (total thickness 4 mm) is also used for the faces of the electronics box. The resulting thermal resistances of the isolation are denoted in Fig. 8 by $R_{\mathrm{iso},1}$ to $R_{\mathrm{iso},6}$.

The heat fed into the electronics box by the pins can be significantly reduced by only feeding the required gate and source terminals of the switches into the electronics box with 10 mil narrow, 35 μm thick and 10 mm long tracks ($R_{\mathrm{cu,pins}}$ in Fig. 8). This leads to an increase of a factor of 10 of the thermal resistance of each connection ($27\,\frac{\mathrm{K}}{\mathrm{W}}$ for each TO-247 pins compared to $300\,\frac{\mathrm{K}}{\mathrm{W}}$ for each PCB track). Additionally, the drain and diode pins are interconnected on the vertical PCBs in between the heatsinks (*cf.* Fig. 6) so that only 6 times 1 gate and source connections, 3 times 2 tracks for the current measurement and 1 times 2 tracks for the voltage measurement (20 in total) need to be fed into the control electronics box. Overall, a total amount of 20 W needs to be pumped out of the electronics box. Including a safety margin, the Peltier cooler is designed in Section IV-B for a removal of 30 W out of the electronics box.

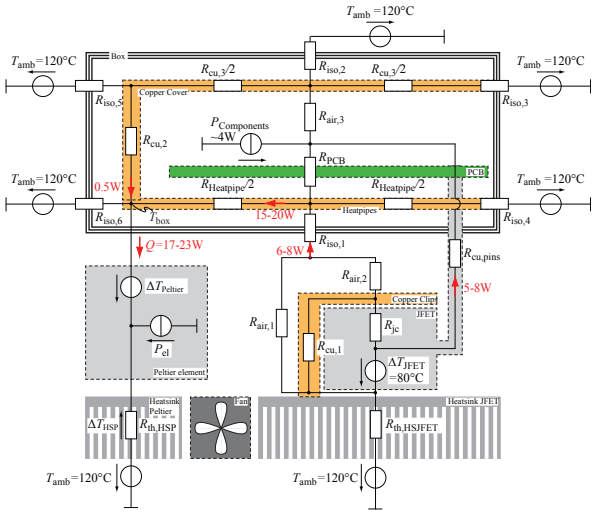

Fig. 8. Equivalent circuit model to calculate the heat induced into the control electronics box (20 W) and to derive a model for the Peltier cooling.

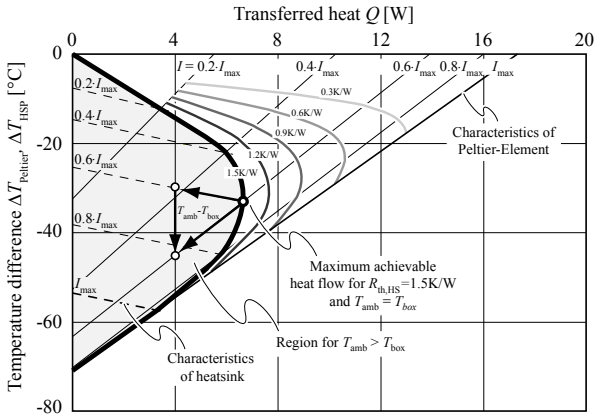

Fig. 9. Characteristic curves of Peltier element (solid lines) and heatsink for the Peltier element (dashed lines). Intersections (thick solid line) mark the possible operating points where the temperature inside the box is at the same level as the ambient temperature. This front is shifted for different heatsink sizes. The most right point on each front designates the maximum achievable heat flow with a certain heatsink.

As can be seen from Fig. 7 and Fig. 8, the largest portion of heat is fed into the box above the power semiconductors on the right side of the box. On the left side, the Peltier element pumps the heat out of the box. To enable a even temperature distribution in the box, heat pipes are soldered on the bottom layer of the PCB and thermally short circuit the PCB to the Peltier element. Furthermore, a copper bow is soldered to the upper control electronics PCB in order to provide a low thermal resistance path to the Peltier cooler for the upper control electronics PCB.

B. Design of Peltier Element for Optimum Cooling

By feeding electrical power P_{el} into the Peltier element, heat Q is transported from the cold side of the Peltier cooler to the hot side. At the hot side, the sum $P_{\mathrm{el}} + Q$ has to be fed to the heatsink.

The characteristics of a Peltier element are shown in Fig. 9 (solid lines) and include the maximum cooling power (only available at zero temperature difference $\Delta T_{\mathrm{Peltier}}$ between hot and cold side) and the maximum temperature difference ΔT_{max} between the cold and hot side. At a constant supply current, the cooling power decreases with increasing $\Delta T_{\mathrm{Peltier}}$ linearly and is zero at ΔT_{max}. The electrical power P_{el} fed into the cooler is proportional to its supply voltage. With the supply current decreasing, the load line is shifted towards lower cooling power and P_{el} decreases. This can lead to a higher efficiency. Hence, the cooling system is not necessarily smallest at a maximum supply current I_{max}.

With increasing $\Delta T_{\mathrm{Peltier}}$ the cooling power and efficiency of the Peltier cooler decrease. To be able to use a small Peltier element, $\Delta T_{\mathrm{Peltier}}$ should be kept at a low level. This makes a small thermal resistance $R_{\mathrm{th,HSP}}$ of the heatsink necessary and thus leads to a bulky heatsink.

On the other hand, with a large $\Delta T_{\mathrm{Peltier}}$, a higher thermal resistance and thus a smaller heatsink is feasible, on the expense of a larger area Peltier cooler. The resulting optimum with respect to the volume of the heatsink can be calculated using a "temperature loop" in Fig. 8.

$$\Delta T_{\mathrm{Peltier}} = T_{\mathrm{box}} - T_{\mathrm{amb}} + \Delta T_{\mathrm{HSP}} \tag{9}$$

as $T_{\mathrm{box}} = T_{\mathrm{amb}} = 120\,^{\circ}\mathrm{C}$. P_{el} and Q depend on the chosen Peltier element. As similar Peltier elements have got comparable characteristics, the calculation is conducted with the single-stage Peltier element QC-31-1.4-8.5M manufactured by Quick-cool. The following calculation leads to a total area needed for the Pelter elements. This area can be filled by several smaller peltier elements or a single one having the required size.

$R_{\mathrm{th,HSP}}$ depends on the fan, the volume of the heatsink and choice of fin geometry. The width and height of the heatsink is given by the choice of power semiconductors and fans (*cf.* Section III-A). To calculate the power that can be dissipated by the Peltier cooler, the thermal resistance $R_{\mathrm{th,HSP}} = 1.5\ \frac{\mathrm{K}}{\mathrm{W}}$ of a heatsink for the Peltier element having the same size as the Peltier element is determined in the same way as for the heatsinks of the power semiconductors (*cf.* Section III-D). In addition to the characteristic curves depicted in Fig. 9, the characteristic curves of the heatsink (shown as dashed lines in Fig. 9) can be calculated according to

$$\Delta T_{\mathrm{HSP}} = R_{\mathrm{th,HSP}} \left(Q + P_{\mathrm{el}} \right). \tag{10}$$

For this inverter system, T_{box} equals T_{amb}, leading to $\Delta T_{\mathrm{Peltier}} = \Delta T_{\mathrm{HSP}}$. This corresponds to the intersections of the Peltier and heatsink characteristic curves (thick solid line in Fig. 9). This front is shifted for different thermal resistances and thus volumes of the Peltier heatsink. Here, the maximum heat flow of 7.5 W can be achieved for approximately $0.6 I_{\mathrm{max}}$. With the required total heat flow of 30 W (*cf.* Section IV-A), four $20\,\mathrm{mm} \cdot 20\,\mathrm{mm}$ or one $40\,\mathrm{mm} \cdot 40\,\mathrm{mm}$ sized Peltier elements are needed.

Here, the current of $0.6 I_{\mathrm{max}}$ is a fixed value. If the pumped heat is lower (e. g. 4 W instead of 7.5 W for each Peltier element), the operating point of the Peltier cooler is shifted

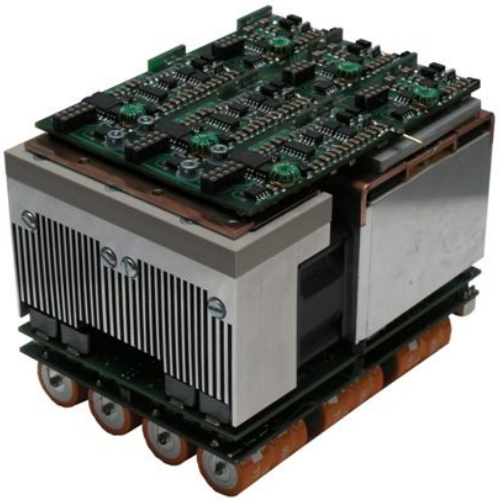

Fig. 10. Hardware prototype of 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system for experimental analysis and validation of the theoretical considerations shown in Section II to Section IV. The key specifications can be found in Table I. Not shown is the thermal isolation and cooling box of the control electronics.

away from the intersections line. The smaller amount of heat leads to a smaller temperature drop across the heatsink, but to a larger temperature $\Delta T_{\mathrm{Peltier}}$ drop across the Peltier element. This causes a temperature difference between the ambient air T_{amb} and within the box T_{box} such that the temperature level inside the box is lower. If the pumped heat Q increases to values larger than 7.5 W, the temperature in the box will be higher than the ambient air.

V. Conclusion

The shown 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system demonstrates how restrictions of today's power electronic converters in HEVs with respect to the ambient temperature level can be overcome. It has to be noted though, that this is possible only on the expense of a significantly higher complexity, affected efficiency and power density of the overall converter. The volume needed for the active cooling of the control electronics accounts for 20% of the overall converter volume. Further investigations will include experimental results of the inverter operation at high ambient temperatures and of the cooling box. Further research is needed e. g. in the area of high-temperature fans that are able to operate at air temperatures of 150 °C and more.

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