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SWISS Rectifier – A Novel Three-Phase Buck-Type PFC Topology for Electric Vehicle Battery Charging

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***Abstract*—This paper introduces a novel three-phase buck-type unity power factor rectifier appropriate for high power Electric Vehicle battery charging mains interfaces. The characteristics of the converter, named the SWISS Rectifier, including the principle of operation, modulation strategy, suitable control structure, and dimensioning equations are described in detail. Additionally, the proposed rectifier is compared to a conventional 6-switch buck-type ac-dc power conversion. According to the results, the SWISS Rectifier is the topology of choice for a buck-type PFC. Finally, the feasibility of the SWISS Rectifier concept for buck-type rectifier applications is demonstrated by means of a hardware prototype.**

I. INTRODUCTION

Charging of Electric Vehicle (EV) batteries inherently requires conversion of energy from the ac mains into dc quantities. Several charging voltage and power levels have been defined by different standardization organizations (IEC 61851, IEC62196, SAE J1772). Single-phase Power Factor Corrector (PFC) mains interfaces are commonly employed for low charging power levels (e.g. $P < 5$ kW), whereas for higher power levels, three-phase PFC mains interfaces have to be applied [1]. The EV chargers, typically implemented as two-stage systems, i.e. comprising a PFC rectifier input stage followed by a dc-dc converter, can be either integrated into the car (on-board) or accommodated in specially designed EV charging stations (off-board) [2].

In the particular case of fast charging stations (off-board), the power electronic system should be able to guarantee voltage adaptation to cope with different specifications of several types of vehicles. Typically, for three-phase 400 V or 480 V (line-to-line *rms* voltage) ac mains, EV chargers with a dc-bus voltage in the range of 250 V to 450 V are used [1].

Buck-type three-phase PFC rectifiers are appropriate for high power EV chargers (> 5 kW), as a direct connection to the dc-bus can be used. If isolation of the dc-bus from the PFC rectifier is required for safety reasons, this can be facilitated by an isolated dc-dc converter connected in series, which can additionally be used for voltage regulation. Compared to boost-type topologies, buck-type systems provide a wider output voltage control range, while maintaining PFC capability at the input, enable direct start-up, and allow for dynamic current limitation at the output [3]-[7]. Three-phase boost rectifiers produce an output voltage (typ. 700 V to 800 V) that is too high to directly feed the dc-bus of EVs and thus require a step-down dc-dc converter at their output.

This paper presents a novel three-phase buck-type PFC rectifier topology, referred to as the SWISS Rectifier (cf. **Fig. 1**), appropriate for high power EV battery charging systems. Other suitable applications include supplies for dc power distribution systems in telecommunication, future more electric aircraft, variable speed ac drives, and high power lighting systems. The SWISS Rectifier was first introduced in [7] and [8], however, only a brief description of the rectifier concept was given. In this paper, after the explanation of the principle of operation of the new rectifier topology, which employs a three-phase active third harmonic injection rectifier, in **Section II**, the derivation of the input current space vectors and the calculation of the relative on-times of the active switches guaranteeing PFC operation are presented in **Section III**. A PWM-control method using triangular carriers is proposed in **Section IV**. The analytical expressions for

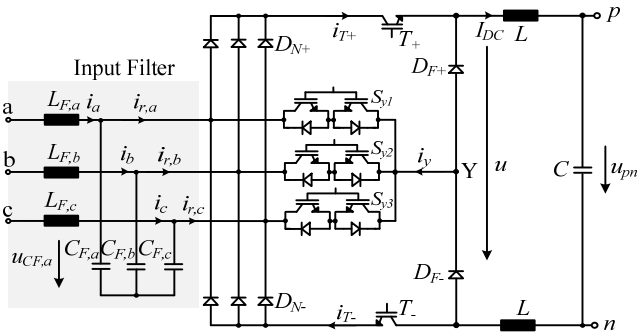

Fig. 1: Circuit topology of the proposed three-phase SWISS Rectifier with *LC* input filter.

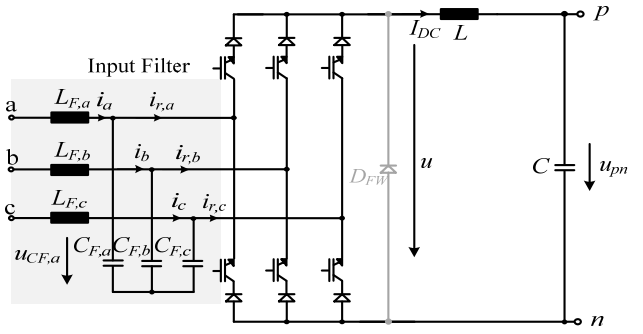

Fig. 2: Circuit topology of a three-phase 6-switch buck-type PFC rectifier with *LC* input filter and explicit freewheeling diode D_{FW}.

calculating the stresses of the main semiconductors and passive components in dependency on the input current amplitude and the voltage transfer ratio of the converter are given in **Section V**. A 7.5 kW SWISS Rectifier is designed to attest the feasibility of the proposed rectifier concept. Finally, in **Section VI**, the SWISS Rectifier is systematically compared with a 6-switch buck-type PFC rectifier, shown in **Fig. 2**, which represents the standard three-phase buck-type topology.

II. NOVEL THREE-PHASE BUCK-TYPE PFC RECTIFIER

A novel three-phase PFC rectifier solution combining buck dc-dc converters and an active 3rd harmonic current injection circuit, referred to here as the SWISS Rectifier, is shown in **Fig. 1**. Other 3rd harmonic injection topologies are described in [9]-[11], including the dual converter of the SWISS rectifier, a boost-type rectifier.

The SWISS Rectifier allows the currents in the positive and negative active switches, i_{T+} and i_{T-}, to be formed proportionally to the two phase voltages involved in the formation of the output voltage of the diode bridge. If the difference of i_{T+} and i_{T-} is fed back into the mains phase with the currently smallest absolute voltage value via a current injection network, formed with three four-quadrant switches gated at twice the mains frequency, a sinusoidal input current shape can be assured for all mains phases while the dc-dc converters guarantee the output voltage regulation.

A circuit implementation with a single output inductor is feasible, however, in the proposed circuit, shown in **Fig. 1**, the total dc inductance is split evenly between the positive and negative output bus in order to provide symmetric attenuation impedances for conducted common mode noise. The conduction losses in the freewheeling state could be reduced by implementation of an additional freewheeling diode D_{FW} as is shown for the 6-switch buck-type PFC rectifier in **Fig. 2**.

For the SWISS Rectifier, the output voltage range is limited by the minimal value of the six-pulse diode bridge output voltage, given by (1) and therefore is identical to the output voltage range for the 6-switch buck-type PFC rectifier, shown in **Fig. 2**. Contrary to the 6-switch buck-type PFC systems, the rectifier diodes of the SWISS Rectifier are not commuted with switching frequency. Correspondingly, the conduction losses can be reduced employing devices with a low forward voltage drop (and a higher reverse recovery time). In addition, the mains commutated injection switches could be implemented with an anti-parallel connection of RB-IGBTs with a low forward voltage drop.

$$u_{pn} < \sqrt{\frac{3}{2}} u_{N,l-l,rms} \tag{1}$$

III. CONDUCTION STATES, MODULATION, AND DUTY CYCLE CALCULATION

For the analysis of the conduction states, the derivation of the current space vectors and the calculation of the relative turn-on times, symmetric mains conditions are assumed. The mains currents $i_{a,b,c}$ are considered to be equal to the fundamental component of the rectifier input currents $i_{r,a,b,c,(1)}$. Hence, the reactive currents due to the filter capacitors are also neglected. Moreover, the filter capacitor voltages $u_{CF,a,b,c}$ at the input of the rectifier are considered purely sinusoidally shaped and in phase with the mains voltages $u_{a,b,c}$. The current in the dc inductors I_{DC} is assumed to be constant. Finally, all the analyses consider one of the twelve 30°-wide sectors of the mains period, i.e. $0° < \varphi_N < 30°$ with $\varphi_N = \omega_N t$ which is characterized by the mains phase relation $u_a > u_b > u_c$. For the remaining sectors, the calculations can be performed in a similar manner.

The modulation of the current injection circuit is performed at low frequency, following the rectifier input voltages $u_{CF,a,b,c}$ in such a way that the active current injection occurs always into only one mains phase as presented in **Tab. I** (cf. **Fig. 3**). Accordingly, in each of the 30°-wide sectors of the mains period, four different conduction states can be defined by the switches T_+ and T_- within a pulse period T_P, where the dc current I_{DC} impressed by the dc inductors is distributed to two of the input phases or is kept in a freewheeling state. The rectifying discrete converter input current space vector can be calculated by

$$\underline{i}_r = \frac{2}{3}\left(i_{r,a} + e^{j2\pi/3} i_{r,b} + e^{j4\pi/3} i_{r,c}\right). \tag{2}$$

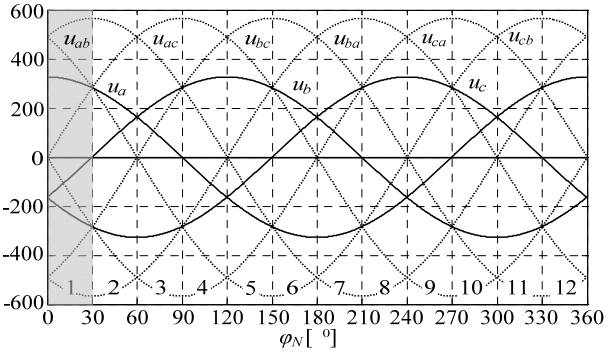

Fig. 3: Mains sectors 1 to 12 defined by the different relations of the instantaneous values of the mains phase voltages $u_{a,b,c}$.

TABLE I: Modulation of the current injection circuit (cf. **Fig. 4**).

Sector	S_{y1}	S_{y2}	S_{y3}	Sector	S_{y1}	S_{y2}	S_{y3}
0°-30°	0	1	0	180°-210°	0	1	0
30°-60°	0	1	0	210°-240°	0	1	0
60°-90°	1	0	0	240°-270°	1	0	0
90°-120°	1	0	0	270°-300°	1	0	0
120°-150°	0	0	1	300°-330°	0	0	1
150°-180°	0	0	1	330°-360°	0	0	1

Fig. 4(a) presents the four conduction states of the SWISS Rectifier for the interval $\varphi_N \in [0°, 30°]$. For the switching state j = (ON, ON), where $j = (T_+, T_-)$ indicates a combination of the switching functions of the two fast switches (T_+ and T_-) and ON means that the respective switch is turned on, while OFF indicates an off-state of the switch, the rectifier input currents are $i_{r,a} = I_{DC}$, $i_{r,b} = 0$, and $i_{r,c} = -I_{DC}$. Therefore, the rectifier input current space vector for this switching state results in

$$\underline{i}_{r,(ON,ON)} = \frac{2}{\sqrt{3}} I_{DC} e^{j\pi/6}. \tag{3}$$

Analogously, the three remaining space vectors can be calculated as

$$\underline{i}_{r,(ON,OFF)} = \frac{2}{\sqrt{3}} I_{DC} e^{-j\pi/6}, \tag{4}$$

$$\underline{i}_{r,(OFF,ON)} = \frac{2}{\sqrt{3}} I_{DC} e^{j\pi/2}, \tag{5}$$

$$\underline{i}_{r,(OFF,OFF)} = 0. \tag{6}$$

With these four space vectors, a resulting input current space vector $\underline{i}^*_r$ can be formed [cf. **Fig. 4(b)**] so that it is in phase with the mains voltage vector $\underline{u}^*_r$ and has the required amplitude according to the actual power demand.

The proper selection of the switching state sequences allows control over the current ripple Δi_{DC} of the dc inductor current I_{DC} and Δi_y of the phase injection current i_y. Accordingly, the converter can be modulated in order to minimize the current ripple of i_y or that of the inductor current I_{DC}.

For the first mains sector ($0° < \varphi_N < 30°$), the SWISS Rectifier can operate with minimal injection current ripple Δi_y and consequently lower ripple values of the input capacitor voltages $u_{CF,a,b,c}$ if a vector modulation with the switching sequence (ON, ON) - (ON, OFF) - (OFF, OFF) - (ON, OFF) - (ON, ON), arranged symmetrically around the middle of the pulse interval, is applied [cf. **Fig. 5(a)**]. As can be seen in **Fig. 5(a)**, the input phase currents are formed by segments of the dc current I_{DC} defined by the relative on-times k_i of the current vectors

$$i_{r,a} = I_{DC}(k_1 + k_2);\ i_{r,b} = -I_{DC}k_2;\ i_{r,c} = -I_{DC}k_1. \tag{7}$$

The output voltage u_{pn} is formed by the line-to-line voltages u_{ab} and u_{ac} rated by the relative on-time of the respective current vectors

$$u_{pn} = k_1 u_{ac} + k_2 u_{ab}. \tag{8}$$

Note that the output voltage range is limited by the minimal value of the six-pulse diode bridge output voltage

$$u_{pn} < \sqrt{\frac{3}{2}} u_{N,l-l,rms}. \tag{9}$$

Finally, PFC operation in the first mains sector can be achieved with relative on-times k_i, reliant on the modulation

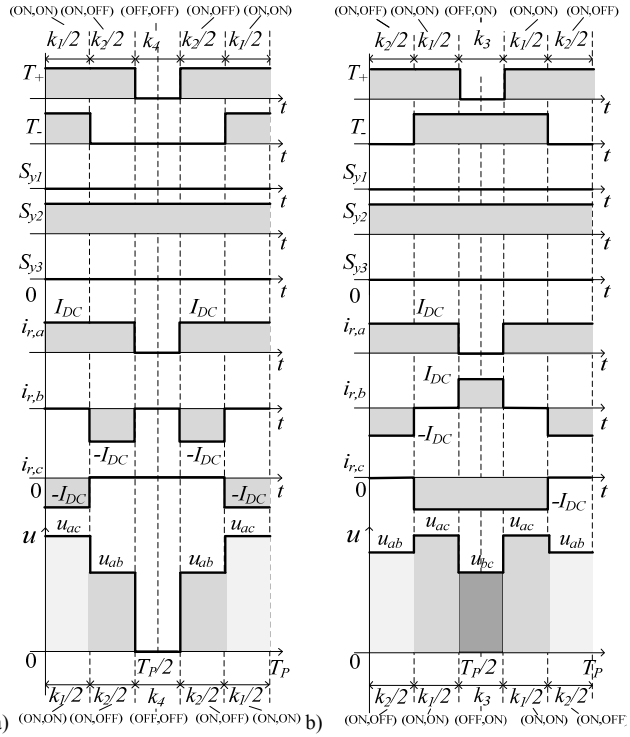

Fig. 5: Modulation scheme for **a)** minimal injection current ripple Δi_y or **b)** minimal dc current ripple Δi_{DC} for $\varphi_N \in [0°, 30°]$.

index M, the instantaneous values of $u_{a,b,c}$, and the amplitude of the mains phase voltages $\hat{U}_N$ given by

$$M = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N}, \tag{10}$$

$$k_1 = -M\frac{u_c}{\hat{U}_N},\ k_2 = -M\frac{u_b}{\hat{U}_N}, \text{ and } k_4 = 1 - M\frac{u_a}{\hat{U}_N}. \tag{11}$$

Note that the switch duty cycles α_+ (for transistor T_+) and α_- (for transistor T_-) for symmetric mains ($u_a + u_b + u_c = 0$) are defined according to

$$\alpha_+ = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_a = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}(-u_b - u_c) = k_1 + k_2, \tag{12}$$

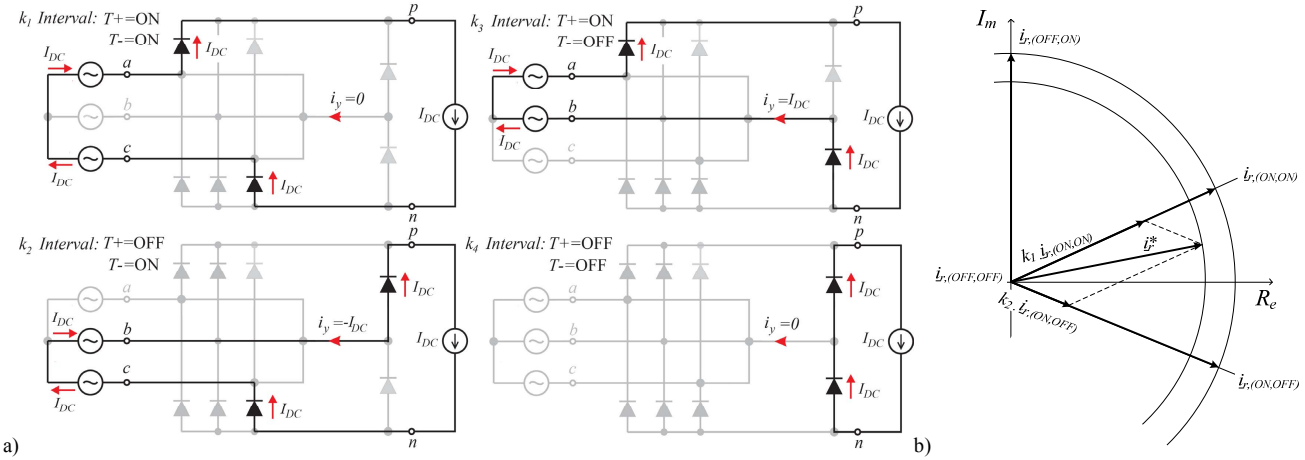

Fig. 4: a) Conduction states and **b)** input current space vector diagram of the SWISS Rectifier for $\varphi_N \in [0°, 30°]$.

$$\alpha_{-} = -\frac{2}{3}\frac{u_{pn}}{\hat{U}_N^2}u_c = k_1 . \quad (13)$$

Alternatively, for the first mains sector ($0° < \varphi_N < 30°$), the SWISS Rectifier can operate with minimized dc inductor current ripple Δi_{DC} and consequently reduced ripple values of the output low-pass filtering if a vector modulation with the switching sequence (ON, OFF) - (ON, ON) - (OFF, ON) - (ON, ON) - (ON, OFF), arranged symmetrically around the middle of the pulse interval, is applied [cf. **Fig. 5(b)**]. As can be seen in **Fig. 5(b)**, the (locale average) input phase currents are defined by the dc current I_{DC} and the relative on-times k_i of the current vectors

$$i_{r,a} = I_{DC}(k_1 + k_2);\ i_{r,b} = I_{DC}(k_3 - k_2);\ i_{r,c} = -I_{DC}(k_1 + k_3). \quad (14)$$

The output voltage u_{pn} is formed by the line-to-line voltages u_{ab}, u_{bc}, and u_{ac}, weighted by the relative on-times of the respective current vectors

$$u_{pn} = k_1 u_{ac} + k_2 u_{ab} + k_3 u_{bc} . \quad (15)$$

Finally, PFC operation in the first mains sector can be achieved with relative on-times k_i, dependent on the modulation index M, instantaneous input voltage values $u_{a,b,c}$, and the amplitude of the mains phase voltages $\hat{U}_N$ given by

$$k_2 = 1 + M\frac{u_c}{\hat{U}_N},\ k_3 = 1 - M\frac{u_a}{\hat{U}_N},\ k_1 = 1 - k_2 - k_3 = M\frac{u_a - u_c}{\hat{U}_N} - 1. \quad (16)$$

IV. PWM CONTROL SCHEME

A possible implementation of a control scheme for the SWISS Rectifier is shown in **Fig. 6**. This feedback PWM control comprises a superimposed output voltage controller $R(s)$ and a subordinate output current controller $G(s)$. Finally, a feed-forward loop adds the normalized modulation functions defined by the positive and negative diode bridge output voltage and the system output voltage reference value u^*_{pn} to the dc current controllers in order to directly generate the input current forming voltage u.

In the proposed control structure, setting the PWM modulator for T_+ and T_- to operate with in-phase carriers allows the system to work similarly as if it would be controlled with the vector modulation described in **Fig. 5(a)**, where the current ripple Δi_y is minimized while Δi_{DC} is maximized. On the other hand, operation using carriers with a phase difference of 180° (interleaved carriers) permits the system to work similarly as if it would be controlled with the vector modulation depicted in **Fig. 5(b)**, where the dc current ripple Δi_{DC} is minimized while Δi_y is maximized.

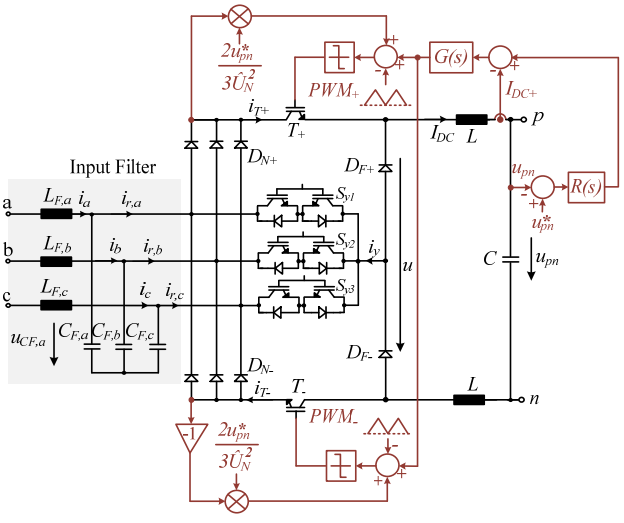

Fig. 6: PWM control structure for the SWISS Rectifier.

Simulation results, depicting the principle of operation of the SWISS Rectifier, are shown in **Fig. 7**. The converter specifications, given in **Tab. II**, are considered in the simulation where operation with in-phase or interleaved PWM carriers and a load step (from 3.75 kW to 7.5 kW) are presented. As can be observed, the results demonstrate that the line currents $i_{a,b,c}$ can effectively follow the sinusoidal input phase voltages $u_{a,b,c}$ even in case of load steps, attesting the feasibility of the proposed rectifier and PWM control.

TABLE II: SWISS Rectifier prototype specifications.

Input phase voltage $u_{a,b,c}$	230 V *rms* ±10%
Mains frequency f_N	50 Hz
Switching frequency f_P	36 kHz
Rated output power P_0	7.5 kW
Output capacitor C	470 µF
DC inductor L	305 µH

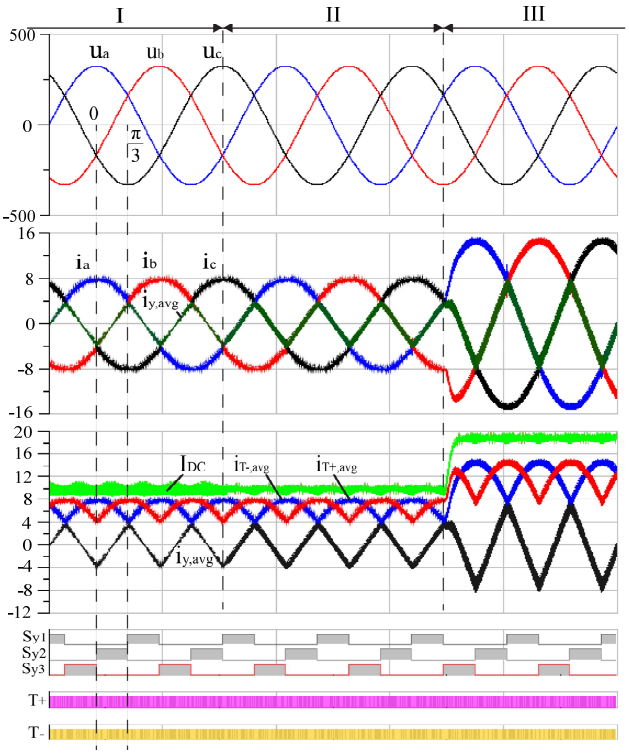

Fig. 7: Simulation results of the SWISS rectifier operating with **(I)** in-phase or **(II)** interleaved PWM carriers; **(III)** load step from 50% to 100% of the rated output power (3.75 kW to 7.5 kW).

V. SWISS RECTIFIER SYSTEM DESIGN

In this section, in order to provide a clear and general guideline for the components selection for the SWISS Rectifier design, the stresses of the active and passive components of the converter are calculated analytically with dependence on the operating parameters of the rectifier. As an application

case, a 7.5 kW unity power factor rectifier system shall be dimensioned that should provide a constant output voltage of $u_{pn} = 400$ V for operation at a mains with 230 Vrms phase voltage ($u_{a,rms} = 230$ V ±10%) and a switching frequency of $f_P = 36$ kHz.

A. Semiconductor Voltage and Current Stresses

The maximum voltage stress on the line diodes, D_{N+} and D_{N-}, is defined by the line-to-line voltage $u_{N,l-l,max}$

$$u_{DN,\max} = u_{N,l-l,\max} = \sqrt{2}\sqrt{3}u_{a,rms}\left(1+10\%\right) = 620\text{V}\,. \quad (17)$$

All the remaining semiconductors (T_+, T_-, D_{F+}, D_{F-}, and S_y) have to block a maximum voltage which corresponds to the 60° sinusoidal progression of the maximum line-to-line input voltage $u_{N,l-l,max}$

$$u_{DF,\max} = u_{T,\max} = u_{Sy,\max} = \frac{\sqrt{3}}{2}u_{N,l-l,\max} = 537\text{V}\,. \quad (18)$$

Note that the selections of the blocking voltage capability of the power transistors and diodes have to consider a additional safety margin δ for undesirable oscillations of the rectifier input voltage in case of low passive damping of the input filter. Therefore, 1200 V power diodes and IGBTs (55% > δ > 48%) or 900 V MOSFETs ($\delta \approx 40\%$) are suitable for the full silicon implementation of the SWISS Rectifier.

In order to determine the on-state losses of the semiconductors, the current *rms* and average values have to be calculated and therefore, simple analytical approximations are derived. For the following calculations, it is assumed that the rectifier has

- a purely sinusoidal phase current shape,
- ohmic fundamental mains behavior,
- a constant dc current I_{DC},
- no low-frequency voltage drop across the input filter inductors, therefore $u_{C,a,b,c} = u_{a,b,c}$, and
- a switching frequency $f_P >> f_N$.

1) Current Stress of the Bidirectional Switches S_y and D_y

With a defined modulation index M, the average and *rms* currents of the two transistors and diodes forming a bidirectional switch finally result in

$$I_{\frac{Dy}{Sy},avg} = I_{DC}M\frac{2-\sqrt{3}}{2\pi} \text{ and } I_{\frac{Dy}{Sy},rms} = I_{DC}\sqrt{M\frac{2-\sqrt{3}}{2\pi}}\,. \quad (19)$$

2) Current Stress of the Rectifier Diodes D_{N+} and D_{N-}

The average and *rms* currents of the rectifier diodes can be calculated as

$$I_{DN,avg} = I_{DC}M\frac{\sqrt{3}}{2\pi} \text{ and } I_{DN,rms} = I_{DC}\sqrt{\frac{\sqrt{3}M}{2\pi}}\,. \quad (20)$$

3) Current Stress of the Fast Diodes D_{F+} and D_{F-}

The average and *rms* currents of the fast freewheeling diodes can be determined as

$$I_{DF,avg} = I_{DC}\left(1-\frac{3\sqrt{3}}{2\pi}M\right) \text{ and } I_{DF,rms} = I_{DC}\sqrt{1-\frac{3\sqrt{3}}{2\pi}M}\,. \quad (21)$$

4) Current Stress of the Power Transistors T_+ and T_-

The average and *rms* currents of the PWM modulated power transistors are determined by

$$I_{T,avg} = I_{DC}M\frac{3\sqrt{3}}{2\pi} \text{ and } I_{T,rms} = I_{DC}\sqrt{\frac{3\sqrt{3}M}{2\pi}}\,. \quad (22)$$

B. Passive Components: Voltage and Current Stresses

1) DC Inductor L

The voltage across each of the dc inductors L is equivalent to half of the value of the maximum allowed line-to-line input voltage $u_{N,l-l,max}$

$$u_{L+} + u_{L-} = u_{N,l-l,\max} \;\therefore\; u_{L+} = \frac{u_{N,l-l,\max}}{2} = 310\text{V}\,. \quad (23)$$

The current flowing through L is defined by the full dc (load) current I_{DC} and a current ripple $\Delta i_{L,pp,max}$ which is limited to a given value, i.e. 25% of I_{DC}. The current ripple peak-to-peak value and the *rms* value of the dc inductor current, $\Delta i_{L,pp}$ and $i_{L,rms}$, can be determined as follows

$$I_{DC} = \frac{P_0}{u_{pn}}, \quad (24)$$

$$\Delta i_{L,pp,\max} = \sqrt{\frac{2}{3}}\frac{u_{pn}}{L}\left(\frac{1-M}{f_P}\right), \quad (25)$$

$$i_{L,rms} = \sqrt{I_{DC}^2 + \frac{\Delta i_{L,pp,\max}^2}{18}}\,. \quad (26)$$

The inductance value of the dc inductor can then be selected according to

$$L \geq \frac{\sqrt{3}u_{pn}}{2\Delta i_{L,pp,\max}}\left(\frac{1-M}{f_P}\right). \quad (27)$$

2) Output Capacitor C

When selecting the output capacitor C, the value of the controlled output voltage u_{pn} and an additional over-shoot margin to enable safe operation during load transients (around 10% of u_{pn}), must be taken into consideration

$$u_C > 1.1u_{pn} = 440\text{V}\,. \quad (28)$$

The *rms* value of the output capacitor current ripple $\Delta i_{C,rms}$ and the peak-to-peak value of the output voltage ripple $\Delta u_{C,pp}$ are given by

$$\Delta i_{C,rms} = \sqrt{\frac{\Delta i_{L,pp,\max}^2}{18}} \text{ and } \Delta u_{C,pp} = \frac{u_{pn}}{L}\left(\frac{1-M}{8f_P^2C}\right). \quad (29)$$

The capacitance value of the dc output capacitor can then be determined according to

$$C \geq \frac{u_{pn}}{L}\left(\frac{1-M}{8f_P^2\Delta u_{C,pp,\max}}\right). \quad (30)$$

C. Simple DM and CM Noise Models of the SWISS Rectifier

The semiconductors of a power electronics converter are typically mounted on a common heat sink which is usually connected to ground (PE). Therefore, parasitic capacitances to ground exist, leading to propagation of common-mode (CM) noise currents in the circuit (cf. **Fig. 8**).

Due to the discontinuous input current of the SWISS Rectifier, at least a single-stage differential mode (DM) input filter, i.e. $L_{F,i}$ and $C_{F,i}$, is necessary. However, for full compliance to EMC standards [12], the conducted DM and CM noise emissions propagating to the mains have to be attenuated sufficiently. In order to design a proper EMI filter, the CM and DM noise levels of the SWISS Rectifier need to be determined. Accordingly, the modeling approach given in [12] and [13] is extended to this three-phase converter.

The DM noise is generated by the pulsating input currents $i_{r,a,b,c}$ at switching frequency and is attenuated by the input filter capacitors $C_{F,a,b,c}$ and the ac side filter inductors $L_{F,a,b,c}$. The CM noise is caused within each pulse period T_P by the switched line-to-line voltages during the formation of the output voltage and for the distribution of the dc current to the mains phases. For the SWISS Rectifier, this pulsed voltage u_{CM} has a maximum high frequency peak-to-peak amplitude $U_{CM,pp,max}$ of approximately

$$U_{CM,pp,max} \approx \frac{3}{\sqrt{8}} u_{a,rms} \,. \tag{31}$$

Fig. 8 defines the simplified circuits to evaluate CM and DM noise sources for the SWISS Rectifier. There, the CM voltage u_{CM}, the DM current i_{DM}, and the stray capacitances, C_g and C_{Eq}, model the power converter CM and DM noise circuits. The capacitances C_g and C_{Eq} are lumped representations of all relevant stray capacitances included in the CM propagation path. C_g represents mainly the capacitances of the positive and negative output voltage bus to ground C_{pn}, and from the load to earth C_0, while C_{Eq} models the stray capacitances from the semiconductors to the heatsink (C_{DN}, C_{Sy}, C_T, and C_{DF}) and the power connection terminals to earth, C_{XZ}.

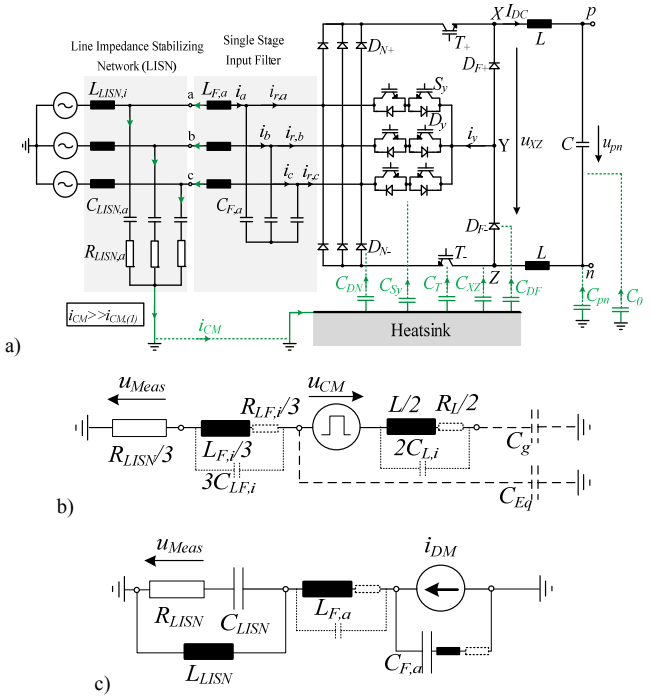

Fig. 8: a) Model for the propagation of the common mode currents in the SWISS Rectifier used for deriving the CM noise model. Simplified high-frequency model for **b)** CM and **c)** DM emissions, including the high-frequency equivalent circuit of the LISN and a single stage DM input filter with parasitics of inductive and capacitive elements shown.

A simplified time domain simulation of the system is sufficient to obtain the DM current and CM voltage sources, i_{DM} and u_{CM}. The CM voltage can be calculated by measuring the voltages $u_{X,PE}$ and $u_{Z,PE}$,

$$u_{CM} = \frac{u_{X,PE} + u_{Z,PE}}{2} \,, \tag{32}$$

and the DM currents are computed directly from the input currents as long as no CM paths exist in the simulation circuit. For simplicity, the current measured in phase a is used so that

$$i_{DM} = i_{r,a} \,. \tag{33}$$

A simulation of the SWISS Rectifier in GeckoCIRCUITs [14] is used for determining the CM and DM noise sources. The converter specifications listed in **Tab. II** are used to perform the simulation. The time behavior of the CM voltage u_{CM} and DM current i_{DM} for both space vector modulations described in Section III are presented in **Fig. 9**, where it can be seen that the CM voltage is formed with combinations of the input voltages, while the DM current is formed by the switched dc current I_{DC}. Finally, the low frequency component $i_{DM,(1)}$ shows a nearly ideal sinusoidal behavior, thus PFC at the input of the converter is obtained.

It can be observed that the different modulation strategies result in different CM and DM waveforms which would finally lead to different EMI filter requirements. As an example, by comparing the calculated DM noise emissions for both modulations to the CISPR 22 Class B limit at $f = 180$ kHz (first multiple of the switching frequency ($f_P = 36$ kHz) within the EMC measurement band), the required suppression for the EMI filter can be determined. As a result, with quasi-peak measurement (QP), the necessary attenuation of noise for the modulation, which minimizes the ripple Δi_y, is $Att_{req} = 75$ dB, while for the modulation, which minimizes the ripple Δi_{DC}, the necessary noise suppression is slightly higher, i.e. $Att_{req} = 78$ dB.

Due to the high required filter attenuations a second filter stage is recommended. For control stability reasons, the attenuation of the first stage filter, $L_{F,a,b,c}$ and $C_{F,a,b,c}$, has to be higher than for the second stage. As a design criteria, the suppression of the first DM filter stage will be considered as follows (cf. [13])

$$Att_{LF,CF}[dB] = (0.7,...,0.8)\, Att_{req}[\text{dB}] \,. \tag{34}$$

Additionally, the selection of needs to limit the voltage ripple peak-to-peak value across $C_{F,i}$ to about 5% to 10% in order to ensure correct detection of the input line-to-line voltages that is required for the system modulation [13]. On the other hand, high values of $C_{F,i}$ lead to a low power factor at low load operation, therefore, as a compromise the value of $C_{F,i}$ is defined in the range

$$C_{F,i} = (3\,\mu\text{F},...,13\,\mu\text{F}) \,. \tag{35}$$

Finally, the range of the inductance value of the filter inductors can be determined for Att_{req}[dB] = 78 dB

$$L_{F,i} = \frac{10^{Att_{LF,CF}[dB]/20}}{4\pi^2 C_{F,i} \left(f = 180\text{kHz}\right)^2} = (32\,\mu\text{H},...,344\,\mu\text{H}) \,. \tag{36}$$

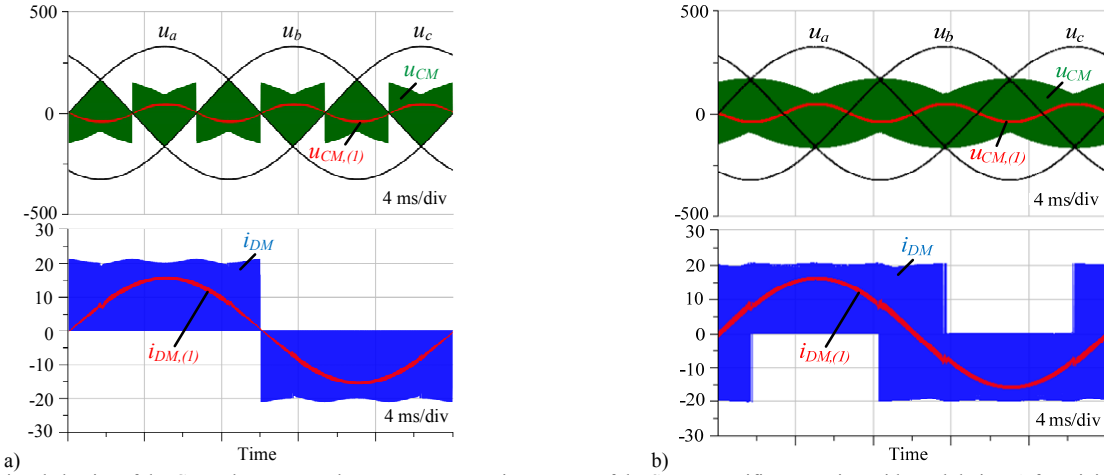

Fig. 9: Time behavior of the CM voltage u_{CM} and DM current i_{DM} noise sources of the SWISS Rectifier operating with modulation **a)** for minimal injection current ripple Δi_y [cf. **Fig. 5(a)**] and **b)** for minimal dc inductor current ripple Δi_{DC} [cf. **Fig. 5(b)**].

D. Swiss Rectifier Model Accuracy

In order to verify the accuracy of the derived equations modeling the voltage and current stresses of the SWISS Rectifier, an appropriate switching frequency and the values of the passive components according to (27), (30), (35), and (36) have been selected. A switching frequency of $f_P = 36$ kHz is designated as it constitutes a good compromise between high efficiency, high power density, and high control bandwidth. Advantageously, the fourth switching frequency harmonic is found near, but still below the beginning of the considered the EMC measurement range at 150 kHz. With $f_P = 36$ kHz, the values for the output filter $L = 305$ μH and $C = 470$ μF are selected. The component values of the first input filter stage is $L_{F,i} = 85$ μH and $C_{F,i} = 4.4$ μF.

In **Tab. III**, the values of the average and *rms* component stresses calculated with the respective expressions are compared to the results obtained with a simulation performed in GeckoCIRCUITs [14] and show a very good accuracy.

TABLE III: SWISS Rectifier: comparison of active and passive component stresses determined by analytical calculations and digital simulations.

	Analytical Calculations	**Simulation**	**Deviation [%]**
$I_{Sy,avg}$	0.66	0.68	-2.94
$I_{Sy,rms}$	3.51	3.57	-1.68
$I_{DN,avg}$	4.24	4.22	+0.47
$I_{DN,rms}$	8.91	8.91	0.00
$I_{T,avg}$	12.71	12.68	+0.24
$I_{T,rms}$	15.44	15.44	0.00
$I_{DF,avg}$	6.04	6.06	+0.33
$I_{DF,rms}$	10.64	10.67	+0.28
$i_{L,rms}$	18.78	18.78	0.00
$\Delta i_{L,pp,max}$	4.66	4.57	+1.97
$\Delta i_{C,rms}$	1.10	1.13	-2.65

E. 7.5 kW Hardware Demonstrator

A laboratory prototype of the SWISS Rectifier according to the specifications given in **Tab. II** has been built. The implemented prototype is shown in **Fig. 10**. The overall dimensions of the system are 210 mm x 132 mm x 92 mm, hence leading to a power density of 2.94 kW/dm^3. For nominal operation, the total efficiency is approximately 96.5%.

Note that for the selection of the 7.5 kW SWISS Rectifier components, the analytical equations (17)-(36) were utilized, considering the worst case operating condition for each specific component. For instance, the semiconductors have to cope with the highest current stress which occurs at the maximum modulation index ($M \approx 0.91$). According to (17) and (18), IGBTs and diodes with a blocking voltage capability of 1200 V have been chosen.

In respect of the operating principle of the converter, the injection switches $S_{y,i}$ are implemented with latest generation Trench and Fieldstop (T&FS) IGBTs (1200 V / 25 A, IKW25N120, Infineon) with an anti-parallel freewheeling diode that are optimized for low conduction losses as they are switched with only twice the mains frequency. For the transistors T_+ and T_-, high-speed T&FS IGBTs (1200 V / 40 A, IGW40N120H3, Infineon) are used in combination with SiC MPS diodes (1200 V / 20 A, C2D20120A, CREE) for D_{F+} and D_F to enable low switching losses at the selected switching frequency of $f_P = 36$ kHz (cf. **Fig. 11**).

A list of the employed semiconductor devices and passive components is given in **Tab. IV** along with the key design parameters.

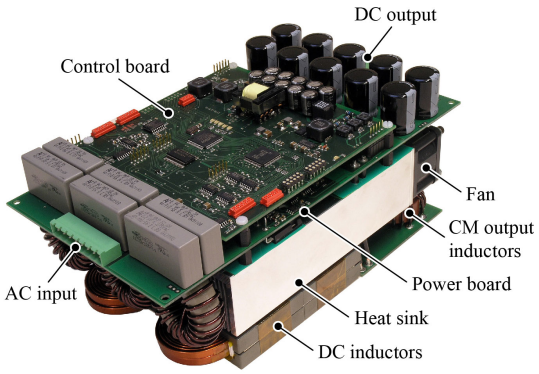

Fig. 10: Implemented 7.5 kW SWISS Rectifier hardware prototype, using 1200 V Trench and Fieldstop IGBTs and 1200 V SiC MPS freewheeling diodes. (Mechanical dimensions: 210 mm x 132 mm x 92 mm; power density: 2.94 kW/dm^3 = 48 W/in^3, switching frequency: $f_P = 36$ kHz.).

TABLE IV: Selected main components of the SWISS Rectifier hardware prototype (cf. **Fig. 10**).

Component	Device Description
S_y / D_y	Si T&FS IGBTs, 1200 V / 25 A, IKW25N120, Infineon
T_+ / T_-	Si HighSpeed T&FS IGBTs, IGW40N120H3, Infineon
D_{N+} / D_{N-}	Si fast recovery diode, DSEP060-12AR, IXYS
D_{F+} / D_{F-}	SiC Schottky diodes, 1200 V / 20 A, C2D20120A, CREE
L	305 µH, 2 x E64-50-10 cores, 3C91 ferrite, Ferrox Cube N_L = 16 turns, Cu wire cross section $A_{w,L}$ = 8.5 mm^2
C	10 x 47 µF / 450 V, electrolytic capacitors, EPCOS
$L_{F,abc}$	85 µH, High Flux 58254 powder core, Magnetics N_{Lf} = 22 turns, Cu wire cross section $A_{w,Lf}$ = 3.1 mm^2
$C_{F,abc}$	2 x 2.2 µF, 305 V X2, MKP foil, Arcotronics

VI. COMPARATIVE EVALUATION

In order to evaluate and compare the SWISS Rectifier, specified according to **Tab. II** with a standard buck-type ac-dc converter, i.e. the 6-switch buck-type PFC rectifier (cf. **Fig. 2**), several normalized performance indices are defined according to [7, 8]. Based on these performance metrics, a comparative evaluation of the proposed systems is performed graphically, as illustrated in **Fig. 11**. The power devices listed in **Tab. IV** are used for the assessment. An advantageous system would preferably cover the smallest area in the selected graphical representation.

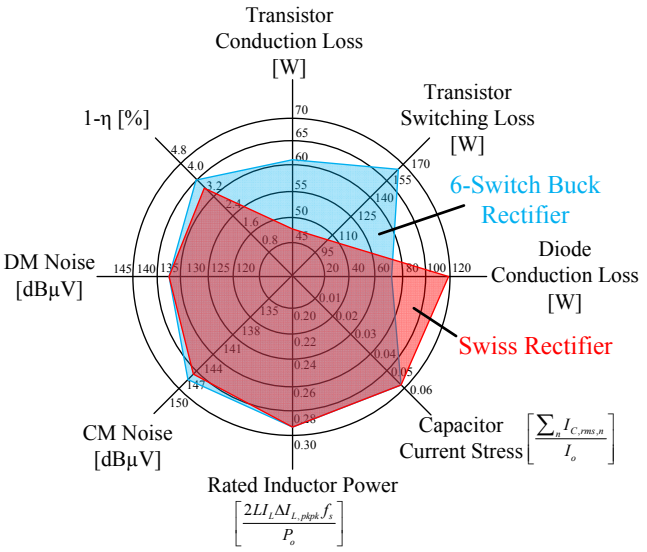

Fig. 11: Comparative evaluation of the Swiss Rectifier with the 6-switch buck-type rectifier. (The more advantageous system covers the smaller area in the diagram.)

The main advantage of the SWISS Rectifier is not only seen in the slightly higher achievable efficiency but also that the system can be controlled similar to a dc-dc converter. Accordingly, basic knowledge of the function of a buck-type dc-dc converter and a three-phase passive diode rectifier is sufficient to implement a three-phase PFC rectifier with sinusoidal input currents and a controlled output voltage.

VII. CONCLUSION

This paper proposes a novel three-phase unity power factor buck-type PFC rectifier, named the SWISS Rectifier, appropriate not only for high power EV battery charging systems, but also for power supplies for telecommunication, future more electric aircraft, variable speed ac drives, and high power lighting systems.

The complete design procedure of this system based on analytical expressions of the current stresses of the active and passive power components, including a simplified EMI DM/CM modeling for conducted emission and filter design, as well as the control analysis, has been described. Additionally, a 7.5 kW SWISS Rectifier hardware prototype has been implemented. Finally, the new rectifier concept has been compared with a conventional 6-switch buck-type PFC rectifier. According to the results, the SWISS Rectifier is a very suitable topology for the implementation of a buck-type PFC mains interface for an EV battery charger.

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