

Transient Behavior of Solid-State Modulators With Matrix Transformers

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Abstract—Solid-state modulators based on pulse transformers offer the advantage that, with the turns ratio of the transformer, the primary voltage could ideally be adapted to available switch technology, and a series connection of switches could be avoided. To increase the power level, several semiconductor switches must be connected in parallel, and a balancing between the different switches must be guaranteed. Here, the matrix transformer concept, which is based on multiple primary and/or secondary windings, as well as flux adding, offers superior performance with respect to the achievable rise times. However, the influence of the parasitic elements on the voltage and current distribution is quite involved. In this paper, the influence of the parasitic elements of the matrix transformer on the current balancing and on the winding voltages is investigated based on reluctance models. Additionally, the inherent current balancing of the matrix transformer for windings mounted on different cores is explained. Furthermore, the influence of parasitic load/transformer capacitances on the turnoff transient is discussed in detail.

Index Terms—Pulse power systems, pulse transformers.

I. INTRODUCTION

IN MANY pulsed-power applications, e.g., the medical, accelerator, or radar area, rectangular pulses with a flat top, a fast rise time, and variable pulsewidth are required. For generating such pulses with variable pulsewidth, three different modulator types can be used, i.e., direct-switch modulators [1], multicell-type generators (e.g., Marx generator) [2]–[6], and transformer-based modulators [7], [8], as well as a combination of the three.

In all of these modulator types, the achievable rise and fall times of the pulses are mainly determined by the parasitic capacitances and inductances in the power circuit, usually consisting of a capacitor bank, switches, interconnections, and the load. Due to the insulation requirements, the same minimal distances are required in the design of any type of modulator. Therefore, all modulator types basically can achieve similar minimal rise and fall times since these are determined by the parasitic, and the parasitics are closely linked with the insulation distance. Furthermore, the voltage droop of the pulse top is relatively independent of the modulator type since it is

determined mainly by the amount of stored energy and/or by an existing droop compensation. Consequently, no modulator concept has fundamental advantages with respect to the achievable transients and the voltage droop.

However, modulators based on pulse transformers offer an additional degree of freedom—the turns ratio—which enables the adaption of the primary voltage on the available switch technologies, so that, advantageously, standard semiconductor switches, which are used, e.g., in traction applications, can also be employed in solid-state modulators. Moreover, a series connection of switching devices with its critical dynamic voltage balancing could be avoided.

To increase the pulsed power of a transformer-based modulator system, the switches on the primary side of the transformer could be connected in parallel, which is basically simpler than a series connection. The current balancing between the parallel-connected switches could be, e.g., relatively simply achieved by scheduling the gate pulses with an active gate control, as shown in [9]. Moreover, for some special transformer concepts, e.g., the matrix/split core transformer, an inherent current balancing between the switches on the primary side is given in case there is a separate core for each switch, as will be explained in this paper. This further simplifies the design of the modulator system. Additionally, the matrix transformer leads to a reduction in the leakage inductance, which results in an improved pulse performance.

In order to fully utilize the core material and reduce the weight of the core, a reset circuit [10]–[13] is required, allowing a double flux swing during the pulse. This also reduces the leakage inductance since the volume between the primary and secondary windings decreases as the mean turns length decreases with a shrinking core area. The maximal allowed flux swing limits the maximal pulse duration for a given design, and for longer pulses, a larger core area of a large number of primary turns is required. The cooling of the transformer and the allowed negative voltage during premagnetization/reset of the core limits the maximal possible repetition rate, which, however, could be in the range of a few hundred hertz with a proper design. Based on active reset circuits [12], [14], the energy stored in the magnetizing inductance could be recovered, which increases the modulator efficiency and could simplify the circuit design since no additional supply for the reset circuit is required.

A second advantage of the transformer-based modulators is the reduction in the switching losses and the overvoltage at turnoff, due to the parasitic capacitance of the pulse transformer and the load. Additionally, this effect could result in faster turnoff times, as will be shown in this paper. The relation

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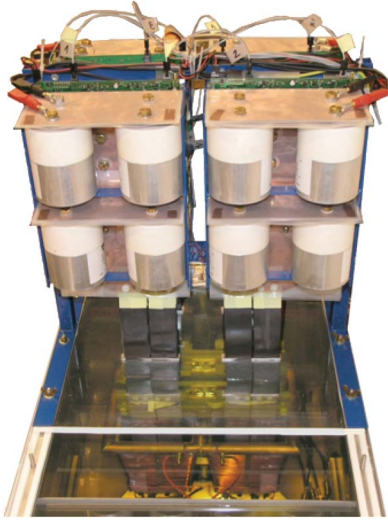


Fig. 1. Twenty-megawatt solid-state modulator with matrix (split core) transformer and the specifications given in Table I.

TABLE I
SPECIFICATION OF THE 20-MW 5- μ s PULSE MODULATOR WITH FOUR PARALLEL-CONNECTED IGBT MODULES AND MATRIX TRANSFORMER

DC Link Voltage V_{DC}	1 kV
Output Voltage V_{out}	170 kV
Pulse Duration T_{pulse}	5 μ s
Rise Time T_{rise}	< 500 ns
Output Power P_{out}	20 MW
Repetition Frequency f_{rep}	200 Hz
Conversion Ratio	1 : 170

between the parasitic capacitance and the leakage inductance must fulfill certain requirements, in order to achieve a fast rise time and a small overshoot, as discussed in [7].

So far, the inherent current sharing of the matrix transformer and the reduction in the turnoff losses for modulators with pulse transformer have not been explained in detail. Therefore, in Section II, first, the influence of the parasitic transformer/load capacitances on the turnoff transient is discussed. Thereafter, the focus is put on transformers with multiple windings and/or cores, which, in general, are called matrix transformers. First, the basic operating principle of the matrix transformer is shortly explained based on reluctance models and compared with other transformer designs in Section III. Additionally, the inherent current balancing between windings mounted on different cores is explained. Thereafter, the transient flux and voltage distribution in case of synchronous and asynchronous operations of the primary switches is explained, and measurement results for the solid-state modulator shown in Fig. 1 with the specifications given in Table I are shown in Section IV.

II. INHERENT CAPACITIVE TURNOFF “SNUBBER”

Independent of the chosen modulator type, the series inductance L_{Com} in the commutation path, which consists, e.g., of the parasitic inductances in the switches, the interconnections, and the capacitor bank, results in overvoltages during turnoff. In Fig. 2(a), the turn-on and turnoff behaviors of a 1.7-kV 3.6-kA insulated-gate bipolar transistor (IGBT) module connected to a

resistive load are shown. Here, clearly, the resulting overvoltage at turnoff of approximately 200 V could be seen, which is caused by $L_{Com} = 40$ nH and $di/dt \approx 5000$ A/ μ s.

In order to limit the overvoltages to safe levels, usually, a reduction in the di/dt and, therewith, an increase in pulse fall time are required. However, with multistage gate drives using different gate resistors during turnoff or gate drives with Zener clamping [9], the overvoltage could be limited without increasing the pulse fall time and increasing the switching losses.

In transformer-based power modulators, however, the distributed capacitance of the pulse transformer helps to limit the overvoltage and also reduce the switching losses without multistage gate drives, as will be explained based on the circuit diagram shown in Fig. 3(a). Here, a simplified equivalent circuit of a single-switch transformer-based power modulator with capacitor bank, semiconductor switch, simple transformer model, and resistive load is shown. L_{Com} is the series inductance in the commutation path, comprising the parasitic inductance of the capacitor bank, the switch, and the interconnection between the capacitor bank and the switch. L_{σ} represents the leakage inductance, L_{mag} is the magnetizing inductance of the transformer, and C_d is the distributed capacitance of the pulse transformer transferred to the primary side.

During the pulse, capacitance C_d is approximately charged to the input voltage V_{dc} (cf. Fig. 3). Assuming a relatively large capacitance C_d , where V_{C_d} changes significantly slower than V_{CE} , the voltage across the parasitic inductors L_{Com} and L_{σ} becomes negative as soon as the switch S_1 is turned off and the voltage V_{CE} starts to rise, as could be seen in the simulated waveforms given in Fig. 3(b). Therefore, the current in the inductors and in the switch S_1 immediately start to decrease.

As soon as the current in the inductor L_{Com} also reaches zero, the voltage across the inductor becomes zero. At this point of time, V_{CE} drops relatively fast to the value $V_{dc} - V_{C_d}$, as could be seen in Fig. 2(b), where the negative voltage drop (oscillation) in the rising edge of V_{CE} occurs. At this time, the voltage of capacitor C_d will also be smaller than the input voltage V_{dc} since C_d is discharged, on the one hand, by the magnetizing current and, on the other hand, by the difference of the load current and $i_{L_{\sigma}}$.

After the current in the inductor L_{Com} reached zero, the rise time of the voltage $V_{CE} = V_{dc} - V_{C_d}$ is mainly determined by the voltage across the capacitance C_d , which is further discharged by the magnetizing current and the load current. Consequently, no overvoltage can be caused by the series inductance L_{Com} . The overvoltage in Fig. 2(b) results from the forward bias of the freewheeling path, where the energy stored in the magnetizing inductance is recovered to premagnetize the core shortly before the next pulse [14]. Due to the turnoff “snubber,” the IGBT can be turned off much faster, which allows a significant reduction in the turnoff losses, compared with the case without capacitor C_d .

However, for large values of C_d , dv/dt could be limited by C_d , so that the rise times increase. In pulsed-power systems with loads having a relatively large parasitic capacitance, e.g., klystrons, similar effects can be observed, even without transformers.

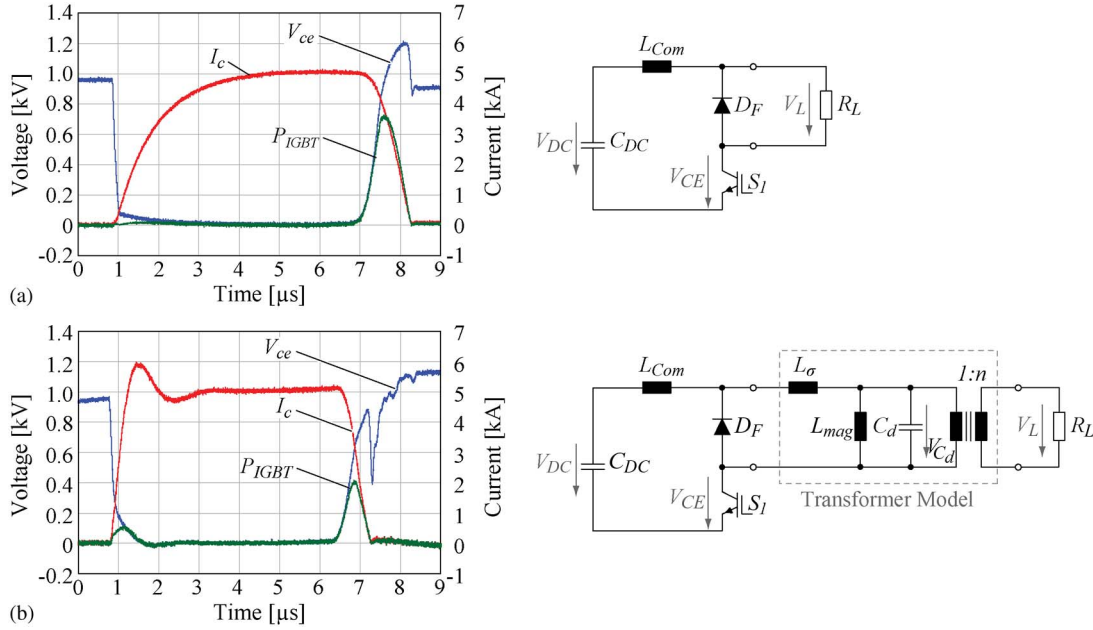


Fig. 2. Measured collector–emitter voltage V_{CE} , collector current I_C , and switching losses P_{IGBT} of a 1.7-kV/3.6-kA IGBT with (a) resistive and (b) capacitive load. Additionally, the respective measurement circuits are shown.

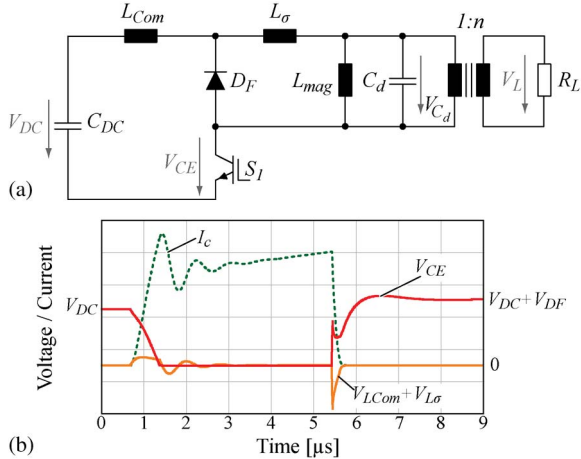


Fig. 3. (a) Equivalent circuit of the single-switch transformer-based power modulator with transformer parasitics, as leakage inductance L_σ , magnetizing inductance L_{mag} , and distributed capacitance C_d . Assuming a purely resistive load, i.e., $C_d = 0$, the series inductance L_{Com} in the commutation path causes overvoltages during turnoff. (b) Simulated collector current I_C , collector–emitter voltage V_{CE} , and voltage across L_{Com} and L_σ for $C_d > 0$, i.e., soft turnoff.

III. MATRIX TRANSFORMERS

In the previous section, the influence of the distributed capacitance C_d on the turnoff transient and the related reduction of the losses/pulse rise time has been discussed. This effect is relatively independent of the transformer configuration. The configuration, however, strongly influences the transient voltage and current distribution in the solid-state modulator, as will be explained here.

In the most simplest case, the pulse transformer of the modulator has only one primary and one secondary winding wound around a core. Considering the pulse specifications given in Table I, i.e., $V_{out} = 170$ kV and $P_{out} = 20$ MW, in the first step of the design process, the turns ratio must be chosen.

The turns ratio is strongly related to the applied switching technology due to the operating/blocking voltage. At the moment, the highest power rating of a single semiconductor switch that is capable of achieving the required rise time of smaller than 500 ns is standard 1.7-kV IGBT modules. These IGBTs are available for pulse currents of approximately 7.2 kA, resulting in a pulsed power of ≈ 7 MW per switch, if an operating voltage of 1 kV is assumed. With these high-power modules, the achievable rise/fall times are mainly limited by the housing designed for applications with low switching speeds, e.g., traction or high-power drives [15].

Based on the aforementioned maximum pulsed-power ratings of the 1.7-kV IGBT modules, a series or parallel connection of four IGBT modules ($\approx 4 \times 7$ MW) would be required for the modulator system with the specifications in Table I, if additional safety margins and the requirement to handle the magnetizing current are considered.

In general, with a series connection, the static and dynamic balancing of the voltage distribution between the different switches is critical and requires either passive balancing elements, which generate additional losses, or a highly dynamic gate drive and measurement setup for actively balancing the voltages. Furthermore, usually, a derating of the switches is necessary due to dynamic overvoltages. In case of a failure, e.g., the turn-on of one switch in the series connection is delayed, the resulting overvoltage across the delayed switch could lead to the destruction of the modulator.

On the other hand, connecting several switches in parallel requires a current balancing, which could be achieved, e.g., by scheduling the gate signals with an active gate drive, as presented in [9]. In case of a failure, one switch would have to conduct a higher current than in the nominal case, which, however, is less critical than an overvoltage.

Based on these considerations, a parallel connection of four 1.7-kV 3.6-kA IGBT modules and a standard transformer with

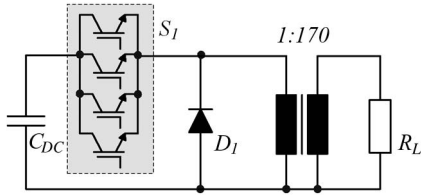


Fig. 4. Parallel-connected IGBTs and transformer with a turns ratio of 1 : 170.

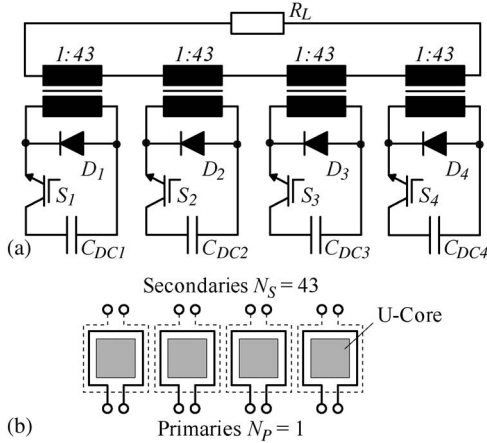


Fig. 5. (a) Series connection of four transformers with a turns ratio of 1 : 43 and parallel-connected storage capacitors. (b) Schematic sketch of the four transformers.

a turns ratio of 1 : 170, as shown in Fig. 4, is the best initial solution. Since the leakage inductance of the transformer, which limits the pulse rise time

$$T_{\text{Rise}} \sim \sqrt{L_P C_P} \quad (1)$$

depends quadratically on the number of turns, the best choice for the number of primary turns is $N_P = 1$. In (1), L_P denotes the parasitic inductance, and C_P is the parasitic capacitance of the modulator, including the transformer with its parasitics.

The number of secondary turns is $N_S = 170$, resulting in a relatively large leakage inductance. Furthermore, an additional control circuitry is required in order to obtain a symmetric current distribution between the parallel-connected switches.

By replacing the single standard transformer by a series connection of four transformers with a turns ratio of 1 : 43 and a slightly reduced input voltage of $V_{dc} = 0.988$ kV, as shown in Fig. 5(a), the current balancing problem could be avoided. Here, the secondary windings are all connected in series, so that the secondary current is the same for all four transformers. Due to the Magnetic Flux Law, the primary currents consequently must be the same, so that the currents in the primary winding and/or the IGBTs are always balanced.

In addition, the voltage balancing on the secondary and primary is inherently guaranteed since, on the one hand, the primary voltages are directly determined by the parallel-connected storage capacitors, which are charged up by the same supply, and, on the other hand, the secondary voltages are given by the turns ratio.

Even in case of failure, if, e.g., one of the four switches is not, or delayed in, turning on, this transformer configuration

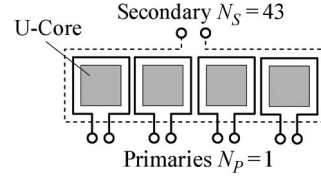


Fig. 6. Schematic sketch of a matrix transformer with four primaries wound on four separate U-cores and a secondary winding enclosing all four cores.

avoids overloads/overcurrents of single switches. In such a case, the output voltage and, consequently, the output power are limited to three fourths of its nominal value in the considered example. The current flowing in the secondary winding of the transformer, whose switch has not turned on yet, induces a current in the primary circuit, which flows through the free-wheeling diode on the primary side, i.e., in the same direction as the switch would be turned on. Therefore, the primary voltage is approximately zero, and no power is transferred to the secondary.

Consequently, the parallel/series connection of four individual transformers solves the balancing problem. However, compared with the standard 1 : 170 transformer, a reduction in the parasitic elements of the achievable rise time [cf. (1)] cannot be achieved.

The total parasitic inductance of the four transformers is a quarter of the standard transformer’s inductance, but the parasitic capacitance is four times higher, so that, in total, the achievable rise time does not change. However, the characteristic impedance of the transformer ($= \sqrt{L_P/C_P}$) is reduced, which results in a larger overshoot at the end of the rising edge.

The parasitic inductance and capacitance of the transformer are largely determined by the distance between the primary and secondary windings, whereas the distance is given by the maximum electric field and/or the voltage between the primary and secondary. Therefore, the voltage distribution of the four individual transformers is basically the same as that of the standard transformer, if a parallel connection of all four primaries is assumed.

Considering an inductive adder topology [16], where each primary circuit is related to an independent electric potential, the distances between each primary and secondary winding could be reduced, which results in a smaller leakage inductance. Here, it is important to minimize the coupling capacitance between all primaries and ground since the additional coupling capacitance also has to be charged during the rising edge of the pulse.

However, due to the isolation of the primary circuits and related charging power supplies, the circuit complexity significantly increases.

Another method to reduce the leakage inductance is enclosing all four cores by a single secondary winding, so that the flux in the four cores adds up in the secondary winding (cf. Fig. 6). Due to adding the fluxes, the voltage induced in the secondary also multiplies by four ($V \sim Nd\Phi/dt$). Therefore, the number of turns on the secondary is also $N_S = 43$ for generating an output voltage of 170 kV. As the secondary winding encloses all four cores, some volume between the primary and secondary windings is saved, as shown in Fig. 7. The saved volume

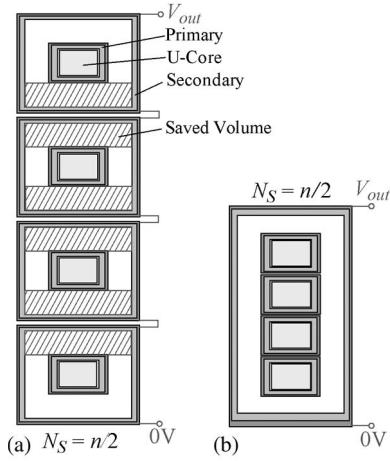


Fig. 7. Saved volume between the primary and secondary windings, resulting in a reduced leakage inductance when using (b) the matrix transformer, instead of (a) a transformer series connection.

directly results in a reduced leakage inductance, compared with the series connection of the standard transformers.

In general, this transformer configuration is called the matrix transformer [17], where the conversion ratio between the primary and secondary voltages is not only defined by the turns ratio but also by the ratio of enclosed core areas, i.e., enclosed flux shares [17]. Here, the voltage ratio is given by

$$\frac{V_S}{V_P} = \frac{N_S}{N_P} \frac{A_S}{A_P} \quad (2)$$

where V_ν denotes the winding voltage, N_ν is the number of turns, and A_ν is the area enclosed by winding ν .

Since the primary windings are electrically isolated and, therefore, only a magnetic coupling via the secondary exists, the dc input voltage could be supplied by a single source, which further simplifies the circuit design of the modulator system. In addition to the matrix transformer, in literature, split-core fractional turn [18] transformer and inductive adders [16] have also been proposed. However, these are just special cases of the matrix transformer concept.

Similar to the configuration with four individual transformers, a matrix transformer with only one primary and/or secondary winding on each core also has the property of inherent current sharing between the primary circuits ($C_{DC\nu}$, S_ν , and D_ν), even if the switches do not turn on at the same time or the parasitic resistances in the circuits are different.

This feature is explained with an equivalent circuit of the matrix transformer consisting of two cores, as shown in Fig. 8(a). In the equivalent circuit, the transformer is replaced by its reluctance model based on the simplified Ampere's and Faraday's law [19] [cf. Fig. 8(b)]. The quantity \mathfrak{R} represents the magnetic reluctance, and the product $N \cdot I$ is known as the magnetomotive force (MMF). Based on Ohm's law

$$N \cdot I = \mathfrak{R} \cdot \Phi \quad (\rightarrow V = R \cdot I) \quad (3)$$

and Kirchhoff's voltage (VL) and current law (CL)

$$\text{VL} : N \cdot I = \Phi \cdot (\mathfrak{R}_1 + \mathfrak{R}_2 \cdots + \mathfrak{R}_n) \quad (\text{for a given path})$$

$$\text{CL} : \Phi_1 + \Phi_2 + \cdots + \Phi_n = 0 \quad (\text{for a given node}) \quad (4)$$

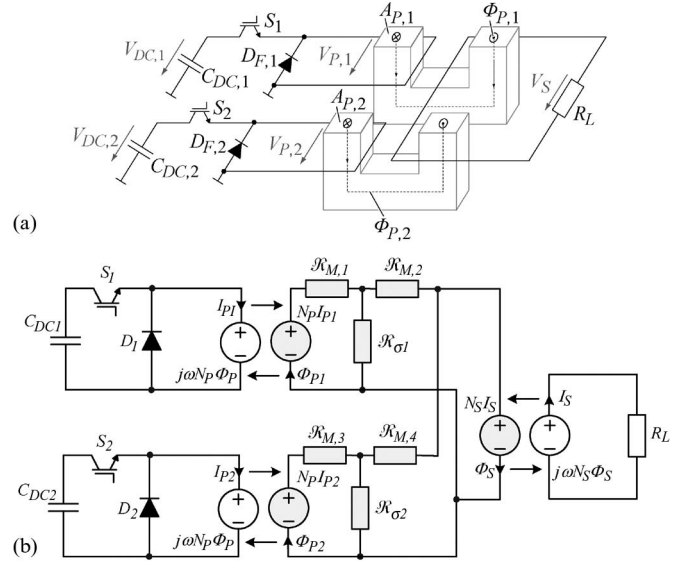


Fig. 8. (a) Simplified matrix transformer consisting of two cores and (b) equivalent circuit for the matrix transformer based on a reluctance circuit (shaded) for the transformer.

for the magnetic circuit, it could be seen that both primary MMF sources ($N_P I_{P1}$ and $N_P I_{P2}$), which correspond to voltage sources in an electric circuit, have to be in the same order of magnitude as the secondary MMF source $N_S I_S$ in order to limit the flux in the cores. Since, for both primary windings, the same number of turns is assumed, this results in similar values for the currents, i.e., $I_{P1} \approx I_{P2}$. If one of the primary MMF sources is significantly different, compared with the secondary source, the flux in the related core will rapidly change. Due to the changing flux, a voltage is induced in the primary winding ($v = Nd\Phi/dt$), which tries to cause a current flow that balances the MMFs.

In the case where one of the primary switches, i.e., S_1 or S_2 , turns on later than the other one, the current that is induced due to the balancing of the MMF sources flows via the respective freewheeling diode $D_{F,\nu}$. As soon as the delayed switch turns on, the conducting freewheeling diode is hard commutated. Depending on the recovery time of the diode, this could lead to a large reverse recovery current and losses.

In order to avoid this commutation in case of a delayed turn-on, each primary circuit could have a winding around each core, as shown in Fig. 9 [20]. However, in case of mismatched turn-on and turnoff times of the switches S_1 and S_2 , the switch current can reach twice the nominal current, due to the additional winding. Therefore, with this solution, on the one hand, the complexity of the transformer design significantly increases. On the other hand, an overload of the switch turning on early could happen. Furthermore, the additional windings are not really necessary since the switching operation could be synchronized relatively simply by an active gate control, as explained in [9]. Here, the rising and falling edges of the switch currents and voltages are measured, and gate signals are scheduled, so that all switches are turned on at the same time. The required current measurement is also used for overcurrent protection of the modulator.

In case of asynchronous switching times, the output voltage of the matrix transformer without cross-coupled windings is

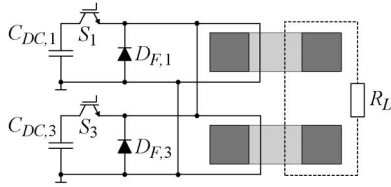
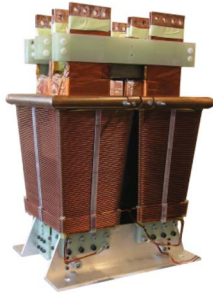
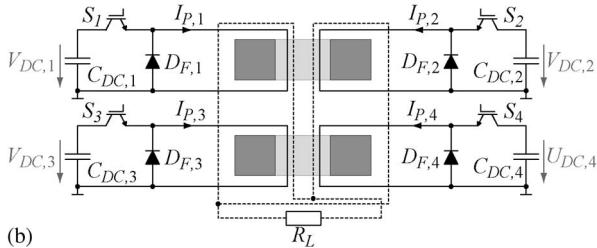


Fig. 9. Cross coupling of primary windings for avoiding turn-on of a free-wheeling diode in case the switches do not turn on synchronously.



(a)



(b)

Fig. 10. (a) Transformer and (b) schematic of the solid-state modulator with two cores, two primary windings around each core, and secondary enclosing both cores.

smaller than the nominal voltage during the conduction interval of the freewheeling diode since the primary circuit with the conducting diode does not generate a flux in the secondary. This could be used to shape the pulse or to compensate the voltage drop of the input capacitors by sequentially turning on the switches in case the modulator has several switches.

Summing up, the matrix transformer basically shows the same behavior as the series connection of standard transformers, as shown in Fig. 5(a). However, due to the reduced leakage inductance, an improved pulse performance could be achieved.

IV. RELUCTANCE MODEL

Based on the considerations about matrix transformers in Section III, now the transient behavior of the matrix transformer applied in the considered power modulator (cf. Fig. 1 and Table I) is discussed more in detail. In Fig. 10, the transformer and a circuit diagram of the modulator are given. The transformer consists of two cores, instead of four, in order to limit the circuit complexity and the magnetizing current. Each core carries two primary windings, and the four primaries are distributed to the four legs of the two U-cores.

The secondary winding encloses both cores in order to add the fluxes, as described in Fig. 8. Additionally, the leakage inductance and the current density in the winding are reduced by connecting two secondary windings in parallel, each enclosing the two legs of the two cores on one side. With the reduction in

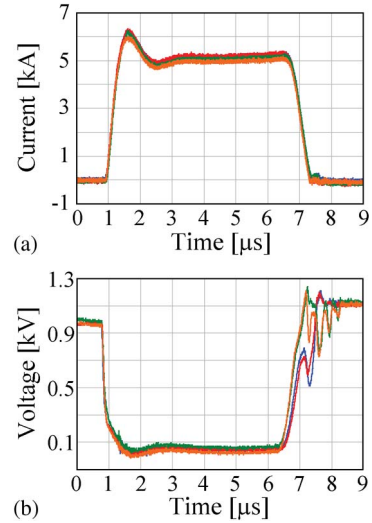


Fig. 11. Measured (a) current and (b) voltage distribution between the four primary windings of the transformer shown in Fig. 10.

leakage inductance, the distributed capacitance is increased, so that, in total, the achievable rise time is not changed.

Since there are two windings on each core, an inherent current balancing is only given between the sum currents $I_{P,1} + I_{P,2}$ and $I_{P,3} + I_{P,4}$ [cf. Fig. 10(b)]. The current balancing between S_1 and S_2 , as well as between S_3 and S_4 , must be actively balanced, e.g., by the scheduling method described in [9]. With this current-balancing method, simultaneous switching times are achieved, as shown in Fig. 11, and the freewheeling diodes do not turn on and do not have to be commutated hard (cf. previous section).

A simplified reluctance model of the matrix transformer is shown in Fig. 12. This consists of four MMF sources for the primary windings, one MMF source for the secondary, the reluctances for the core R_{mag} , and the leakage paths $R_{\sigma,\nu}$. The geometric arrangement of the windings is shown by gray dashed lines for clarifying the model.

The flux distribution for the ideal case, when all four switches simultaneously turn on, is shown in Fig. 13(a). Here, the two fluxes of the primary winding are added in the secondary winding, and the flux in the leakage paths is determined by the MMF sources of the primary windings.

In the following, the situation of asynchronous switching and the influence of the matrix transformer on the voltage/current distribution are considered. Assume, e.g., that switch S_1 turns on before the other three switches. In this case, MMF source 1, i.e., $N_{P,1}I_{P,1}$, causes a flux distribution, as given in Fig. 13(b), until the other three switches also turn on.

Due to the matrix transformer configuration, *Core 2* is magnetically coupled to the primary winding $W_{P,1}$ via the secondary winding, which induces a flux in *Core 2*, so that the effective magnetizing inductance is doubled, i.e., the two cores are connected in parallel and the effective reluctance seen by $W_{P,1}$ is halved in case nothing would be connected to windings $W_{P,3}$ and $W_{P,4}$. However, in the considered case, the freewheeling diodes are connected across the windings, which influences the current and the flux distribution. Before this is

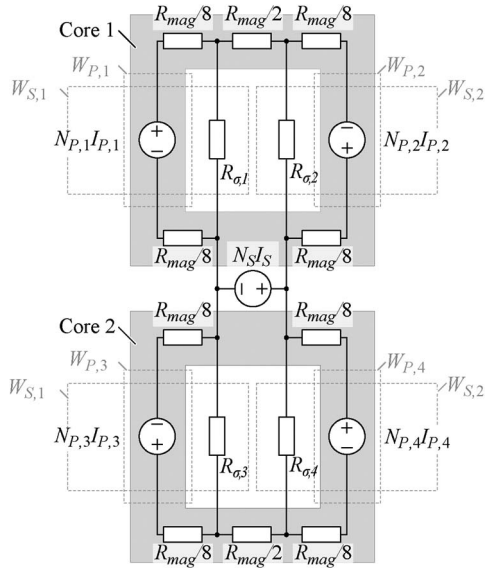


Fig. 12. Reluctance model of the transformer shown in Fig. 10. $W_{P,1}-W_{P,4}$ are the primary windings, and $W_{S,1}$ and $W_{S,2}$ are the parallel connected secondary windings. $R_{mag} = N_P^2/L_{mag}$ is the reluctance of the magnetic core, and R_{σ} describes the leakage between the primary and secondary windings. In the model, the magnetic coupling between the primary windings on different cores is neglected as it has no influence on the transient behavior.

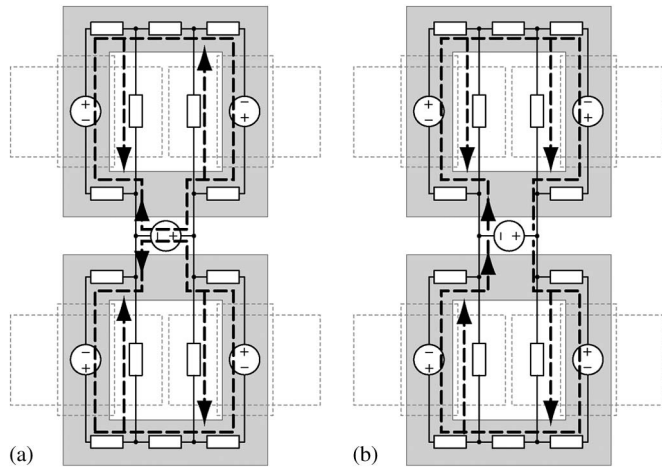


Fig. 13. Flux distribution in the reluctance model given in Fig. 12 for (a) synchronous turn-on of all switches and (b) in case switch S_1 is turned on and the three switches are delayed.

explained, first the situation for the second winding on Core 1 is considered.

In Core 1, the flux through winding $W_{P,2}$ is in the same direction as it would be in the synchronous case, i.e., the induced voltage $W_{P,2}$ has the same polarity as in normal operation and the voltage across switch S_2 decreases. Consequently, the switching losses of switch S_2 are reduced due to the reduced voltage.

The rising edge of the voltage across $W_{P,2}$ is approximately synchronous to that of $W_{P,1}$, although the rising current edge is delayed until S_2 closes since there is no alternative current path in the required direction. The flux in the leakage path $R_{\sigma,2}$, however, is in inverse direction, compared with normal operation. Therefore, the current rise in primary circuit $W_{P,2}$ is

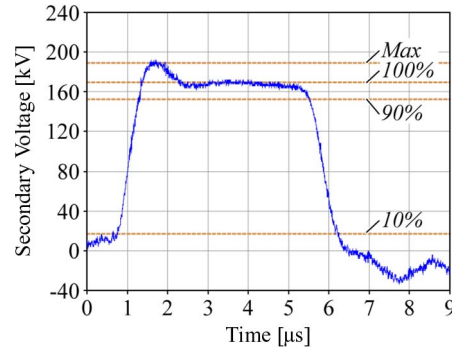


Fig. 14. Full-load output voltage of the modulator with matrix transformer and IGBT synchronization, as shown in Fig. 1.

slower since the flux in the leakage inductance must be reversed when S_2 turns on.

In windings $W_{P,3}$ and $W_{P,4}$, the situation is different. Here, the flux in the windings is in the opposite direction, and the flux in the leakage path is in the same direction, compared with the normal operation given in Fig. 13(a). The inverse flux in the windings results in an inverted voltage at the winding terminals, which is clamped by the freewheeling diodes. The freewheeling diodes keep the voltage constant and the rate of rise of the flux in $W_{P,3}$ and $W_{P,4}$ to very small values. Winding $W_{P,1}$ sees the two freewheeling diodes D_3 and D_4 parallel connected in series to the load R_L and the effective magnetizing inductance seen by $N_{P,1}I_{P,1}$ is equal to the one of Core 1. Due to the freewheeling diodes, the current edges are synchronous with S_1 , but the voltage edges are delayed until the currents are commutated by the switches S_3 and S_4 .

It is important to note that the resulting current in $W_{P,3}$ and $W_{P,4}$ is in the same direction as in the case where switches S_3 and S_4 would be turned on, so that the MMF sources have the correct polarity. This and the flux driven by $W_{P,1}$ lead to a flux direction in the leakage paths $R_{\sigma,3}$ and $R_{\sigma,4}$ of $W_{P,3}$ and $W_{P,4}$, which is the same as in the synchronous case, so there is no additional delay in the currents for reversing the leakage flux as with $N_{P,2}I_{P,2}$.

Considering the described situation, it could be seen that the current edges and the voltage edges are influenced by the matrix transformer and by the turn-on sequence of the single switches. Assuming, for example, that S_1 and S_2 turn on at the same time, then all the rising current edges would be synchronous, although S_3 and S_4 have not turned on yet. The rising edges of the winding voltages, however, are not synchronous, because not all switches are turned on at the same time. For synchronizing the switching transients of all four IGBTs, it is therefore necessary to synchronize the current and the voltage rising edges, e.g., by the scheduling concept presented in [9]. Based on this synchronization method and the matrix transformer with its advantageous characteristics regarding the parasitics and the parallel connection, the full-load output voltage as shown in Fig. 14 is achieved with the modulator system shown in Fig. 1. Here, the overshoot is 10% and almost exactly meets the calculated value of 11% with ohmic load. In combination with a load, which behaves more capacitively as, e.g., a klystron, the overshoot decreases to the required 3%.

Note: In the case previously described, the freewheeling diodes started to conduct/clamp the winding since both switches of the primary circuits mounted on the same core—*Core 2* in this case—are delayed. If one of the two switches— S_3 or S_4 in the considered case—turns on at the same time as S_1 , the freewheeling diodes would not conduct. Therefore, by having more than one primary circuit connected to a core, the probability that a freewheeling diode has to be commutated hard decreases significantly.

V. CONCLUSION

In this paper, the transient flux distribution in the cores and the voltages across the primary windings during turn-on and turnoff of modulators with matrix transformers have been investigated based on reluctance models. In addition, the inherent current edge synchronization in windings on different cores of the matrix transformer has been explained in detail. Furthermore, the influence of parasitic capacitances on the overvoltage and switching losses at turnoff has been discussed.

With deeper understanding of the matrix transformer and its influence on the transients, a better design and a higher performance of solid-state modulators with the matrix transformer are possible.

REFERENCES

- [1] M. P. J. Gaudreau, J. Casey, T. Hawkey, J. M. Mulvaney, and M. A. Kempkes, "Solid-state pulsed power systems," in *Conf. Rec. 23rd Int. Power Modulator Symp.*, Jun. 22–25, 1998, pp. 160–163.
- [2] R. L. Cassel, "An all solid state pulsed Marx type modulator for magnetrons and klystrons," in *Proc. IEEE PPC*, Jun. 13–17, 2005, pp. 836–838.
- [3] L. M. Redondo, H. Canacsinh, and J. F. Silva, "Generalized solid-state Marx modulator topology," *IEEE Trans. Dielectr. Elect. Insul.*, vol. 16, no. 4, pp. 1037–1042, Aug. 2009.
- [4] L. M. Redondo and J. F. Silva, "Repetitive high-voltage solid-state Marx modulator design for various load conditions," *IEEE Trans. Plasma Sci.*, vol. 37, no. 8, pp. 1632–1637, Aug. 2009.
- [5] J. W. Baek, D. W. Yoo, G. H. Rim, and J.-S. Lai, "Solid state Marx generator using series-connected IGBTs," *IEEE Trans. Plasma Sci.*, vol. 33, no. 4, pp. 1198–1204, Aug. 2005.
- [6] C. J. T. Steenkamp and M. P. Bradley, "Active charge/discharge IGBT modulator for Marx generator and plasma applications," *IEEE Trans. Plasma Sci.*, vol. 35, no. 2, pp. 473–478, Apr. 2007.
- [7] J. Biela, D. Bortis, and J. W. Kolar, "Modeling of pulse transformers with parallel- and non-parallel-plate windings for power modulators," *IEEE Trans. Dielectr. Elect. Insul.*, vol. 14, no. 4, pp. 1016–1024, Aug. 2007.
- [8] Y.-H. Chung, H.-J. Kim, and C.-S. Yang, "MOSFET switched 20 kv, 500 a, 100 ns pulse generator with series connected pulse transformers," in *Proc. IEEE Pulsed Power Plasma Sci. Conf.*, 2001, vol. 2, pp. 1237–1240.
- [9] D. Bortis, J. Biela, and J. W. Kolar, "Active gate control for current balancing of parallel-connected IGBT modules in solid-state modulators," *IEEE Trans. Plasma Sci.*, vol. 36, no. 5, pp. 2632–2637, Oct. 2008.
- [10] R. J. Adler, J. Stein, B. Ashcraft, and R. J. Richter-Sand, "Improvements in pulse transformer performance achieved using pulsed reset circuitry," in *Proc. 11th IEEE PPC*, 1997, vol. 1, pp. 616–620.
- [11] D. Bortis, J. Biela, and J. W. Kolar, "Optimal design of a DC reset circuit for pulse transformers," in *Proc. 22nd IEEE APEC*, 2007, pp. 1171–1177.
- [12] D. Bortis, J. Biela, and J. Kolar, "Design and control of an active reset circuit for pulse transformers," *IEEE Trans. Dielectr. Elect. Insul.*, vol. 16, no. 4, pp. 940–947, Aug. 2009.
- [13] L. M. Redondo, J. F. Silva, P. Tavares, and E. Margato, "Solid-state Marx generator design with an energy recovery reset circuit for output transformer association," in *Proc. IEEE PESC*, 2007, pp. 2987–2991.
- [14] J. Biela, D. Bortis, and J. W. Kolar, "Reset circuits with energy recovery for solid-state modulators," *IEEE Trans. Plasma Sci.*, vol. 36, no. 5, pp. 2626–2631, Oct. 2008.
- [15] J. Biela, D. Aggeler, D. Bortis, and J. W. Kolar, "5 kV/200 ns pulsed power switch based on a SiC-JFET super cascode," in *Proc. IEEE Int. Power Modulators High Voltage Conf.*, 2008, pp. 358–361.
- [16] R. L. Cassel, J. E. Delamare, M. N. Nguyen, G. C. Pappas, E. Cook, J. Sullivan, and C. Brooksby, "The prototype solid state induction modulator for SLAC NLC," in *Proc. IEEE Particle Accelerator Conf.*, 2001, vol. 5, pp. 3744–3746.
- [17] E. Herbert, "High frequency matrix transformer," U.S. Patent 4 845 606, Jul. 4, 1989. [Online]. Available: <http://www.eherbert.com>
- [18] M. L. W. Crewson and D. K. Woodburn, "A new solid state high power pulsed modulator," in *Proc. 5th Modulator-Klystron Workshop Future Linear Colliders*, Apr. 2001, S2-3.1–7.
- [19] A. F. Witulski, "Introduction to modeling of transformers and coupled inductors," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 349–357, May 1995.
- [20] W. Crewson and D. K. Woodburn, "Power modulator having at least one pulse generating module; multiple cores; and primary windings parallel-connected such that each pulse generating module drives all cores," Patent U.S. 2003/0 128 554 A1, Jul. 2003.



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