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***Abstract*—This paper addresses the timely issues of modeling, and defining selection criteria for, a solid-state fault isolation device (FID) intended for use in power electronics-based distribution systems (PEDS). The paper subsequently derives the FID parameters in the PEDS envisioned under a new multi-university Engineering Research Center funded by the US National Science Foundation. When conventional circuit breakers are used in distribution systems, they have relatively long clearing times, causing feeder voltages to be reduced for a significant amount of time. Although acceptable in convention systems, this relatively long clearing time would cause significantly long, complete voltage collapses in a PEDS. Sensitive loads such as computers would fail even if the voltage returns within a few seconds. However, if a semiconductor circuit breaker were to be used instead of the conventional system, it would be able to switch fast enough to keep the time of voltage disturbances within acceptable limits. This paper discusses the management of the overvoltage resulting from very fast circuit breaker operation through the use of passive clamping devices and *di/dt* control during turn-off. The paper includes experimental results at medium voltage from a developed hardware prototype. In addition, a validated simulation model of a medium voltage FID was developed for future studies. Simulation results are presented.**

I. INTRODUCTION

In traditional utility type medium-voltage ac power systems, mechanical circuit breakers clear and isolate faults in the shortest possible time (up to several line periods) to allow the continuation of power delivery through the system. Despite the usage of these fast acting mechanical circuit breakers, short disruptions of power flow during faults on an ac distribution system can lead to significant disturbances at critical loads [1]-[3]. Power quality is subject to such effects as availability, voltage distortion, and deviations from nominal values (voltage, frequency) over short periods of time. Power electronics converters and systems can be regarded as one solution to increase power quality in the grid and to integrate distributed renewable energy sources into today's power systems [2].

In power electronics-based distribution systems (PEDS), a solid-state transformer (SST), rather than a traditional transformer, will be used to enable active management of distributed renewable energy resources and loads. Since the SST is a power electronics device, it can provide current limiting functionality for the entire distribution system. However, in order to limit the fault current, the SST will lower the system voltage significantly in all feeders on the secondary side, which is not the case in a conventional distribution system with standard transformers. Hence, it becomes vitally necessary that the circuit breaker disconnect the faulted section as fast as possible to allow for the SST to quickly restore the system voltage after a fault [4].

The simplified three-phase PEDS, shown in Figure 1, was chosen for the purpose of simulating line currents and voltages under normal and fault conditions in order to understand the target specifications and features of a solid-state fault isolation device (FID). Figure 2 shows the grid current and voltage as observed on the secondary side of either of the solid-state transformers during a three-phase fault for the system of Figure 1. Due to the limited short term current carrying capability of the semiconductors within the SST, it has to limit the fault current to approximately two times the rated current. As shown in Figure 2, this inherent fault current limitation causes a significant voltage drop in the entire PEDS. The FID must provide ultra-fast isolation of the fault to quickly restore system voltage to minimize the required ride-through capacities in the system. Thus, very high speed operation of the FID (fault clearing within a few μs) becomes a very desired feature of an FID operating in a PEDS.

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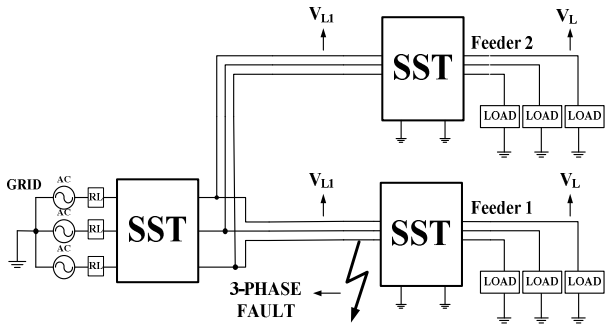

Figure 1. The representative portion of a PEDS

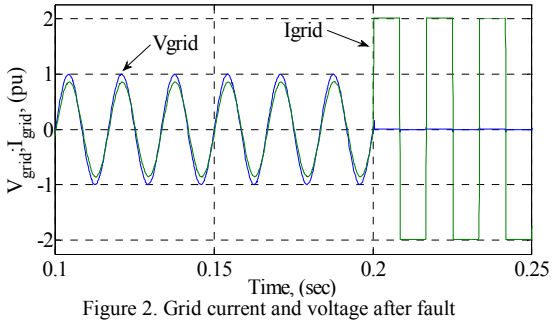

Figure 2. Grid current and voltage after fault

II. SOLID-STATE FID DESIGN

The preferred FID topology for medium voltage applications consists of a configuration of three IGBT modules in series, with each module containing two emitter-connected IGBTs together with freewheeling diodes similar to [5]. This topology is shown in Figure 3. By taking advantage and making use of commercially available, emitter-connected IGBT modules, this topology does not require separate driver circuits or series diodes.

During FID operation, balancing the voltages of the series IGBT modules and control of turn-off overvoltages at their collectors under all operating conditions is critical, as they are directly responsible for the system reliability. In the series connection, as shown in Figure 3, the operating voltage of the FID must be evenly distributed and balanced across each of the individual IGBTs, else the module might be damaged and the overall device might fail [6].

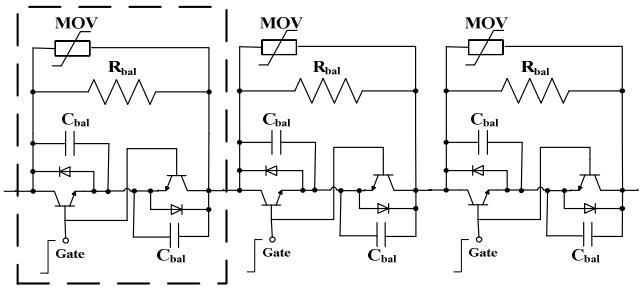

Figure 3. Preferred FID totology for the PEDS

Another key aspect of transient operation is the overvoltage that occurs across the device at turn-off due to stored energy in the line inductance. Though ultra-fast interruption provides very desirable quick isolation of faulted portions of the distribution system, measures must be taken to avoid the large overvoltage resulting from rapid turn-off of the fault current. One method of overvoltage management is to adjust the gate resistance of the IGBT driver to increase turn-off time. As mentioned above, when implemented in the distribution system, the amount of overvoltage that the FID will experience will be determined by factors, such as line impedance, that will change depending on where the FID is placed in the system. Thus, it has become important that active *di/dt* control [7] needs to be explored in addition to the overvoltage management methods described above. Also, to guarantee overvoltage protection during the turn-off event, metal oxide varistors (MOVs) were implemented as shown in Figure 3.

A. FID Circuit Modelling and Simulation

To verify the operation of FID and study its transient recovery voltage (TRV) behavior, including different circuit elements and their parasitics, a detailed circuit model of the medium-voltage 5 MW experimental setup is developed and simulated using SIMetrix® SPICE analog circuit simulator. The FID circuit model used for simulation is shown in Figure 4. As can be seen, the circuit has three major parts: the input voltage source, the FID, and the controller. Similar to the available experimental circuit, the 5 MW variable ac voltage source contains an *LC*-output filter which connects to FID circuit through a 466/4.16 kV step-up transformer as shown in Figure 4.

The corresponding model for each part is shown in Figure 4. All the values are referred to the secondary-side (high voltage side) of the transformer. In the *LC*-filter model, R_d is a virtual element included to model the active damping control of the converter system. In modeling the transformer, the effect of the measured parasitic inter-winding capacitance, C_T, on the high voltage side is also included. TRV behavior of FID, with and without this parasitic capacitance, is of special importance. In modeling FID, the same circuit topology as in Figure 3 is adopted and implemented using 6.5 kV, 200 A Si-IGBT device models. The controller in Figure 4 consists of a logic circuit which detects whenever I_{FID} reaches a threshold level, which is 50A in this case. The required gating signals are then produced. All the circuit parameters are shown in Table 1.

Simulations are carried out to investigate the sharing of the blocking voltage among the individual FIDs during TRV, the effect of gate resistance on TRV dynamics, and the impact of parasitic capacitance, C_T, on TRV. A 3 kV peak ac input voltage is applied to the circuit in Figure 4 with a base load, R_{LOAD}, of 45 ohms. The FID fault current threshold is set to 50 A. Input voltage is near its peak value when current is interrupted. Figure 5 shows transient voltage being shared across the series connected FIDs when the current is interrupted. As can be seen in Figure 5,

though a large transient overshoot occurs, the FIDs share the blocking voltage almost perfectly during the TRV.

In Figure 6 and Figure 7, the effect of gate resistance on TRV is shown when both the parasitic transformer capacitance is not included and is included in the circuit model, respectively. It can be seen that with active gate resistance control, not only can the peak transient blocking voltage can be reduced from 6 kV to 3 kV, but the negative voltage swing can also be eliminated. It is also shown that parasitic capacitance reduced the oscillation frequency from 16.67 kHz to 8.33 kHz, which suggests that the step-up transformer passive components are the major elements of the resonance formed in the circuit. This important fact will be observed in the medium-voltage test circuit experimental results in the next section.

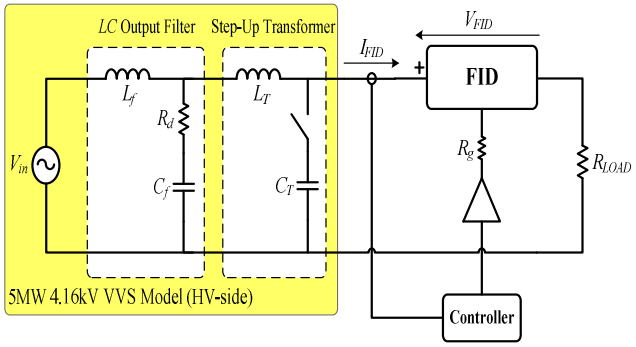

Figure 4. FID circuit model with VVS

Table 1. FID Circuit Parameters

- Input voltage: 3kV line-to-line @ 60Hz **- R_{LAOD} = 45 Ω**				
FID Parameters				
6.5kV 200A Si-IGBT		FID1	FID2	FID3
Balancing resistor (kΩ)		250	255	245
Balancing caps (nF)		100	100	100
Gate	Rg1 (Ω)	50		
	Rg2 (Ω)	1000		
***LC* Output Filter Parameters**				
Lf (mH)		3.2		
Cf (uF)		2.5		
Rd (Ω)		40		
$f_{resonance}$ (kHz)		1.779		
Step-up Transformer Parameters				
LT (mH) - leakage		5.4		
CT (nF) - parasitic		46.5		

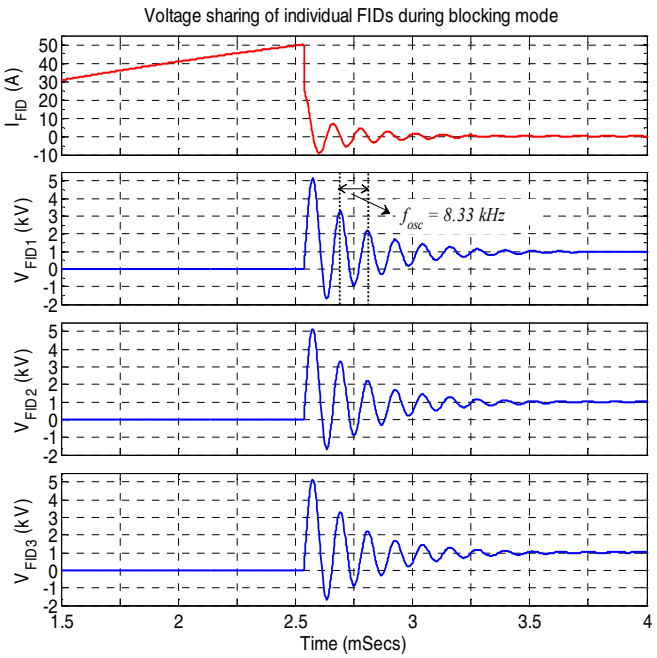

Figure 5. TRV voltage sharing of FIDs

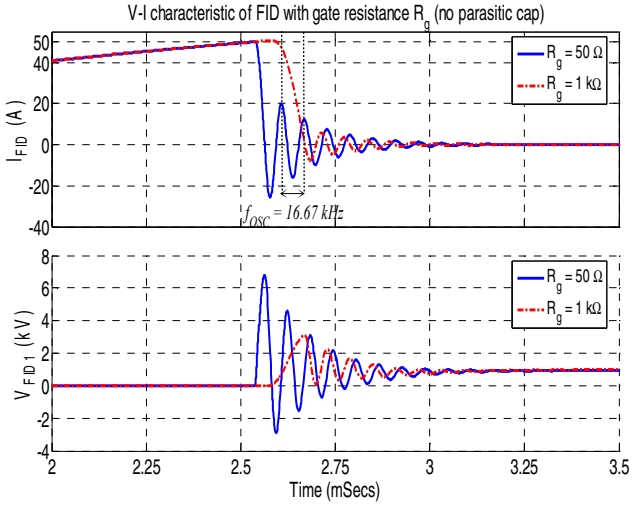

Figure 6. TRV change with gate resistance (no parasitic capacitance C_T)

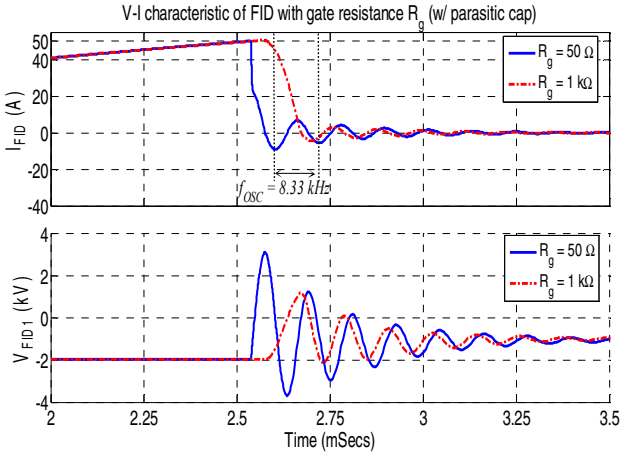

Figure 7. TRV change with gate resistance (w/ parasitic capacitance C_T)

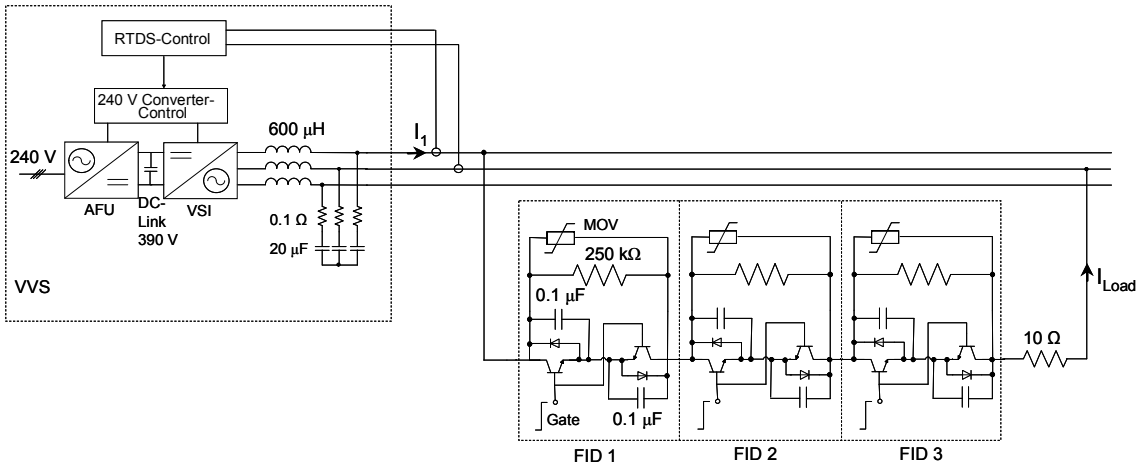

Figure 8. Type 1 Test Circuit

III. Experimental Setups & Results

In order to validate the performance of the proposed FID and create a validated simulation model for the future studies, the FID was tested in low and medium voltage test circuits. In order to examine the FID interaction with a power electronics device, the Type I test circuit was built as shown in Figure 8**.** Figure 8 shows the circuit diagram of a 25 kVA power electronics converter – variable voltage source (VVS). The FID, which consists of three 6.5 kV IGBT modules, was connected in series between two phases of the power electronics converter output.

The VVS, which is based on a power electronics building block (PEBB), is used to amplify arbitrary, instantaneous voltage references provided by the real time digital simulator (RTDS). The VVS consists of an active front unit (AFU), which is interconnected with a voltage source inverter (VSI) through a common dc-bus (390 V) as shown in Figure 8. The AFU control circuit is comprised of six fully controlled IGBT switches in a two-level inverter topology, with three line inductors on the ac side and a capacitor on the dc side. The conventional sine-triangle PWM is used as a modulation strategy for the AFU. The VSI of the VVS, which is based of the same two-level inverter topology as the AFU, utilizes a Reference-Carrier-Modulator (RCM) which uses a Reference-Carrier method for calculation of three-phase patterns [7]. The switching frequency of the VSI in Type I Test Circuit is set to 5 kHz.

The output of the inverter unit is connected to the FID through a second order *LC*-filter, the resonant frequency of of which is defined as:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} = 1.453 \text{ kHz} \qquad (1)$$

The FID is equipped with 100 nF balancing capacitors, 250 kΩ balancing resistors, and the clamping MOVs. For the experiment, an output voltage of 300 V (peak) was requested from the VVS. Figure 9 illustrates the voltages across the three individual FID modules, the full voltage across the entire FID, as well as the load (interrupted) current. At the peak of the current waveform, as defined by a threshold value in RTDS program for FID control, the current was interrupted by the FID. As it can be seen, the quick interruption (~50 µs) of the current causes a transient recovery voltage (TRV) across the FID, whose dynamic behavior is determined by the *LC*-filter of the VVS.

The initial amplitude of the oscillation, which is mainly governed by the line inductance, is approximately two times the steady-state voltage of the VVS. The frequency of the observed oscillations equals the resonant frequency of the *LC*-ripple filter. Consequently, due to the balancing capacitors and resistors, the voltage across each IGBT modules is well balanced as shown in Figure 9. After evaluating and testing the FID in the low voltage test circuit, experimental data was consolidated and testing of the FID at medium voltage commenced.

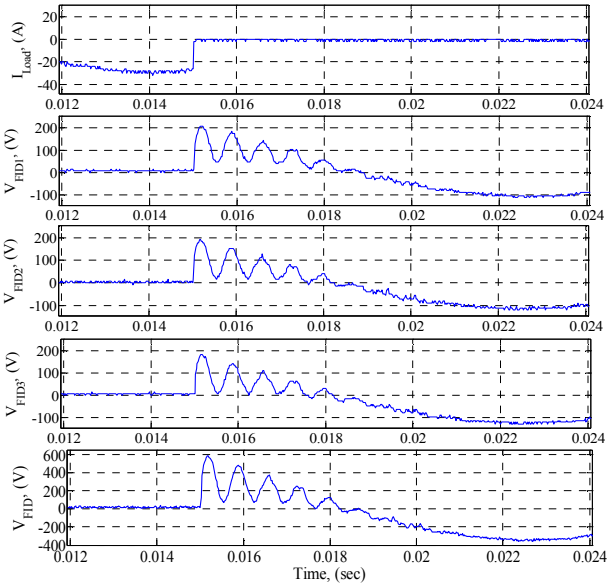

Figure 9. FID experimental results in Type I test circuit

For the medium voltage experiment, a 5 MW VVS was utilized as shown in Figure 10. The 5 MW VVS is a medium voltage variable ac and dc source connected between two 4.16 kV busses through transformers [8]. The VVS, based on a power electronics building block (PEBB), consists of an active front unit (AFU), which is interconnected with the voltage source inverter (VSI) through a common dc-bus. The VSI is connected with the *LC*-ripple filter and the 466/4.16 kV (open-*delta/wye*) step-up transformer in a TWIN topology arrangement [10]. The switching frequency of the VSI is set to 10 kHz. The resonant frequency of the *LC*-filter is 1.779 kHz. The real-time simulator (RTDS) is used to regulate the output voltage at the 4.16 kV experimental bus by providing instantaneous voltage references to the power electronics controller (PEC) of the VVS. The FID was series connected with a base load between two phases of the VVS. The amplitude of the voltage was set to 3 kV (peak) and the applied base load is R_{Load}= 45 Ω. A current threshold was defined in the RTDS program as 50 A. Once the turn-off sequence was enabled in RTDS and the load current had exceeded the specified threshold, the FID interrupted the load current.

Figure 11 shows the experimental results of the FID operation. Considering the TRV, the initial overshoot was approximately 3.5 times the amplitude of the steady-state requested VVS voltage. It is worth mentioning, that the inductance and the parasitic capacitance of the step-up transformer create their own resonant circuit, and once excited by the turn-off of the FID, the TRV across the modules oscillates at 10 kHz instead of the anticipated resonant frequency of the *LC*-filter.

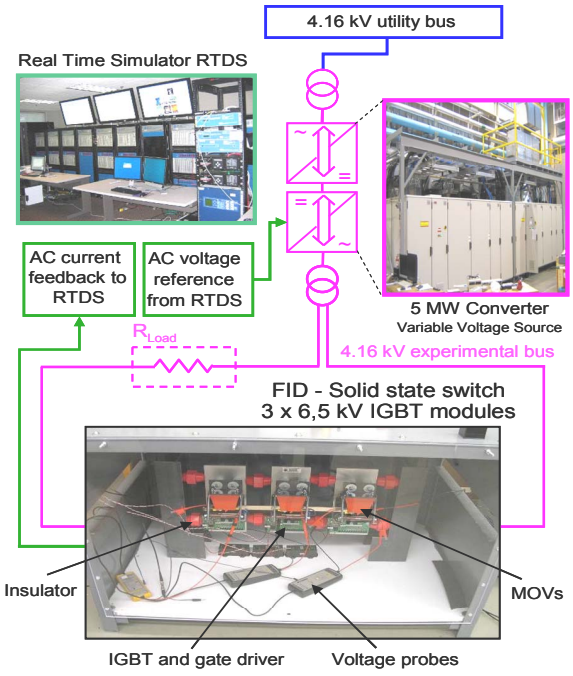

Figure 10. Medium Voltage Test Cicuit

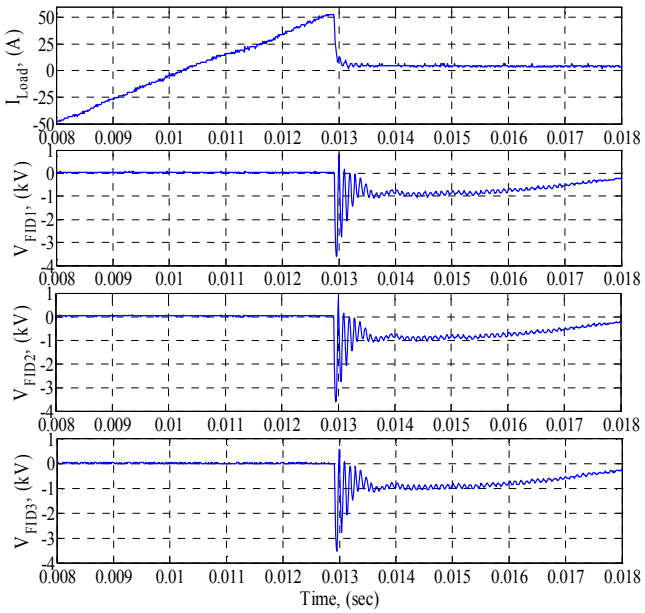

Figure 11. FID experiment results in medium voltage test circuit

A validated PSCAD model of the medium voltage test circuit was used to further examine the TRV behavior. Figure 12 shows that the *di/dt* of the interrupted current affects the magnitude of the TRV. A faster turn-off (higher *di/dt*) of the load current causes a more pronounced TRV, and a slower turn-off (lower *di/dt*) causes a less pronounced TRV. Based on these results, the control of *di/dt* at the turn-off could actively reduce the amplitude of the occurring TRV. Another method to reduce the TRV amplitude would be to add a compensation capacitor to the line circuit. In this case, the PSCAD model was modified by connecting 5 µF line-to-ground at the high voltage side of the transformer in parallel to the present parasitic capacitance of the transformer. Connecting this additional capacitance to the circuit results in different dynamic behavior and changes the oscillation frequency of the TRV as shown in Figure 12.

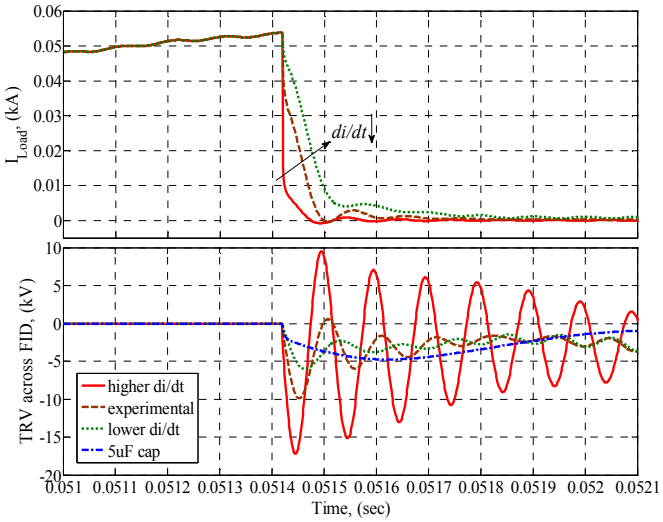

Figure 12. TRV for different current di/dt's and line capacitance

Another approach for protecting the FID from overvoltage during the turn-off event is to utilize passive devices such as MOVs. The presented FID prototype is equipped with three MOV's, one in parallel to each FID module. Figure 13 shows experimental results with and without MOVs. The top graph shows the experimental results of a 50 A turn-off without MOV. The occurring TRV across each individual FID module (only FID1, FID2 shown) peaks at ca. 3.5 kV. The bottom graph illustrates the experimental results for the case when the FID prototype is equipped with MOVs. As can be seen, the MOV's clamp the voltage across the FID modules at 2.2 kV.

In order to determine the power losses of the entire FID, the prototype was connected to a linear current amplifier. The voltage drop across the device was measured, while the amplitude of the 60 Hz sinusoidal reference signal was gradually increased up to 50 A. The power loss of the entire FID device at 50 A is approximately 700 W, as can be seen from Figure 14. In the 1 MW PEDS (7.2 kV L-N rated voltage, 50 A), this corresponds to a power loss of 0.2 %.

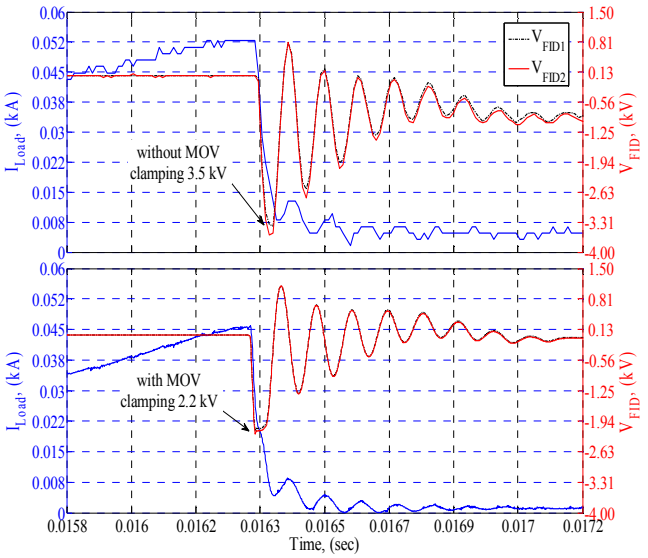

Figure 13. FID operation with and with MOV

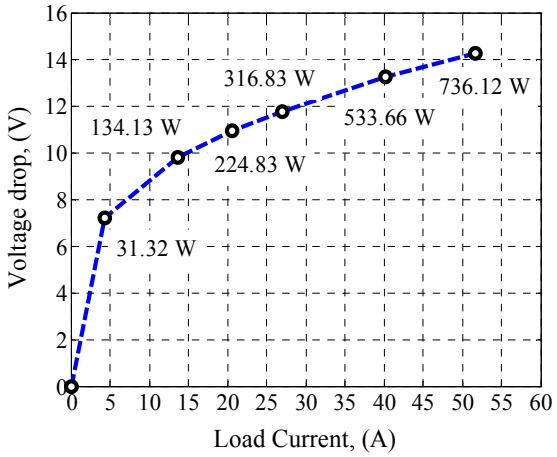

Figure 14. Power loss of the FID device

IV. Conclusions and Future Work

In this paper, the concept of an ultra-fast acting FID intended for medium voltage systems was presented and the FID features were discussed, emphasizing the requirements of the PEDS in which the device is intended to be used. The presented experimental results validated the proposed FID topology, the voltage-balancing snubber circuit design, and the overvoltage FID protection circuit at medium voltage. In addition, the validated simulation model of a medium voltage FID was developed for the future studies. The final paper will present more experimental results at low and medium voltage levels with active *di/dt* control. The circuit interruption requirements and FID location in PEDS will be addressed in the final paper as well. In addition, the PSPICE simulation model of a medium voltage FID (based on 6.5 kV Si-IGBT) will be presented, which can be utilized for detailed device studies and accurate prediction of voltage ringing due to the device parasitics.

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