A 180MW, 450kV Solid State Modulator Based on Press Pack IGBT Technology

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***Abstract*—A new solid state power modulator for free electron laser applications is studied. This modulator comprises a 4.5 kV Press Pack IGBT module that can handle pulsed currents higher than 3 kA. The reliability of this module concerning current distribution among the paralleled IGBT chips is studied, where the internal parasitic components and couplings causing the asymmetries are extracted by means of the Partial Element Equivalent Circuit method. Simulated waveforms showing the currents in each IGBT chip during switching transients are revised together with the dissipated losses for different pulse durations.**

I. Introduction

Presently, X-ray free electron facilities for wavelengths in the range of 0.1 to 10 nm as for example presented in [1] require power modulators which can provide pulses with a voltage of 450 kV and power of 180 MW to drive the klystron amplifiers. Additionally, these pulses have durations of 2 to 10 µs, rise times of 500 ns and must be provided at repetition rates higher than 100 Hz. These specifications are summarized in Table I.

Due to reliability constraints, variable pulse lengths and the desired turn-off capability, such modulators are favorably based on solid state technology [2]. As the maximal operating voltage of fast semiconductor switches is limited to a few kilovolts, the most suitable modulator topologies are based on pulse transformers [3]. These offer an additional degree of freedom for optimally utilizing available high power semiconductor switches.

In this paper, the utilization of a 4.5 kV Press Pack (PP) IGBT module for the 180 MW power modulator is revised. This module is built using single Si IGBT chips placed on a collector baseplate where the connection to the emitter is done using press-pin connectors [4]. A picture of the utilized PP IGBT and its gate-driver is shown in Fig. 1. The PP IGBT module can handle peak currents higher than 3 kA, reaching a pulsed power around 9 MW for a single module, thus the overall output pulsed power of P_{pulse}=180 MW is reached through parallel connection of several power modulators each with a single PP IGBT.

An important issue for the reliability and lifetime of the high power semiconductor switches is the transient current distribution between the IGBT chips during turn-on and -off. To study this phenomenon, the currents in each of the individual chips within a single PP module could be measured using independent current probes, as done in [5]. However, this is an unpractical procedure in most of the cases and therefore other means are required to estimate the internal current distribution. This task can be done using simulation

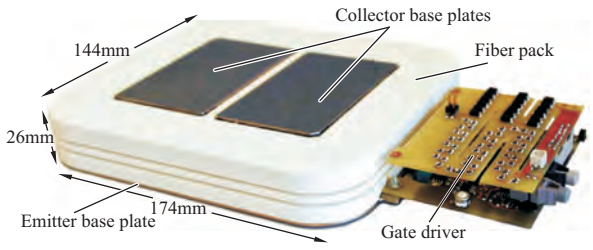

Figure 1: 4.5 kV PP IGBT and gate driver.

TABLE I: Specifications for the klystron driver.

Parameter	Value
Output voltage V_{out}	450 kV
Output pulsed power P_{pulse}	180 MW
Pulse duration T_p	2 -10 µs
Rise time t_s	500 ns
Repetition rate f_r	>100 Hz

tools that provide information about parasitic components within the module and their couplings to the external copper conductors, as they are the main cause for unevenly distributed currents in the module. In this sense, the Partial Element Equivalent Circuit (PEEC) method is an attractive alternative to extract the values of these parasitics, which thereafter enables the study of the current distribution among the IGBT chips during switching processes.

The paper is organized as follows: In **Section II** the PP IGBT internal configuration is presented and the power modulator construction is explained. These descriptions give the geometric definitions used in **Section III** to extract the values of the parasitic components present in the system via PEEC modeling. In **Section IV**, the extracted parameters are used to analyze through electrical simulations the current distribution during the pulse. With this information, the losses generated in each IGBT chip as well as in the complete module are calculated.

II. Press Pack IGBT and Power Modulator

To determine the parasitic elements present in the system, descriptions of the module's internal geometry and the built test setup are required. These descriptions are performed in the following sections.

A. Press Pack IGBT Construction

An exploded 3D CAD drawing of the PP IGBT presented in Fig. 1 is shown in Fig. 3. The studied module is used in traction applications and therefore comprises 12 paralleled IGBTs and 12 antiparallel diodes (cf. Fig. 5). In future, a pulsed-power-optimized switch utilizing only IGBTs will be provided by the manufacturer. The aforementioned semiconductor chips are sitting on two independent collector plates, whereby the contact to the emitter is done through press-pins whose mechanical properties are accurately adjusted to enable even pressure in each of the IGBT chips. The complete setup is then pressed together by an external mechanical structure, where the pressure surplus is taken by the fiber enclosure. Further details about the PP IGBT construction can be found in [4, 6].

B. Power Modulator Mechanical Arrangement

A careful design of the mechanical arrangement of the modulator is a key step in the system design, as it has a considerable influence in the quality of the pulse waveform provided to the load. The schematic representation of the modulator is shown in Fig. 2-a), comprising the capacitor bank, the PP IGBT switch and the load connected through the pulse transformer. Inductor L_{com}

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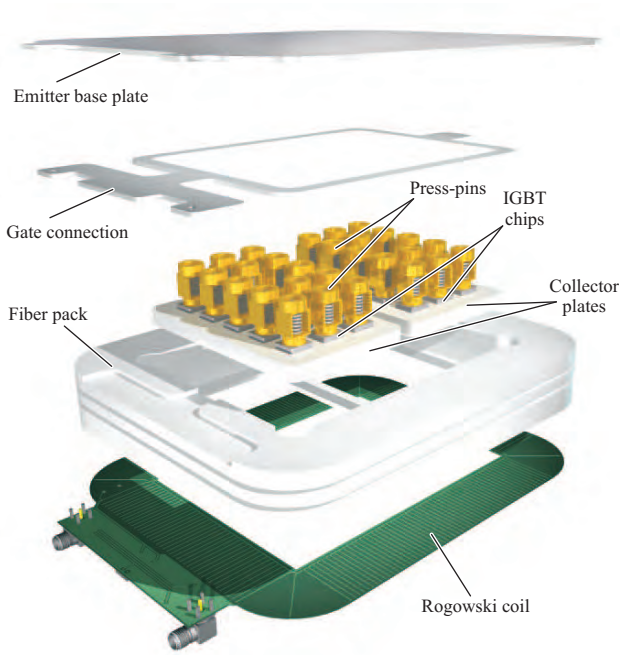

Figure 3: Explode 3D CAD drawing of the PP IGBT showing the module's internal chips and housing.

represents the inductance in the commutation path of the modulator. Additionally, a diode D_f is required in parallel to the transformer to provide a freewheeling path for the load currents once the switch is turned off. This diode is in this case implemented with a PP module comprising only diodes chips. Alternatively, diode D_f can be replaced by an active reset circuit to premagnetize the core before the power pulse takes place, reducing the required transformer size as discussed in [7].

The PP IGBT was originally designed for HVDC applications and multilevel converters, where the high blocking voltage capability of the switching devices is achieved by a series connection of several semiconductors. Here, an easy series connection is achieved through a stacked construction of PP IGBT modules, where module/heat-sink pairs are stacked as shown in Fig. 2-b) [8]. However, in pulsed power applications, fast rising edges in the current pulses applied to the load are one of the main targets (cf. Table I). To achieve these sharp pulses, the interconnections from the capacitor banks through the switches and finally to the load must be carefully designed.

In Fig. 2-b), a typical interconnection which considers a stacked construction with a water-cooled heat-sink between the IGBT and the diode modules is shown together with the current path during conduction of the IGBT. An alternative construction is presented in Fig. 2-c), where the IGBT module is flipped, leaving the heat-sink on the lowest face of the stack. It should be noted that, as the

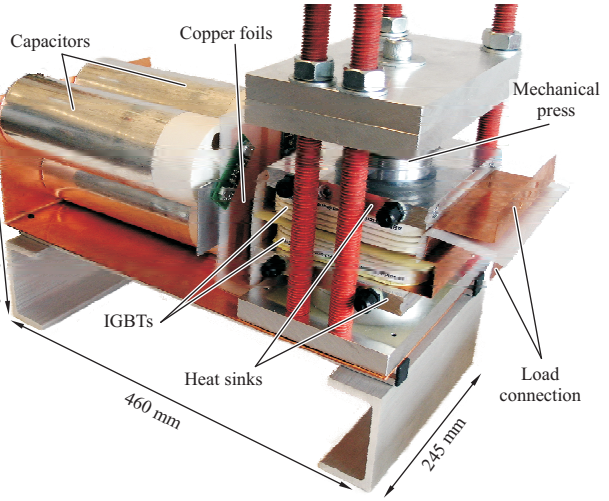

Figure 4: 10 MW power modulator comprising the capacitor bank, the IGBT and diode modules pressed together by the mechanical structure.

silicon chips are placed on the collector plate, the heat-sink must be attached to the collector surface in order to efficiently extract the heat generated by the chips.

The inductance of the commutation path L_{com} is directly related the size of the dashed areas A_c and A_{PP} in Figs. 2 b) and c) where A_c represents area occupied by the diode PP and the water-cooled HS while A_{PP} corresponds to the PP IGBT utilized area. As can be seen, area A_c is larger in the case of the stacked setup due to the insertion of the heat-sink between the modules (cf. Fig. 2-b), leading to larger inductances and consequently longer rising times in the current pulses. Moreover, the heat-sink between the modules would be subject to strong magnetic fields, which added to the HS geometry would lead to large induced eddy currents and additional losses in the system. For these reasons, a construction as displayed in Fig 2-c) was chosen for the test setup. It should be noted that area A_{PP} remains unaltered with this modification and therefore has no effect on the commutation inductance.

A picture of the built test setup is presented in Fig. 4. The capacitor is bank connected to the switches through 0.5 mm thick copper foils as described by Fig. 2-c). The IGBT and diode modules are cooled with respective water-cooled heat-sinks and the whole arrangement is pressed up to 3 Tons by the mechanical setup shown in Fig. 4.

III. Parasitic Components Extraction

The internal arrangement of IGBTs and diodes inside the PP module is shown in the cross sectional view of the module in Fig. 5, where the external copper conductors and the current directions are also depicted. Here, the 12 IGBT chips can be seen along with the 12 diodes and the respective gate connections.

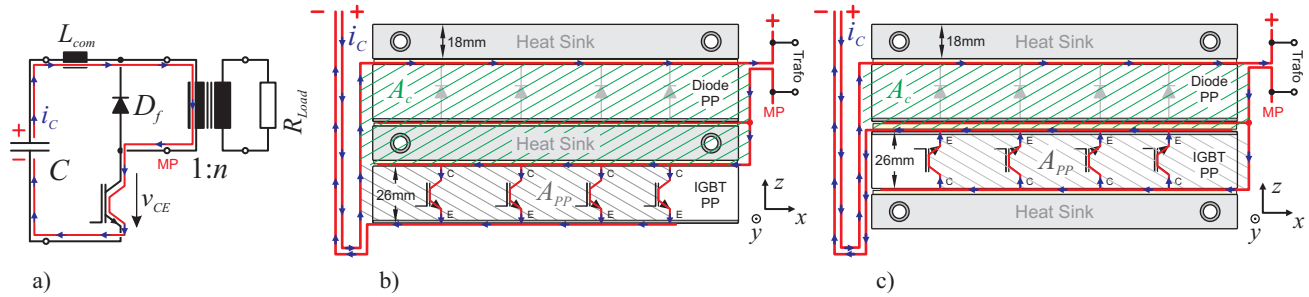

Figure 2: PP IGBT test setup: a) Schematic representation; b) Commutation path using a stacked construction with water-cooled heat-sink between the modules and c) commutation path considering flipped IGBT featuring reduced commutation inductance.

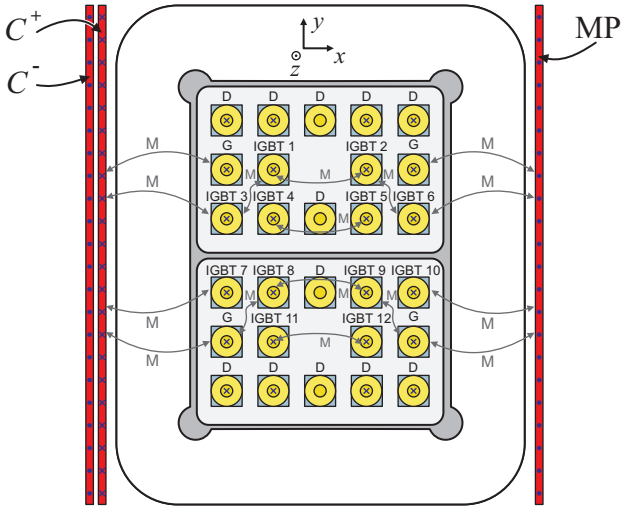

Figure 5: Cross section of the PP IGBT and the copper foils conductors where the arrangement of the 12 IGBT's and 12 diodes is displayed. Arrows and dots show the direction of the current (cf. i_C in Fig. 2-a) through the foils and through the IGBT chips while M denotes magnetic coupling between the different parts.

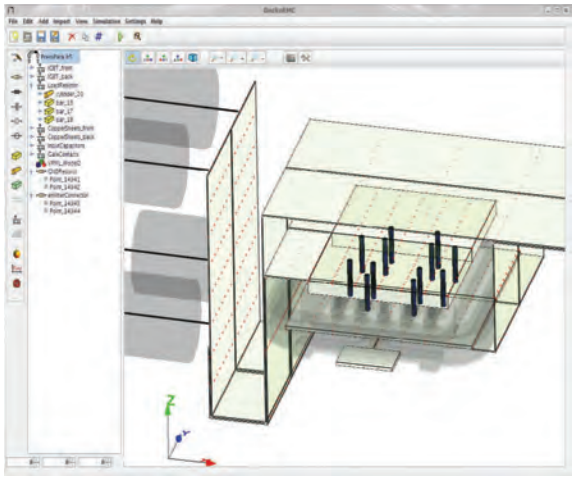

Figure 6: Graphical interface of the electromagnetic solver GeckoEMC used to extract the parasitic components of the power modulator arrangement.

Besides the self inductances of each of the IGBT chips and their gate connections, numerous mutual inductances are present in the module (cf. Fig. 5). To extract the values of these self and mutual inductances, the PEEC method is better suited than 3D Finite Element (FEM) method given the large aspect ratio between length and width of the conducting surfaces of the studied setup [9, 10]. In addition, as PEEC is based on equivalent electric circuits, it can be easily integrated into electric-type simulators, building powerful multidomain simulation environments.

A picture of the graphical interface of the software GeckoEMC used to perform the PEEC simulation is displayed in Fig. 6. To extract the value of the parasitic components, the IGBT chips and their respective press-pins are modeled as cylindric conductors. A current with a slope of 10 kA/µs is then imposed through the copper foil conductors and into these cylindrical conductors, obtaining the waveforms depicted in Fig. 7. It should be noted that for this test, a symmetry axis is found in x (cf. Fig. 5) and therefore only the current in the upper 6 IGBTs is shown. The obtained waveforms are used to extract self and mutual inductances present in the system. Further details about the PEEC modeling of this setup can be found in [11].

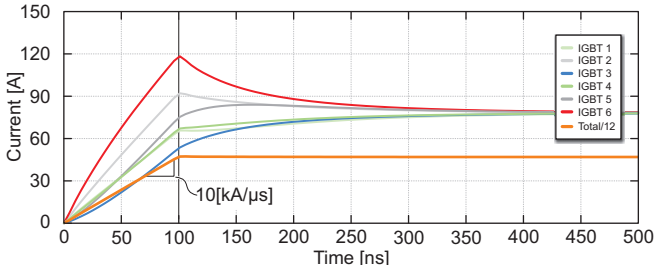

Figure 7: Current distribution among chips when a current ramp is imposed externally to the PP IGBT module. These waveforms are used to extract the parasitic components used to study the current distribution during a pulse.

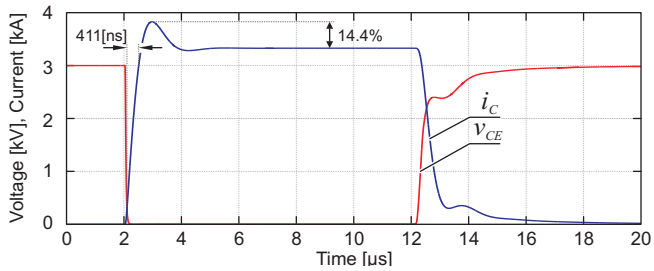

Figure 8: PP IGBT collector current and voltage for a 10 µs pulse. The achieved rising time reaches 140 ns with an overshoot of 14.4 %.

IV. Current Distribution and Losses

With all the couplings of the parasitic components within the module determined, an electrical simulation considering a SPICE model of the IGBT chips was performed. The single IGBTs parameters were adjusted according to datasheet values and curve fitting from experimental switching curves measured at the terminals of the PP module. Also for this simulation, the pulse transformer and a resistive load were included and their parameters were scaled from the setup described in [2] to meet with the power/voltage requirements presented in Table. I.

A simulated result for a pulse of 10 MW with an input voltage of 3 kV and pulse duration of T_p=10 µs is shown in Fig. 8. As can be seen, the rising time (from 10 % to 90 % of the steady state current value) is 411 ns, below the specified rising time of t_s=500 ns (cf. Table I) while the overshoot reaches 14.4 %. It should be noted that this overshoot is considerably reduced when replacing the resistive load by the klystron amplifier, as these amplifiers typically feature a nonlinear impedance. It can be seen in Fig. 8 that the turn-off behavior of the PP IGBT features a long tail current responsible for a large share of the losses generated in the switch during the pulse duration.

The current distribution among the IGBT chips for the pulse described previously is presented in Fig. 9. The currents through the switches are considerably unbalanced during the turn-on process. The zoomed vision of this process is depicted in Fig. 9-b) where it is possible to see that IGBTs 6 and 10 are conduct the largest amount of current. This phenomenon is due to the mutual coupling of these chips to the right hand side conductor shown in Fig. 5. Because of the shorter distance of these chips to the conductor, whose magnetic field is not compensated by a current in the opposite direction as in the left hand side conductors, they are subject to high magnetic fields leading to proximity effects causing the asymmetry in the current distribution. The asymmetry during turn-off is considerably smaller. However, this small asymmetries during turn-off process cause large asymmetries in the dissipated energy, as the turn-off process is responsible for the largest share of the losses during the pulse.

In Fig. 11 the dissipated energy in each chip for different pulse durations is shown together with the average losses for each pulse

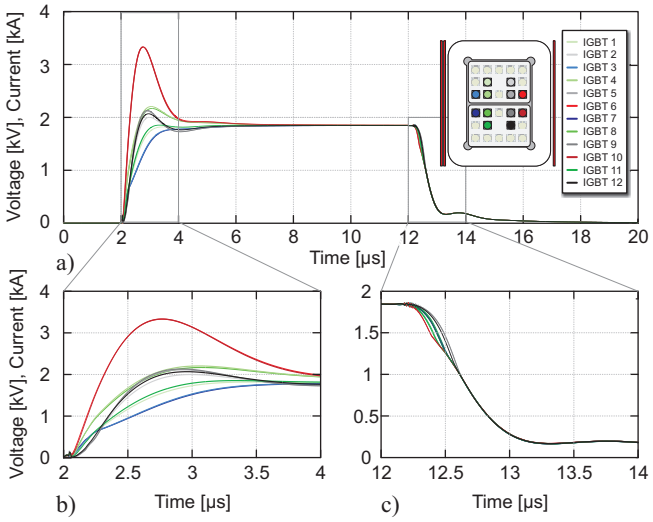

Figure 9: Current distribution among the 12 IGBT chips of PP module (Numbering corresponding to Fig. 5): a) During the 10 µs pulse; b) Detail on turn-on process; c) Detail on turn-off process.

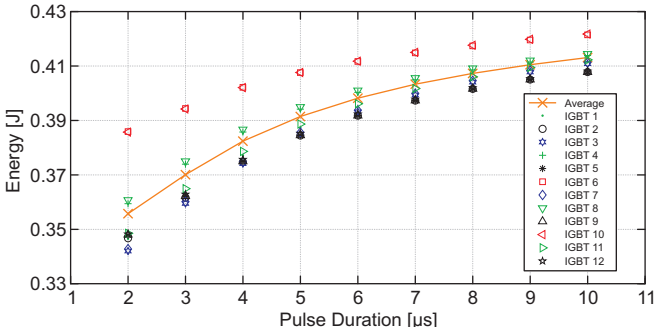

Figure 10: Dissipated energy in each IGBT chips depending on the pulse duration. A large mismatch in the dissipated energy is produced at short pulse durations due to the difference in the turned-off currents.

duration. The calculated energies considers turn-on, turn-off and conduction losses. As expected, IGBTs 6 and 10 dissipate the largest amount of energy due to the asymmetry in the current sharing seen in Fig. 9. As the pulse duration is shortened, the average dissipated energy is reduced mainly due to a reduction in the conduction losses. However, the mismatch in the dissipated energy in each of the IGBTs is increased as the pulse duration is shortened. This effect is caused by the large asymmetry in the current conduction during the turn-on process, which delays the symmetrization of these currents during steady state. As a consequence, with shorter pulses, the difference in the currents at the turn-off instant in each IGBT is increased, leading to larger asymmetries in the dissipated energy. The simulated efficiency of the PP test setup considering a 10 µs pulse is 95 %.

Modifications to the copper foil conductors layout can be made to improve the current conduction distribution and hence the energy dissipation distribution among the IGBT chips as shown in Fig. 10 and treated in [11]. As can be seen, the new copper conductor connected to MP (shown in orange in Fig. 10) compensates the upwards current on the left hand side of setup and therefore, in contrast to the arrangement in Fig. 2-c), two downward currents are left on each side of the module, helping in this way to evenly distribute the currents in the internal chips.

V. Conclusions

A 4.5 kV Press Pack IGBT module was studied for a power modulator that provides 180 MW pulsed power to drive a klystron

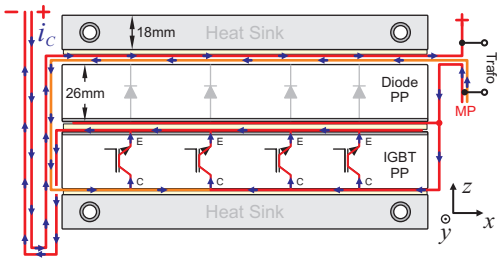

Figure 11: Commutation path with additional copper conductor in mid-point (in orange) to achieve more evenly distributed currents within the PP IGBT module. Further details found in [11].

for free electron laser application. A compact 9 MW test setup was built to test the switch performance.

To study the reliability of the IGBT module used in the setup, the current distribution among its different IGBT chips was studied using PEEC modeling. This method proved useful to estimate the internal parasitic components in the system implemented later in the electrical simulation. When performing this simulation, considerable differences in the current distribution during turn-on process were noticed due to the power modulator copper conductors layout. This differences become larger at shorter pulse durations due to the unsymmetrical currents at the turn-off instant.

In spite the analyzed unsymmetrical current distribution, the Press Pack IGBT module presents an attractive option for the construction of a compact and reliable power modulator.

VI. Acknowledgements

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