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Solid-state fault isolation devices: application to future power electronics-based distribution systems

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Abstract: This study addresses the timely issues of modelling, and defining selection criteria for, a solid-state fault isolation device (FID) intended for use in power electronics-based distribution systems (PEDS). This work subsequently derives the FID parameters by mapping the characteristics of a conventional medium-voltage distribution system onto that of the PEDS envisioned under a new multi-university Engineering Research Centre. When conventional circuit breakers are used in distribution systems, they have a relatively long clearing time, causing the voltage to collapse for a significant time. A semiconductor circuit breaker, however, is expected to be able to switch fast enough to keep a voltage disturbance within acceptable limits. The main focus of this study is to address the operational issues of the interaction between the power electronic converters and the solid-state FID. The utilisation of rate of current decrease (di/dt) control during turn-off in conjunction with passive clamping devices to manage the overvoltage that results from very fast circuit breaker operation is introduced. In contrast to a simple conventional RC-snubber circuit, the proposed overvoltage management avoids high leakage current, which is the undesirable drawback of RC-snubber circuits. The presented prototype is experimentally verified with low and medium-voltage test circuits.

List of abbreviations

AFU	active front-end unit
DESD	distributed energy-storage devices
DRER	distributed renewable energy resources
IGBT	insulated gate bipolar transistor
FID	fault isolation device
LTI	linear time-invariant
MOV	metal oxide varistor
PEBB	power electronics building block
PEDS	power electronics-based distribution system
PWM	pulse-width modulation
RTDS	real-time digital simulator
SST	solid-state transformer
TRV	transient recovery voltage
VCB	vacuum circuit breaker
VSI	voltage-source inverter
VVS	variable voltage source

1 Introduction

This paper reports on the operational issues of a solid-state fast fault isolation device (FID) within power electronics-based distribution systems (PEDS) and proposes an approach for controlling transient over-voltages during FID turn-off for installation in a medium-voltage circuit. Power electronic converters and systems can be regarded as one solution to increase power quality in the grid and to integrate distributed renewable energy sources into today's power systems. In PEDS, a solid-state transformer (SST), rather than a traditional transformer, will be used to enable active management of distributed renewable energy resources (DRER) and loads. The SST is a digitally controlled converter [1] that is capable of controlling power flow, voltage magnitude and various phase relationships of current and voltage. Since the SST is a power electronics device, it can provide a substantial current limiting function for the entire distribution system. However, in order to limit the fault current, the SST will lower the voltage in the entire system significantly during a fault which is not the case in a conventional distribution system with standard transformers. Hence, the circuit breaker must disconnect the faulted section as fast as possible to allow for the SST to restore the system voltage quickly after a fault. Thus, very high speed operation of FID (fault clearing within a few hundreds microseconds) becomes a most desired feature in PEDS system. One way to develop an ultra-fast FID is to replace mechanical circuit breakers with semiconductor switches.

It has already been proven that the use of power semiconductor devices can mitigate short-circuit currents and voltage sags during a short-circuit event [2–7]. Solid-state circuit breakers based on high power semiconductors potentially offer enormous advantages when compared to conventional solutions, since a solid-state breaker is able to

switch in a few microseconds. In this paper, the need for ultra-fast fault isolation in PEDS will be first illustrated by comparing typical system responses to simulated faults in conventional and power electronics-based distribution systems. This paper does not necessarily seek to propose a novel FID topology, but rather to address the issues that arise during FID operation and installation within a PEDS. Therefore the main research topic of this paper is to address the issues of the interaction between power electronic devices in a distribution system. Subsequently, two different FID topologies including a configuration of anti-parallel insulated gate bipolar transistors (IGBT) with series diodes [2] and a configuration of emitter-connected IGBTs featuring freewheeling diodes are compared, considering the requirements of the solid-state breaker application which are considerably different when compared to a conventional mechanical circuit breaker. Finally, the results from the initial hardware tests with the power electronic converters at low and medium voltages are compared to corresponding circuit simulations.

2 Fundamentals of power electronics-based distribution system

A power electronics-based distribution system, such as [8], is envisioned to be an efficient power grid, integrating highly distributed and scalable alternative generating sources and storage with existing power systems to facilitate a green energy-based society, mitigate the growing energy crisis and reduce the impact of carbon emissions on the environment. This type of grid architecture [8] contains a large number of power electronics-based devices, including converters and SSTs, DRER, distributed energy-storage devices (DESD) and loads.

The simplified three-phase PEDS, shown in Fig. 1*a*, was chosen for the purpose of simulating line currents and voltages under normal and fault conditions in order to understand the target specifications and features of a FID. The line-to-ground fault in the presented simulation occurs at 0.2 s. Fig. 1*b* shows the grid current and voltage as observed on the secondary side of either of the solid-state transformers during a line-to-ground fault for the system of Fig. 1*a*. Due to the limited short term current carrying capability of the semiconductors within the SST, it has to limit the fault current to approximately two times the rated current. As shown in Fig. 1*c* and *d*, this inherent fault current limitation causes a significant voltage drop in the entire PEDS. However, the DESD within the individual SSTs serving local loads will continue to provide power to the customers as shown in Fig. 1*d*. Nevertheless, the FID must provide ultra-fast isolation of the fault to quickly restore system voltage to minimize the required ride-through capacities of the many intelligent energy management nodes in the system. The detailed description of the SST topology and its control is presented in [1]. Since the entire PEDS shown in Fig. 1*a* is an ongoing research hardware development, in order to experimentally evaluate FID performance in a power electronics-based environment, a simplified test circuit which considers only one power electronic converter (for example, Feeder I as shown in Fig. 1*a*) will be utilized.

In contrast, a fault in conventional distribution systems will not cause a significant voltage drop in the entire distribution system, provided that the fault current is primarily limited by the respective line impedance, that is, the fault is

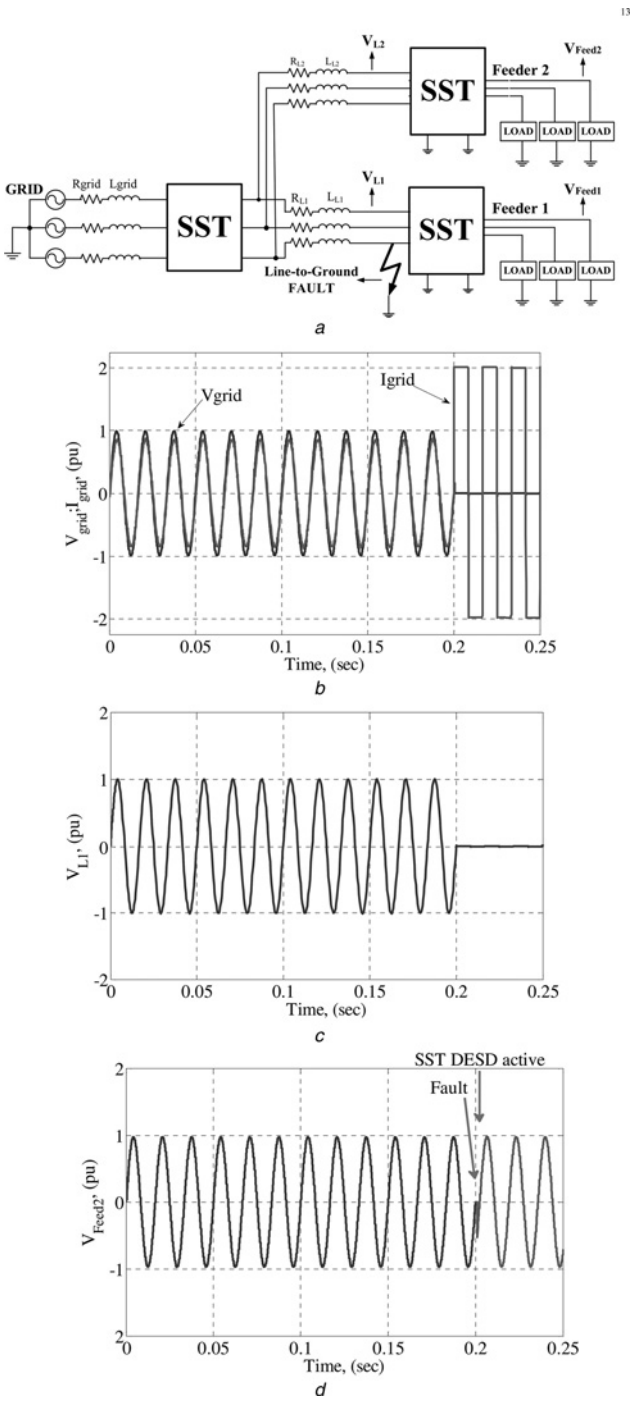

Fig. 1 *Fault in PEDS*

a Representative portion of a power electronics-based distribution power system
b Grid current and voltage before and after fault
c Voltage before and after fault V_{L1}
d Voltage before and after fault V_{Feed2} at Feeder 2

electrically far away from the substation. Since the conventional distributional system does not provide any fault current limitation, a current limiter (in addition to the circuit breaker) must therefore be designed to limit either the peak value of the initial transient fault current and/or its steady-state value [5].

The occurrence of a line fault can be identified by a sudden reduction in voltage. At the fault location, the voltage will be zero, increasing gradually towards the source(s). The other indication of fault occurrence is the square-wave-shaped

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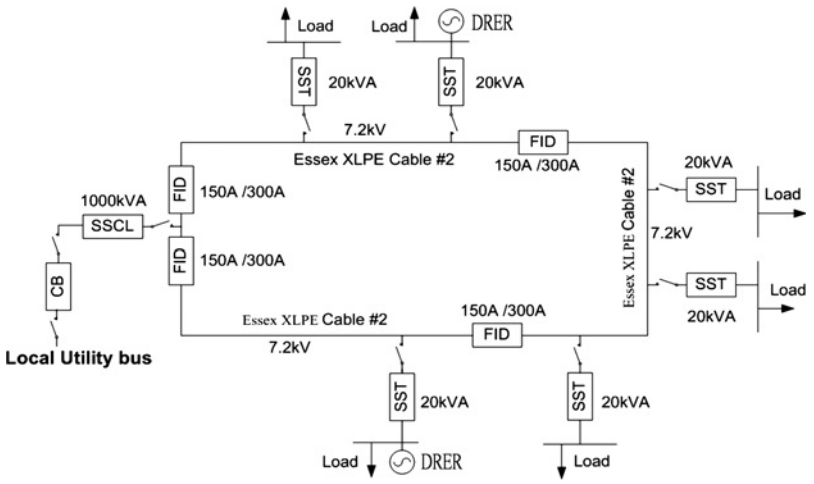

Fig. 2 *Conceptual connection diagram of a PEDS system loop*

current. This generates large harmonic components in both current and voltage. Increase in low-frequency harmonics (typically fifth and seventh) in either current or voltage can be used for fault identification in this system.

Since conventional relay coordination is not feasible in this case, we are currently pursuing identification of the fault location by using wide area differential protection. This method measures the incoming and outgoing currents in each section and the sum of the currents in a section is zero if the fault is outside the section and non-zero if the fault is in the section.

Fig. 2 shows a representative loop of a sample PEDS system. The loop is divided into sections; each section is terminated by two FIDs. The loads and local distributed generations are connected to the loop through high-frequency SSTs. Here we assume a feed from a conventional distribution system with a circuit breaker (CB). Hence, instead of a SST, a solid-state current limiter clips the short-circuit current and produces the square-wave current shown in Fig. 2*b*, which is typically around two times the rated current.

As described in [9], the concept of wide area differential protection can also be applied for backup protection. In [9], the authors describe a 'super loop', which measures the sum of all currents in the system. If the sum of the synchronised current samples is non-zero, there is a fault in the system, and additional backup protection is provided by recognising the voltage collapse at the terminal of the current limiter and the sudden increase of current and voltage harmonics.

3 Solid-state FID design

One possible choice for designing a solid-state FID would be to build a thyristor-based CB. However, the main disadvantage of thyristors is the fact that thyristor CBs will turn off the current only when the current commutates to zero [3, 10]. In a 60 Hz ac system, this natural line commutation will occur only every 8.3 ms, during which time the voltage of the PEDS will collapse, potentially leading to a power interruption. As previously noted, the SST provides the current limiting function, thus very high speed operation of the FID (a few microseconds) is essential in order to minimise the impact of the fault. An FID based on power semiconductors with turn-off capability, for example, gate turn-off thyristors, integrated gate commutated thyristor and IGBTs, potentially offers a much faster clearing of the fault, typically within a few tens of microseconds [3, 4]. In contrast to inverter applications, the switching losses of these devices will only be a minor issue in this application, since in the normal operation mode, the solid-state breaker is always on, turning off only during the occurrence of a fault and therefore, the conduction losses dominate and may well be the limiting factor in the acceptance of semiconductor CBs [3]. However, augmenting the solid-state breaker with an ultra-fast mechanical bypass switch, as similar to the concepts presented in [6, 7] may significantly further reduce on-state losses.

3.1 FID topological considerations and overvoltage management for turn-off event

The main factors that should determine the topology of the FID are on-state loss and cost. In addition, the FID design should be modular to achieve flexible adaptation for different current and voltage levels. Assuming a power rating of 1 MVA at 7 kV for the PEDS demonstration system [8], a rated current of 48 A was chosen as a specification for the design of the first prototype. Furthermore, with 6.5 kV IGBTs commercially available, a series connection of three such devices provided an appropriate safety margin with respect to the expected 7 kV line-neutral voltage.

Two potential topologies for an FID based on IGBTs have been considered. The first topology consists of anti-parallel IGBTs as shown in Fig. 3*a* [2]. The disadvantages of this topology are (i) two series diodes, that have to be rated at full voltage and current, must be included in order to avoid reverse conduction through the IGBT-related anti-parallel diodes; (ii) separate driver circuits and isolated power supplies are needed for the two IGBTs, thus six are required for the entire FID.

The preferred FID topology consists of a configuration of three IGBT modules in series (FID1, FID2, FID3), with each module containing two emitter-connected IGBTs together with freewheeling diodes. This topology is shown in Fig. 3*b*. By taking advantage and making use of commercially available, emitter-connected IGBT modules, this topology does not require separate driver circuits or series diodes, however, it still requires the use of three

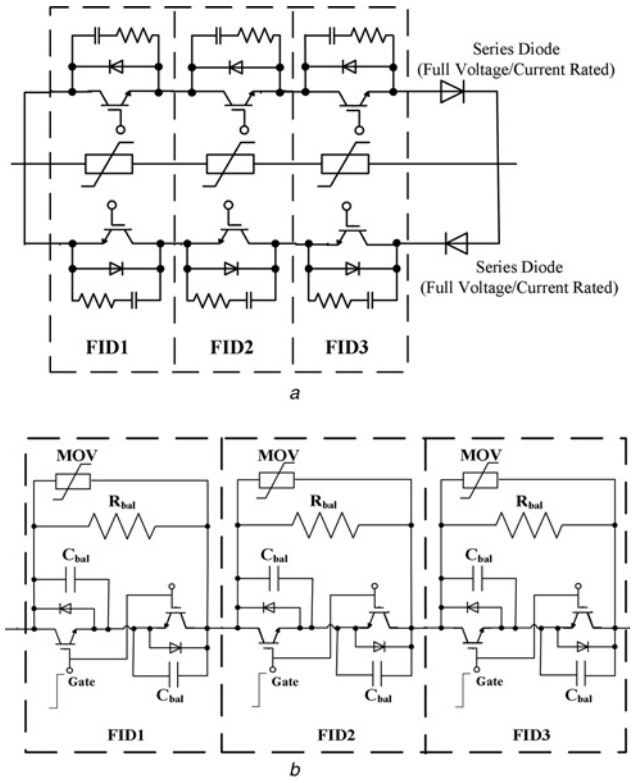

Fig. 3 *FID topologies for the PEDS*

a FID topology with anti-parallel IGBTs and series diode
b Preferred FID topology for the PEDS

separate driver circuits with power supplies and six anti-parallel diodes that are rated at full current.

During FID operation, the balancing of the series IGBT modules and the control of turn-off overvoltages at their collectors under all operating conditions is critical, as they are directly responsible for the system reliability. In the series connection, as shown in Fig. 3, the operating voltage of the FID must be evenly distributed and balanced across each of the individual IGBTs, else the module might be damaged and the overall device might fail [11].

There are multiple parameter differences that cause imbalances in series-connected IGBTs, both in static and dynamic operation [11]. In the presented FID prototype, the balancing resistor (during static operation) value $R_{\text{bal}} = 250\ \text{k}\Omega$ and the balancing capacitor (during dynamic operation) value $C_{\text{bal}} = 0.1\ \mu\text{F}$ were chosen based on the specific parameters in the datasheet of the utilised IGBTs.

Another key aspect of transient operation is the overvoltage that occurs across the device at turn-off due to stored energy in the line inductance. Even though ultra-fast interruption provides very desirable quick isolation of faulted portions of the distribution system, measures must be taken to avoid the resulting large overvoltages. The proposed method of overvoltage management is to adjust the gate resistance of the IGBT driver to increase turn-off time.

Experimentation on low and medium-voltage test circuits illustrated that the increase of R_G was highly effective in adjusting the turn-off time and reducing the collector–emitter overvoltage during interruption. For the FID design, the most suitable value of R_G in terms of turn-off time was determined experimentally to be $R_G = 270\ \Omega$. Also, to guarantee overvoltage protection during the turn-off event, metal oxide varistors (MOV) were implemented as shown in Fig. 3. The proposed method of overvoltage management avoids the high leakage current that would have resulted from the high capacitance needed for a simple conventional RC-snubber circuit. This is not an issue with the utilised balancing capacitors, as their capacitance is much lower than what would be needed for a clamping circuit. One of the limiting factors of the presented technology could be the installed energy absorption capacity of the MOV-element, as compared to stored energy in the line and a more specific design of the MOV element must be done as a function of the parameters of the definitive application.

As mentioned above, when implemented in the distribution system, the amount of overvoltage that the FID will experience will be determined by factors, such as line impedance, that will change depending on where the FID is placed in the system. In the presented application, it was demonstrated that the adjustment of R_G is sufficient to achieve the desired operation. However, for general applications other methods of overvoltage management should be explored. One method that might prove effective is rate of current decrease (di/dt) control during the turn-off event in addition to the overvoltage management methods described above. For example, in [12], a closed-loop op-amp circuit is used to actively control the collector voltage during switching transients. In [13], methods are presented in which the turn-off di/dt is controlled by using a small external inductance in series with the switch emitter to sense the di/dt value and generate a feedback voltage that controls a dependent current source from the switch's gate, the value of which is the voltage of the external inductance multiplied by an adjustable gain. It is still being considered as to which type of active di/dt control should be implemented in the FID.

4 Experimental results

To validate the performance of the proposed FID and to create a validated simulation model for the future studies, the FID has been tested in low and medium-voltage test circuits.

4.1 Type I test circuit

To examine the FID interaction with a power electronic device, the Type I test circuit was built as shown in Fig. 4. Fig. 4*a* shows the circuit diagram of a 25 kW power electronic converter – variable voltage source (VVS). The FID, which consists of three 6.5 kV IGBT modules, was connected in series between two phases of the power electronic converter output.

The VVS, based on a power electronics building block (PEBB), is used to amplify arbitrary, instantaneous voltage references provided by the real-time digital simulator (RTDS). The VVS consists of an active front end unit (AFU), which is interconnected with the voltage-source inverter (VSI) through a common dc-bus (390 V) as shown in Fig. 4*a*. The AFU control circuit consists of six fully controlled IGBT switches (two-level inverter topology), three line inductors on the ac side and a capacitor on the dc side. The conventional sine-triangle pulse-width modulation (PWM) is used as a modulation strategy for the AFU. The VSI of the VVS, which is based on the same two-level inverter topology as the AFU, utilises a reference-carrier-modulator, which uses a reference-carrier method for calculation of three-phase patterns [14]. The switching frequency of the VSI in Type I test circuit is set to 5 kHz based on PWM controller settings [14]. The output of the

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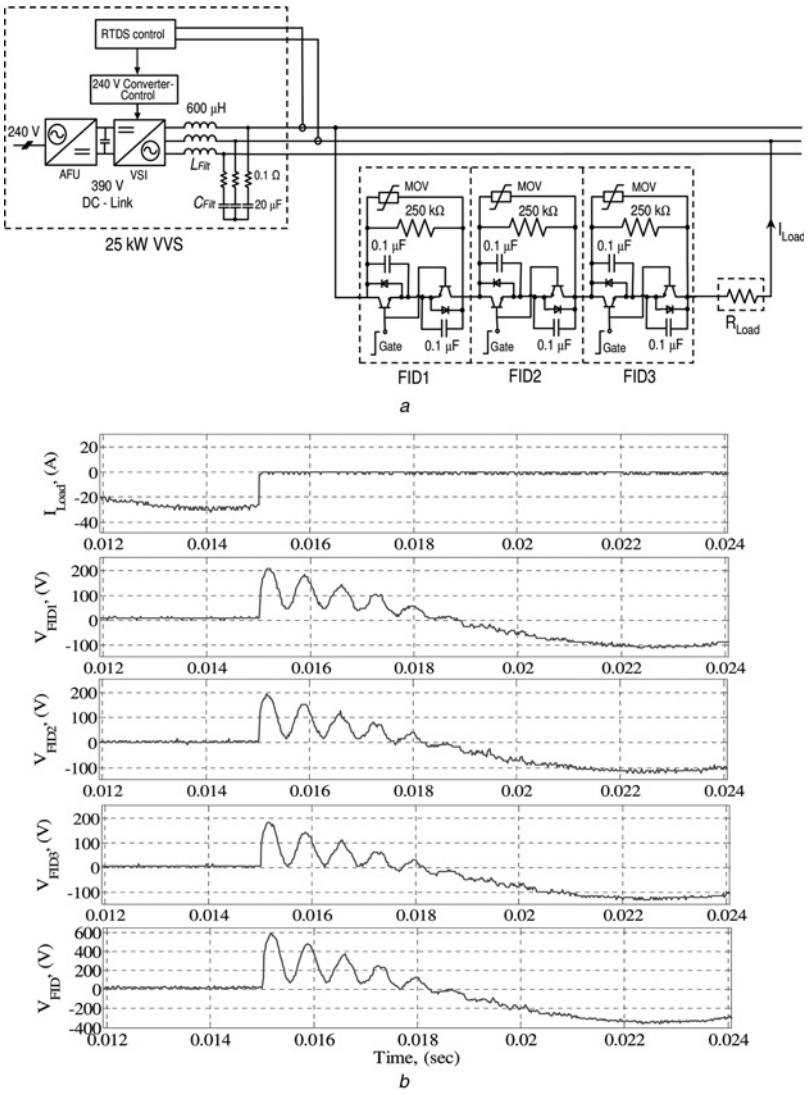

Fig. 4 *Type I test circuit*

a Circuit diagram
b Experimental results in Type I test circuit

inverter unit is connected to the FID through a second order LC-filter.

The FID is equipped with 0.1 μF balancing capacitors, 250 kΩ balancing resistors and the clamping MOVs. For the experiment, an output voltage of 370 V (peak) was requested from the VVS and the applied base load is $R_{\text{Load}} = 12\ \Omega$. Fig. 4*b* illustrates the voltages across the three individual FID modules, the full voltage across the entire FID, as well as the load (interrupted) current. At the peak of the current waveform, as defined by a threshold value in RTDS program for FID control, the current was interrupted by the FID. As it can be seen, the quick interruption (~70 μs) of the current causes a transient recovery voltage (TRV) across the FID, whose dynamic behaviour is determined by the LC-filter of the VVS.

The initial amplitude of the oscillation, which is mainly governed by the line inductance, is approximately two times the steady-state voltage of the VVS. The frequency of the observed oscillations equals the resonant frequency of the LC-ripple filter ($f_{\text{res}} = 1.453$ kHz). Consequently, owing to the balancing capacitors and resistors, the voltage across each IGBT modules is well balanced as shown in Fig. 4*b*. After evaluating and testing the FID in the low-voltage test circuit, experimental data were consolidated and testing of the FID at medium voltage commenced, and the experiment results are presented in the next subsection.

4.2 Type II test circuit

For the medium-voltage experiment, a 5 MW VVS was utilised as shown in Fig. 5. The 5 MW VVS is a medium-voltage variable ac and dc source connected between two 4.16 kV buses through transformers. The VVS consists of two individual power converters, which can provide up to a 5 MW power level when operated in parallel. Each single converter contains two low-voltage PEBB modules for the ac/dc conversion (AFU) and two more for the dc/ac conversion (VSI). The two modules of the inverter section are series-connected to the open delta windings of the applied output transformer in a twin connection topology [15]. The switching frequency of the VSI in the experimental test circuit is set to 10 kHz as a default setting specified by the manufacturer. The FID, which consists of three 6.5 kV IGBT modules, was connected in series between two phases of the power electronic converter output.

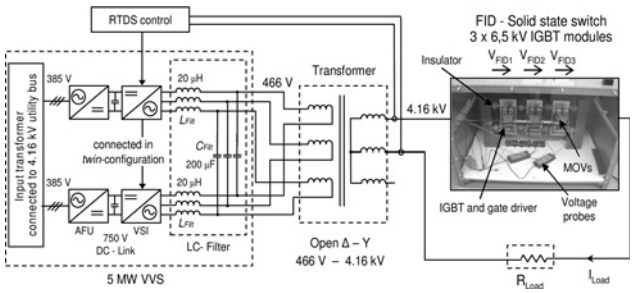

Fig. 5 *Type II test circuit*

The LC-ripple filter ($2L_{Filt} = 40$ uH, $C_{Filt} = 200$ uF) for the 5 MW VVS is connected in series with the 0.466/4.16 kV (open-delta/wye) step-up transformer, where the LC-filter capacitor is connected line-to-line in parallel to the transformer winding. Similar to the Type I test circuit, the RTDS is used to regulate the output voltage at the 4.16 kV experimental bus by providing instantaneous voltage references to the power electronic controller of the VVS. The FID was series-connected with a base load between two phases of the VVS. The amplitude of the voltage was set to 3 kV (peak) and the applied base load is $R_{Load} = 45\ \Omega$. Similar to the previous experiment, a current threshold was defined in the RTDS program as 50 A. Once the turn-off sequence was enabled in RTDS and the load current had exceeded the specified threshold, the FID interrupted the load current. Fig. 6 shows the experimental results of the FID operation. Similar to Fig. 4*b*, it shows the load (interrupted) current and the voltages across the three individual FID modules. It should be noted that the interrupted current does not decay to zero due to current transducer calibration.

Considering the TRV, the initial overshoot was approximately 3.5 times the amplitude of the steady-state requested VVS voltage. Owing to the output transformer, the line inductance, which is an equivalent representation of the transmission line inductance, is substantially higher than the line inductance in the Type I test circuits, thus causing the higher voltage overshoot in the Type II test circuit experiment. It should be noted that TRV amplitude is proportional to the interrupted current. Based on Fig. 6, for example, 100 A would cause the TRV amplitude of ca. 7 kV, an overvoltage which would certainly damage the

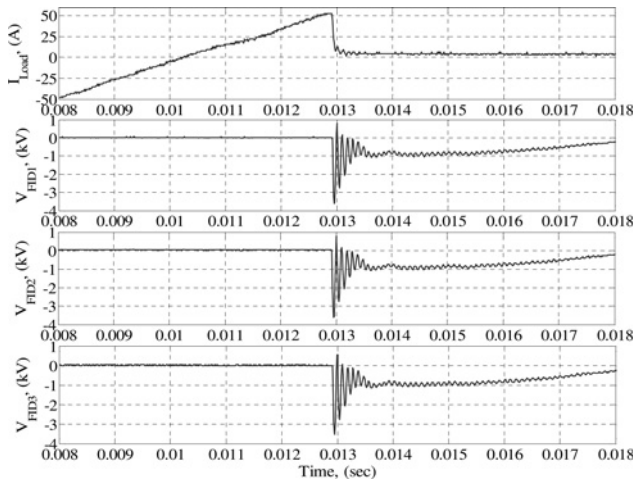

Fig. 6 *FID experimental results in Type II test circuit*

6.5 kV-rated IGBTs in the FID. For the FID protection, the MOV operation will be described below.

A more detailed view of the TRV oscillation across the entire FID and the current turn-off is shown in Fig. 7, which shows that the TRV oscillates at 10 kHz and not at the anticipated resonant frequency of the LC-filter ($f_{res} = 1.779$ kHz). The figure also includes an overlay of the simulation results from a PSCAD model of the experimental test circuit. The developed PSCAD model has been evaluated against experimental results in various test circuits; it demonstrates good agreement with the experimental results and will be utilised in the future studies. It should be noted, however, that for the future simulation on a power electronics level, a SPICE or SABER-based simulation software should be considered.

In order to evaluate the FID turn-off operation, Table 1 was constructed to compare the turn-off time of FID with other types of breakers from the literature. The turn-off time defined is the time at which the interrupted current crosses the lower threshold (1% of the rated current) and stays below this threshold becoming zero amperes.

To further examine the observed dynamic behaviour, a linear time-invariant (LTI) system was derived by considering a simplified, single-phase representation of the Type II test circuit, as shown in Fig. 8. The representation system consists of the output ripple filter (L_{Filt}, C_{Filt} and R_{Damp}), the transformer leakage inductance (L_{Xfrmr}) and parasitic capacitance (C_{Par}), the load resistance (R_{Load}) and the variable resistance (R_{FID}) which represents the FID. It is worth mentioning that the control system of the 5 MW VVS applies active damping, and thus R_{Damp} exists only virtually and is not part of the physical circuit. The twin configuration was taken into account by doubling the filter inductance L_{Filt}. The applied step-up transformer was modelled by considering only the leakage inductance and the parasitic capacitance of the transformer.

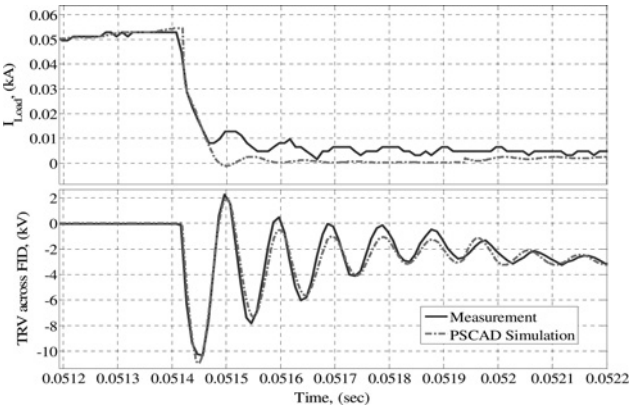

Fig. 7 *TRV and current turn-off in Type II test circuit*

Table 1 Turn-off time of different switches and fault current levels

	Interrupted fault current	Turn-off time
FID	50 A	120 μs
Hybrid breaker [7]	5 kA	1.6 ms
Mechanical breaker [16]	18 kA	3–5 power frequency cycles

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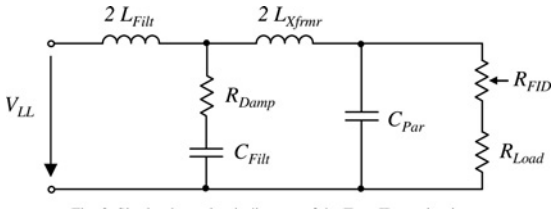

Fig. 8 *Single-phase circuit diagram of the Type II test circuit*

The derived LTI-model can be used to examine the case when the FID has interrupted the circuit ($R_{\mathrm{FID}} \gg R_{\mathrm{Load}}$). Table 2 shows the parameter values of the experimental test circuit. All the values in the table are referred to the low-voltage (primary) side of the transformer. Thus, one of the systems complex conjugate pole's natural frequency is approximately 10 kHz.

In other words, the inductance and the parasitic capacitance of the step-up transformer create their own resonant circuit, and once excited by the turn-off of the FID ($R_{\mathrm{FID}} \rightarrow \infty$), the TRV across the modules oscillates at 10 kHz. It should be noted that the TRV resulting from the ultra-fast FID operation, within the power electronic converters, is not influenced by the switching frequencies of the power electronic converters, and is only determined by line parameters such as line inductance and line capacitance.

Subsequently, the validated PSCAD model of the experimental test circuit can be used to further examine the TRV behaviour. Fig. 9 shows that di/dt of the interrupted current affects the magnitude of the TRV. A faster turn-off (higher di/dt) of the load current causes a more pronounced TRV, and a slower turn-off (lower di/dt) causes a less-pronounced TRV. Based on these results, the control of di/dt at the turn-off could actively reduce the amplitude of the occurring TRV. The desirable di/dt can be achieved by using active di/dt control as described in Section 3.

Table 2 Parameter values for the LTI system

Parameter	Value
L_{Filt}	20 [μH]
C_{Filt}	200 [μF]
R_{Damp}	0.5 [Ω]
L_{Xfrmr}	2.7 [mH]
C_{Par}	46.47 [nF]

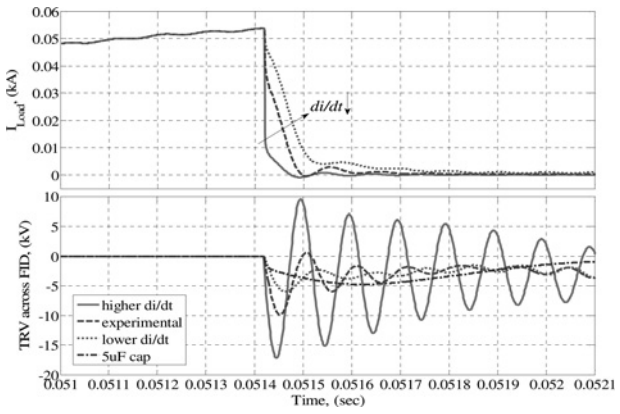

Fig. 9 *TRV for different current di/dt's and line capacitor (PSCAD simulation)*

Another method to reduce the TRV amplitude would be to add a compensation capacitor to the line circuit. In this case, the PSCAD model was modified by connecting 5 μF line-to-ground at the high voltage side of the transformer in parallel to the present parasitic capacitance of the transformer. Connecting this additional capacitance to the circuit results in different dynamic behaviour and changes the oscillation frequency of the TRV as shown in Fig. 9. The figure shows that adding 5 μF to the circuit dramatically reduces both amplitude and frequency (decreased to approximately 1.15 kHz) of the occurring TRV as compared to the experimental graph, which corresponds to the validated PSCAD simulation of the physical experimental test circuit. It should be noted that a compensation capacitor does not affect the current slope during turn-off event, only the TRV. However, this method requires expensive medium-voltage rated ac capacitors.

Another approach for protecting the FID from overvoltage during turn-off event is to utilise passive devices such as MOVs. The presented FID prototype is equipped with three such MOVs, one in parallel to each FID module. Fig. 10 shows experimental results with and without MOVs. The top graph shows the experimental results of a 50 A turn-off without MOVs. The occurring TRV across each individual FID module (only FID1, FID2 shown) peaks at ca. 3.5 kV. The bottom graph illustrates the experimental results for the case when the FID prototype is equipped with MOVs. As can be seen, the MOVs clamp the voltage across the FID modules at 2.2 kV.

From Fig. 10, a simple calculation revealed that the MOV had to absorb roughly 2 J in order to sufficiently suppress the TRV's amplitude. The rated transient energy of a single MOV is 3800 J (2 ms). Since the current through the FID drops rapidly to zero after a turn-off, it is very unlikely that the energy absorption of the MOV would exceed its rated value.

It should be noted that based on experimental results, an active clamping function similar to that in [17] does not clamp overvoltage during the turn-off event and cannot be utilised in FID operation.

4.3 Power losses

Classical mechanical CBs have a very small contact resistance (a few micro-ohms) in the closed position, and represent a galvanic separation in their open state. However, these devices have a long reaction time (typically 3–5 power frequency cycles) due to the need of blowing the arc in the chute [16]. Arc occurrence leads to contact erosion and, consequently, a short lifetime (ca. 30 000 operations) and

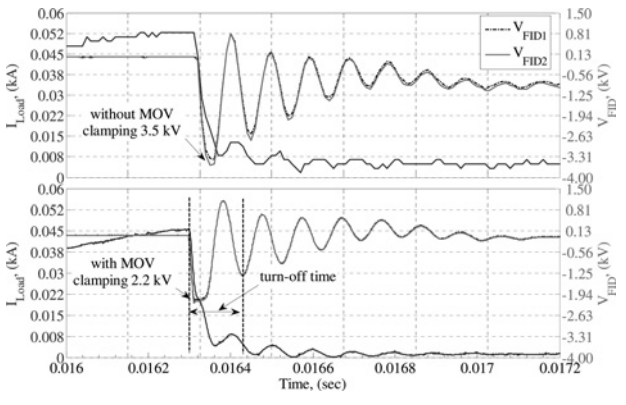

Fig. 10 *FID operation without and with MOV*

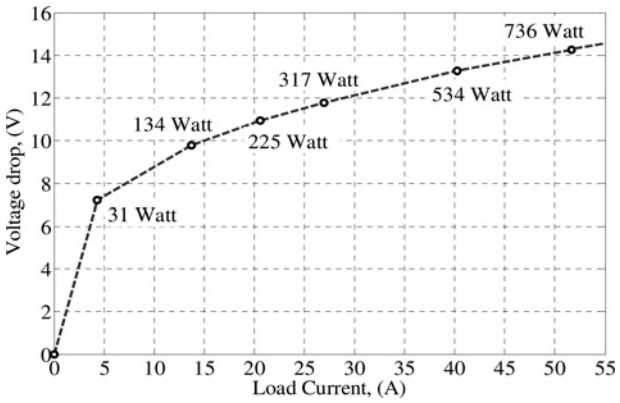

Fig. 11 *Measured voltage drop across and power loss within the FID device against load current*

high maintenance costs [10]. In comparison, the lifetime of FID is primarily determined by its high-voltage capacitors and utilised semiconductors.

In order to determine the power losses of the entire FID, the prototype was connected in series with a small base resistance (3 Ω) to a linear current amplifier. The voltage drop across the device (across all three modules) was measured, while the amplitude of the 60 Hz sinusoidal reference signal was gradually increased up to 50 A. The power loss of the entire FID device at 50 A is approximately 700 W, as can be seen from Fig. 11. In the 1 MW PEDS (7.2 kV L–N rated voltage, 50 A), this corresponds to a power loss of 0.2%. It should be noted, however, that a 15 kV-class CB (e.g. BreakMaster™ Load Interrupter Switch) has significantly lower power loss value, which is ca. 200 mW per pole at 50 A.

In order to reduce this loss, the FID may be bypassed using, for example, a vacuum circuit breaker (VCB). The VCB opens on detecting a short-circuit fault in the downstream power network. In addition, as mentioned above, augmenting the solid-state breaker with an ultra-fast mechanical bypass switch, as similar to the concepts presented in [6, 7] may significantly further reduce on-state losses.

5 Conclusion

In this paper, the concept of an ultra-fast acting FID intended for medium-voltage systems was presented and the FID features were discussed, emphasising the requirements of the power electronics-based distribution systems in which the device is intended to be used. The ultra-fast FID operation was confirmed in experimental test circuits, utilising power electronic converters in different topologies with different switching frequencies. It was identified that FID operation is not influenced by the switching frequencies of the power electronic converters and their topologies, and is only determined by line parameters such as line inductance and line capacitance. The presented FID prototype operates very fast and might be able to interrupt the short-circuit current before it reaches the maximum value. Owing to its demonstrated ultra-fast operation, the presented device shows promise for use as a short-circuit current limiter. Since the semiconductor devices that are currently on the market are not capable of blocking sufficiently high voltages, a series connection of three modules (building blocks) was required for 4.16 kV system. The overvoltage management of an FID, utilising passive elements such as MOVs and active d*i*/d*t* control, is presented in the paper. In addition, the validated simulation model of a medium-voltage FID was developed for future studies. Further investigation of active d*i*/d*t* control for overvoltage management and implementation of a PEDS protection algorithm is needed and could be implemented in the future.

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