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Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications

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***Abstract*—An efficiency-optimized modulation scheme and design method are developed for an existing hardware prototype of a bidirectional dual active bridge (DAB) dc/dc converter. The DAB being considered is used for an automotive application and is made up of a high-voltage port with port voltage V_1, 240 V $\leq V_1 \leq$ 450 V, and a low-voltage port with port voltage V_2, 11 V $\leq V_2 \leq$ 16 V; the rated output power is 2 kW. A much increased converter efficiency is achieved with the methods detailed in this paper: The average efficiency, calculated for different voltages V_1 and V_2, different power levels, and both directions of power transfer, rises from 89.6% (conventional phase shift modulation) to 93.5% (proposed modulation scheme). Measured efficiency values, obtained from the DAB hardware prototype, are used to verify the theoretical results.**

***Index Terms*—Battery chargers, circuit optimization, dc-dc power conversion, design methodology, digital systems.**

Nomenclature

D_1	Duty cycle used for the HV full bridge.
D_2	Duty cycle used for the LV full bridge.
φ	Phase angle between v_{T1} and v_{T2}.
f_{S}	Switching frequency.
i_{T1}	Transformer current, HV side.
i_{T2}	Transformer current, LV side.
$I_{\mathrm{S1,sw,min}}$	Minimum HV MOSFET current needed to achieve low switching losses, HV side.
$I_{\mathrm{S2,sw,opt}}$	LV MOSFET current needed to achieve minimum switching losses on the LV side.
L	DAB converter inductance.
n	Transformer turns ratio.
P_1	HV port power.
P_2	LV port power.
P_{out}	Converter output power.
$P_{\mathrm{out,d}}$	Designated output power (mod. scheme).
$P_{\triangle,\mathrm{a,max}}$	Maximum power of the modified triangular current mode modulation for $V_2 \leq V_{2,\mathrm{lim}}$.
$P_{\triangle,\mathrm{b,max}}$	Maximum power of the modified triangular current mode modulation for $V_2 \geq V_{2,\mathrm{lim}}$.
$P_{\triangle,\mathrm{V2\,lim,max}}$	Maximum power of the modified triangular current mode modulation at $V_2 = V_{2,\mathrm{lim}}$.
$P_{\mathrm{opt,a,min}}$	Minimum power of the high-power mod. scheme for $V_2 \leq V_{2,\mathrm{lim}}(P_{\mathrm{opt,a,min}} > P_{\triangle,\mathrm{a,max}})$.
$P_{\mathrm{opt,b,min}}$	Minimum power of the high-power mod. scheme for $V_2 \geq V_{2,\mathrm{lim}}(P_{\mathrm{opt,b,min}} > P_{\triangle,\mathrm{b,max}})$.
$P_{\mathrm{opt,a,hi}}$	Transition power level with $D_1 = D_2 = 0.5$ for $V_2 \leq V_{2,\mathrm{lim}}(P_{\mathrm{opt,a,hi}} > P_{\mathrm{opt,a,min}})$.
P_{max}	Maximum output power of the DAB.
T_{S}	Switching period, $T_{\mathrm{S}} = 1/f_{\mathrm{S}}$.
V_1	HV port voltage.
V_2	LV port voltage.
$V_{2,\mathrm{lim}}$	Defines the boundary between different operating modes of the DAB.
v_{T1}	AC volt. generated by the HV full bridge.
v_{T2}	AC volt. generated by the LV full bridge.

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I. Introduction

RECENT trends in the automotive industry toward electric vehicles, hybrid electric vehicles, and fuel-cell-powered vehicles create the need for highly compact, lightweight, and efficient power converters [1], to exchange electrical power between the various on-board power sources [2]. In order to further push existing limits, a procedure for efficiency-optimized converter design and modulation scheme are presented for a bidirectional automotive dc/dc converter. The dc/dc converter investigated here transfers power between the high-voltage (HV) dc port of a fuel cell stack and the dc port of a low-voltage (LV) battery [3], [4]. The converter specifications are:

- HV port: 240 V $\leq V_1 \leq$ 450 V, nominal voltage: 340 V;
- LV port: 11 V $\leq V_2 \leq$ 16 V, nominal voltage: 12 V.

The rated output power of the dc/dc converter considered here is 2 kW within the above specified voltage ranges and bidirectional converter operation. A high converter efficiency of more than 90%, high reliability, and high power density are required with respect to the application in a car [5]; moreover, the HV dc port must be isolated galvanically from the LV dc port [3].

Typical topology candidates with these specifications include half- and full-bridge topologies with one or more dc inductors [6]–[8], the dual active bridge (DAB) converter [9]–[11], and resonant converter topologies [12]. Fig. 1(a) depicts the DAB converter, which is selected for the given application due to its soft-switching properties and the low number of passive components [13], making a highly compact converter feasible [7].

The conventional modulation scheme employed for the DAB converter [9], the so-called phase shift modulation, only achieves high converter efficiency for operating voltages close to $V_1 \approx nV_2$ (Section V-C). For $V_1 \ll nV_2$ or $V_1 \gg nV_2$, the transformer rms currents, the inductor and transformer copper losses, and the semiconductor conduction losses

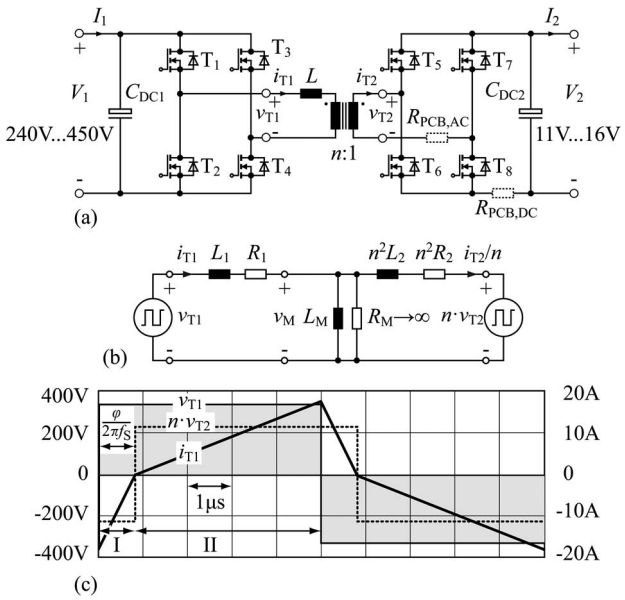

Fig. 1. (a) DAB topology; the resistors $R_{\mathrm{PCB,AC}}$ and $R_{\mathrm{PCB,DC}}$ model the printed circuit board (PCB) conduction losses; (b) employed electrical DAB model, which considers conduction losses and magnetizing current [11], [13]; and (c) calculated voltage and current waveforms for phase shift modulation, $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, $L = 26.7$ μH, $n = 19$.

increase considerably [14]. Fig. 1(c) depicts typical current and voltage waveforms for phase shift modulation. The respective duty cycles D_1 and D_2 (defined in Fig. 3) are $D_1 = 0.5$ and $D_2 = 0.5$ for phase shift modulation.

Considerably increased converter efficiency can be achieved for a given DAB converter with the use of alternative modulation schemes, which use $D_1 \leq 0.5$ and/or $D_2 \leq 0.5$. This paper aims to find a modulation scheme which enables converter operation at (or close to) maximum converter efficiency.

Initial investigations on alternative modulation schemes are given in [15] for a bidirectional ac/dc converter: The proposed alternative modulation schemes extend the zero-voltage switching (ZVS) range of the DAB and reduce the transformer rms currents (the principle of operation of ZVS is discussed in [16]). Detailed investigations of the modulation schemes presented in [15] with either $D_1 \leq 0.5 \wedge D_2 = 0.5$ or $D_1 = 0.5 \wedge D_2 \leq 0.5$ are presented in [17], [18]. The 1-D optimization problem (either D_1 or D_2 changes) with respect to maximal converter efficiency is solved in [17].

Highly efficient operation of the DAB is also achieved with modulation schemes employing $D_1 \leq 0.5$ and $D_2 \leq 0.5$ [19]–[22]. However, compared to the aforementioned 1-D problem, it is more complex to solve the resulting 2-D problem with respect to maximal efficiency [23]. Therefore, a more intuitive method is typically used to determine D_1 and D_2, e.g., in [19], [21], where triangular or trapezoidal transformer currents are generated in order to achieve low switching and low conduction losses. Further efficiency improvements are reported with the use of a combination of different existing modulation schemes [24], [25].

This paper presents a systematic approach to derive an efficiency-optimized modulation scheme for the DAB, which enables ZVS on the HV side without the need for additional circuitry [26] and goes on to propose an efficiency-optimized selection of the transformer turns ratio n and the converter inductance L used. Section II outlines the working principles of the DAB converter and Section III summarizes the converter loss model employed. Section IV details the results of the numerical search for efficiency-optimal values D_1 and D_2. Based on these results, the efficiency-optimized modulation scheme is developed in Section V and an efficiency-optimized converter design is proposed in Section VI. Finally, in Section VII, the analytically calculated efficiencies are verified with measured efficiencies obtained from an experimental setup.

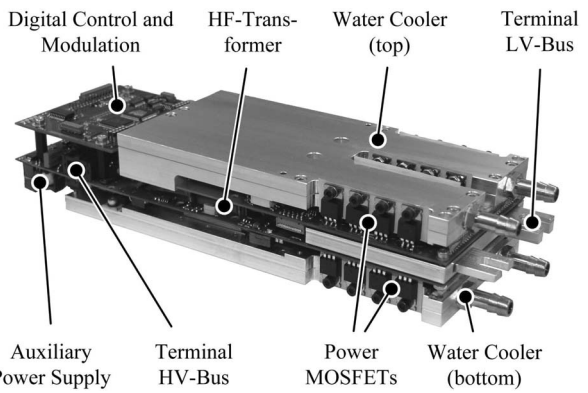

Fig. 2. 2-kW automotive DAB converter (273 mm × 90 mm × 53 mm); rated voltage transfer ratio: $V_1 = 340$ V, $V_2 = 12$ V.

II. Automotive DAB, Working Principle

The basic technical data of the DAB used and depicted in Fig. 2 is listed below.

- PCB: four-layer PCB, 200 μm copper on each layer.
- Switches (HV side): SPW47N60CFD.
- Switches (LV side): 8 × IRF2804 in parallel.
- DC capacitor (HV side): 6 × 470 nF/630 V in parallel.
- DC capacitor (LV side): 96 × 10 μF/25 V/X5R in parallel.
- Transformer core: two planar E58 cores.
- Transformer turns ratio, DAB inductance (cf. Section VI):
  - phase shift modulation: $n = 19$: 1, $L = 26.7$ μH;
  - optimized modulation: $n = 16$: 1, $L = 22.4$ μH.
- Switching frequency: $f_S = 100$ kHz.

The switching frequency is selected based on converter optimization results obtained for similar systems in order to achieve a high-efficiency and small-volume DAB converter:

- for a resonant LCC dc/dc converter with an input voltage of 320 V, an output voltage of 26 V, and an output power of 3.9 kW, a maximum power density of 13.3 kW/dm^3, and converter efficiency of $\eta = 93.7\%$ are calculated for a switching frequency of 176 kHz [27];
- for a current doubler dc/dc converter (input voltage: 400 V, output voltage range: 48 V $\leq V_2 \leq$ 56 V, output power: 5 kW), a maximum power density of 10.2 kW/dm^3, and converter efficiency of $\eta = 96.1\%$ are calculated for a switching frequency of 92.9 kHz [28].

The switching frequency considered for the DAB converter, $f_S = 100$ kHz, is selected close to 92.9 kHz, due to the impact of skin and proximity effects on the copper losses and due to high switching losses on the LV side. All semiconductor

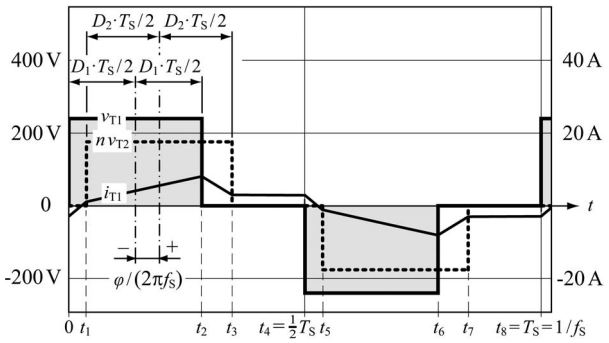

Fig. 3. The four DAB control parameters: φ denotes the phase shift between v_{T1} and v_{T2}, D_1, and D_2 are the respective duty cycles, and f_S is the switching frequency. The phase shift φ is measured between the centers of the positive active time intervals of v_{T1} and v_{T2}; $\varphi > 0$ applies in this figure. The selected definitions of φ, D_1, and D_2 can directly be used together with the fundamental component approximation approach, often used to analyze the DAB (e.g., [19]): the amplitudes of the fundamental components of v_{T1} and v_{T2} are $V_{1,f} = 4V_1 \sin(\pi D_1)/\pi$ and $V_{2,f} = 4V_2 \sin(\pi D_2)/\pi$, respectively, and φ is the phase shift between the cosine-shaped functions of the fundamental components. Employed operating point: $V_1 = 240$ V, $V_2 = 11$ V, $P_{out} = 500$ W (cf. (4)); $n = 16$, $L = 22.4\ \mu$H.

switches are realized using MOSFETs: In respect of the selected switching frequency, and the required current and voltage ratings, MOSFETs are found to be superior to insulated-gate bipolar transistors.

The voltage-sourced full-bridge circuits on the HV side and on the LV side, depicted in Fig. 1(a), can be replaced by the respective voltage sources v_{T1} and v_{T2} to simplify the investigations on the DAB converter. Fig. 1(b) shows the converter model used and which is developed in [13]; it assumes:

1) negligible parasitic capacitances of the transformer, e.g.; no coupling capacitance between LV and HV sides;
2) all quantities being referred to the HV side;
3) constant supply voltages V_1 and V_2.

The DAB converter model is parameterized in Section VI.

The DAB output power is adjusted by varying one or more of the four control parameters shown in Fig. 3 and listed below.

- phase shift between $v_{T1}(t)$ and $v_{T2}(t)$: $-\pi < \varphi < \pi$;
- duty cycle D_1 of $v_{T1}(t)$ with $0 < D_1 \leq 0.5$ [Fig. 3];
- duty cycle D_2 of $v_{T2}(t)$ with $0 < D_2 \leq 0.5$;
- switching frequency f_S.

Phase shift modulation uses constant switching frequency and maximum duty cycles, $D_1 = D_2 = 0.5$, and the controller varies solely the phase shift φ to achieve the required power transfer [29]. Assuming a loss-less DAB converter and a negligible magnetizing current, the transferred power

$$P = P_1 = P_2 = \frac{nV_1V_2\varphi \cdot (\pi - |\varphi|)}{2\pi^2 f_S L} \qquad \forall -\pi < \varphi < \pi \quad (1)$$

results [10], whereas $L \approx L_1 + n^2 L_2$ applies. Maximum power transfer is achieved for $\varphi = \pm\pi/2$ and the sign of P characterizes the power transfer direction

$$\begin{aligned} &P > 0 : \text{power transfer to the LV port(HV} \rightarrow \text{LV)};\\ &P < 0 : \text{power transfer to the HV port(LV} \rightarrow \text{HV)}. \end{aligned} \quad (2)$$

Fig. 4 depicts the power transfer characteristics of the DAB calculated with (1).

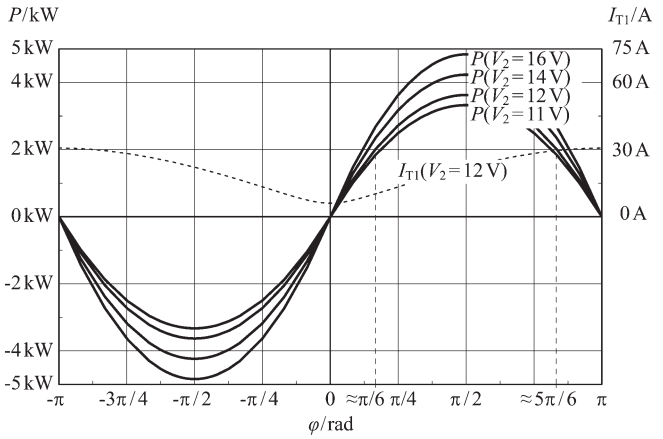

Fig. 4. DAB power transfer characteristics for phase shift modulation on the assumption of a loss-less converter ($P = P_1 = P_2$), $V_1 = 340$ V, and different voltages V_2; transformer rms current I_{T1} for $V_2 = 12$ V. The DAB is designed according to Section VI: $n = 19$, $L = 26.7\ \mu$H. Maximum power transfer, $|P| = P_{max}(V_1, V_2)$, is achieved at $\varphi = \pm\pi/2$. For power levels $|P| < P_{max}(V_1, V_2)$, two solutions exist for φ within $-\pi \leq \varphi < \pi$. For $|\varphi| > \pi/2$, increased rms currents result in the high-frequency transformer, the DAB inductor L, and the semiconductor switches; therefore, $|\varphi| < \pi/2$ is preferred.

The simplicity of phase shift modulation and the possibility of using half-bridge circuits to generate the high-frequency transformer voltages $v_{T1}(t)$ and $v_{T2}(t)$ are the main reasons for the wide use of this modulation method. Disadvantages are the limited operating range where low switching losses occur (soft-switching range [11]) and large rms currents in the high-frequency transformer for most operating points when the DAB is operated within wide input and/or output voltage ranges [14]. As a consequence, maximal converter efficiency is achieved only in a small area of the whole operating region (cf. Fig. 17).

III. DAB Loss Model

In order to develop an efficiency-optimized modulation scheme (Sections IV and V), the DAB loss model detailed in [13] is employed. This loss model considers the semiconductor's conduction and switching losses, the copper and core losses of the inductor and the transformer, and the gate driver power dissipation. The total converter losses$P_t = P_1 - P_2$ are calculated with (13) in [13] and the efficiency is

$$\eta = \frac{|P_{out}|}{|P_{out}| + P_t}. \quad (3)$$

Moreover, the converter output power P_{out} depends on the direction of power transfer

$$\begin{aligned} &\text{HV} \rightarrow \text{LV}: \quad P_{out} = P_2\\ &\text{LV} \rightarrow \text{HV}: \quad P_{out} = P_1. \end{aligned} \quad (4)$$

In anticipation of the results obtained in Section IV, low conduction and low switching losses are particularly important to achieve a high efficiency of the given DAB converter. The conduction losses are calculated with the transformer rms currents I_{T1} (HV side) and I_{T2} (LV side) [13]. Due to the complexities of the employed electrical DAB model [Fig. 1(b)] and the employed converter loss model [13], only numerical

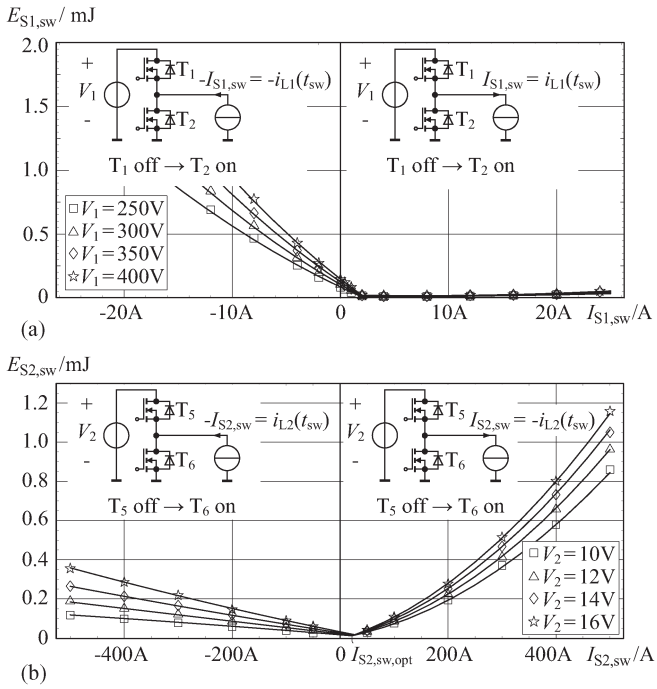

Fig. 5. Measured switching losses for a single-switching action (junction temperature: $T_j = 25$ °C) (a) HV side and (b) LV side. $I_{S1,sw}$ and $I_{S2,sw}$ indicate the switched current levels. Negative currents $I_{S1,sw}$ and $I_{S2,sw}$ denote hard switching; for positive currents $I_{S1,sw}$ and $I_{S2,sw}$ the condition for ZVS is satisfied. On the LV side, however, ZVS is not achieved for $I_{S2,sw} > 50$ A due to parasitic inductances in series to the semiconductor switches leading to high switching losses there [13]. The depicted circuits illustrate the respective switching operation of a half bridge with regard to the sign of $I_{S1,sw}$ or $I_{S2,sw}$.

TABLE I
EXPRESSIONS REQUIRED TO OBTAIN $I_{S1,sw}$ AND $I_{S2,sw}$ FROM THE RESPECTIVE INSTANTANEOUS TRANSFORMER CURRENTS $i_{T1}(t_{sw})$ AND $i_{T2}(t_{sw})$ AT A SWITCHING INSTANT t_{sw}; E.G., IN FIG. 3, AT $t = 0$, A RISING EDGE OF v_{T1} OCCURS AND THUS, THE HV SIDE FULL BRIDGE SWITCHES $I_{S1,sw} = -i_{T1}(0)$

HV Side, Edge Type of v_{T1}	$I_{S1,sw}$
Rising edge of $v_{T1}(t = t_{sw})$:	$I_{S1,sw} = -i_{T1}(t_{sw})$
Falling edge of $v_{T1}(t = t_{sw})$:	$I_{S1,sw} = i_{T1}(t_{sw})$
LV Side, Edge Type of v_{T2}	$I_{S2,sw}$
Rising edge of $v_{T2}(t = t_{sw})$:	$I_{S2,sw} = i_{T2}(t_{sw})$
Falling edge of $v_{T2}(t = t_{sw})$:	$I_{S2,sw} = -i_{T2}(t_{sw})$

solutions are feasible for I_{T1} and I_{T2}; the numerical solver algorithm employed is outlined in Appendix A.

The switching losses are determined based on the measurement results presented in Fig. 5 and the respective instantaneous transformer currents i_{T1} (HV side full bridge) and i_{T2} (LV side full bridge) at the switching instant. The instantaneous transformer currents i_{T1} and i_{T2} are calculated with the procedure summarized in Appendix A. The expressions given in Table I are used to determine the respective values $I_{S1,sw}$ and $I_{S2,sw}$, required to evaluate the switching loss functions depicted in Fig. 5. The measurement results depicted in Fig. 5 represent the total switching loss energy of one-half bridge due to a single switching process: Negative currents $I_{S1,sw}$ and $I_{S2,sw}$ denote hard switching and for positive currents $I_{S1,sw}$ and $I_{S2,sw}$, the condition for ZVS is satisfied [13].

IV. NUMERICAL EFFICIENCY OPTIMIZATION

The optimization procedure shown here determines the duty cycles D_1 and D_2 and the phase shift angle φ with respect to maximal converter efficiency in steady-state operation for selected operating points defined by the DAB port voltages V_1 and V_2 and the required output power P_{out} (cf. (4)). The output power for any $0 < D_1 \leq 0.5$, $0 < D_2 \leq 0.5$, and $-\pi < \varphi < \pi$ can either be calculated using an electric circuit simulator or with the procedure outlined in Appendix A.

The optimization procedure shown in this section can be used to obtain efficiency-optimal control parameters for arbitrary DAB converters. The calculated results are thereafter used in Section V in order to synthesize a new modulation scheme, which facilitates highly efficient operation of the investigated DAB converter.

In general, for a given operating point and given duty cycles, two solutions exist for the phase shift angle φ. For example, in Fig. 4, two phase shift angles, $\varphi_1 \approx \pi/6$ and $\varphi_2 \approx 5\pi/6$, generate an output power of 2 kW for $V_1 = 340$ V and $V_2 = 12$ V. The presented optimization procedure employs the minimal phase shift angle φ_{min}, required to obtain the specified output power, according to

$$\varphi_{min}(V_1, V_2, P_{out}, D_1, D_2) = \min|\varphi(V_1, V_2, P_{out}, D_1, D_2)| \cdot \operatorname{sgn}(\varphi(V_1, V_2, P_{out}, D_1, D_2)) \quad (5)$$

since φ_{min} allows for lower rms currents I_{T1} and I_{T2} and results in lowest conduction losses (cf. I_{T1} in Fig. 4). Thus, the considered converter efficiency η_0, calculated with (3) and (5), depends on the operating point and the two duty cycles

$$\eta_0(V_1, V_2, P_{out}, D_1, D_2) = \eta(V_1, V_2, P_{out}, D_1, D_2, \varphi_{min}(V_1, V_2, P_{out}, D_1, D_2)). \quad (6)$$

In order to determine the maximum efficiency at a given operating point, a numerical solver varies D_1 and D_2:

$$\eta_{opt} = \max(\eta_0(V_1, V_2, P_{out}, D_1, D_2)) \quad \forall 0 < D_1 \leq 0.5 \wedge 0 < D_2 \leq 0.5. \quad (7)$$

(on the assumption of constant V_1, V_2, and P_{out}).

A thorough investigation of different operating points within the full specified operating range reveals essentially different results for $V_1 > nV_2$ and $V_1 < nV_2$. Therefore, two meaningful examples are used to summarize the results of the investigations obtained for the DAB with $n = 16$ and $L = 22.4$ μH designed in Section VI:

1) $V_1 > nV_2$: $V_1 = 340$ V, $V_2 = 12$ V, $P_2 > 0$ [cf. (2)];
2) $V_1 < nV_2$: $V_1 = 240$ V, $V_2 = 16$ V, $P_2 > 0$.

A. $V_1 > nV_2$: $V_1 = 340$ V, $V_2 = 12$ V, $P_2 > 0 (HV \rightarrow LV)$

Analytical optimization of D_1 and D_2 with respect to the transformer rms current reveals that minimal rms current is achieved with the triangular current mode modulation [19] depicted in Fig. 6(a).[1] Due to considerable switching losses,

[1]The respective derivation considers the loss-less DAB model given in [11] and assumes an infinitely large transformer magnetizing inductance.

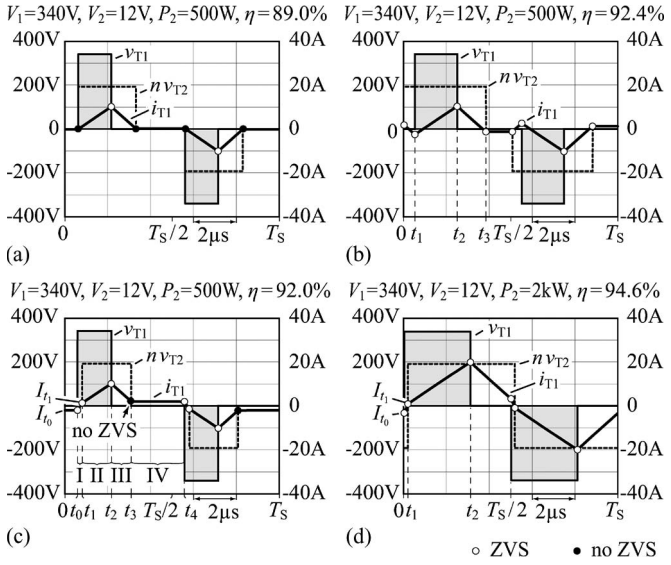

Fig. 6. Waveforms of v_{T1}, v_{T2}, and i_{T1} (cf. Fig. 1(a)) obtained for $V_1 = 340$ V, $V_2 = 12$ V, and different operating conditions; (a) triangular current mode modulation according to [19] and $P_{out} = 500$ W; (b), (c) modulation at $P_{out} = 500$ W: optimal and suboptimal converter efficiency, η_{opt} and η_{subopt} in Fig. 7(a), respectively; besides, (c) illustrates the modified triangular current mode modulation detailed in Section V-A1; and (d) optimal converter efficiency at $P_{out} = 2$ kW. Employed DAB: $n = 16$, $L = 22.4$ μH.

however, the efficiency obtained with the triangular current mode modulation is not maximal: At $P_{out} = 500$ W, $\eta = 89\%$ results.

Fig. 7 depicts the calculated converter efficiencies within $0 < D_1 \leq 0.5$ and $0 < D_2 \leq 0.5$ and for different output power levels. The efficiency η_{opt} marks the locations of the global efficiency maxima. Besides, for $P_{out} = 500$ W [Fig. 7(a)] and $P_{out} = 1$ kW [Fig. 7(b)], local efficiency maxima, marked with η_{subopt}, are observed. According to Fig. 7, with increasing output power, the global and the local efficiency maxima shift toward $D_2 = 0.5$. Above a certain power level, only a global maximum remains; this is shown in Fig. 7(c) and (d) for $P_{out} = 1.5$ kW and $P_{out} = 2$ kW. Fig. 7 further indicates, that the local maximum depicted in Fig. 7(a) and (b) shifts toward $D_2 = 0.5$ with increasing P_{out} and becomes a global maximum in Fig. 7(c) and (d). As a consequence, a step in the efficiency-optimal control parameters D_1, D_2, and φ can be observed in Fig. 8(a) between $P_{out} = 1.1$ kW and $P_{out} = 1.2$ kW.

The different properties of the most interesting operating points, i.e., operation at global and local efficiency maxima, need to be investigated in order to synthesize an efficiency-optimized modulation scheme. At the global efficiency maximum and $P_{out} = 500$ W, a converter efficiency of $\eta_{opt} = 92.4\%$ is achieved. There, the DAB converter experiences slightly increased conduction losses due to increased transformer rms currents; however, according to Figs. 5 and 6(b), minimal switching losses are achieved, since best possible instantaneous transformer currents (and thus switch currents) occur during switching:

- $I_{S1,sw,1} = -i_{T1}(t_1) \approx I_{S1,sw,min}$ (ZVS, cf. Appendix B);
- $I_{S1,sw,2} = +i_{T1}(t_2) > I_{S1,sw,min}$ (ZVS);
- $I_{S2,sw} = n i_{T1}(0) = n_{T1}(t_3) \approx 20$ A (ZVS).

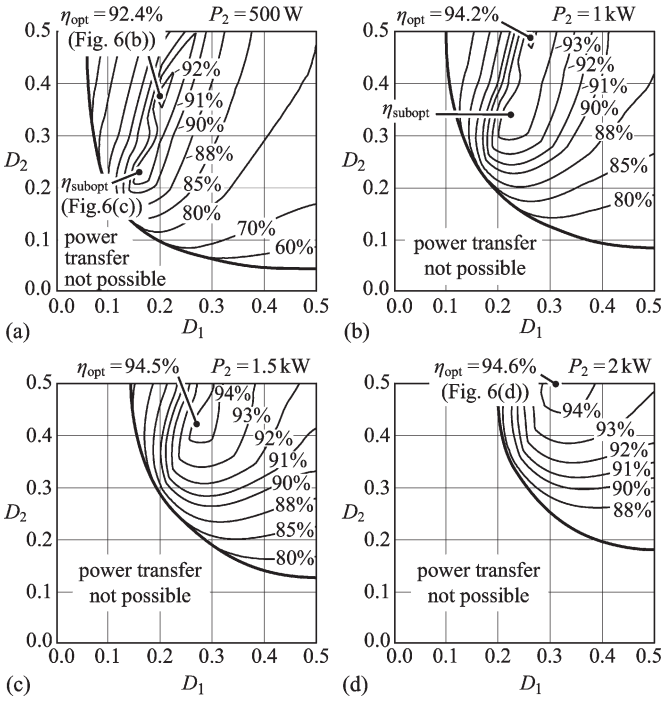

Fig. 7. Converter efficiency determined according to Section III and (6) for $0 < D_1 \leq 0.5$, $0 < D_2 \leq 0.5$, fixed operating voltages ($V_1 = 340$ V, $V_2 = 12$ V), and different power levels: (a) $P_{out} = 500$ W, (b) $P_{out} = 1$ kW, (c) $P_{out} = 1.5$ kW, (d) $P_{out} = 2$ kW. For low power levels, depicted in Fig. 7(a) and (b), a global maximum, η_{opt}, and a local maximum, η_{subopt}, occurs; for high power levels, Fig. 7(c) and (d), only a global maximum remains. Power transfer is not possible for combinations of D_1 and D_2 outside the indicated boundary. In that case, no solution exists for φ with respect to the required output power. On the contrary, the required output power can be achieved with any combination of D_1 and D_2 inside the indicated boundary. Employed DAB converter: $n = 16$, $L = 22.4$ μH.

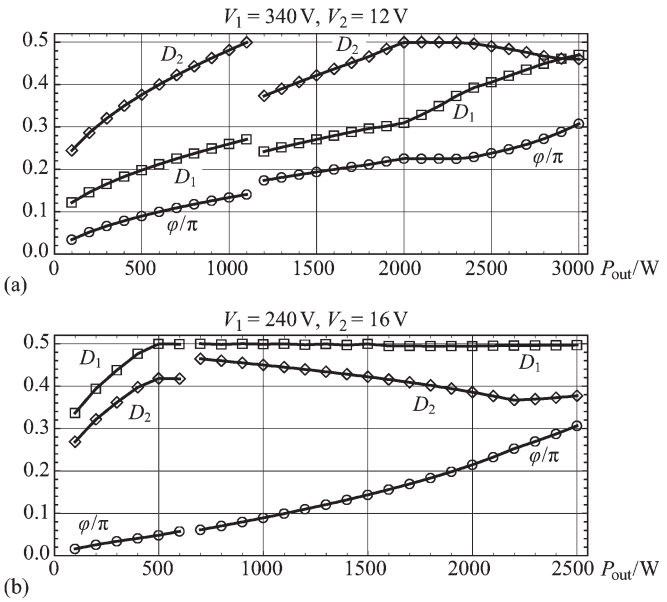

Fig. 8. (a) D_1, D_2, and φ required to achieve maximum converter efficiency for $V_1 = 340$ V, $V_2 = 12$ V, and power being transferred to the LV port: for P_{out} between 1.1 and 1.2 kW, a step change in D_1, D_2, and φ occurs; (b) D_1, D_2, and φ for maximum converter efficiency, $V_1 = 240$ V, $V_2 = 16$ V, and power being transferred to the LV port: for P_{out} between 600 and 700 W, $D_2(P_{out})$ exhibits a step change. Employed DAB converter: $n = 16$, $L = 22.4$ μH.

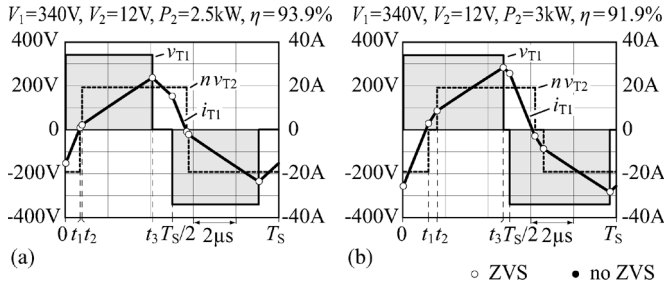

Fig. 9. Waveforms of v_{T1}, v_{T2}, and i_{T1} obtained for $V_1 = 340$ V, $V_2 = 12$ V, and efficiency-optimal operation at very high power levels (exceeding the rated power of 2 kW): (a) $P_2 = 2.5$ kW and (b) $P_2 = 3$ kW. Employed DAB converter: $n = 16$, $L = 22.4\ \mu$H.

Due to the parasitic effective output capacitances of the HV MOSFETs used, a minimum current $I_{\mathrm{S1,sw,min}}$ is required to obtain low switching losses on the HV side [13]; the optimal selection of $I_{\mathrm{S1,sw,min}}$ is given in Appendix B. On the LV side, minimum switching losses are obtained for

$$I_{\mathrm{S2,sw}} \approx I_{\mathrm{S2,sw,opt}} \approx 20\ \mathrm{A}\ (\text{cf. Fig. 5(b)}). \tag{8}$$

At the local efficiency maximum and $P_{\mathrm{out}} = 500$ W, a converter efficiency of $\eta = 92.0\%$ is achieved. The LV side full bridge there exhibits switching losses due to hard-switching operation at $t = t_3$ [Fig. 6(c)]. This operating mode is nonetheless employed for the suboptimal modulation scheme discussed in Section V, in order to avoid the step of D_1, D_2, and φ shown in Fig. 8(a), and is termed modified triangular current mode modulation.

According to Figs. 7(d) and 8(a), optimal operation at rated power $P_{\mathrm{out}} = 2$ kW is achieved with $D_1 = 0.31$ and $D_2 = 0.5$. Fig. 6(d) depicts the corresponding current and voltage waveforms. Minimal reactive power is achieved on the LV side, since the instantaneous power $p_2(t)$

$$p_2(t) = v_{\mathrm{T2}}(t) \cdot i_{\mathrm{T2}}(t) \approx v_{\mathrm{T2}}(t) \cdot n i_{\mathrm{T1}}(t) \tag{9}$$

does (virtually) not change sign during $0 < t < T_{\mathrm{S}}$ [22] and thus, minimal conduction losses are achieved on the LV side. Moreover, minimal switching losses are achieved due to ZVS operation of the HV full bridge (cf. Table I) and due to the operation of the LV side full bridge with instantaneous switch currents $I_{\mathrm{S2,sw}}$ close to zero.

The optimization algorithm increases D_1 with increasing power levels and keeps D_2 close to 0.5. This can be observed in Fig. 8(a) for power levels between 2 and 2.4 kW.

At very high power levels, finally, large phase shift angles and duty cycle values close to 0.5 are needed. As a consequence, the transformer rms currents rise considerably [19] and the instantaneous currents during switching increase. According to Fig. 8(a), the optimization algorithm reduces D_2 for $P_{\mathrm{out}} > 2.4$ kW. A reduction of the switching losses is achieved on the LV side with this, as illustrated in Fig. 9(b): Only two LV switches (e.g., T_5 and T_6) switch $I_{\mathrm{S2,sw}} > I_{\mathrm{S2,sw,opt}}$; the remaining two (e.g., T_7 and T_8) switch $I_{\mathrm{S2,sw}} \approx I_{\mathrm{S2,sw,opt}}$ (cf. Table I).

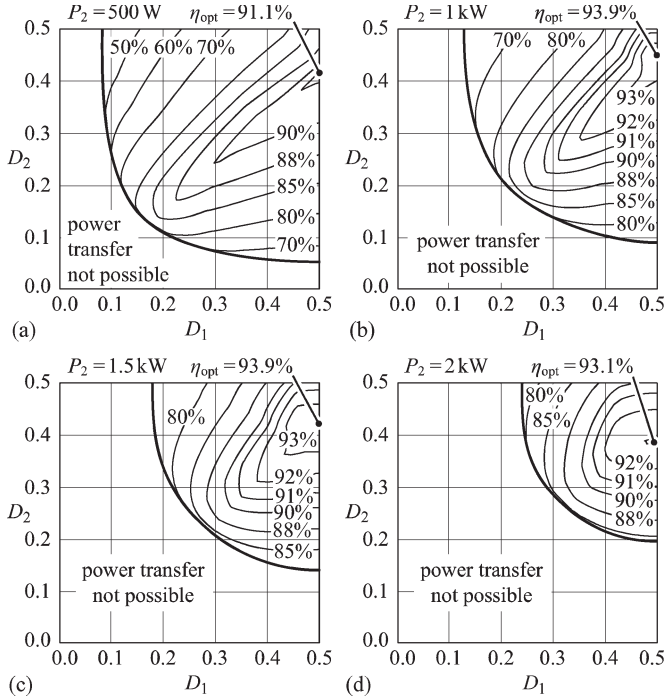

Fig. 10. Converter efficiency calculated for $0 < D_1 \leq 0.5$, $0 < D_2 \leq 0.5$, $V_1 = 240$ V, $V_2 = 16$ V, and different power levels: (a) $P_{\mathrm{out}} = 500$ W, (b) $P_{\mathrm{out}} = 1$ kW, (c) $P_{\mathrm{out}} = 1.5$ kW, and (d) $P_{\mathrm{out}} = 2$ kW. Employed DAB: $n = 16$, $L = 22.4\ \mu$H.

B. $V_1 < nV_2$: $V_1 = 240$ V, $V_2 = 16$ V, $P_2 > 0 (HV \rightarrow LV)$

The efficiency maps calculated for $V_1 = 240$ V and $V_2 = 16$ V (Fig. 10) are entirely different to the efficiency maps calculated in the previous Section IV-A. The optimization procedure varies D_2 and keeps D_1 close to 0.5. Again, local and global efficiency maxima occur and the efficiency-optimal duty cycle D_2 exhibits a step change as shown in Fig. 8(b). However, compared to Section IV-A, the effect is less distinct and not visible in the efficiency maps depicted in Fig. 10.

The waveforms related to optimal DAB operation are shown in Fig. 11. Fig. 11(a) depicts the waveform of the transformer current i_{T1} for $P_{\mathrm{out}} = 500$ W: i_{T1} is nearly triangular and thus, low conduction losses result. Moreover, the instantaneous transformer currents during switching facilitate low switching losses due to the reasons given in Section IV-A and thus, a high total converter efficiency of 91.1% is achieved. However, similar to the DAB operation at $V_1 = 340$ V, $V_2 = 12$ V, and $P_{\mathrm{out}} = 500$ W, the discontinuous duty cycle function shown in Fig. 8(b) complicates the practical implementation.

A considerably reduced complexity is achieved if the modified triangular current mode modulation is used; typical current and voltage waveforms are depicted in Fig. 11(b). This modulation scheme facilitates a seamless transition between the operation with $V_1 < nV_2$ and the operation with $V_1 > nV_2$ due to the similarities to the modified triangular current mode modulation depicted in Fig. 6(c).[2] The converter achieves nonetheless very high efficiency in the region of η_{opt} (e.g., $\eta = 90.7\%$ for $P_{\mathrm{out}} = 500$ W).

[2]More precisely, the modified triangular current mode modulation scheme facilitates a seamless transition between $V_2 \leq V_{2,\mathrm{lim}}$ and $V_2 \geq V_{2,\mathrm{lim}}$, cf. Section V-A3: (21) and (22).

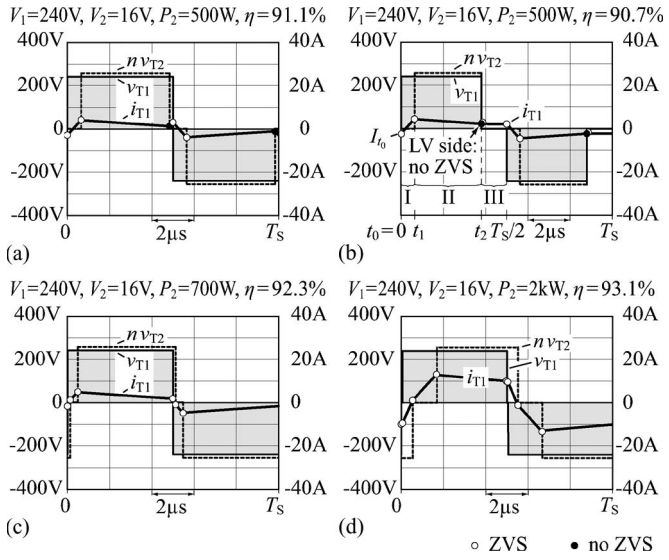

Fig. 11. Waveforms of v_{T1}, v_{T2}, and i_{T1} obtained for $V_1 = 240$ V, $V_2 = 16$ V, and different operating conditions; (a) efficiency-optimal modulation at $P_{\mathrm{out}} = 500$ W (η_{opt} in Fig. 10(a)); (b) modified triangular current mode modulation detailed in Section V-A-2 at $P_{\mathrm{out}} = 500$ W; (c), (d) modulation for optimal converter efficiency at $P_{\mathrm{out}} = 700$ W (cf. Fig. 8(b)) and at $P_{\mathrm{out}} = 2$ kW (η_{opt} in Fig. 10(d)), respectively. Employed DAB: $n = 16$, $L = 22.4\ \mu$H.

By use of $P_{\mathrm{out}} = 700$ W, depicted in Fig. 11(c), the DAB exceeds the maximum output power possible with the modulation scheme shown in Fig. 11(a). The optimization procedure there selects $D_1 = 0.5$ and $D_2 < 0.5$ in order to achieve ZVS on the HV side and low switching losses on the LV side (according to Fig. 11(c); however, only one LV side half bridge switches $I_{\mathrm{S2,sw}} \approx I_{\mathrm{S2,sw,opt}}$; due to $V_1 < nV_2$, it is unavoidable that the other LV half bridge switches $I_{\mathrm{S2,sw}} > I_{\mathrm{S2,sw,opt}}$). This scheme remains unchanged with increasing output power. Fig. 11(d) illustrates the calculated voltage and current waveforms for $P_{\mathrm{out}} = 2$ kW. Again, large duty cycles and large phase shift angles are needed at very high power levels, which is shown in Fig. 8(b) (cf. Section IV-A), and the efficiency-optimal results for D_1, D_2, and φ violate $I_{\mathrm{S2,sw}} \approx I_{\mathrm{S2,sw,opt}}$ at very high power levels; nonetheless $D_1 = 0.5$ remains.

V. Suboptimal Modulation Scheme

The findings obtained in the previous Section IV facilitate the development of an optimized modulation scheme in order to operate the given DAB close to the maximum achievable efficiency. The proposed modulation scheme therefore minimizes the impact of the most important DAB loss mechanisms:

- conduction losses;
- HV side switching losses (ZVS is required);
- LV side switching losses ($I_{\mathrm{S2,sw}} \approx I_{\mathrm{S2,sw,opt}}$, cf. (8)).

No closed-form solutions exist for the control parameters D_1, D_2, and φ, due to the complexities of the electrical DAB model employed [Fig. 1(b)] and the converter loss model used [13]. Numerical solvers are used to evaluate the equation systems developed in this section in order to obtain values for D_1, D_2, and φ. Currently, all solvers are implemented in Mathematica and a computer calculates the control parameters offline for 8192 different operating points according to the explanations given in this section. The results calculated are then postprocessed in order to reduce the effects of current-dependent time delays caused by the DAB hardware [30]. The control data so obtained is stored in a table that resides in the digital control part of the DAB converter i.e., a digital signal processor (DSP). The DSP finally uses linear interpolation to approximately determine the required control parameters [31].[3]

This description of the optimized modulation scheme is limited to a power transfer to the LV side; however, the principles discussed apply to power transfer in any direction and it is straightforward to extend the modulation scheme in order to permit a power transfer to the HV side. Furthermore, a negligible magnetizing current is considered, i.e., $i_{\mathrm{T1}} \approx i_{\mathrm{T2}}/n$ applies.

A. Optimized DAB Operation at Low Power Levels: Modified Triangular Current Mode Modulation

According to Section IV, highly efficient converter operation close to η_{opt} is achieved by the DAB converter with the modified triangular current mode modulation scheme. Typical current and voltage waveforms are shown in Fig. 6(c) for nominal converter operation.

The original version of the triangular current mode modulation scheme distinguishes between $V_2 < V_1/n$ and $V_2 > V_1/n$ in order to calculate D_1, D_2, and φ, due to essentially different characteristics of the transformer currents; the respective calculation is thoroughly discussed in [14], [19]. Detailed investigations show that the modified triangular current mode modulation scheme distinguishes between $V_2 \leq V_{2,\mathrm{lim}}$ (mode a) and $V_2 \geq V_{2,\mathrm{lim}}$ (mode b), whereas

$$V_{2,\mathrm{lim}} < V_1/n. \tag{10}$$

The actual computation of $V_{2,\mathrm{lim}}$ is explained in Section V-A3, subsequent to the discussion of the modified triangular current mode modulation schemes; a typical characteristics of $V_{2,\mathrm{lim}}$ is shown in Fig. 14. An analytical investigation of the modified triangular current mode modulation scheme reveals that $V_{2,\mathrm{lim}} = V_1/n$ would be achieved for a loss-less converter and for $-I_{t_0} = I_{t_1}$ in Fig. 6(c). However, based on the results of Section IV, i.e., due to the different switching loss characteristics of the HVMOSFETs and the LV MOSFETs, $-I_{t_0} > 2$ A and $I_{t_1} = I_{\mathrm{S2,sw,opt}}/n \approx 20/n = 1.25$ A are required on the HV side and on the LV side, respectively (cf. (8); $n = 16$ is assumed). Therefore, the inequality (10) results.

It is important to note that the modified triangular current mode modulation scheme achieves ZVS on the HV side; however, one hard-switching process per half-cycle occurs on the LV side, e.g., at $t = t_3$ in Fig. 6(c) and at $t = t_2$ in Fig. 11(b).

[3]The actual implementation employs 16 values for V_1, 16 values for V_2, and 16 values for P_{out} in either direction of power transfer. Due to the linear interpolation, a maximum absolute error of 58 W is calculated for the output power with the basic values being evenly distributed. Moreover, the resistive dividers employed to measure V_1 and V_2 consist of resistors with an accuracy of 0.1%. In order to eliminate the errors due to the linear interpolation and the voltage measurements, a current controller is required (cf. [29]).

1) $V_2 \le V_{2,\mathrm{lim}}$ (mode a: Fig. 6(c)): During $0 < t < t_0$, both full bridges remain in their freewheeling states, i.e., $v_{\mathrm{T1}} = v_{\mathrm{T2}} = 0$, and a negative transformer current $i_{\mathrm{T1}}(t_0) = I_{t_0}$ enables ZVS at $t = t_0$; subsequently, during $t_0 < t < t_1$, the HV full bridge applies $v_{\mathrm{T1}} = V_1$. The transformer current i_{T1} increases to $i_{\mathrm{T1}}(t_1) \approx I_{t_1} = I_{\mathrm{S2,sw,opt}}/n \approx 20$ A/n: At $t = t_1$, the LV full bridge switches to $v_{\mathrm{T2}} = V_2$ and thereby generates minimal switching losses (cf. Fig. 5(b)). Due to $V_1 > nV_2$, i_{T1} continues to increase during $t_1 < t < t_2$ until the HV full bridge switches to its freewheeling state at $t = t_2$ (ZVS). During time interval III, the transformer current decreases to $i_{\mathrm{T1}}(t_3) = -I_{t_0}$. At $t = t_3$, the LV full bridge switches to $v_{\mathrm{T2}} = 0$ (hard switching operation) and the remaining transformer current during $t_3 < t < t_4$, $i_{\mathrm{T1}}(t) = -I_{t_0}$, enables ZVS for the HV full bridge at $t = t_4$. During the second half-cycle ($T_{\mathrm{S}}/2 < t < T_{\mathrm{S}}$), the voltage and current waveforms repeat with reverse sign.

The durations of the respective time intervals I, II, and III are calculated thus in order to

- provide the specified output power P_{out} (cf. (4));
- generate the freewheeling current $I_{t_0} = -I_{\mathrm{S1,sw,min}}$ (enables ZVS on the HV side, cf. Appendix B);
- generate the current $I_{t_1} = I_{\mathrm{S2,sw,opt}}/n$ (cf. (8)) to achieve low switching losses on the LV side.

The computation of the respective control parameters D_1, D_2, and φ employs an approximate value of the duration of time interval I in Fig. 6(c), T_{I}, in order to reduce the computational effort

$$T_{\mathrm{I}} = \frac{L \cdot (-I_{t_0} + I_{t_1})}{V_1} = \frac{L \cdot (I_{\mathrm{S1,sw,min}} + I_{\mathrm{S2,sw,opt}}/n)}{V_1}. \quad (11)$$

The calculation of D_1, D_2, and φ employs

$$\frac{D_1}{2f_{\mathrm{S}}} + \frac{|\varphi|}{2\pi f_{\mathrm{S}}} = T_{\mathrm{I}} + \frac{D_2}{2f_{\mathrm{S}}} \Rightarrow D_1 = D_2 - \frac{|\varphi|}{\pi} + 2T_{\mathrm{I}} f_{\mathrm{S}} \quad (12)$$

for mode a, which can be derived from Figs. 3 and 6(c). A numerical search algorithm seeks suitable values D_2 and φ that meet the requirements

$$P_{\mathrm{out}}(D_1, D_2, \varphi) = P_{\mathrm{out,d}} \text{ and} \quad (13)$$
$$I_{t_0}(D_1, D_2, \varphi) = -I_{\mathrm{S1,sw,min}} \quad (14)$$
$$\forall\, V_2 \le V_{2,\mathrm{lim}} \wedge P_{\mathrm{out}} \le P_{\triangle,\mathrm{a,max}} \quad (15)$$

in order to achieve the designated output power $P_{\mathrm{out,d}}$ and the freewheeling current $I_{\mathrm{S1,sw,min}}$, cf. (50). The algorithm discussed in Appendix A calculates P_{out} and I_{t_0}.

Similar to the triangular current mode modulation scheme presented in [19], the maximum possible output power is limited according to (15). At $P_{\mathrm{out}} = P_{\triangle,\mathrm{a,max}}$, the expression $D_1/2 + |\varphi|/(2\pi) + D_2/2 = 1/2$ applies (cf. Fig. 3 for $t_3 = T_{\mathrm{S}}/2$) and with (12), the equation system needed to solve for $P_{\triangle,\mathrm{a,max}}$ becomes

$$[I_{t_0}(D_1, D_2) = -I_{\mathrm{S1,sw,min}} \wedge D_2 = 0.5 - T_{\mathrm{I}} f_{\mathrm{S}}] \Leftrightarrow P_{\mathrm{out}}(D_1, D_2) = P_{\triangle,\mathrm{a,max}}. \quad (16)$$

2) $V_2 \ge V_{2,\mathrm{lim}}$ (Mode b: Fig. 11(b)): During $t_0 < t < t_1$, the HV full bridge applies $v_{\mathrm{T1}} = V_1$, the LV full bridge remains in its freewheeling state, and the transformer currents increase; again, $i_{\mathrm{T1}}(t_0) = I_{t_0}$ enables ZVS on the HV side. At $t = t_1$, the LV full bridge switches to $v_{\mathrm{T2}} = V_2$ and during $t_1 < t < t_2$, the transformer currents decrease due to $V_1 < nV_2$. At $t = t_2$, the transformer current $i_{\mathrm{T1}}(t_2)$ reaches $-I_{t_0}$ and both full bridges simultaneously switch to the freewheeling states $v_{\mathrm{T1}} = v_{\mathrm{T2}} = 0$ (ZVS on the HV side, hard switching on the LV side).

The durations of the time intervals I and II are such that:

- the specified output power P_{out} (cf. (4)) is obtained
- the freewheeling current $I_{t_0} = -I_{\mathrm{S1,sw,min}}$ is generated.

The computation of D_1, D_2, and φ employs

$$\frac{D_1}{2f_{\mathrm{S}}} = \frac{|\varphi|}{2\pi f_{\mathrm{S}}} + \frac{D_2}{2f_{\mathrm{S}}} \Rightarrow D_2 = D_1 - \frac{|\varphi|}{\pi} \quad (17)$$

which can be derived from Figs. 3 and 11(b). A numerical search algorithm determines the values for D_1 and φ that satisfy (13) and (14) within

$$V_2 \ge V_{2,\mathrm{lim}} \wedge P_{\mathrm{out}} \le P_{\triangle,\mathrm{b,max}}. \quad (18)$$

The maximum possible output power $P_{\triangle,\mathrm{b,max}}$ is obtained from (17) and $D_1 = 0.5$:

$$\left[I_{t_0}(D_2, \varphi) = -I_{\mathrm{S1,sw,min}} \wedge D_1 = 0.5 \wedge D_2 = 0.5 - \frac{|\varphi|}{\pi}\right] \Leftrightarrow P_{\mathrm{out}}(D_2, \varphi) = P_{\triangle,\mathrm{b,max}}. \quad (19)$$

3) Calculation of $V_{2,\mathrm{lim}}$: At $V_2 = V_{2,\mathrm{lim}}$, both modified triangular current mode modulation schemes, i.e., mode a and mode b, can be used. The respective maximum possible power levels are identical there and are termed $P_{\triangle,\mathrm{V2\,lim,max}}$

$$P_{\triangle,\mathrm{V2\,lim,max}} = P_{\triangle,\mathrm{a,max}}(V_2 = V_{2,\mathrm{lim}}) = P_{\triangle,\mathrm{b,max}}(V_2 = V_{2,\mathrm{lim}}). \quad (20)$$

At $P_{\mathrm{out}} = P_{\triangle,\mathrm{V2\,lim,max}}$, for a given V_1 and with (11), (16), and (19), the control parameters become constant and the numerical solver solely needs to vary V_2 in order to satisfy $I_{t_0} = -I_{\mathrm{S1,sw,min}}$ and to calculate $V_{2,\mathrm{lim}}(P_{\triangle,\mathrm{V2\,lim,max}})$

$$[I_{t_0}(V_2) = -I_{\mathrm{S1,sw,min}} \wedge D_1 = 0.5 \wedge D_2 = 0.5 - T_{\mathrm{I}} f_{\mathrm{S}} \wedge \varphi = \pi T_{\mathrm{I}} f_{\mathrm{S}} \mathrm{sgn}(P_{\mathrm{out,d}})] \Leftrightarrow [V_2 = V_{2,\mathrm{lim}}(P_{\triangle,\mathrm{V2\,lim,max}}) \wedge P_{\mathrm{out}} = P_{\triangle,\mathrm{V2\,lim,max}}]. \quad (21)$$

The overview of all employed modulation schemes depicted in Fig. 14 shows that $V_{2,\mathrm{lim}}$ decreases with decreasing $P_{\mathrm{out}} < P_{\triangle,\mathrm{V2\,lim,max}}$. Since $I_{t_0} = -I_{\mathrm{S1,sw,min}}$ needs to be satisfied for mode a and mode b, and with (11) and (17), the respective equation system needed to compute $V_{2,\mathrm{lim}}(P_{\mathrm{out,d}})$ is

$$[P_{\mathrm{out}}(D_1, V_2) = P_{\mathrm{out,d}} \wedge I_{t_0}(D_1, V_2) = -I_{\mathrm{S1,sw,min}} \wedge \varphi = \pi T_{\mathrm{I}} f_{\mathrm{S}} \mathrm{sgn}(P_{\mathrm{out,d}}) \wedge D_2 = D_1 - \frac{|\varphi|}{\pi}] \Leftrightarrow V_2 = V_{2,\mathrm{lim}}(P_{\mathrm{out,d}}) \forall P_{\mathrm{out,d}} < P_{\triangle,\mathrm{V2\,lim,max}}. \quad (22)$$

A close inspection of the modulation schemes employed for $P_{\mathrm{out}} > P_{\triangle,\mathrm{V2\,lim,max}}$, i.e., at high power levels, reveals that $V_{2,\mathrm{lim}}(P_{\mathrm{out}})$ remains approximately equal to $V_{2,\mathrm{lim}}(P_{\triangle,\mathrm{V2\,lim,max}})$ (cf. Fig. 14).

B. Optimized DAB Operation at High Power Levels: Mode c

The duration of the freewheeling time interval used in the modified current mode modulation scheme decreases if the output power increases and reaches zero at $P_{\mathrm{out}} = P_{\triangle,\mathrm{a},\max}$ for $V_2 \leq V_{2,\mathrm{lim}}$ and at $P_{\mathrm{out}} = P_{\triangle,\mathrm{b},\max}$ for $V_2 \geq V_{2,\mathrm{lim}}$. The results obtained in Section IV suggest a new modulation scheme to be used at high power levels, which complies with the conditions listed below.

- $v_{\mathrm{T1}}(t)$ changes from V_1 to $-V_1$ during the time interval with constant voltage $v_{\mathrm{T2}}(t) = V_2$ or $v_{\mathrm{T2}}(t) = -V_2$.
- $v_{\mathrm{T2}}(t)$ changes from V_2 to $-V_2$ during the time interval with constant voltage $v_{\mathrm{T1}}(t) = V_1$ or $v_{\mathrm{T1}}(t) = -V_1$.

For example, Figs. 6(d), 9, and 11(c) and (d) satisfy these conditions; moreover, phase shift modulation (Section II) represents a special case and satisfies these conditions for all $0 < |\varphi| < \pi$. The operation with this new modulation scheme is denoted DAB operating mode c.

It can be shown, e.g., based on Figs. 3 and 9(b), that the operation within mode c requires

$$\frac{|\varphi|}{2\pi} + \frac{D_2}{2} \geq \frac{D_1}{2} + \left(\frac{1}{2} - D_1\right) \vee \frac{D_1}{2} \geq \frac{|\varphi|}{2\pi} - \frac{D_2}{2}. \quad (23)$$

In summary, φ is limited according to

$$\text{mode c} : 1 - (D_1 + D_2) \leq |\varphi|/\pi \leq D_1 + D_2. \quad (24)$$

Similar to Section V-A, D_1, D_2, and φ are determined in a different way for $V_2 \leq V_{2,\mathrm{lim}}$ and $V_2 \geq V_{2,\mathrm{lim}}$.

1) $V_2 \leq V_{2,\mathrm{lim}}$: D_1 and D_2 are selected according to the results depicted in Figs. 6(d), 7(d) and 8(a).

- $D_1 \leq 0.5$ in order to achieve low switching losses: the HV side full bridge needs to be operated with ZVS and on the LV side, switching currents close to $I_{\mathrm{S2,sw,opt}}$ (cf. (8)) result;
- $D_2 = 0.5$ (or D_2 close to 0.5 for very high power levels, cf. Section IV-A) in order to achieve low transformer rms currents and low conduction losses.

The respective computation of D_1 and D_2 distinguishes between three different output power levels.

1) $P_{\triangle,\mathrm{a},\max} < P_{\mathrm{out}} \leq P_{\mathrm{opt,a,min}}$: transition from mode a to high-power modulation.
2) $P_{\mathrm{opt,a,min}} < P_{\mathrm{out}} \leq P_{\mathrm{opt,a,hi}}$: $D_1 \leq 0.5$, $D_2 = 0.5$.
3) $P_{\mathrm{opt,a,hi}} < P_{\mathrm{out}} \leq P_{\max}$: $D_1 = 0.5$, $D_2 \leq 0.5$ in order to achieve reduced switching losses on the LV side.

The power level $P_{\triangle,\mathrm{a},\max}$ is given with (16), $P_{\mathrm{opt,a,min}}$, $P_{\mathrm{opt,a,hi}}$, and $P_{\max}$ are defined in this section.

Both duty cycles D_1 and D_2 are less than 0.5 at $P_{\mathrm{out}} = P_{\triangle,\mathrm{a},\max}$ [Fig. 12(a)]. Moreover, hard switching occurs on the LV side, e.g., at $t = T_{\mathrm{S}}/2$ in Fig. 12(a).

According to the results obtained in Section IV, low conduction losses and low switching losses are achieved with $D_2 = 0.5$, $i_{\mathrm{T1}}(0) \leq -I_{\mathrm{S1,sw,min}}$, and $i_{\mathrm{T1}}(t_1) = i_{\mathrm{T1}}(t_2) \approx I_{\mathrm{S2,sw,opt}}/n$, which is given in Fig. 12(b). The respective output power $P_{\mathrm{opt,a,min}}$ is higher than $P_{\triangle,\mathrm{a},\max}$ and is computed with

$$\begin{aligned}&[i_{\mathrm{T1}}(t = 0, D_1, \varphi) = -I_{\mathrm{S1,sw,min}} \wedge i_{\mathrm{T1}}(t = t_1, D_1, \varphi)\\ &\quad = I_{\mathrm{S2,sw,opt}}/n \wedge D_2 = 0.5]\\ &\Leftrightarrow P_{\mathrm{out}}(D_1, \varphi) = P_{\mathrm{opt,a,min}}. \end{aligned} \quad (25)$$

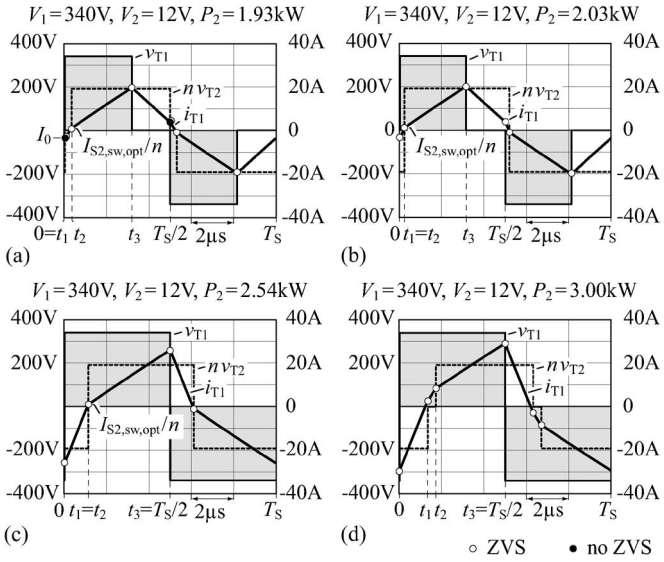

Fig. 12. Calculated waveforms $v_{\mathrm{T1}}(t)$, $v_{\mathrm{T2}}(t)$, and $i_{\mathrm{T1}}(t)$ for DAB operation at $V_1 = 340$ V and $V_2 = 12$ V, using the optimized modulation scheme: (a) $P_{\mathrm{out}} = 1.93$ kW, (b) $P_{\mathrm{out}} = 2.03$ kW, (c) $P_{\mathrm{out}} = 2.54$ kW, and (d) $P_{\mathrm{out}} = 3.00$ kW; $n = 16$, $L = 22.4\ \mu$H, and $L_{\mathrm{M}} = 1.9$ mH (thus, $i_{\mathrm{T1}} \approx i_{\mathrm{T2}}/n$ applies); Fig. 12(a)–(c) depict the limits of the respective operating modes: (a) $P_{\mathrm{out}} = P_{\triangle,\mathrm{a},\max}$; (b) $P_{\mathrm{out}} = P_{\mathrm{opt,a,min}}$; (c) $P_{\mathrm{out}} = P_{\mathrm{opt,a,hi}}$.

$P_{\mathrm{opt,a,min}} \approx 2$ kW applies for the given DAB converter at $V_1 = 340$ V and $V_2 = 12$ V. The control parameters D_1, D_2, and φ for output power levels between $P_{\triangle,\mathrm{a},\max}$ and $P_{\mathrm{opt,a,min}}$ are obtained from

$$\begin{aligned}&P_{\mathrm{out}}(D_1, D_2, \varphi) = P_{\mathrm{out,d}}\\ &i_{\mathrm{T1}}(t = 0, D_1, D_2, \varphi) = I_{t_0}\\ &i_{\mathrm{T1}}(t = t_1, D_1, D_2, \varphi) = I_{\mathrm{S2,sw,d}}/n\\ &\forall\, V_2 \leq V_{2,\mathrm{lim}} \wedge P_{\triangle,\mathrm{a},\max} < P_{\mathrm{out}} \leq P_{\mathrm{opt,a,min}}\end{aligned} \quad (26)$$

whereas a linear transition is employed for the LV side switch current $I_{\mathrm{S2,sw,d}}$,

$$\begin{aligned}I_{\mathrm{S2,sw,d}} = I_{\mathrm{S2,sw},\triangle,\mathrm{a},\max} + (I_{\mathrm{S2,sw,opt}} - I_{\mathrm{S2,sw},\triangle,\mathrm{a},\max})\\ \cdot \frac{P_{\mathrm{out,d}} - P_{\triangle,\mathrm{a},\max}}{P_{\mathrm{opt,a,min}} - P_{\triangle,\mathrm{a},\max}}\end{aligned} \quad (27)$$

with $I_{\mathrm{S2,sw},\triangle,\mathrm{a},\max} = n \cdot i_{\mathrm{T1}}(t = 0, P_{\mathrm{out}} = P_{\triangle,\mathrm{a},\max}) = n \cdot I_{t_0}$.

According to Fig. 8(a), for 2 kW $< P_{\mathrm{out}} <$ 2.5 kW, $D_2 = 0.5$ is approximately constant. In order to achieve low losses, D_1 and φ are calculated in order to satisfy

$$\begin{aligned}&P_{\mathrm{out}}(D_1, D_2 = 0.5, \varphi) = P_{\mathrm{out,d}} \text{ and}\\ &i_{\mathrm{T1}}(t = t_1, D_1, D_2 = 0.5, \varphi) = I_{\mathrm{S2,sw,opt}}/n\\ &\forall V_2 \leq V_{2,\mathrm{lim}} \wedge P_{\mathrm{opt,a,min}} < P_{\mathrm{out}} \leq P_{\mathrm{opt,a,hi}}.\end{aligned} \quad (28)$$

The control parameters D_1 and φ calculated with this equation system additionally guarantee ZVS on the HV side due to the high output power levels and due to $V_2 \leq V_{2,\mathrm{lim}}$. Moreover, D_1 increases with increasing output power; D_1 becomes equal to 0.5 at $P_{\mathrm{out}} = P_{\mathrm{opt,a,hi}}$ [Fig. 12(c)]:

$$\begin{aligned}&[i_{\mathrm{T1}}(t = t_1, \varphi) = I_{\mathrm{S2,sw,opt}}/n \wedge D_1 = 0.5 \wedge D_2 = 0.5]\\ &\Leftrightarrow P_{\mathrm{out}}(\varphi) = P_{\mathrm{opt,a,hi}}.\end{aligned} \quad (29)$$

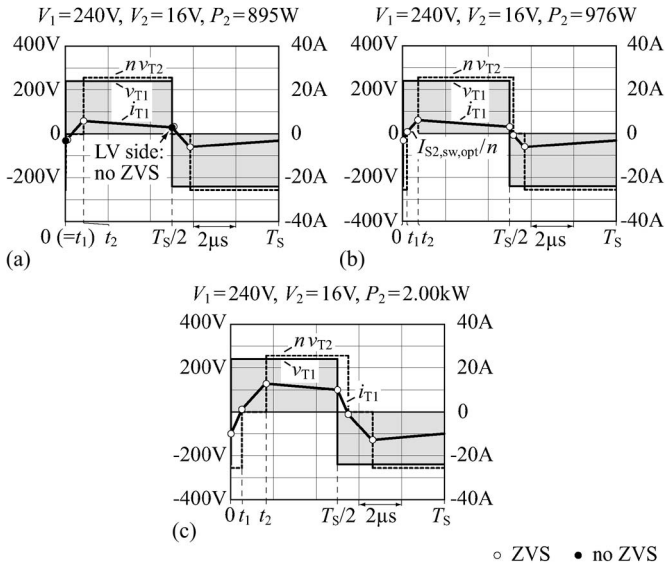

Fig. 13. Calculated waveforms $v_{\mathrm{T1}}(t)$, $v_{\mathrm{T2}}(t)$, and $i_{\mathrm{T1}}(t)$ for DAB operation at $V_1 = 240$ V and $V_2 = 16$ V, using the optimized modulation scheme: (a) $P_{\mathrm{out}} = 895$ W, (b) $P_{\mathrm{out}} = 976$ W, and (c) $P_{\mathrm{out}} = 2.00$ kW; $n = 16$, $L = 22.4\ \mu$H, and $L_{\mathrm{M}} = 1.9$ mH; Fig. 13(a) and (b) depict the limits of the respective operating modes: (a) $P_{\mathrm{out}} = P_{\triangle,\mathrm{b,max}}$; (b) $P_{\mathrm{out}} = P_{\mathrm{opt,b,min}}$.

A reduced duty cycle $D_2 < 0.5$ is employed on the LV side if the required output power level exceeds $P_{\mathrm{opt,a,hi}}$ in order to reduce the switching losses. This can be observed in Fig. 12(d): At $t = t_1$, the current during switching is close to $I_{\mathrm{S2,sw,opt}}$. The duty cycle $D_1 = 0.5$ remains constant in order to achieve low transformer rms currents and D_2 and φ are determined with respect to maximum total efficiency

$$\begin{aligned}&P_{\mathrm{out}}(D_1 = 0.5, D_2, \varphi) = P_{\mathrm{out,d}}\\ &\eta(D_1 = 0.5, D_2, \varphi) = \max\left[\eta(D_1 = 0.5, D_2, \varphi)\right]\\ &i_{\mathrm{T1}}(t = t_1, D_1 = 0.5, D_2, \varphi) > I_{\mathrm{S2,sw,opt}}/n\\ &\forall V_2 \le V_{2,\mathrm{lim}} \wedge P_{\mathrm{opt,a,hi}} < P_{\mathrm{out}} \le P_{\mathrm{max}}.\end{aligned} \tag{30}$$

Analytical investigations show that maximum output power P_{max} is achieved with phase shift modulation. The respective value is computed with a numerical maximum search

$$(D_1 = 0.5 \wedge D_2 = 0.5) \Leftrightarrow P_{\mathrm{max}} = \max\left[P_{\mathrm{out}}(\varphi)\right]. \tag{31}$$

2) $V_2 \ge V_{2,\mathrm{lim}}$: D_1 and D_2 are selected according to Fig. 8(b) at high power levels, Figs. 10(d) and 11(d).

- $D_1 = 0.5$ in order to achieve low conduction losses.
- $D_2 \le 0.5$ in order to achieve low switching losses.

The computation of D_1 and D_2 distinguishes between two different output power levels:

1) $P_{\triangle,\mathrm{b,max}} < P_{\mathrm{out}} \le P_{\mathrm{opt,b,min}}$: transition from mode b to high-power modulation,
2) $P_{\mathrm{opt,b,min}} < P_{\mathrm{out}} \le P_{\mathrm{max}}$: operation in mode c with $D_1 = 0.5$, $D_2 \le 0.5$.

The power level $P_{\triangle,\mathrm{b,max}}$ is given with (19), $P_{\mathrm{opt,b,min}}$ is defined with (32) in this section, and P_{max} is defined with (31).

At $P_{\mathrm{out}} = P_{\triangle,\mathrm{b,max}}$, the duty cycles $D_1 = 0.5$ and $D_2 < 0.5$ result; typical current and voltage waveforms are shown in Fig. 13(a). Furthermore, hard switching occurs on the LV side at $t = t_1 = 0$. With increasing output power, D_2 and φ increase, and the current $i_{\mathrm{T1}}(t_1)$ becomes equal to $I_{\mathrm{S2,sw,opt}}/n$ at $P_{\mathrm{out}} = P_{\mathrm{opt,b,min}}$ as shown in Fig. 13(b):

$$\begin{aligned}&[i_{\mathrm{T1}}(t = 0, D_2, \varphi) = -I_{\mathrm{S1,sw,min}} \wedge i_{\mathrm{T1}}(t = t_1, D_2, \varphi)\\ &\quad = I_{\mathrm{S2,sw,opt}}/n \wedge D_1 = 0.5]\\ &\Leftrightarrow P_{\mathrm{out}}(D_2, \varphi) = P_{\mathrm{opt,b,min}}.\end{aligned} \tag{32}$$

For $P_{\triangle,\mathrm{b,max}} < P_{\mathrm{out}} \le P_{\mathrm{opt,b,min}}$, a numerical search algorithm seeks suitable values for D_2 and φ to satisfy

$$\begin{aligned}&P_{\mathrm{out}}(D_1 = 0.5, D_2, \varphi) = P_{\mathrm{out,d}} \text{ and}\\ &i_{\mathrm{T1}}(t = t_1, D_1 = 0.5, D_2, \varphi) = I_{\mathrm{S2,sw,d}}/n\\ &\forall\, V_2 \ge V_{2,\mathrm{lim}} \wedge P_{\triangle,\mathrm{b,max}} < P_{\mathrm{out}} \le P_{\mathrm{opt,b,min}}.\end{aligned} \tag{33}$$

A linear transition is used to determine the LV side switch current $i_{\mathrm{T1}}(t_1) = I_{\mathrm{S2,sw,d}}/n$

$$\begin{aligned}I_{\mathrm{S2,sw,d}} = I_{\mathrm{S2,sw},\triangle,\mathrm{b,max}} + (I_{\mathrm{S2,sw,opt}} - I_{\mathrm{S2,sw},\triangle,\mathrm{b,max}})\\ \cdot \frac{P_{\mathrm{out,d}} - P_{\triangle,\mathrm{b,max}}}{P_{\mathrm{opt,b,min}} - P_{\triangle,\mathrm{b,max}}};\end{aligned} \tag{34}$$

$I_{\mathrm{S2,sw},\triangle,\mathrm{b,max}}$ is equal to $n \cdot i_{\mathrm{T1}}(0)$ at $P_{\mathrm{out}} = P_{\triangle,\mathrm{b,max}}$, e.g., $I_{\mathrm{S2,sw},\triangle,\mathrm{b,max}} \approx 16 \cdot (-3\ \mathrm{A}) \approx -50$ A in Fig. 13(a).

The maximum achievable output power P_{max} is again calculated with (31). $D_1 = 0.5$ remains for output power levels between $P_{\mathrm{opt,b,min}}$ and P_{max}, and D_2 and φ are adjusted in order to obtain maximum efficiency

$$\begin{aligned}&P_{\mathrm{out}}(D_1 = 0.5, D_2, \varphi) = P_{\mathrm{out,d}}\\ &\eta(D_1 = 0.5, D_2, \varphi) = \max\left[\eta(D_1 = 0.5, D_2, \varphi)\right]\\ &i_{\mathrm{T1}}(t = t_1, D_1 = 0.5, D_2, \varphi) > I_{\mathrm{S2,sw,opt}}/n\\ &\forall V_2 \ge V_{2,\mathrm{lim}} \wedge P_{\mathrm{opt,b,min}} < P_{\mathrm{out}} \le P_{\mathrm{max}}.\end{aligned} \tag{35}$$

Fig. 13(c) shows the corresponding current and voltage waveforms in mode c for $V_1 = 240$ V, $V_2 = 16$ V$(> V_{2,\mathrm{lim}} = 14.5$ V), and $P_{\mathrm{out}} = 2$ kW.

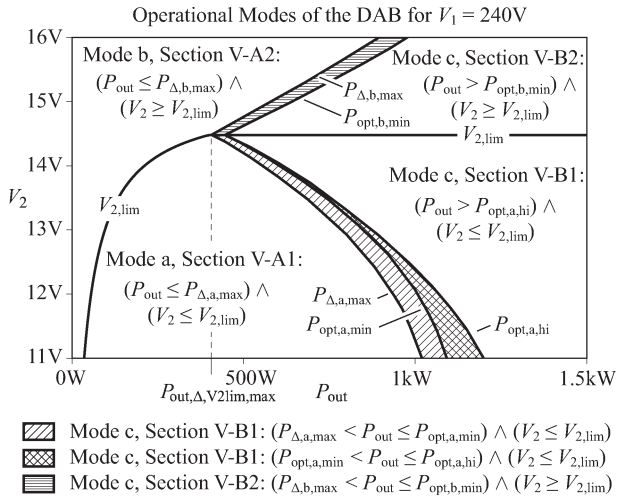

Fig. 14. DAB operating modes for $V_1 = 240$ V, different voltages V_2, different output power levels P_{out}, $n = 16$, and $L = 22.4\ \mu$H.

C. Suboptimal Modulation Scheme, Summary, and Results

Fig. 14 presents an overview of the operating modes detailed in this section for $V_1 = 240$ V, $11\ \mathrm{V} \le V_2 \le 16$ V, $0 \le P_{\mathrm{out}} \le 1.5$ kW, $n = 16$, and $L = 22.4\ \mu$H.

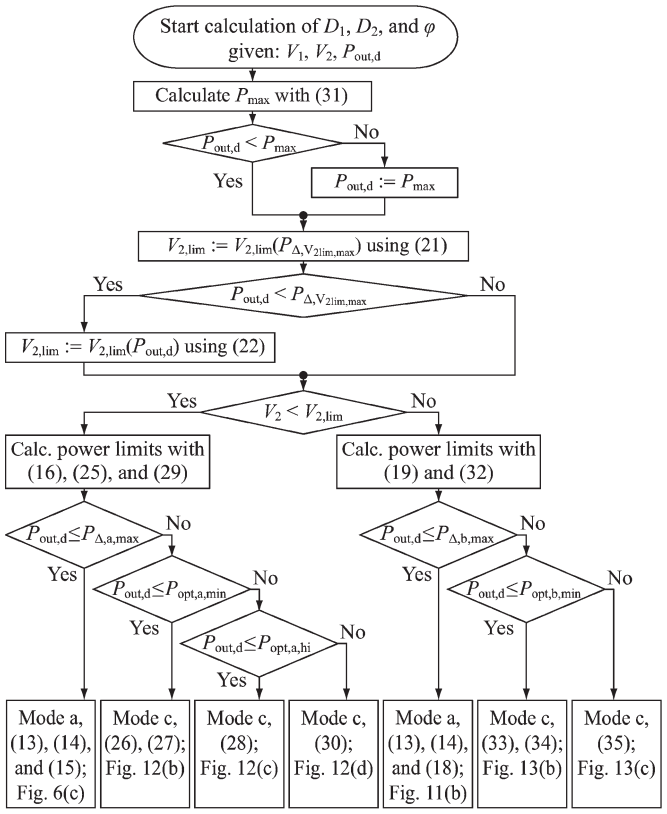

Fig. 15. Flowchart used to determine the correct equation system of the suboptimal modulation scheme and to compute D_1, D_2, and φ.

The flowchart depicted in Fig. 15 illustrates the algorithm which is needed to choose the correct equation system: First, the designated output power $P_{\mathrm{out,d}}$ is limited to the maximum output power $P_{\max}$, then $V_{2,\mathrm{lim}}$ is calculated according to Section V-A3 and the appropriate equation system is selected based on the present value of the port voltage V_2 and the value of $P_{\mathrm{out,d}}$. Finally, the control parameters D_1, D_2, and φ are computed by solving the respective equation system.

A little example is used to clarify the calculation of D_1, D_2, and φ; this example employs the given DAB converter with $n = 16$ and $L = 22.4\ \mu$H, $V_1 = 240$ V, $V_2 = 12$ V, and $P_{\mathrm{out,d}} = 200$ W. In a first step, the maximum power is calculated according to (31) since $P_{\mathrm{out,d}}$ needs to be limited to $P_{\max}$; $P_{\max} = 2.3$ kW results and thus, $P_{\mathrm{out,d}} = 200$ W remains. In a second step, $V_{2,\mathrm{lim}}$ is calculated; therefore, (21) is solved. The results are $V_{2,\mathrm{lim}}(P_{\triangle,\mathrm{V2\,lim,max}}) = 14.5$ V and $P_{\triangle,\mathrm{V2\,lim,max}} = 410$ W. The corresponding current and voltage waveforms are shown in Fig. 16(b). Since $P_{\mathrm{out,d}} < P_{\triangle,\mathrm{V2\,lim,max}}$ applies, $V_{2,\mathrm{lim}}(P_{\mathrm{out,d}} = 200\ \mathrm{W})$ needs to be determined using (22). The calculated solution is $V_{2,\mathrm{lim}}(200\ \mathrm{W}) = 14.0$ V; Fig. 16(a) illustrates the respective waveforms. Due to $V_2 = 12\ \mathrm{V} < V_{2,\mathrm{lim}} = 14.0$ V, either mode a or mode c applies (Fig. 14). (16) yields $P_{\triangle,\mathrm{a,max}} = 927$ W and thus, mode a is used. The control parameters are finally obtained from (13)–(15): $D_1 = 0.20$, $D_2 = 0.19$, and $\varphi = 0.18$.

The calculated efficiencies for power being transferred to the LV port are shown in Fig. 17 for $V_1 = 340$ V, $V_2 = 12$ V [Fig. 17(a)] and $V_1 = 240$ V, $V_2 = 16$ V [Fig. 17(b)]: with phase shift modulation, high efficiency is only achieved for

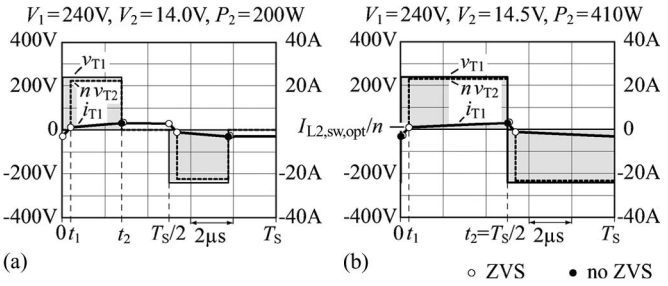

Fig. 16. Current and voltage waveforms for $V_1 = 240$ V and $V_2 = V_{2,\mathrm{lim}}$, i.e., at the transition between mode a and mode b: (a) $P_2 = 200$ W, (b) $P_2 = P_{\triangle,\mathrm{V2\,lim,max}} = 410$ W (cf. (21)); at $P_2 = P_{\triangle,\mathrm{V2\,lim,max}}$, the DAB is operated at the transition between the operating modes a, b, and c.

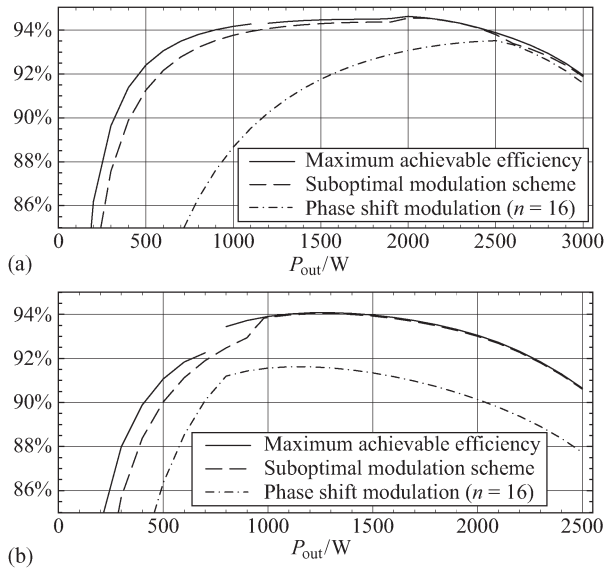

Fig. 17. Efficiency calculated for different modulation schemes: (a) $V_1 = 340$ V, $V_2 = 12$ V; (b) $V_1 = 240$ V, $V_2 = 16$ V. Highly efficient converter operation, close to maximum efficiency, is achieved with the suboptimal modulation scheme ($n = 16$, $L = 22.4\ \mu$H).

$V_1 = 340$ V, $V_2 = 12$ V, and $P_{\mathrm{out}} > 2.5$ kW. In contrast, with the suboptimal modulation scheme detailed in this section, the DAB converter operates close to the maximal achievable efficiency. Due to the use of the modified triangular current mode modulation depicted in Figs. 6(c) and 11(b) the efficiency is approximately 1%–2% below the maximum possible efficiency for $P_{\mathrm{out}} < 1000$ W and less than 0.5% below the maximum achievable efficiency for $P_{\mathrm{out}} > 1000$ W [Fig. 17(a)]; moreover, at $P_{\mathrm{out}} \approx P_{\mathrm{opt,a,hi}}$(29), reduced efficiency is observed ($P_{\mathrm{out}} \approx 2.6$ kW in Fig. 17(a)).

VI. Optimized DAB Converter Design

The design of the DAB is an iterative process: In a first step, appropriate values for n and L are assumed (e.g., according to [11]) and approximate values of the component stresses, i.e., maximum blocking voltages, maximum rms currents, and maximum magnetic field densities, are calculated with a simple DAB converter model. The results obtained enable a first selection of the DAB converter components, e.g., semiconductor switches, transformer core. Thereafter, the DAB loss model (Section III) is parameterized in order to permit an accurate prediction of the converter efficiency [13].

A. Design Procedure

The focus of this converter design is on the appropriate choice of the converter inductance L and the transformer turns ratio n in order to obtain maximum average converter efficiency $\overline{\eta}$. The design procedure therefore considers the DAB outlined in Section II, i.e., the semiconductor switches, the transformer core, and the dc capacitors are given. The average efficiency $\overline{\eta}$ is calculated over 36 different operating points

$$\overline{\eta} = \frac{1}{36}\sum_{i=1}^{3}\sum_{j=1}^{3}\sum_{k=1}^{4}\left(\eta|_{V_1=\vec{V}_{1,i},V_2=\vec{V}_{2,j},P_{\rm out}=\vec{P}_{{\rm out},k}}\right), \quad (36)$$

$$\vec{V}_1 = (240\ \text{V} \quad 340\ \text{V} \quad 450\ \text{V}), \quad (37)$$

$$\vec{V}_2 = (11\ \text{V} \quad 12\ \text{V} \quad 16\ \text{V}), \quad (38)$$

$$\vec{P}_{\rm out} = (-2\ \text{kW} \quad -1\ \text{kW} \quad 1\ \text{kW} \quad 2\ \text{kW}). \quad (39)$$

Thus, the proposed design method emphasizes on operation with nominal voltages V_1 and V_2, but also includes operation with minimum and/or maximum voltages V_1 and V_2, i.e., the edges of the specified voltage ranges. Bidirectional operation and part load operation are considered due to (39).[4]

Additionally, the magnetizing inductance $L_{\rm M}$ may be included in the design process: Increased magnetizing currents improve the ZVS properties of the DAB [11]; additionally, however, the rms values of the transformer currents $i_{\rm T1}$ and $i_{\rm T2}$ increase, which increases the copper losses and the conduction losses. Therefore, and due to the measured switching loss characteristics shown in Fig. 5, the investigated DAB converter shows highest average efficiency if the magnetizing currents are negligibly small. Moreover, the values of the dc capacitors $C_{\rm DC1}$ and $C_{\rm DC2}$ are not included in the design process, since the employed converter model considers constant dc voltages V_1 and V_2. Thus, $C_{\rm DC1}$ and $C_{\rm DC2}$ can be selected independent of n and L, provided that the ac voltage superimposed on V_1 and V_2 is negligible.

B. Model Parameterization

The loss model outlined in Section III is parameterized for $n = 24$ and is not readily applicable for $n \neq 24$; however, for $n \neq 24$, most parameters of the employed DAB loss model remain unchanged, i.e., conduction losses caused from MOSFETs and PCB, switching losses, power demand of the auxiliary power. The remaining components are the high-frequency transformer and the additional converter inductance $L_{\rm HV}$, placed on the HV side in series to the transformer and required to provide the total converter inductance L. Analytical calculations show that the transformer parameters, i.e., winding resistances $R_{\rm tr1}$ (HV side) and $R_{\rm tr2}$ (LV side), winding stray inductances $L_{\rm tr1}$ (HV side) and $L_{\rm tr2}$ (LV side), and the transformer magnetizing inductance $L_{\rm M}$, are approximately proportional to the square of the employed number of turns for a given transformer core. The inductor $L_{\rm HV}$ needs to be designed separately for each combination of n and L. An automated design script, based on explanations given in [32], is used to design the inductor, to calculate the respective copper and core losses, and to determine its equivalent loss resistance $R_{L_{\rm HV}}$.

[4]If a dedicated evaluation criteria is specified, then (36)–(39) need to be modified accordingly; consequently, different values for n and L may result.

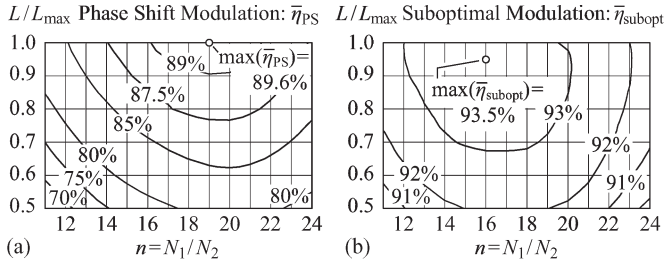

Fig. 18. (a) Calculated average efficiencies for phase shift modulation, different transformer turns ratios $n = N_1/N_2$, and different DAB inductances L ($L_{\max}$ denotes the maximum allowable inductance with respect to the given converter specifications, cf. (1); e.g., for $n = 19$, $L_{\max} = 26.7\ \mu$H is determined); (b) calculated average efficiencies for the suboptimal modulation scheme; $L_{\max} = 23.6\ \mu$H is calculated for $n = 16$. Table II summarizes the design results.

The resistance and inductance values employed for the electrical converter model shown in Fig. 1(b) and given with (40)–(44) are based on measurement results obtained from the final DAB prototype [13].

$$\begin{aligned} R_1 &= R_{\rm HV} + R_{\rm tr1} \\ &= \underbrace{166\ \text{m}\Omega}_{\text{HV MOSFETs}} + \underbrace{R_{L_{\rm HV}}}_{\text{resistance of the external inductor } L_{\rm HV}} \\ &\quad + \underbrace{\frac{N_1^2}{24^2}\cdot 93\ m\Omega}_{\text{transformer,HV side}} \end{aligned} \quad (40)$$

$$\begin{aligned} R_2 &= R_{\rm LV} + R_{\rm tr2} \\ &= \underbrace{1.18\ \text{m}\Omega}_{\text{LV MOSFETs,PCB}} + \underbrace{273\ \mu\Omega}_{\text{transformer,LV side}} \end{aligned} \quad (41)$$

$$\begin{aligned} L_1 &= L_{\rm HV} + L_{\rm tr1} \\ &= \underbrace{L_{\rm HV}}_{\text{external inductor}} + \underbrace{\frac{N_1^2}{24^2}\cdot 5\ \mu\text{H}}_{\text{stray ind.,HV side}} \end{aligned} \quad (42)$$

$$\begin{aligned} L_2 &= L_{\rm LV} + L_{\rm tr2} \\ &= \underbrace{5\ \text{nH}}_{\text{PCB,MOSFETs}} + \underbrace{8.7\ \text{nH}}_{\text{stray ind.,LV side}} \end{aligned} \quad (43)$$

$$\begin{aligned} L_{\rm M} &= \frac{N_1^2}{24^2} L_{\rm M}(N_1 = 24) \\ &= \frac{N_1^2}{24^2}\cdot 4.3\ \text{mH}. \end{aligned} \quad (44)$$

C. Design Results for n and L

The average efficiencies calculated for phase shift modulation and different values n and $L/L_{\max}$ are shown in Fig. 18(a): For $n = 19$ and $L = L_{\max}$, the maximum average efficiency $\max(\overline{\eta}_{\rm PS}) = 89.6\%$ is achieved. The value $L_{\max}$ denotes the upper limit for L with respect to the specified output power, cf. (1), and depends on the turns ratio n; for $n = 19$, $L_{\max} = 26.7\ \mu$H is calculated. The respective maximum transformer rms currents are $I_{\rm T1} = 15.6$ A (HV side) and $I_{\rm T2} = 294$ A (LV side). Hard-switching operation of the HV side full bridge occurs for certain operating points [11] and considerably reduces

TABLE II
DESIGN SUMMARY FOR THE TWO DIFFERENT MODULATION SCHEMES; I_{T1} AND I_{T2} DENOTE THE RMS VALUES OF THE RESPECTIVE TRANSFORMER CURRENTS (HV AND LV SIDES); $I_{C,DC1}$ AND $I_{C,DC2}$ ARE THE RESPECTIVE CAPACITOR RMS CURRENTS IN C_{DC1} AND C_{DC2} [ON THE ASSUMPTION OF CONSTANT CURRENTS I_1 AND I_2 IN FIG. 1(a)]; $\hat{B}_{tr}$ DENOTES THE PEAK FLUX DENSITY IN THE TRANSFORMER CORE

Property	*Phase Shift Mod.*	*Suboptimal Mod.*
L	26.7 µH	22.4 µH
n	19	16
$\max(I_{T1})$	15.6 A	15.1 A
$\max(I_{T2})$	294 A	240 A
$\max(I_{C,DC1})$	14.9 A	12.1 A
$\max(I_{C,DC2})$	245 A	138 A
$\max(\hat{B}_{tr})$	142 mT	129 mT

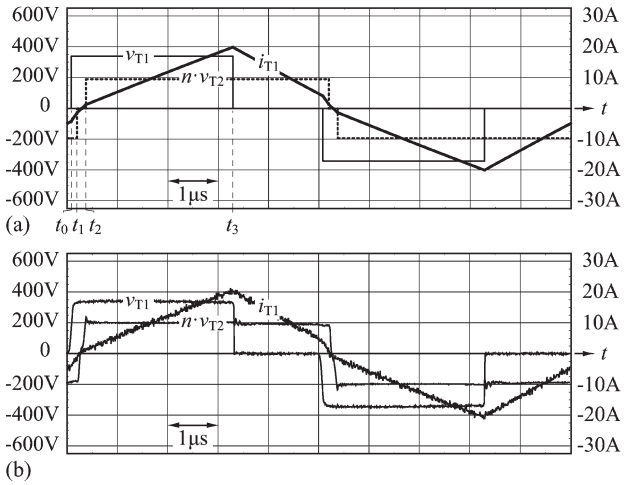

Fig. 19. (a) Calculated and (b) measured voltage and current waveforms obtained with the optimized modulation scheme for $V_1 = 340$ V, $V_2 = 12$ V, $P_2 = 2$ kW, $n = 16$, and $L = 22.4$ μH; with the DAB model depicted in Fig. 1(b) and the loss model presented in Section III and [13], good matching between calculated and measured waveforms is achieved.

the converter efficiency (cf. Fig. 5(a); this typically occurs at low-load conditions, e.g., at $V_1 = 240$ V, $V_2 = 16$ V, and $P_{out} = 200$ W). The capacitor rms currents reach values of up to 245 A on the LV side (Table II).

The average efficiency achieved increases considerably by using the suboptimal modulation scheme [Fig. 18(b)]: for $n = 16$ and $L = 22.4$ μH, $\overline{\eta}_{subopt}$ is 93.5%. Compared to phase shift modulation, reduced maximal transformer rms currents (HV side: 15.1 A, LV side: 240 A) and reduced capacitor rms currents are achieved (138 A; cf. Table II). Moreover, the HV side full bridge operates with ZVS within the full specified voltage and power ranges.

VII. RESULTS

The procedure outlined in Appendix A is used to calculate the transformer current waveforms i_{T1} and i_{T2}, which need to be known in detail in order to predict the conduction losses, the copper losses, and the switching losses [13]. Measured and calculated voltage and current waveforms for nominal operation are shown in Fig. 19. There, the calculated and measured waveforms of i_{T1} and v_{T1} match closely; solely the depicted

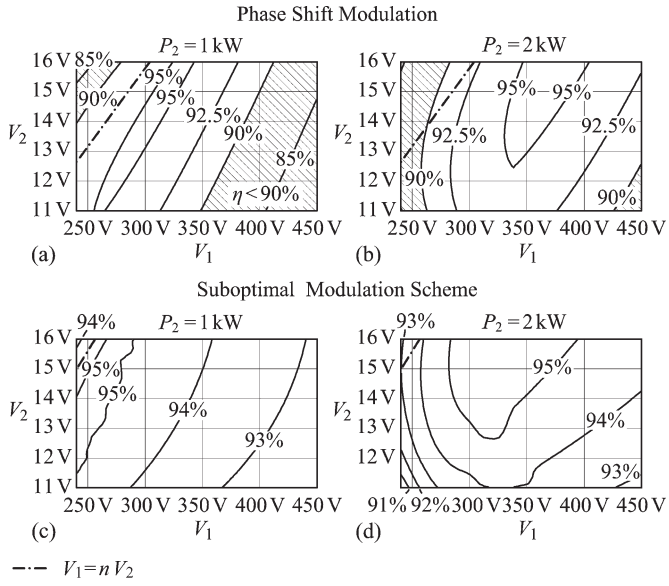

Fig. 20. Efficiencies calculated for power being transferred to the LV port: (a) and (b) phase shift modulation with $P_2 = 1$ kW and $P_2 = 2$ kW ($n = 19$, $L = 26.7$ μH); (c) and (d) suboptimal modulation with $P_2 = 1$ kW and $P_2 = 2$ kW ($n = 16$, $L = 22.4$ μH); for the suboptimal modulation scheme, Fig. 20(c) and (d), unsteady contour lines result due to the employed efficiency calculation method which considers interpolation errors (by reason of the linear interpolation algorithm used in the DSP, cf. Section V, [31]) in order to get as close as possible to the actual efficiency obtained with the DAB hardware prototype. Hatched areas denote $\eta < 90\%$.

waveforms of v_{T2} are slightly different. This difference is due to the interaction of the dead time interval (LV side: $T_d = 240$ ns), employed to prevent a shoot through in the half-bridges, and the switching process at $t = t_1$ close to the zero crossing of $i_{T1}(\approx i_{T2}/n)$ (cf. Fig. 2 in [30]). Even though, the control parameters used for the DAB hardware compensate for the respective time delays, minor errors still occur. A more advanced calculation procedure—e.g., an electrical circuit simulator—may be used in order to further improve the quality of the predicted waveforms.

Fig. 20 (calculated efficiency maps) allows for a comparison between the efficiencies obtained for phase shift modulation and the suboptimal modulation scheme. The achieved efficiency improvement is particularly obvious for $P_2 = 1$ kW (power is transferred to the LV port, cf. (2)): With phase shift modulation, $\eta > 90\%$ is only achieved within a limited band; the calculated minimum efficiency is 80.5% at $V_1 = 450$ V and $V_2 = 11$ V in Fig. 20(a). The minimum efficiency for $P_2 = 1$ kW is 92.2% at $V_1 = 450$ V and $V_2 = 11$ V with the suboptimal modulation scheme [Fig. 20(c)]. For $P_2 = 2$ kW, the converter efficiency achieved increases considerably: With phase shift modulation, the minimum efficiency is 84.6% [Fig. 20(b): $V_1 = 240$ V, $V_2 = 16$ V] and with the suboptimal modulation scheme $\eta > 90.2\%$ is achieved [Fig. 20(d); minimum at $V_1 = 240$ V and $V_2 = 11$ V].

The converter efficiency is measured for the suboptimal modulation scheme and different operating points in order to verify the calculated results. Fig. 21 illustrates the result (the □ symbols indicate measured values and solid lines denote calculated results). The results depicted show good matching between calculated and measured results for $P_2 > 500$ W. At

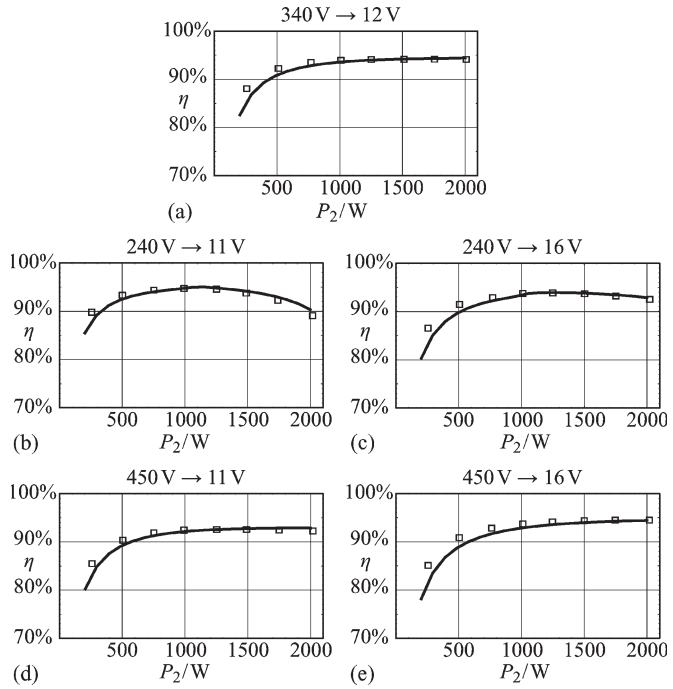

Fig. 21. Predicted efficiencies (solid lines) and measured efficiencies (□) obtained with the optimized modulation scheme and power being transferred from the HV port to the LV port: (a) $V_1 = 340$ V, $V_2 = 12$ V, (b) $V_1 = 240$ V, $V_2 = 11$ V, (c) $V_1 = 240$ V, $V_2 = 16$ V, (d) $V_1 = 450$ V, $V_2 = 11$ V, (e) $V_1 = 450$ V, $V_2 = 16$ V; employed DAB converter: $n = 16$ and $L = 22.4$ μH. The efficiencies are calculated with the DAB loss model presented in Section III and [13]; the efficiency measurement is carried out at an ambient temperature of $T_A = 25$ °C.

very low power levels, i.e., $P_2 \approx 250$ W, uncertainties in the predicted loss components accumulate and cause a maximum difference between calculated and predicted efficiencies of 4%; still, the loss model (Section III) correctly predicts the trends of the efficiencies at low power levels.

The shown results are obtained for a DAB converter with a constant switching frequency of 100 kHz. Detailed analytical investigations show that the presented suboptimal modulation scheme also enables highly efficient converter operation for a switching frequency different to 100 kHz; solely the values $I_{\mathrm{S1,sw,min}}$ and $I_{\mathrm{S2,sw,opt}}$ need to be adjusted. $I_{\mathrm{S1,sw,min}}$ and $I_{\mathrm{S2,sw,opt}}$ decrease with decreasing switching frequency and approach zero if the switching frequency approaches zero, since this selection reduces the rms currents in the transformer and in the switches. A noticable effect, however, requires a very much reduced switching frequency (e.g., $f_S = 20$ kHz) being used for the given hardware setup due to the present switching losses shown in Fig. 5.

The suboptimal modulation scheme facilitates reduced transformer rms currents according to the results listed in Table II. As a consequence, the given DAB converter could be operated at a maximum output power higher than 2 kW without considerably changing the hardware: the suboptimal modulation scheme reaches the maximum transformer current of phase shift modulation, $I_{\mathrm{T2}} = 294$ A, at $|P_{\mathrm{out}}| = 2.5$ kW with $n = 16$ and $L = 17.7$ μH. The respective average efficiency, calculated for $\vec{P}_{\mathrm{out}} = (-2.5\ \mathrm{kW}\ -1.25\ \mathrm{kW}\ 1.25\ \mathrm{kW}\ 2.5\ \mathrm{kW})$, is still high: $\overline{\eta}_{\mathrm{subopt}} = 93.1\%$.

VIII. Conclusion

The paper presented here describes a general method to determine efficiency-optimal control parameters for a bidirectional DAB dc/dc converter. The resulting control parameters, calculated for a specific automotive DAB converter with a low-voltage/high-current port are used to synthesize an efficiency-optimized suboptimal modulation scheme. The paper goes on to propose an efficiency-optimized design procedure in order to determine the optimal transformer turns ratio n and the optimal DAB converter inductance L for a given converter setup.

Converter operation close to the maximum possible efficiency is achieved with the proposed modulation scheme. Thus, at the rated output power of 2 kW, a minimum efficiency of 90.2% is obtained for all port voltages within the voltage ranges specified in Section I (as opposed to 84.6% obtained with phase shift modulation). At lower output levels, the achieved efficiency improvement is even more distinct: With 1 kW output power, the achieved minimum converter efficiency increases from 80.5% (phase shift modulation) to 92.2%.

Considerably increased converter efficiency is thus achieved for a given DAB converter, using an optimized modulation scheme: The optimization of the modulation scheme is the first step toward a complete DAB converter optimization. Optimal hardware parameters n and L are calculated in a second step. The presented findings could be used in future research to design an optimal DAB converter using a design procedure similar to the procedure given in [28], e.g., with respect to maximum efficiency or power density.

Appendix

A. DAB Currents and Voltages for Arbitrary D_1, D_2, and φ

In order to allow for the analysis presented in Sections IV and V, the currents $i_{\mathrm{T1}}(t)$, $i_{\mathrm{T2}}(t)$ and the voltage applied to the transformer core, v_{M}, [Fig. 1(b)] need to be determined for arbitrary D_1, D_2, and φ. A time domain analytical approach is detailed in [23] where different modulation modes are considered separately. In this paper, all results are obtained with a numerical evaluation procedure (on the assumption of constant port voltages V_1 and V_2; the considered time interval is one-half cycle, e.g., $t_0 < t < t_0 + T_S/2$ in Fig. 6(c)).

1) Start and end times of the time intervals with constant voltages $v_{\mathrm{T1}}(t)$ and $v_{\mathrm{T2}}(t)$ for a given set of D_1, D_2, and φ, e.g., time intervals I, II, III, and IV in Fig. 6(c), are stored in a time data list (together with the respective values of v_{T1} and v_{T2}).
2) Steady-state values of all transformer currents are calculated, e.g., at $t = t_0$ in Fig. 6(c), using the time and voltage data stored in the time data list.
3) Waveforms $i_{\mathrm{T1}}(t)$, $i_{\mathrm{T2}}(t)$, and $v_{\mathrm{M}}(t)$ are calculated with the stored time data and the steady-state currents.

The resulting functions $i_{\mathrm{T1}}(t)$ and $i_{\mathrm{T2}}(t)$ and the known voltages $v_{\mathrm{T1}}(t)$ and $v_{\mathrm{T2}}(t)$ enable the calculation of the port power levels P_1 and P_2 and the calculation of all required rms currents (transformer windings, switches, capacitors). The

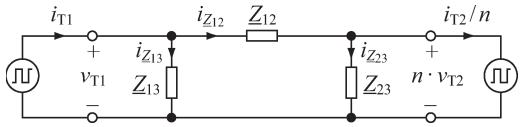

Fig. 22. The delta representation of the circuit shown in Fig. 1(b).

corresponding integrals are again split up into k time intervals with constant voltages v_{T1} and v_{T2}, e.g., for P_1

$$P_1 = \frac{2}{T_S}\int_0^{T_S/2} v_{T1}(t) i_{T1}(t) dt = \sum_{j=0}^{k-1}\left[v_{T1}(t_{j^+}) \frac{2}{T_S} \int_{t_j}^{t_{j+1}} i_{T1}(\tau) d\tau \right] \quad (45)$$

(t_j denotes the beginning of the jth time interval and $v_{T1}(t_{j^+})$ is the voltage v_{T1} during the jth time interval). Thus, (45) requires the average currents during the k different time intervals to be determined.

The calculation of the currents i_{T1} and i_{T2} can further be simplified by using the Wye-delta transformation (Fig. 22), since the voltages applied to $\underline{Z}_{13}$, $\underline{Z}_{23}$, and $\underline{Z}_{12}$ are known in advance. On the assumptions $R_1 \ll sL_1$, $R_2 \ll sL_2$, and $R_M \gg sL_M$, simple expressions result for $\underline{Z}_{12}$, $\underline{Z}_{13}$, and $\underline{Z}_{23}$

$$\underline{Z}_{12} \approx R_1 + n^2 R_2 + s(L_1 + n^2 L_2 + n^2 L_1 L_2 / L_M) \quad (46)$$

$$\underline{Z}_{13} \approx (R_1 + sL_1)\left(1 + \frac{L_M}{n^2 L_2}\right) + sL_M \quad (47)$$

$$\underline{Z}_{23} \approx n^2 (R_2 + sL_2)\left(1 + \frac{L_M}{L_1}\right) + sL_M \quad (48)$$

each being equal to a series connection of an inductor and a resistor. The currents i_{T1} and i_{T2} are calculated with

$$i_{T1} = i_{\underline{Z}_{12}} + i_{\underline{Z}_{13}} \text{ and } i_{T2} = n\left(i_{\underline{Z}_{12}} - i_{\underline{Z}_{23}}\right). \quad (49)$$

During time intervals with constant voltages v_{T1} and v_{T2}, the currents $i_{\underline{Z}_{12}}(t)$, $i_{\underline{Z}_{13}}(t)$, $i_{\underline{Z}_{23}}(t)$ can easily be derived. Closed-form expressions can be derived for all required rms currents and for the port power levels for time intervals with constant voltages; however, a mathematical software tool (e.g., Mathematica, Maple) is used to solve the integrals since rather large expressions result.

An electrical circuit simulator can be used instead of the discussed procedure; the simulator is more flexible but slower.

B. Selection of $I_{S1,sw,min}$

On the HV side, low switching losses are achieved with $I_{S1,sw} > 2$ A [Fig. 5(a)]. Thus, during the dead time interval (200 ns on the HV side), a constant current $i_{T1}(t) \geq 2$ A is needed in order to charge and discharge the drain to source capacitances of the respective HV MOSFETs and to achieve ZVS (on the assumption of a falling edge of $v_{T1}(t)$, cf. Table I). However, during normal converter operation, $i_{T1}(t)$ changes during the dead time interval. In order to achieve ZVS, a minimum charge must be provided by $i_{T1}(t)$ during the dead time interval and this may demand for $I_{S1,sw,min} > 2$ A; a detailed discussion is given in [13] in Section IV-C. The required currents $I_{S1,sw,min}$ have been measured with the final full-bridge setup (MOSFETs: SPW47N60CFD). An approximate expression for $I_{S1,sw,min}(V_1)$ from these measurement results has been estimated for $L = 22.4\ \mu$H

$$I_{S1,sw,min}(V_1) \approx 0.65\text{ A} + V_1 \cdot 8.5 \cdot 10^{-3}\text{ A/V} \quad (50)$$

e.g., at $V_1 = 340$ V, $I_{S1,sw,min} = 3.5$ A results.

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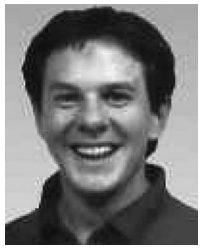

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