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***Abstract*—The strings of photovoltaic panels have a significantly reduced power output when mismatch between the panels occurs, as, e.g., caused by partial shading. With mismatch, either the panel-integrated diodes are bypassing the shaded panels if the string is operated at the current level of the unshaded panels, or some power of the unshaded panels is lost if the string current is reduced to the level of the shaded panels. With the implementation of dc–dc converters on panel level, the maximum available power can be extracted from each panel regardless of any mismatch. In this paper, different concepts of PV panel-integrated dc–dc converters are presented and their suitability for panel integration is evaluated. The buck–boost converter is identified as the most promising concept and an efficiency/power density (η-ρ) Pareto optimization of this topology is shown. Based on the optimization results, two 275 W converter prototypes with either Silicon MOSFETs with a switching frequency of 100 kHz or gallium nitride FETs with a switching frequency of 400 kHz are designed for an input voltage range of 15 to 45 V and an output voltage range of 10 to 100 V. The theoretical considerations are verified by efficiency measurements which are compared to the characteristics of a commercial panel-integrated converter.**

***Index Terms*—GaN transistors, pareto optimization, photovoltaic (PV) panel-integrated dc–dc converter, prototype comparison.**

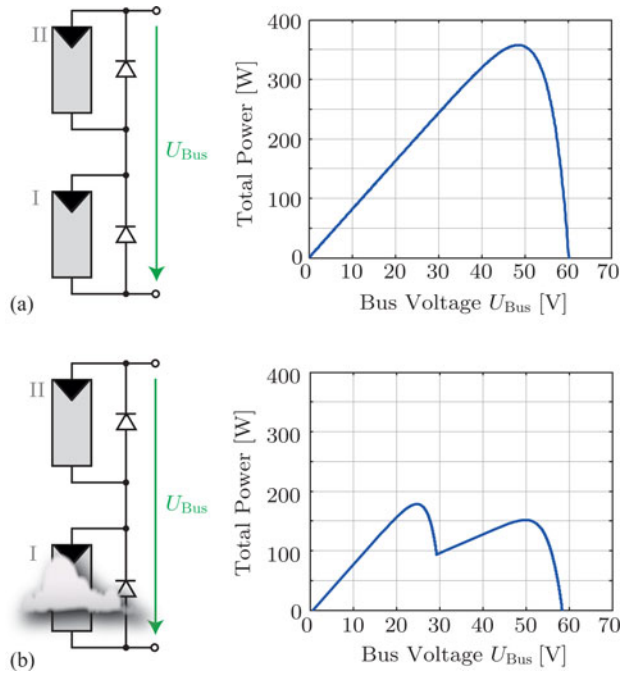

Fig. 1. Impact of shading on a simplified string formed by only two PV panels: (a) output power of the PV string with only unshaded panels receiving equal irradiance and (b) with the shaded panel (plotted versus the total bus voltage U_{Bus}).

I. Introduction

RENEWABLE energy sources, including hydro power, wind power etc., are gaining an increasing share of the global electricity generation and reached a share of 19.3% in 2009 [1]. Among those, especially the photovoltaic (PV) technology has been in the focus of many governments and, due to substantial subsidies, experienced a steep rise in the numbers of installations in those countries. In some countries, e.g., in Germany, the electricity generated by PV systems already amounts to 30% of the electricity generation during some days with a record high of almost 50% in 2012 [2]. With the ongoing trend of declining PV panel prices from \$4.90/$\mathrm{W_{pk}}$ in 1998 to \$1.28/$\mathrm{W_{pk}}$ in 2011 [3], the rate of growth of new PV system installations is expected to remain on a high level and to compensate for diminishing subsidies in the future.

In the state-of-the-art PV system installations for residential as well as commercial or utility-scale application, PV panels are connected in series so that the panel output voltages, usually in the range of 15 to 45 V, add up to a voltage of at least around 400 V which is required (in Europe) to feed power into the public grid by means of a central dc–ac inverter. Due to this series connection, the output current of all panels is equal to the string current. The current generation of a PV panel, however, is dependent on the irradiance level. In case all the PV panels in a string receive the same level of irradiance, the whole string of panels has only one maximum power point (MPP), and all panels contribute to the total power of the string [see Fig. 1(a)]. In contrast, if the PV panels in a string are subject to different levels of irradiance, e.g., due to local shading of some panels, the output currents are unequal and the string shows multiple MPPs as visualized in Fig. 1(b). In that case, those panels generating less current than the string current will get reverse biased and their internal bypass diodes will conduct the string current and consequently those will be shorted out, i.e., their power cannot be harvested. Alternatively, the string current,

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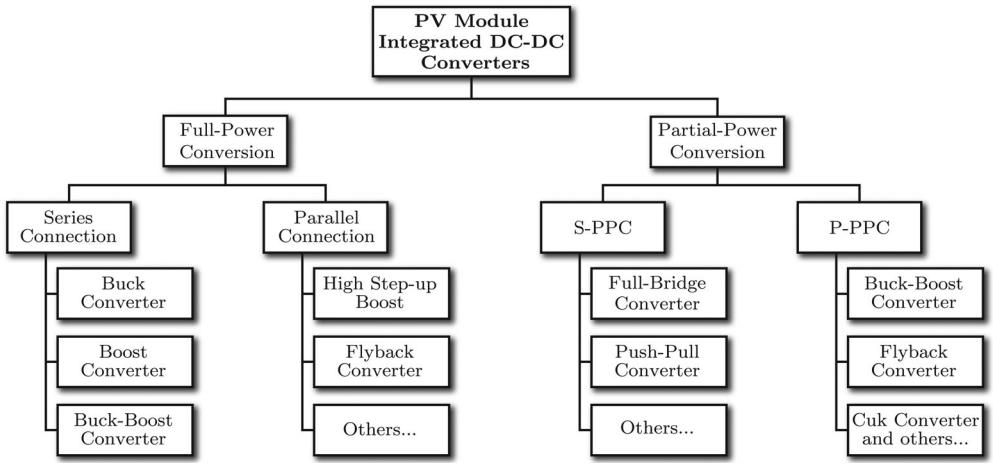

Fig. 2. Classification of PV module integrated dc–dc converter concepts into full-power and partial-power processing converters, each with subcategories of series and parallel connection.

which is controlled by the central inverter, can be lowered so that the shaded panels are not bypassed. But then the unshaded panels will not be operating at their MPP. In both scenarios, not the whole theoretically available power $P_{\mathrm{tot,th}}$ of a PV string with N PV panels which is the sum of MPPs of all PV panels

$$P_{\mathrm{tot,th}} = \sum_{i=1}^{N} P_{\mathrm{MPP},i} \tag{1}$$

can be harvested. This problem of unequal current generation of series-connected PV panels within a string—often referred to as mismatch—is not only caused by shading but also by other factors such as different orientation of PV panels, dirt or dust on panels, different panel manufacturers, unequal aging, etc. Especially, building integrated PV modules are prone to orientation mismatch and partial shading.

By equipping each PV panel with a dc–dc converter, the panels can be operated independently from each other in their MPP and the aforementioned problems can be mitigated. Those module integrated converters (MICs) allow to harvest the theoretically available string power $P_{\mathrm{tot,th}}$. However, some reduction of the power generation due to the finite efficiency of the dc–dc converters has to be accepted. In this paper, the concepts of suitable dc–dc converters for PV panel integration are presented and classified. The most promising concept for series-connected PV panels is selected for a multiobjective, i.e., efficiency/power density (η-ρ) Pareto-optimization. The experimental results of two prototypes are presented in order to show the potential of gallium nitride (GaN) FETs in comparison to the state-of-the-art Silicon (Si) MOSFETs.

II. Evaluation of Converter Topologies

Possible dc–dc converter topologies for PV panel integration can be classified into the two groups of full-power and partial-power converters as shown in Fig. 2. In a full-power converter, the whole amount of panel power is processed by the converter, whereas in a partial-power converter only a fraction of the panel power has to be converted. The full-power converter concepts can be further divided into series and parallel connected concepts [4]. In a similar way, the partial-power converter category contains the subcategories of series-connected partial-power converter (S-PPC), which are adding or subtracting a voltage in series to the panel output voltage, and parallel-connected partial-power converters (P-PPC) which are equalizing the PV panel voltages. The P-PPC concept is also known as "energy shuffler" or "current diverter" concept [5].

Due to the fact that nowadays in PV installations the PV panels are connected in series, only topologies that still allow for a series connection of PV panels will be regarded in this paper. These topologies are shown in Fig. 3 in its basic form.

A. Full Power Converters

For full-power conversion [see Fig. 3(a)] either buck, boost, or buck–boost converters can be used [6]. Other, more complex topologies like, e.g., the Ćuk or SEPIC converter are not considered here due to their higher system complexity. When the PV panels are equipped with buck converters, the output voltage of shaded panels can be stepped down in order to increase their output current until it matches the current of the unshaded panels [cf., Fig. 4(a)]. Vice versa, if boost converters are employed, the output voltage of unshaded PV panels can be increased in order to lower the output current until it matches the MPP current of the shaded panels [cf., Fig. 4(b)]. The greatest flexibility is given with buck–boost converters [cf., Fig. 4(c)] where any string current value can be matched by the output currents of the converters.

These three different concepts also have different implications on the number of PV panels per string which are required in order to reach a given bus voltage U_{Bus} of, e.g., 400 V despite different levels of irradiance. In a string where all panels are equipped with buck converters, the string voltage may drop below $400\,V$ if panels are shaded, since the adaption to match the current of the unshaded panels is achieved by lowering the voltage of shaded panels. Thus, a minimum number of panels per string is required to guarantee the generation of the bus voltage up to a certain degree of shading. The upper limit of the number

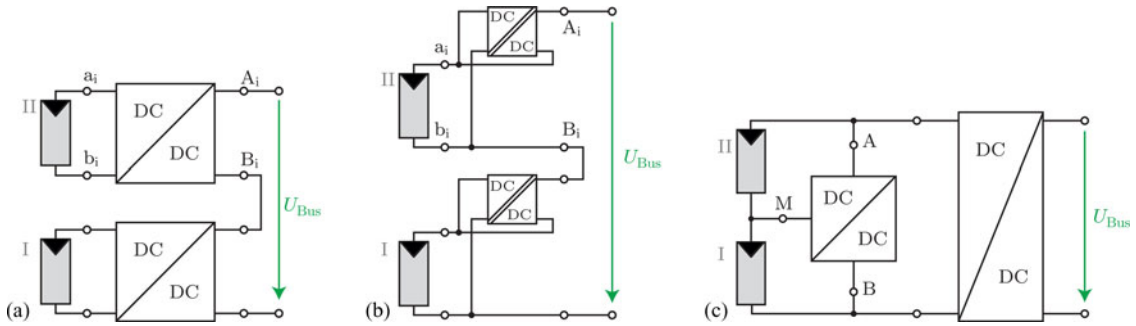

Fig. 3. Possible dc–dc converter topologies ensuring MPP operation of PV panels in series connection: (a) full-power converters, (b) series-connected partial-power converters (S-PPC), and (c) parallel-connected partial-power converter (P-PPC).

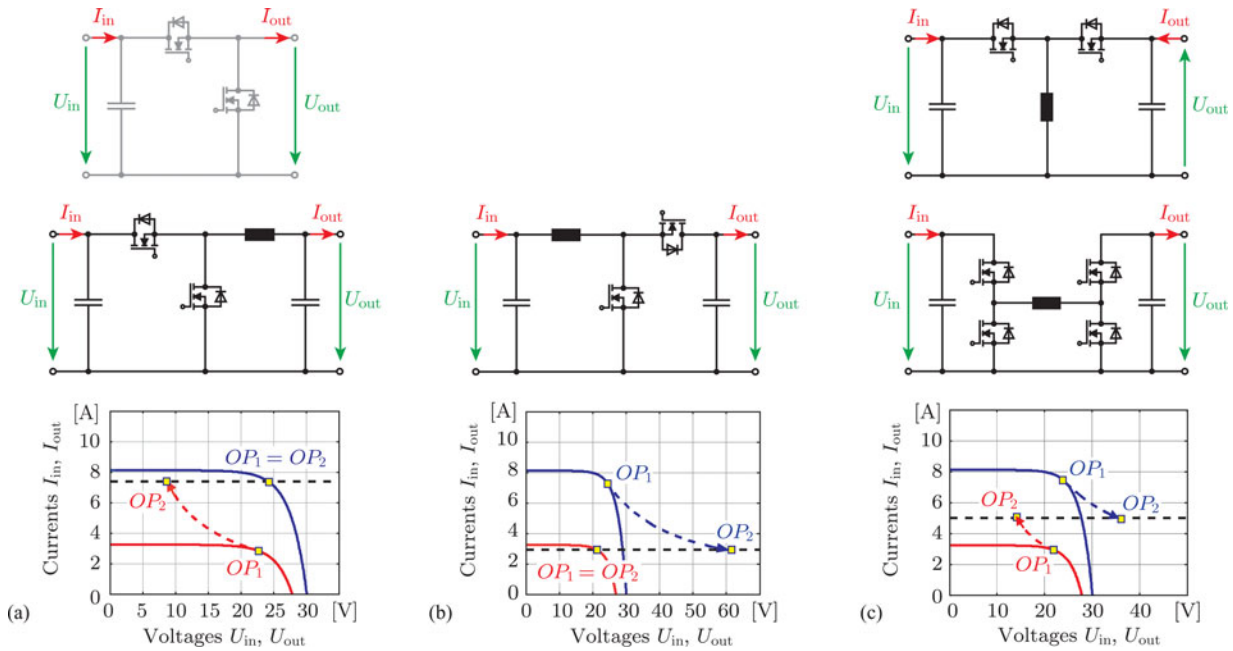

Fig. 4. Working principles of full-power converters for series connection of shaded (red) and unshaded (blue) panels: (a) buck converter, (b) boost converter, and (c) buck–boost converter. OP_1: converter input ($U_{\rm in}$, $I_{\rm in}$) related to MPP of a PV panel. OP_2: operating point characterizing the converter output ($U_{\rm out}$, $I_{\rm out}$). The first converter of (a) (cf., step inverter in [7]), here shown in gray, can either connect the converter output to the PV panel output or bypass the PV panel. The string voltage of a PV string equipped with this converter type exhibits voltage steps, and thus a LC filter (not shown) needs to be connected to the string.

of PV panels with a buck converter in a string depends on the maximum output current rating of the converters.

With boost converters the string voltage is prone to exceed the level of $400\,V$ during shading, since unshaded panels increase their output voltage to reach the lower current level of shaded panels. Thus, a maximum number of PV panels per string can be defined for a certain degree of shading. Furthermore, the lower limit of PV panels with boost converters in each string depends on the maximum output voltage rating of the converters.

Buck–boost converters allow to keep the bus voltage constant since any level of string current can be set. Thus, the upper limit of PV panels per string for the buck–boost converter concept depends on the maximum output current rating, and the lower limit depends on the maximum output voltage rating of the buck–boost converters. In Table I, the equations for the maximum and minimum numbers of PV panels per string are given for the three different full-power converter topologies under the assumption that all panels should be able to feed power into the string under a given shading condition which can be expressed as $\Delta = \frac{P_{\rm PV,unsh}}{P_{\rm PV,sh}}$.

TABLE I

MAXIMUM, RESP. MINIMUM NUMBER OF PV PANELS PER STRING FOR DIFFERENT MIC TOPOLOGIES WHERE $I_{\rm Out,Max}$ DENOTES THE MAXIMUM OUTPUT CURRENT OF THE CONVERTER, $U_{\rm MPP}$ THE PV PANEL VOLTAGE IN A TYPICAL MPP, Δ THE FRACTION $\frac{P_{\rm PV,unsh}}{P_{\rm PV,sh}}$ AND $P_{\rm PV,max}$ THE MAXIMUM OUTPUT POWER OF THE PV PANEL

Type	Max. no. of PV panels	Min. no. of PV panels
Buck	$\frac{U_{\rm Bus}}{P_{\rm PV,max}} I_{\rm out,max}$	$\left(\frac{U_{\rm Bus}}{U_{\rm MPP}}\right)\Delta + 1$
Boost	$\frac{U_{\rm Bus}+(\Delta-1)U_{\rm MPP}}{\Delta \cdot U_{\rm MPP}}$	$\left(\frac{U_{\rm Bus}}{U_{\rm out,max}} - 1\right)\Delta + 1$
Buck-boost	$\frac{U_{\rm Bus}}{P_{\rm PV,max}} I_{\rm out,max}$	$\left(\frac{U_{\rm Bus}}{U_{\rm out,max}} - 1\right)\Delta + 1$

An example of those limitations is depicted in Fig. 5. In case only boost converters are used, the number of panels per PV string has to be in the range of 6–11; if all PV panels are

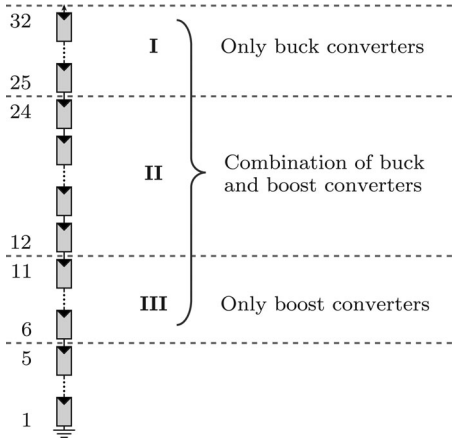

Fig. 5. Example of maximum and minimum number of PV panels per string when either only buck converters (**I**) or only boost converters (**III**) are used. The buck–boost converters combine those two regions and extend it to the previously unreachable area **II**. (Numbers used for this example: $U_{\mathrm{Bus}} = 400$ V, $U_{\mathrm{MPP}} = 25$ V, $P_{\mathrm{PV,max}} = 250$ W, $\Delta = 1.5$, $I_{\mathrm{out,max}} = 20$ A, $U_{\mathrm{out,max}} = 100$ V.)

equipped with buck converters only, the number of panels has to be between 25 and 32. So, if either only buck or boost converters are chosen, there is no possibility to have between 12 and 24 PV panels in the string. However, with buck–boost converters, any number of PV panels between 6 and 32 can be connected in series. Thus, based on the limitations which buck as well as boost converter topologies imply on the number of panels in a PV string, the buck–boost concept is chosen for further consideration. Since MICs in general target residential applications which are more susceptible to shading than industrial applications, the flexibility provided by buck–boost converters is not only advantageous for the design of a PV system regarding shading, but also allows to fully utilize the available space on a rooftop by setting up multiple PV strings with different lengths.

The global irradiance consists of at least one quarter to one third of indirect irradiance, i.e., diffuse irradiance and reflected irradiance. Therefore, the maximum shading condition $\Delta_{\max}$, up to which all PV panels should be able to operate in their MPP, is around $\Delta_{\max} = 3 \ldots 4$. Further, in order to set up a PV system with the greatest flexibility in the number of panels per string, the maximum number of PV panels $N_{\max}$ should be equal to $(2 \cdot N_{\min})$. This allows, for example, to split up a string with more panels than $N_{\max}$ into two strings with at least $N_{\min}$ panels. Based on that, the required maximum output current can be calculated with the formulas for the minimum and maximum converters in a PV string with buck–boost converter (cf., Table I) as

$$I_{\mathrm{out,max}} = \frac{2 \cdot P_{\mathrm{Pv,max}}(U_{\mathrm{out,max}} + U_{\mathrm{Bus}} \cdot \Delta_{\max} - U_{\mathrm{out,max}} \cdot \Delta_{\max})}{U_{\mathrm{Bus}} \cdot U_{\mathrm{out,max}}}. \tag{2}$$

B. Partial Power Converters

Common to all PPCs is the possibility to compensate the mismatch between the PV panels by processing only a fraction

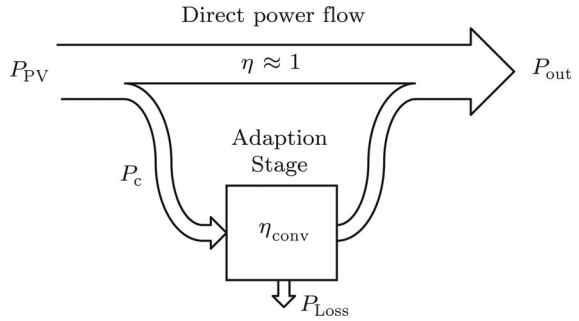

Fig. 6. Splitting of the power flow into two parallel power flow paths given for PPCs. The direct path transfers power from the PV panel to the output without any conversion stage. Only a fraction P_{c} of the panel output power P_{PV} is processed by a voltage (or current) adaption stage with efficiency η_{conv}.

of the full panel power. Hence, the total efficiency η_{tot} of the mismatch compensation depends only to certain extent on the converter efficiency η_{conv} itself [8], [9]. The PPCs are characterized by a splitting of the power conditioning into two power flow paths (cf., Fig. 6) [10], [11]. If one of the paths is highly efficient, e.g., direct power flow from the source to the load with $\eta \approx 1$, then the effective conversion efficiency is increased. The ratio of the power P_{c} which is processed by the PPC to the total power P_{PV} taken from the PV panel, determines the influence of the converter efficiency on the total efficiency

$$\eta_{\mathrm{tot}} = 1 - \frac{P_{\mathrm{c}}}{P_{\mathrm{PV}}}(1 - \eta_{\mathrm{conv}}). \tag{3}$$

This means, if less power is processed by the PPC, a higher system efficiency is achieved. Thus, in the ideal case with no mismatch, the PPC does not have to process any power and the total efficiency approaches 100% (neglecting load independent converter losses, e.g., due to control electronics). Furthermore, the PPC can be optimized for a high part-load efficiency, since it will only process large fractions of the PV panel power if high conversion ratios are required.

With the S-PPC the output voltage of the converter can be added to the panel output voltage (boost operation) and/or subtracted from the panel voltage (buck operation). The S-PPC converter with only boost functionality is also often referred to as series connected boost (SCB) converter [12], [13]. This converter type can be realized with a transformer with either a full-bridge, half-bridge, or push–pull stage on the primary side and a full-bridge diode rectifier, center-tapped rectifier, or voltage doubler rectifier on the secondary side [14]. Topologies which allow for buck and boost operation are presented in [15], [16], and [17]. For the same reasons as explained for the full-power converter concept, an S-PPC converter with buck–boost voltage conversion capability is favorable. In Appendix typical realizations of the S-PPC concept with boost functionality are compared to the full-power boost converter based on component load factors (CLF) [18]. The results show that the S-PPC concept only offers an advantage if a slight adaption of the PV panel current is used, and thus the rated power of the converter can be relatively low, which yields low CLF values.

Consequently, the possibility to exploit the advantages of S-PPCs as PV panel-integrated dc–dc converters mainly depends

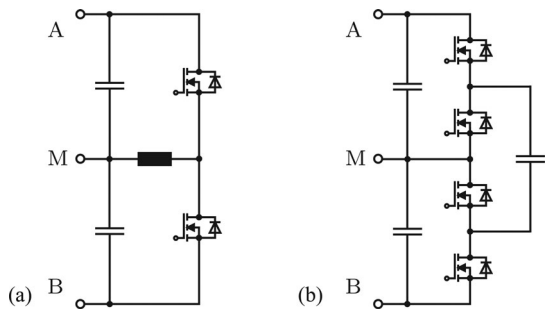

Fig. 7. Possible realizations of the parallel connected partial-power converter (P-PPC): (a) converter based on a bidirectional buck–boost converter and (b) a switched-capacitor converter.

on the required voltage conversion ratio. As already mentioned in Section II-A, the output voltages of the converters have to cover a wide range (up to a factor of four between the minimum and maximum voltage) in order to cope with the most challenging shading scenarios which, in combination with a relatively high complexity of the S-PPC buck–boost concept, renders the S-PPC as unsuitable for PV panel integration.

The P-PPC concept is well known from battery management systems used for the charge equalization of battery cells [19], [20] which are realized, e.g., as bidirectional buck–boost converters [cf., Fig. 7(a)] [21] or without magnetic components as a switched-capacitor circuit [cf., Fig. 7(b)] [22], [23]. This concept of voltage equalization applied to PV panels leverages the fact that the MPP voltages of the PV panels hardly depend on the level of irradiance but primarily on the panel temperature [cf., Fig. 8(a)]. Thus, due to the P-PPCs, all panels operate at the same voltage which is also close to their MPP voltage [24]. With such a technique the share of string current which is greater than the MPP current of a shaded panel is bypassed around that panel which means that all panels can operate close to their MPP despite different MPP currents. This concept can be used both on the panel and on submodule level. In a string with N PV panels, the string MPP current $I_{\mathrm{String,MPP}}$ depends on the MPP currents of the individual panels by

$$I_{\mathrm{String,MPP}} = \frac{\sum_{i=1}^{N} I_{\mathrm{MPP},i}}{N} \tag{4}$$

which can be derived for the condition of equal PV panel voltages from (17) in [25]. As a result, the whole string exhibits only one MPP at a certain operating point which has to be tracked by the central inverter or an additional dc–dc converter. This additional string dc–dc converter for the P-PPC concept must also be considered in order to ensure a fair comparison with the aforementioned categories of panel-integrated dc–dc converters that are directly able to adapt the string voltage to a certain bus voltage U_{Bus}. The output voltage of commonly used crystalline Silicon PV panels is strongly dependent on the panel temperature and can vary by a factor of two if the minimum MPP voltage and the maximum open-circuit voltage are considered over a large temperature range ($-10 \ldots 70\,^{\circ}\mathrm{C}$) [26]. Thus, if multiple strings of PV panels have to be connected in parallel in order to interface with the central dc–ac inverter, each of those strings needs to be equipped with a dc–dc converter or a multistring inverter has to be used. Moreover, the adaption of the string voltage to a specific bus voltage benefits the system efficiency as the central ac–dc inverters exhibit a peak efficiency at a certain bus voltage [27]. However, the dc–dc converter stage required for the P-PPC introduces additional losses which can be assumed to have a typical peak efficiency of around 98% (which most 3-ph. inverters also reach [28]) unless it can be bypassed if all string voltages are equal. Therefore, aiming for the most efficient MIC concept, the P-PPC is not suitable for panel integration and will not be considered any further in this paper.

III. Converter Dimensioning and Optimization

As a result of the evaluation process of Section II, the full power buck–boost converter concept is selected as the best suited MIC concept for series-connected PV panels due to its high flexibility in the number of PV panels per string.

A. Choice of the Converter Topology

The buck–boost converter can be realized by either a two-switch topology or a four-switch topology as shown in Fig. 4(c). These two converter topologies are compared to each other regarding their switching and conduction losses, under the assumption that the same total silicon area A_{Si} and the same switching frequency is used for both converter topologies. As a result, the conduction losses and switching losses of the converters can be set in relation. For the reasons of simplification, it is also assumed that the four-switch and the two-switch buck–boost converter comprise the same kind of switches with a specific on-state resistance $R^{*}_{\mathrm{DS(on)}} = R_{\mathrm{DS(on)}} \cdot A_{\mathrm{Si}}$.

Since the four-switch converter is either working in buck or boost mode, with only one bridge-leg being switched, the conduction losses can be obtained in dependence of the transfer ratio $T_F = U_2/U_1$ as

$$P_{\mathrm{cond,4sw}} = \begin{cases} 2 \cdot \dfrac{R^{*}_{\mathrm{DS(on)}} \cdot 4}{A_{\mathrm{Si}}} \cdot \left(\dfrac{P}{T_F \cdot U_1} \right)^2, & \text{if } T_F \leq 1 \text{ (buck)} \\ 2 \cdot \dfrac{R^{*}_{\mathrm{DS(on)}} \cdot 4}{A_{\mathrm{Si}}} \cdot \left(\dfrac{P}{U_1} \right)^2, & \text{if } T_F > 1 \text{ (boost)} \end{cases} \tag{5}$$

where $R^{*}_{\mathrm{DS(on)}}$ characterizes the switch technology for a certain voltage blocking capability [8]. The conduction losses of the two-switch buck–boost converter can be expressed in a similar way by

$$P_{\mathrm{cond,2sw}} = \frac{R^{*}_{\mathrm{DS(on)}} \cdot 2}{A_{\mathrm{Si}}} \cdot \left(\frac{P(1+T_F)}{T_F U_1} \right)^2. \tag{6}$$

For the calculation of the switching losses it can be assumed that only the capacitances C_{OSS} of the transistors are determining the switching losses during the turn-on operation, while the contribution of the junction capacitances and the reverse recovery current of the diodes as well as other parasitic capacitances are neglected. By taking into account the voltage dependence of

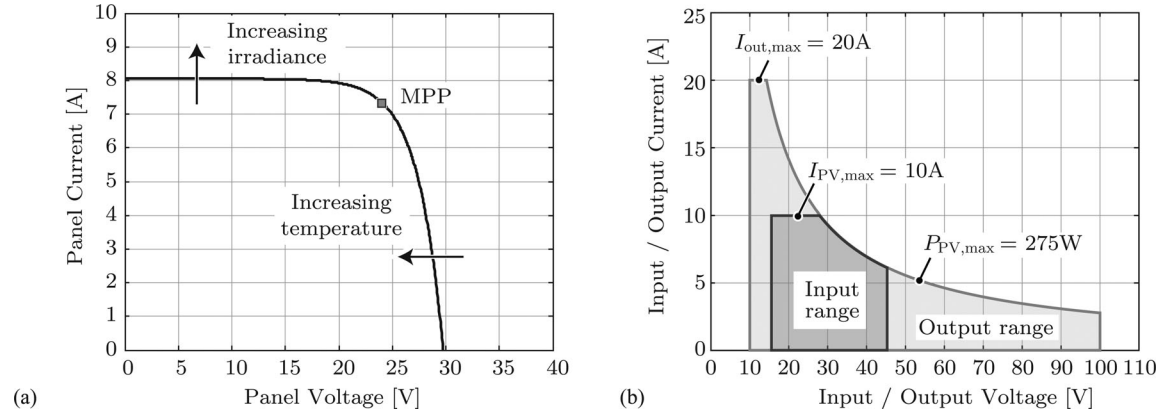

Fig. 8. (a) Influence of temperature and irradiance on electrical characteristic of PV panel and (b) derived input and output specifications of the PV panel-integrated converter.

$C_{\text{OSS}}(U_{\text{DS}})$, the loss of energy can be expressed as (cf., [29])

$$E_{\text{S,turn-on}} = \frac{2}{3} C_{\text{OSS,ref}} \sqrt{U_{\text{DS,ref}}} U_{\text{DS}}^{(3/2)} \,. \tag{7}$$

Furthermore, the four-switch buck–boost converter can operate in pass-through mode if the voltage tranfer ratio T_F is equal to one. Hence, the switching losses of the four-switch converter are given by

$$P_{\text{sw,4sw}} = \begin{cases} \frac{2}{3} C^*_{\text{OSS,ref}} \frac{A_{\text{Si}}}{4} \sqrt{U_{\text{DS,ref}}} U_1^{(3/2)} f_{\text{sw}}, & \text{if } T_F < 1 \text{ (buck)} \\ 0, & \text{if } T_F = 1 \\ \frac{2}{3} C^*_{\text{OSS,ref}} \frac{A_{\text{Si}}}{4} \sqrt{U_{\text{DS,ref}}} (T_F U_1)^{(3/2)} f_{\text{sw}}, & \text{if } T_F > 1 \text{ (boost)} \end{cases} \tag{8}$$

and for the two-switch converter by

$$P_{\text{sw,2sw}} = \frac{2}{3} C^*_{\text{OSS,ref}} \frac{A_{\text{Si}}}{2} \sqrt{U_{\text{DS,ref}}} \left(\frac{U_1}{1 - \frac{T_F}{1+T_F}} \right)^{(3/2)} f_{\text{sw}} \,. \tag{9}$$

The values $R^*_{\text{DS(on)}}$ and $C^*_{\text{OSS,ref}}$ are defining a figure of merit (FOM) (see eq. (34) in [30]) which denotes a technology limit

$$\text{FOM}_{\eta\rho 1} = \frac{1}{\sqrt{R^*_{\text{DS(on)}} C^*_{\text{OSS,ref}}}} \,. \tag{10}$$

The previously calculated semiconductor losses of the two-switch converter in relation to the four-switch converter are shown in Fig. 9. It can be revealed that the four-switch converter features lower switching losses but larger conduction losses in the whole operating range. However, in this comparison only the conduction losses in the semiconductors have been considered. Since the inductor current in the two-switch converter is larger than in the four-switch converter, the ohmic losses of the inductor and of the PCB tracks of the two-switch converter will probably be higher than the ones of the four-switch converter and difference of the conduction losses will decrease.

Furthermore, the relative volume of the passive components can be compared between the two converter types by assessing the stored energy in the inductor and capacitors. With the introduction of tolerable relative voltage and current ripples,

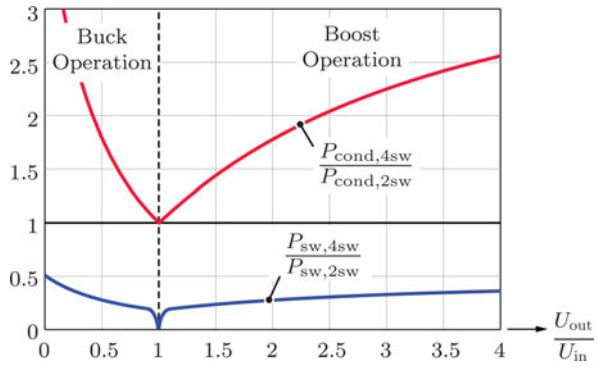

Fig. 9. Relation of semiconductor losses, i.e., conduction losses P_{cond} and switching losses P_{sw}, between the four-switch and the two-switch buck–boost converter under the assumption that the same total silicon area is used for both converter designs.

$\varepsilon_{uC} = \Delta u_C / U_C$ and $\varepsilon_{iL} = \Delta i_L / I_L$, respectively, ($U_C$ and I_L denominate the rated values of the capacitor voltage and inductor current, respectively), the energy stored in the capacitors (which is related to the physical capacitor volume, see ch. 5 in [31]) can be expressed for the four-switch converter as

$$E_{\text{C,4sw}} = \begin{cases} \frac{1}{4}(1 - T_F) \frac{P}{f_{\text{sw}}} \frac{\left(1 + \frac{\varepsilon_{uC}}{2}\right)^2}{\frac{\varepsilon_{uC}}{2}}, & \text{if } T_F \leq 1 \text{ (buck)} \\ \frac{1}{4} \frac{T_F - 1}{T_F} \frac{P}{f_{\text{sw}}} \frac{\left(1 + \frac{\varepsilon_{uC}}{2}\right)^2}{\frac{\varepsilon_{uC}}{2}}, & \text{if } T_F > 1 \text{ (boost)} \end{cases} \tag{11}$$

and for the two-switch converter as

$$E_{C,\text{2sw}} = \frac{1}{4} \frac{P}{f_{\text{sw}}} \frac{\left(1 + \frac{\varepsilon_{uC}}{2}\right)^2}{\frac{\varepsilon_{uC}}{2}} \,. \tag{12}$$

In an analogous fashion, the equations for the stored energy in the inductor (which is again related to the component volume

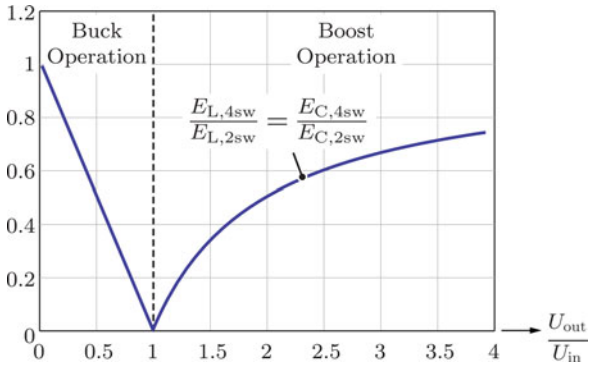

Fig. 10. Relation of the energy stored in the inductors and/or capacitors of the two-switch and the four-switch buck–boost converter under the assumption of a certain equal relative current and/or voltage ripple $\varepsilon_{uC} = \varepsilon_{iL}$.

[31]) can be expressed for the four-switch converter as

$$E_{\mathrm{L,4sw}} = \begin{cases} \frac{1}{4}(1-T_F)\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{iL}}{2}\right)^2}{\frac{\varepsilon_{iL}}{2}}, & \text{if } T_F \le 1 \text{ (buck)} \\ \frac{1}{4}\frac{T_F-1}{T_F}\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{iL}}{2}\right)^2}{\frac{\varepsilon_{iL}}{2}}, & \text{if } T_F > 1 \text{ (boost)} \end{cases} \tag{13}$$

and for the two-switch converter as

$$E_{\mathrm{L,2sw}} = \frac{1}{4}\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{iL}}{2}\right)^2}{\frac{\varepsilon_{iL}}{2}}. \tag{14}$$

The energy storage requirements of both converter topologies can now be directly related, which yields

$$\frac{E_{\mathrm{L,4sw}}}{E_{\mathrm{L,2sw}}} = \frac{E_{C,\mathrm{4sw}}}{E_{C,\mathrm{2sw}}} = \begin{cases} (1-T_F), & \text{if } T_F \le 1 \text{ (buck)} \\ \frac{T_F-1}{T_F}, & \text{if } T_F > 1 \text{ (boost)} \end{cases} \tag{15}$$

as shown in Fig. 10. The comparison of semiconductor losses as well as the ratio of the stored energies and/or volumes of passive components indicates benefits for the four-switch topology, which is selected for the further dimensioning and optimization. In addition, with a special modulation scheme, the four-switch converter can also be operated in a soft-switching mode [32] which results in lower switching losses. However, this modulation scheme induces higher RMS values of the inductor current and an increased complexity in the control scheme and thus is not considered in this study.

B. Modeling of Converter Losses

In this section, the general converter optimization procedure is described and the results for a converter realization with Si MOSFETs with a switching frequency of 100 kHz, and a converter with GaN FETs with a switching frequency of 400 kHz are shown.

As a first step of the optimization, the converter specifications have to be defined. The converter input operating range depends on the electrical output characteristic of the PV panel, i.e., dependence of the output current on the output voltage of a PV panel. This characteristic changes with temperature and irradiance level [cf., Fig. 8(a)] but also depends on the type of PV panel (e.g., polycristalline or monocristalline). In order to cope with these variations, a converter input operating range can be defined as shown in Fig. 8(b), whereas the full set of converter specifications is summarized in Table II.

TABLE II
SPECIFICATIONS OF MODULE INTEGRATED DC–DC CONVERTERS

Parameter	Variable	Value
Max. converter power	P_{conv}	275 W
Input voltage	U_{in}	15 V...45 V
Max. input current	$I_{\mathrm{in,max}}$	10 A
Output voltage	U_{out}	10 V...100 V
Max. output current	$I_{\mathrm{out,max}}$	20 A
Ambient temperature	T_{amb}	$-20°\mathrm{C}...+80°\mathrm{C}$
Bus voltage	U_{Bus}	400 V

For a comprehensive and meaningful modeling of the converter, the tradeoff between efficiency and power density can be visualized by means of a η-ρ-Pareto front. There the volume of the employed components and their losses have to be identified for each design, as shown in the design procedure of Fig. 12. The main losses can be categorized as follows:

1) switching losses (P_{semi}) of MOSFETs including gate drive losses;
2) DC, skin effect, and proximity effect winding losses ($P_{\mathrm{DC}}, P_{\mathrm{sk}}$, and P_{pr}) and core losses (P_{core}) of the inductor;
3) ohmic losses of the PCB tracks (P_{PCB}) and conduction losses due to the on-state resistance of the MOSFETs ($P_{\mathrm{Rds,on}}$);
4) constant losses (P_{const}), i.e., power consumption of the auxiliary supply for the DSP, current and voltage sensors, and other peripheral electronics.

1) Switching Losses (P_{Semi}): The choice of input side switches is based on the required blocking voltage, which is defined by the upper limit $U_{\mathrm{in,max}}$ of the converter input voltage range. Thus, MOSFETs with a blocking voltage capability of at least 60 V are required for the input side and MOSFETs with a voltage rating of around 150 V are sufficient for the output side. Resulting from the wide operating range, the output side switches virtually have to cope with a power of $U_{\mathrm{out,max}} \cdot I_{\mathrm{out,max}} = 2$ kW. The switching losses of the MOSFETs strongly depend on the specific PCB layout which has to be optimized with regard to parasitic inductances in the commutation paths. This is in particular the case for low-load impedances, i.e., for operating points with low voltage and high current as it could occur in buck operation. In combination with different gate drives and variations of the gate resistance, an accurate analytical modeling of the switching losses becomes very challenging. Thus, switching loss measurements have been conducted with a small set of suitable switches from different manufactures and, where applicable, LTSPICE simulations have been performed to build up a loss database containing the energy loss E_{semi} occuring within a switching period depending on the switched current and voltage for a certain junction temperature.

2) Inductor Design and Losses ($P_{\mathrm{DC}}, P_{\mathrm{pr}}, P_{\mathrm{sk}}$, and P_{Core}): The converter is designed to work in continuous conduction

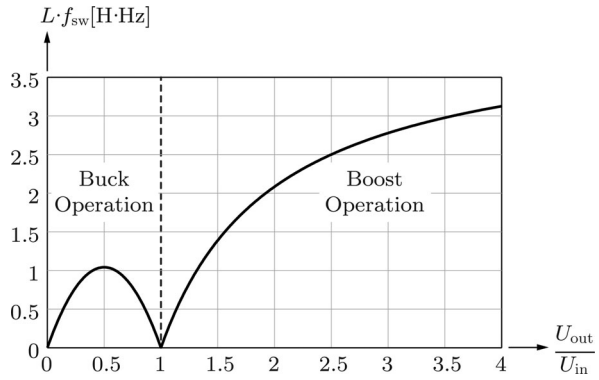

Fig. 11. Normalized inductance value in dependence of the output to input voltage ratio for an operating point of $U_{\mathrm{in}} = 25$ V and a maximum current ripple of $\pm 30\%$ of $I_{\mathrm{in,max}}$.

mode and thus shows a dc inductor current with superimposed switching frequency-dependent ripple. The value of the inductor is chosen considering a limitation of the current ripple to a maximum of ± 3 A which is equal to $\pm 30\%$ of the maximum input current $I_{\mathrm{in,max}}$. As shown in Fig. 11, the worst case requirement to maintain this limit is given by the highest boost ratio operating point, i.e., for $U_{\mathrm{out,max}} = 100$ V. Moreover, an inductor design is only valid, if the maximum flux density B_{pk} in the core with cross section A_c is well below the saturation flux density of the core material. The peak flux density can be calculated by

$$B_{\mathrm{pk}} = \frac{L \cdot I_{\mathrm{pk}}}{N \cdot A_c} \tag{16}$$

where N is the number of turns and I_{pk} the peak current which can be determined as sum of the maximum average current according to (2) and the ripple current. The core losses of the inductor can be calculated for nonsinusoidal flux waveforms with the improved generalized Steinmetz equation [33] which yields the power loss per unit volume

$$P_{\mathrm{V,core}} = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt \tag{17}$$

with ΔB being the peak-to-peak flux density and

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{18}$$

where α, β, and k are material parameters that can be deduced from manufacturer's data sheets of a core material by curve fitting. According to [34], these parameters have to be adapted to take the dc-bias into account. Furthermore, (17) can be simplified for piece-wise linear flux density waveforms as present in the converter.

The winding losses are caused by the conduction losses of the dc inductor current and by eddy currents which are increasing with increasing frequency. The eddy currents lead to skin effect and proximity effect losses which can be determined by means of FEM simulations for a specific core design or by analytical approximations as summarized in [35].

3) Capacitor Selection: Similar to the current ripple criterion for the inductor value, a voltage ripple criterion has to be defined for the input and output capacitors. In [36] it was shown, that the voltage ripple at the PV panel should be kept below 8.5% of the MPP voltage in order to extract 98% of the available panel power. This statement mainly focuses on MPP trackers which periodically change the converter input voltage in order to track the MPP of the PV panel. The voltage ripple which is caused by the switching transients should be kept to a minimum in order to not influence the MPP tracker. Thus, the maximum relative peak-to-peak voltage ripple at the input and output is limited to around 2%, which yields $C_{\mathrm{in}} \cdot f_{\mathrm{sw}} \approx 7\,\mathrm{F} \cdot \mathrm{Hz}$ and $C_{\mathrm{out}} \cdot f_{\mathrm{sw}} \approx 4.5\,\mathrm{F} \cdot \mathrm{Hz}$.

IV. Optimization Results and Experimental Verification

In this section, the optimization results for two semiconductor technologies, i.e., Si and GaN, are shown and experimentally verified as prototypes. First, the GaN technology is described and the differences to Si and SiC are pointed out. Furthermore, the different ways of measuring a converter efficiency are compared and the measurement setup which was used for the measurements of the prototypes is described. In addition, the control scheme of the converter as well as the PV system composed of multiple PV panels with module integrated dc–dc converters and the subsequent inverter are presented.

A. GaN Transistor Technology

For the past 30 years, after its first appearance in 1976 as an alternative to bipolar transistors, the Si MOSFET has dominated the area of switching power conversion in the low-power range due to its properties as an unipolar device with no threshold voltage in forward direction, easy controllability of the switching speed via gate resistances, the lack of tail currents, its ruggedness, and its fast switching speeds [37]. But, since the development of superjunction MOSFETs and the related overcoming of the silicon limit, the rate of improvement has slowed down. However, with the recent introduction of enhancement-mode gallium-nitride-on-silicon transistors, the switching figure of merit ($R_{\mathrm{DS,on}} \cdot Q_{\mathrm{GD}}$) of Si MOSFETs could be significantly improved by a factor of six for 200 V devices and by a factor of two to three for 40 and 100 V devices [38]. The major benefits of GaN FETs arise from the physical properties of gallium nitride as a wide band-gap material like silicon carbide (SiC). Wide band-gap materials posses a higher critical electric field strength than silicon which allows to manufacture devices with a lower on-state resistance $R_{\mathrm{DS,on}}$ at a given maximum blocking voltage capability. A distinctive feature of GaN in combination with an AlGaN layer is the formation of a 2-D electron gas (2-DEG) with unusually high electron mobility that facilitates even smaller devices for a certain on-resistance and maximum operating voltage than realizable with SiC [38]. The maximum allowed operating voltage of this type of devices is not defined by an avalanche break-down mechanism as for a pn-junction, a metal–semiconductor contact (Schottky barrier) or metal–oxide–semiconductor but by a subthreshold leakage current that increases with increasing drain-source voltage [39], [40]. Furthermore, due to the pure lateral structure of

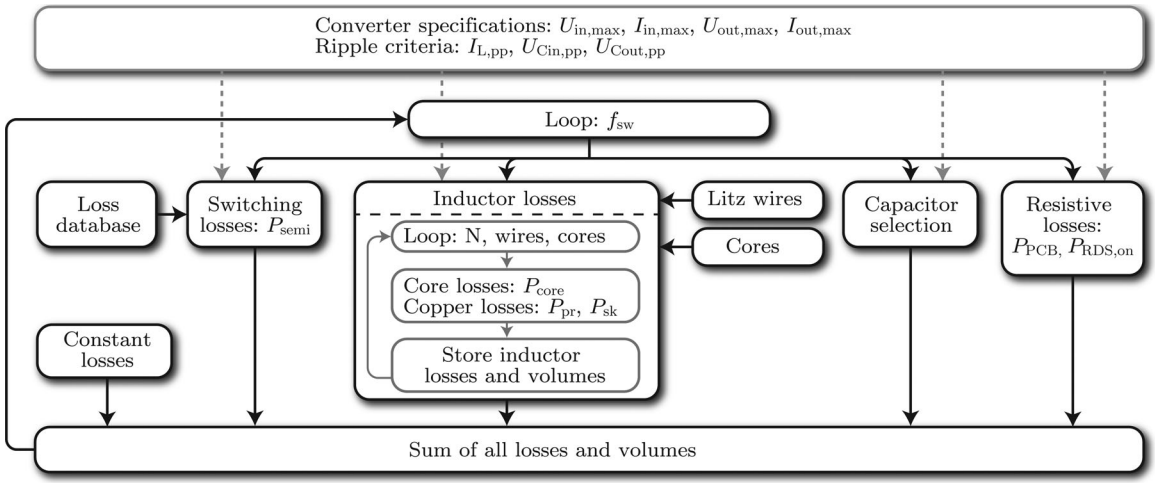

Fig. 12. η-ρ-Pareto optimization algorithm for the four-switch buck–boost converter: A loop over a range of switching frequencies is executed and for each switching frequency a converter design is calculated based on the converter specifications and ripple criteria. This includes the design of the main inductor which is executed in an inner loop to minimize the losses, where all available core sizes are considered. As a result of the optimization all converter losses and the converter volume are stored in order to plot efficiency versus power density characteristic.

GaN FETs, no parasitic pn-diode is inherently present as given for vertical Si MOSFET structures. However, a reversed bias GaN FET operates in a similar manner as a body diode but due to a different mechanism [38]. Thus, for reverse conduction no minority carriers are involved so that no reverse recovery losses are generated. These advantages enable the design of converter systems with higher switching frequencies at the same efficiency which leads to reduced volumes of passive components and thus to an overall increase in power density.

As a drawback, the recent generation of GaN FETs is not avalanche rated, thus special care has to be taken to prevent transient overvoltages. Moreover, the gate-source voltage must not exceed an upper limit of $6\,V$ which requires the application of gate drives with voltage clamping. Because of a rather low threshold voltage of around $U_{\mathrm{GS,th}} = 1.6\,V$, the gate to source path needs to be designed for minimum inductance in order to prevent an erroneous turn-on of the switch due to fast switching transients in rectifier operation.

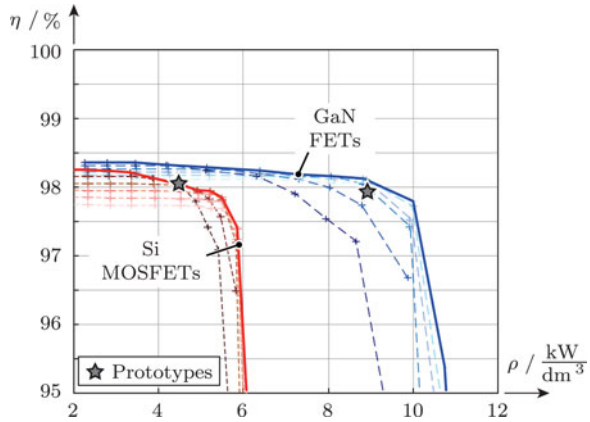

Fig. 13. Results of the η-ρ Pareto optimization for a four-switch buck–boost converter with either Si MOSFETs or GaN FETs. The efficiency is calculated as the mean value of two operating points, i.e., at an input voltage of 30 V and an output voltage of 20 V and/or 40 V with an input power of 200 W. The solid lines represent the Pareto fronts of each semiconductor technology, whereas the dashed lines are results for specific switching frequencies (20 kHz . . . 500 kHz).

B. Optimization Results and Prototype Realizations

The results of the η-ρ Pareto optimization of the buck–boost converter are comparatively shown for both semiconductor technologies, i.e., Si MOSFETs and GaN FETs, in Fig. 13. In order to ensure a fair comparison, the efficiency shown in the graph is calculated as mean value of the efficiencies given for boost operation ($U_{\mathrm{in}} = 30$ V, $U_{\mathrm{out}} = 40$ V) and buck operation ($U_{\mathrm{in}} = 30$ V, $U_{\mathrm{out}} = 20$ V) at an input power of 200 W. The advantages of lower switching losses of GaN FETs in comparison to Si MOSFETs can be leveraged in two dimensions: a converter system can be realized with a higher power density at the same efficiency or with a higher efficiency at the same power density compared to the Si-based system. Based on the results of the Pareto optimization two converter designs with different switching frequencies but same efficiency have been selected for realization as prototypes (cf., Fig. 13).

The Si MOSFET-based converter prototype [see Fig. 14(a)] operates at a switching frequency of $100\,kHz$. The main inductor ($L \approx 30\,\mu$H) of the converter is realized using an N87 ETD34 ferrite core.

For the second prototype [see Fig. 14(b)] GaN FETs have been selected as input and output side switches in combinations with the recommended half-bridge gate driver IC LM5113/TI for GaN FETs. Since the switches and the gate drives are only rated for $100\,V$, the boost operation range is limited to a maximum output voltage of around 70 V. The prototype features a main inductance of $7\,\mu$H consisting of an EFD25 core, also made of N87 ferrite material. Consequently the inductor volume is decreased from 22.6 cm^3 to 8.7 cm^3 ($\approx -62\%$).

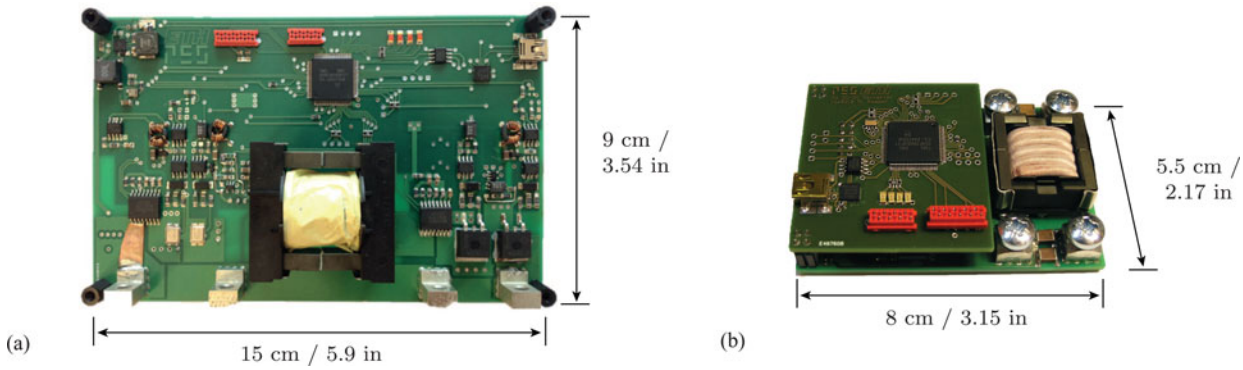

Fig. 14. PV panel-integrated buck–boost converter prototypes: (a) Prototype with Si MOSFETs (input side: IPB072N15N3/Infineon in D2Pak packagage, output side: BSB028N06NN3/Infineon in CanPak package) and 100 kHz switching frequency, and (b) prototype with GaN FETs (EPC2001/EPC) and 400 kHz switching frequency.

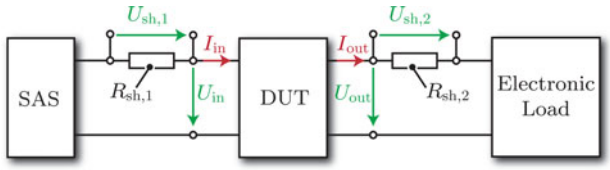

Fig. 15. High precision efficiency measurement setup comprising a solar array simulator, the converter as device under test), an electronic load, highly accurate voltmeters, and shunt resistors for current measurements.

C. Efficiency Measurement Setup

For highly accurate efficiency measurements of converters with losses in the lower watt range, a special measurement setup is required. In general, there are basically three possibilities how efficiency measurements can be performed:

1) measurement of input and output using a power analyzer;
2) separate measurements of input and output voltages and currents, which allows a high accuracy in case of dc quantities;
3) calorimetric measurements, i.e., direct measurement of the losses in combination with a measurement of the input or output power.

Using a power analyzer is the most convenient way and therefore usually the first choice. However, measurements of a dc–dc converter for a typical operating point of PV module even with a high performance power anaylzer such as the WT3000/Yokogawa lead to an efficiency accuracy of only $\pm$ 0.18%. This would mean, that a measurement result of, e.g., 98.5% would only indicate that the actual value is in between 98.32% and 98.68%.

With calorimetric methods the efficiency is determined by measuring the dissipated heat [8]. However, this method requires a special equipment such as a calorimetric chamber and for each measurement some time has to be allowed until a thermal steady state has been reached. Thus, this method is not suitable, especially for measurements of several different operating points.

Consequently, the efficiency measurements have been performed by separately measuring input and output voltages and currents as shown in Fig. 15. The setup consists of a solar array simulator (E4360/Agilent) as a power source, two calibrated measurement shunts (1282/Burster), and four high-precision voltmeters (34410A/Agilent) for the measurements of the converter input and output voltage and the voltage across the shunt resistors for precise current measurements and an electronic load (63202/Chroma). The voltmeters are synchronously triggered by a function generator (33220A/Agilent) in order to measure all values at the same point in time. All devices are centrally controlled by a computer via MATLAB. The converter efficiency can thus be calculated as

$$\eta_{\mathrm{Conv}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{U_{\mathrm{out}} I_{\mathrm{out}}}{U_{\mathrm{in}} I_{\mathrm{in}}} = \frac{U_{\mathrm{out}} \frac{U_{\mathrm{sh},2}}{R_{\mathrm{sh},2}}}{U_{\mathrm{in}} \frac{U_{\mathrm{sh},1}}{R_{\mathrm{sh},1}}}. \tag{19}$$

The accuracy of this method for a typical operating point is $\pm$ 0.05%, i.e., over three times more accurate than a measurement using a power analyzer.

D. Experimental Results

The efficiency measurements have been performed at a fixed input voltage of 30 V and for different output voltages and input power levels. The results for the Si and GaN converters are depicted in Fig. 16(a) for buck operation with output voltages of 20 and 25 V as a function of the input power. In a similar way, the results for boost operation are depicted in Fig. 16(b) for both converter prototypes for output voltages of 35 and 40 V for different input power values.

A comparison of measured efficiency values of both converter prototypes together with results for a commercial converter for PV panel integration, which employs the same four-switch buck–boost topology as the prototypes, is depicted in Fig. 17. In addition, the measured efficiency of the GaN converter for 100 kHz switching frequency is also shown. Due to the lower switching frequency and in order to mainly compare the semiconductor devices, the main inductor of the Si converter was used in the GaN converter for this measurement. The results show, that the GaN converter has higher conduction losses, since the efficiency in buck mode (with decreasing output voltage and thus rising output current) drops below the efficiency of the Si converter for the same switching frequency (100 kHz). This is due to the fact, that, according to the data sheets, the

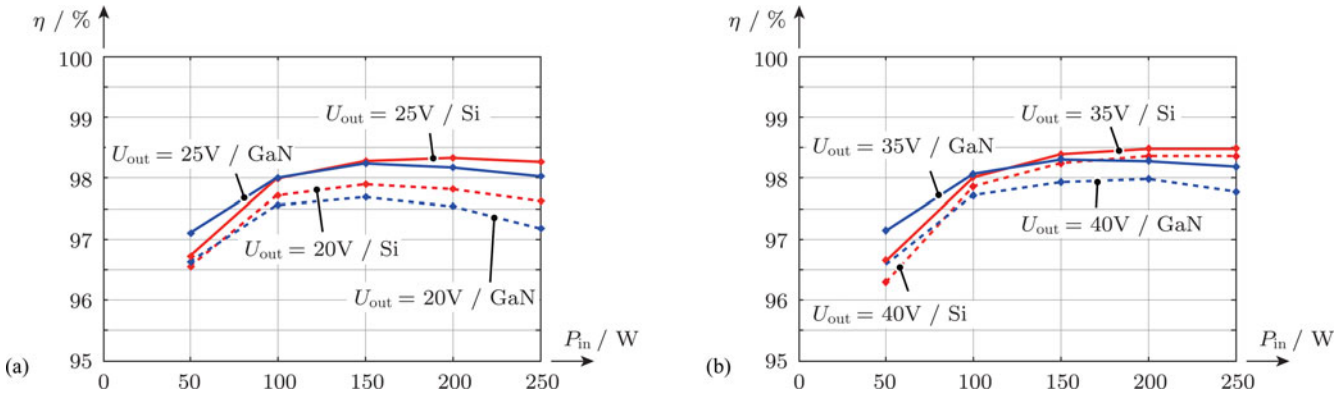

Fig. 16. Efficiency measurement results of the Si converter prototype (f_{sw} = 100 kHz) and the GaN prototype (f_{sw} = 400 kHz): (a) Buck operation at 30 V input voltage and output voltages of 20 and 25 V for different levels of input power P_{in} and (b) boost operation at 30 V input voltage and for output voltages of 35 and 40 V for the same levels of input power P_{in}.

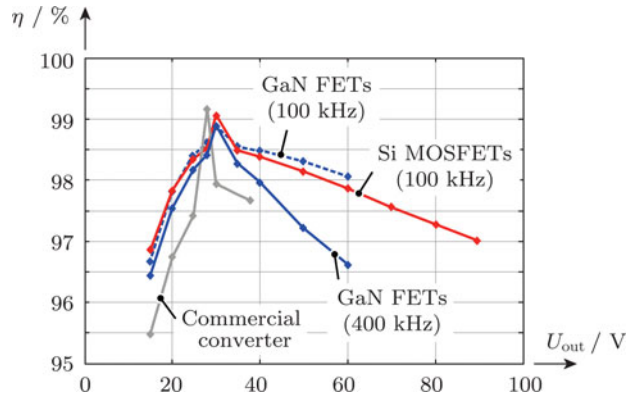

Fig. 17. Efficiency measurement results of the Si converter prototype with a switching frequency of 100 kHz, and the GaN converter with a switching frequency of 400 kHz and also with 100 kHz in comparison to a commercial PV panel-integrated buck–boost converter. The measurements were performed with an input voltage U_{in} of 30 V and an input power P_{in} of 200 W.

total $R_{DS(on),max}$ value of the switches in the Si converter is only 10 mΩ, whereas in the GaN converter the total value is 14 mΩ (+40%). Furthermore, since the chip area of the GaN switches is very small, the PCB copper traces are in general somewhat shorter but also less wide and therefore very likely leading to higher conduction losses on the PCB. If the GaN converter is operated at a switching frequency of 400 kHz, then, besides four times higher switching losses, also higher inductor losses occur.

E. Control of the Converter and PV System

The PV panel exhibits one operating point (U_{PV}, I_{PV}) that results in a maximum panel output power at a certain irradiance and temperature. The panel-integrated converter thus needs to constantly track this operating point as it changes during the course of the day due to the moving sun and shadows, e.g., caused by passing clouds. In the literature many MPP tracking algorithms have been proposed and comparatively evaluated [41]. The perturb and observe (P&O) method provides a good performance with low complexity and is thus selected for implementation in the prototypes. The controller consists of a

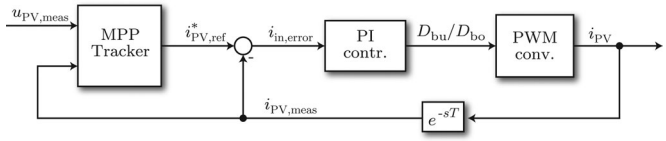

Fig. 18. Cascaded converter control with the MPP tracker as (slow) outer control loop and the PV current controller as (fast) inner control loop.

cascaded structure where the outer loop comprises the MPP tracker that multiplies the measured values of panel voltage and current to determine the panel output power (cf., Fig. 18). The inner loop controls the panel current which receives reference values from the MPP tracker. The MPP tracker is constantly varying the current reference value and the direction of perturbation is based on the previous step and the corresponding change in panel power.

The current controller has to be comparably fast in order to decouple the control loops. The transfer function of the converter changes as the converter operation moves from buck to boost mode or vice versa which has to be considered in the design of the current controller. The small-signal transfer function of the duty cycle to the PV panel current can be found using the state-space averaging approach [42] for the buck converter with stationary duty cycle D_{bu} as

$$G_{id,buck}(s) = \frac{I_0 \cdot L \cdot C \cdot s^2 + C \cdot D_{bu} \cdot U_{PV} \cdot s + I_0}{C \cdot L \cdot s^2 + 1} \quad (20)$$

and for the boost converter with duty cycle D_{bo} as

$$G_{id,boost}(s) = \frac{(1 - D_{bo})I_0 + C \cdot U_{PV} \cdot s}{(1 - D_{bo})^2 + C \cdot L \cdot s^2} \quad (21)$$

where I_0 denotes the converter output current, i.e., the string current. The string current is controlled by the central (string) inverter and thus exhibits slower dynamics. The transition from buck to boost mode and vice versa is implemented as described in [43]. When the output voltage is equal to input voltage a so-called pass-through mode can be activated where only the upper switches of each bridge-leg are activated which allows to mitigate any switching losses by connecting the converter input via the inductor with the converter output. However, in

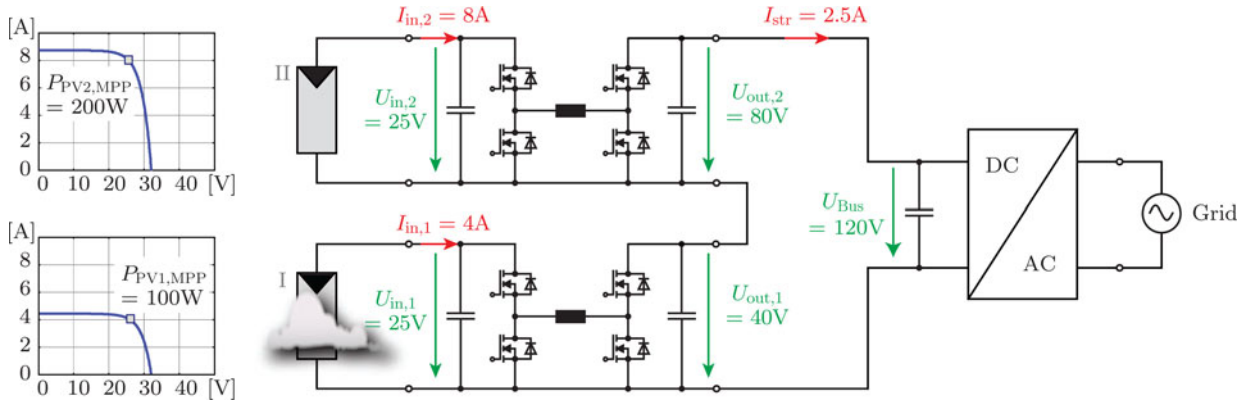

Fig. 19. Example of a PV system which employs for reasons of simplification only two PV panels with integrated buck–boost converters and generates accordingly a low bus voltage U_{Bus} of only 120 V. Each converter tracks the MPP of the attached PV panel and the central dc–ac inverter controls the bus voltage with a reference value of 120 V. The converter output voltages $U_{\mathrm{out},1}$ and $U_{\mathrm{out},2}$ reach a steady-state value according to (22).

this case the controllability is lost as the MPP tracker can no longer determine whether the panel is operated in its MPP. One method to overcome this problem is to periodically leave the pass-through mode and to sweep through a certain range of operating points in order to determine whether other operating points can deliver more power [44].

The control of the full system does neither require any communication between the individual PV panel-integrated converters nor between the panel-integrated converters and the central dc-ac grid inverter. Each panel-integrated converter can track the MPP of the attached PV panel as described previously. As a consequence, the converter output voltage is not controlled by the panel-integrated converter but its value depends on the output power of the attached PV panel and the string current which is common for all converters. Thus, the central dc–ac inverter can control the bus voltage U_{Bus} by adapting the string current I_{str}. The steady-state output voltages of the converters can be calculated for a system with N PV panels as

$$U_{\mathrm{out},i} = \frac{P_{\mathrm{PV},i}}{I_{\mathrm{str}}} = \frac{P_{\mathrm{PV},i} \cdot U_{\mathrm{Bus}}}{P_{\mathrm{PV,tot}}} = \frac{P_{\mathrm{PV},i} \cdot U_{\mathrm{Bus}}}{\sum_{j=1}^{N} P_{\mathrm{PV},j}}, \quad i \in \{1, 2, \ldots, N\}. \tag{22}$$

An example of a PV system with only two PV panels with buck–boost converters and a bus voltage of only 120 V is depicted in Fig. 19. For extreme irradiance differences (shading) between the panels, the converter output voltage of the panel with the highest output power might reach the upper limit. In that case, the converters has to deliberately move the operating point out of the MPP to reduce the input power until the output voltage is no longer at the maximum value. To overcome this problem additional communication between the panels or with a supervisory control circuit would be necessary [45].

V. Conclusion

In this paper, an overview of the possible topologies for module integrated dc–dc converters is given. The converter concepts can be divided into full power and partial-power converters both with subcategories of series and parallel connection. The full power buck–boost converter is identified as the most promising concept for series-connected PV panels due to the great flexibility it provides regarding the number of panels per PV string for a fixed dc bus voltage. An optimization/modeling procedure is described in detail which allows to obtain an efficiency/power densitiy (η-ρ) Pareto front. Based on the results of the analytical modeling, two prototypes of the full-power processing buck–boost concept are realized for a rated power of 275 W and an input/output voltage range of $U_{\mathrm{in}} = 15-45$ V and $U_{\mathrm{out}} = 12.5-100$ V with either Silicon MOSFETs with a switching frequency of 100 kHz or gallium nitride FETs with a switching frequency of 400 kHz. Both converters feature efficiencies up to 98.5% in switched mode operation and 99% in pass-through operation.

Appendix
Converter Topology Evaluation Criteria

In order to assess the potential of S-PPC in comparison to full-power converters the concept of CLF [18] is selected among different evaluation methodologies such as calculating component utilization quantities [42], [46]–[48] and other criteria [49]. According to [18], the CLF is calculated by relating the apparent power of a component to the active output power of a system

$$\sigma = \frac{V^* I^*}{P_{\mathrm{tot}}}. \tag{23}$$

A total CLF can be derived for each component type, i.e., for transistors, diodes, inductive components, and capacitors by adding the values of the individual components of the same type. A low CLF indicates low component and/or low realization effort due to a good utilization of the components. Depending on the type of component, the values of V^* and I^* can be peak, RMS, or peak-to-peak values. The quantity P_{tot} is the total output power which for PPCs is the sum of the power directly transferred to the load and the power processed by the converter (cf., Fig. 6). In the following, three different topologies of S-PPC boost converters [cf., Fig. 20(b)–(d)] are evaluated and compared to the standard full-power boost converter [see Fig. 20(a)]. All values related to the full-power boost converter are labeled by the subscript FP as an acronym for full power. The S-PPC converter topology shown in Fig. 20(b) [50] is labeled

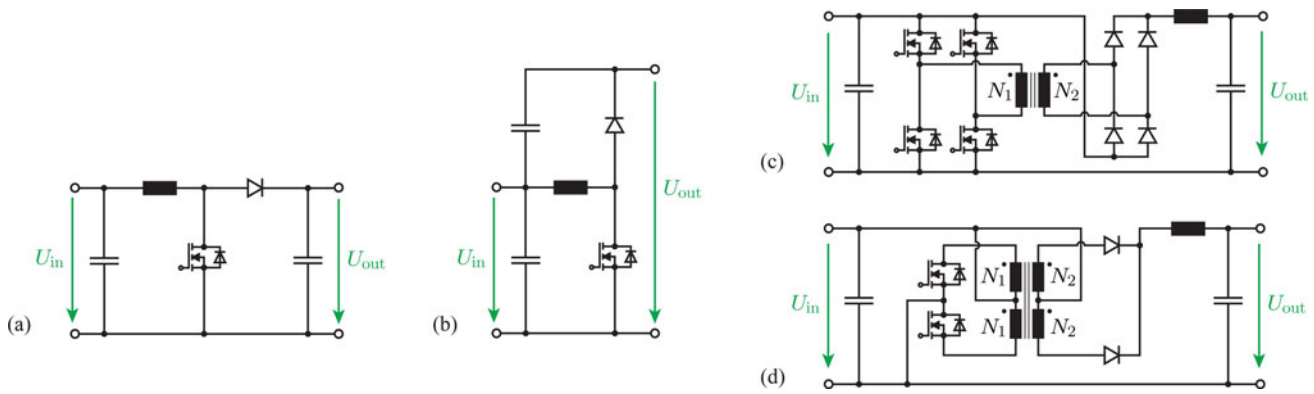

Fig. 20. Full-power and S-PPC boost converter topologies. (a) Standard full-power boost converter used as reference (label: FP), (b) cascaded S-PPC consisting of a buck–boost converter with cascaded input and output voltages (label: CAS), (c) S-PPC with a MOSFET full-bridge on primary side and full-bridge diode rectifier on the secondary side (label: PP1), and (d) S-PPC with a push–pull stage on the primary side and center-tapped rectifier on the secondary side (label: PP2).

with the subscript CAS since it can be seen as a boost converter with input/output voltage cascading. (The topology is similar to voltage balancer converter shown in Fig. 7(a) even if both converters perform a different function.) The other two topologies are a subset of possible S-PPC realizations of the SCB converter [12], [13] that can comprise either a full-bridge, half-bridge, or push–pull topology on the primary side or a full-bridge rectifier, voltage-doubler, current-doubler, or center-tapped rectifier on the secondary side [14], [16], [17]. The converter of [Fig. 20(c)] is labeled with PP1 and the one from [Fig. 20(d)] with PP2. For a meaningful comparison the duty cycles of all topologies have to be given as a function of the voltage transfer ratio $T_F = U_{\mathrm{out}}/U_{\mathrm{in}}$

$$D_{\mathrm{FP}} = D_{\mathrm{CAS}} = \frac{T_F - 1}{T_F} \tag{24}$$

$$D_{\mathrm{PP1}} = D_{\mathrm{PP2}} = (T_F - 1)\frac{N_1}{N_2}. \tag{25}$$

For the deduction of the CLF values, following assumptions were made [18]:

1) ripple currents in filter chokes are neglibly small;
2) converter losses are negligble, thus $P_{\mathrm{in}} = P_{\mathrm{out}}$.

A. Transistor CLFs

As MOSFETs have resistive on-state behavior, the RMS current is chosen as I^*. For V^*, the peak blocking voltage is selected based on the simplification that no over voltage occurs during the switching transient. This yields as total transistor CLF values

$$\sigma_{\mathrm{S,FP}} = \frac{\sqrt{D_{\mathrm{FP}}}}{1 - D_{\mathrm{FP}}} \tag{26}$$

$$\sigma_{\mathrm{S,CAS}} = \frac{\sqrt{D_{\mathrm{CAS}}}}{1 - D_{\mathrm{CAS}}} \tag{27}$$

$$\sigma_{\mathrm{S,PP1}} = 4\sqrt{\frac{D_{\mathrm{PP1}}}{2}}\frac{1}{1 + \frac{N_2}{N_1}D_{\mathrm{PP1}}}\frac{N_2}{N_1} \tag{28}$$

$$\sigma_{\mathrm{S,PP2}} = 2\sqrt{\frac{D_{\mathrm{PP2}}}{2}}\frac{1}{1 + \frac{N_2}{N_1}D_{\mathrm{PP2}}}\frac{N_2}{N_1}\,. \tag{29}$$

B. Diode CLFs

The conduction losses of diodes are mainly determined by the average diode current chosen as I^*. Similar to the transistor CLF, the peak diode blocking voltage is chosen as V^*. The total diode CLF values can be determined as

$$\sigma_{\mathrm{D,FP}} = 1 \tag{30}$$

$$\sigma_{\mathrm{D,CAS}} = 1 \tag{31}$$

$$\sigma_{\mathrm{D,PP1}} = 2\frac{1}{1 + \frac{N_2}{N_1}D_{\mathrm{PP1}}}\frac{N_2}{N_1} \tag{32}$$

$$\sigma_{\mathrm{D,PP2}} = 2\frac{1}{1 + \frac{N_2}{N_1}D_{\mathrm{PP2}}}\frac{N_2}{N_1}. \tag{33}$$

C. Inductor CLFs

For the inductors, the average current is approximately equal to the RMS current if a low current ripple is assumed and is accordingly selected as I^*. For V^*, the average ac voltage is chosen, which is the product of applied voltage and duty cycle if a square wave excitation voltage is assumed [18]. The energy stored in an inductor is equal to $W = L \cdot I_{\mathrm{DC}}^2/2$, where the inductance value L is determined by the current ripple ΔI and the applied voltage; $L = V \cdot D/(f_{\mathrm{sw}} \cdot \Delta I)$. With an allowed current ripple of $\varepsilon_{\mathrm{iL}} = \Delta I/I_{\mathrm{DC}}$ the energy can be expressed as $W = I_{\mathrm{DC}} \cdot V \cdot D/(2 \cdot \varepsilon_{\mathrm{iL}} \cdot f_{\mathrm{sw}})$ which yields $W = I^* \cdot V^*/(2 \cdot \varepsilon_{\mathrm{iL}} \cdot f_{\mathrm{sw}})$ and therefore justifies the selection of the aforementioned values for the calculation of the CLF. This results in

$$\sigma_{\mathrm{L,FP}} = D_{\mathrm{FP}} \tag{34}$$

$$\sigma_{\mathrm{L,CAS}} = D_{\mathrm{CAS}} \tag{35}$$

$$\sigma_{\mathrm{L,PP1}} = D_{\mathrm{PP1}}(1 - D_{\mathrm{PP1}})\frac{1}{1 + \frac{N_2}{N_1}D_{\mathrm{PP1}}}\frac{N_2}{N_1} \tag{36}$$

$$\sigma_{\mathrm{L,PP2}} = D_{\mathrm{PP2}}(1 - D_{\mathrm{PP2}})\frac{1}{1 + \frac{N_2}{N_1}D_{\mathrm{PP2}}}\frac{N_2}{N_1}. \tag{37}$$

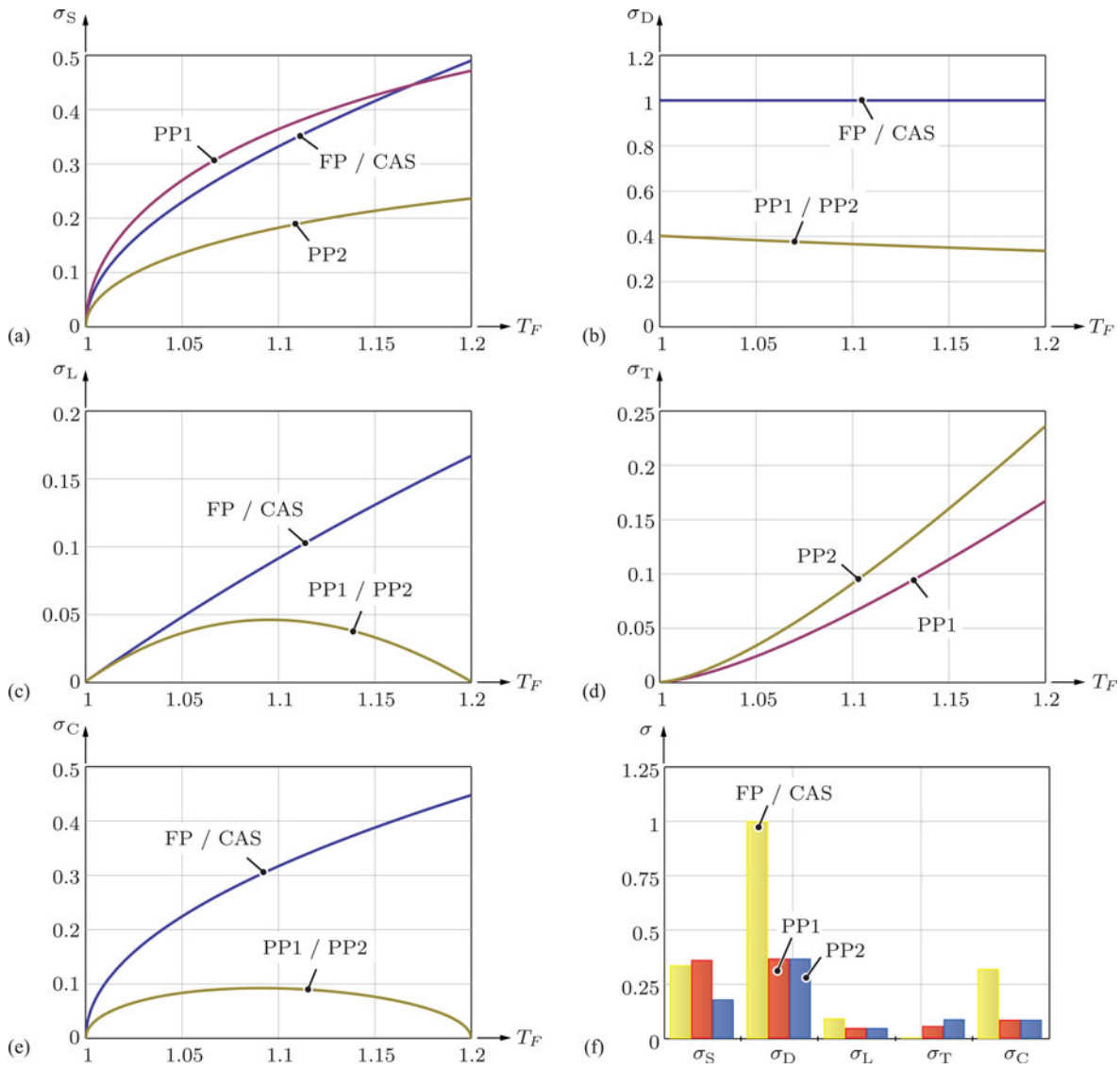

Fig. 21. CLF values of the different component types for the converters of Fig. 20: (a) transistor CLF (σ_S), (b) diode CLF (σ_D), (c) inductor CLF (σ_L), (d) transformer CLF (σ_T), and (e) capacitor CLF. In (f) the different CLF values are plotted for a transfer ratio of $T_F = 1.1$.

D. Transformer CLFs

Only the topologies shown in Fig. 20(c) and (d) comprise a transformer for which again a CLF can be computed for each transformer winding. The average ac voltage and the RMS current are selected as V^* and I^*, respectively, and the transformer load factor is calculated as the sum of the load factors of all windings

$$\sigma_{T,PP1} = D_{PP1}\sqrt{D_{PP1}}\frac{1}{1+\frac{N_2}{N_1}D_{PP1}}\frac{N_2}{N_1} \tag{38}$$

$$\sigma_{T,PP2} = 2D_{PP2}\sqrt{\frac{D_{PP2}}{2}}\frac{1}{1+\frac{N_2}{N_1}D_{PP2}}\frac{N_2}{N_1}\,. \tag{39}$$

This concept is different to the definition of the rated power of a transformer which is calculated by dividing the sum of all apparent power values of all windings by two.

E. Capacitor CLFs

The capacitor design is determined by the current stress and the voltage rating (besides a voltage ripple condition defining a minimum capacitance value). Thus, the RMS current is chosen as I^* and the dc voltage as V^*. The CLF values can be derived as

$$\sigma_{C,FP} = \frac{1}{1-D_{FP}}\sqrt{(1-D_{FP})D_{FP}} \tag{40}$$

$$\sigma_{C,CAS} = \frac{1}{1-D_{CAS}}\sqrt{(1-D_{CAS})D_{CAS}} \tag{41}$$

$$\sigma_{C,PP1} = \frac{1}{1+\frac{N_2}{N_1}D_{PP1}}\frac{N_2}{N_1}\sqrt{(1-D_{PP1})D_{PP1}} \tag{42}$$

$$\sigma_{C,PP2} = \frac{1}{1+\frac{N_2}{N_1}D_{PP2}}\frac{N_2}{N_1}\sqrt{(1-D_{PP2})D_{PP2}}\,. \tag{43}$$

F. Comparison of the Results

The CLFs are evaluated for the requirement of a maximum transfer ratio of $T_F = 1.2$, which yields a transformer winding ratio of $N_2/N_1 = 0.2$ for the PPCs. The results for each component type are shown in Fig. 21(a)–(e) versus T_F for the topologies of Fig. 20. As already visible from the derived CLF equations aforementioned, the full-power boost converter and the cascaded S-PPC exhibit the same CLF values for all components. Thus, in this case the cascaded S-PPC (CAS) potentially does not exhibit any advantages in terms of converter losses and/or realization effort. Conversely, the other two concepts (PP1 and PP2) exhibit lower values of the diode CLF (σ_D), the inductor CLF (σ_L), and the capacitors CLF (σ_C) than the full-power boost converter and the PP2 topology also features a lower CLF value of the transistors (σ_S). Yet, the PPCs require the use of a transformer which yields an additional CLF value. Thus, in order to facilitate an easier assessment of the CLF values of the different topologies, the CLF results for a transfer ratio of $T_F = 1.1$ are shown for the different topologies in the bar chart of Fig. 21(f).

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