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Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters

F. Krismer
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Closed Form Solution for Minimum Conduction Loss Modulation of DAB Converters

Florian Krismer, *Student Member, IEEE*, and Johann W. Kolar, *Fellow, IEEE*

***Abstract*—An optimal modulation scheme that enables minimum conduction and copper losses is presented for a bidirectional dual active bridge (DAB) dc–dc converter. The considered converter system is employed for an automotive application and comprises of a high voltage (HV) port with port voltage V_1, $240\,\mathrm{V} \leq V_1 \leq 450\,\mathrm{V}$, and a low voltage (LV) port with port voltage V_2, $11\,\mathrm{V} \leq V_2 \leq 16\,\mathrm{V}$; the rated output power is $2\,\mathrm{kW}$. The closed-form expressions for the optimal control parameters are derived and implementation details are presented in order to facilitate the direct application to a given DAB converter. The paper further details the properties of the presented modulation scheme with respect to switching losses. Experimental results confirm a considerable increase of the converter efficiency achieved with the proposed optimal modulation scheme, compared to the efficiency obtained with conventional phase shift modulation. The efficiency increase is most distinct at $V_1 = 450\,\mathrm{V}$ and $V_2 = 11\,\mathrm{V}$ with an increase from 78.6% to 90.6% at $1\,\mathrm{kW}$ output power and from 85.9% to 90.7% at rated output power as compared to conventional phase shift modulation.**

***Index Terms*—Battery charger, circuit analysis, DC–DC power conversion, digital systems, optimal control.**

NOMENCLATURE

n	Transformer turns ratio.
L	DAB converter inductance.
f_S	Switching frequency.
T_S	Switching period, $T_\mathrm{S} = 1/f_\mathrm{S}$.
V_1	HV port voltage.
V_2	LV port voltage.
I_L	RMS value of the current through L.
P	DAB power (assuming a lossless DAB).
P_1	Port 1 power ($= P$ for a lossless DAB).
P_2	Port 2 power ($= P$ for a lossless DAB).
$v_{\mathrm{ac}1}$	AC volt. generated by the HV full bridge.
$v_{\mathrm{ac}2}$	AC volt. generated by the LV full bridge.
D_1	Duty cycle used for the HV full bridge.
D_2	Duty cycle used for the LV full bridge.
φ	Phase angle between $v_{\mathrm{ac}1}$ and $v_{\mathrm{ac}2}$.
V_ref	Reference voltage; can be selected arbitrarily, e.g., $V_\mathrm{ref} = 340\ \mathrm{V}$.
$Z_\mathrm{ref} = 2\pi f_\mathrm{S} L$	Reference impedance.
$I_\mathrm{ref} = V_\mathrm{ref}/Z_\mathrm{ref}$	Reference current.
$P_\mathrm{ref} = V_\mathrm{ref}^2/Z_\mathrm{ref}$	Reference power.
$\overline{V}_1 = V_1/V_\mathrm{ref}$	Normalized dc voltage V_1.
$\overline{V}_2 = n\,V_2/V_\mathrm{ref}$	Normalized dc voltage V_2.
$\overline{P} = P/P_\mathrm{ref}$	Normalized converter power level.
$\overline{I}_L = I_L/I_\mathrm{ref}$	Normalized inductor rms current.
CPM	Conventional phase shift modulation.
DAB	Dual Active Bridge.
FSM	Finite State Machine.
HF	High Frequency.
HV	High Voltage.
LV	Low Voltage.
OTM	Optimal Transition Mode Modulation.
TCM	Triangular Current Mode Modulation.

I. INTRODUCTION

THE fuel cell vehicles' power system presented in [1] requires a bidirectional and isolated dc–dc converter to provide power to the HV power train in order to start the car. Thereafter, during normal vehicle operation, the same dc–dc converter powers the LV ancillary loads and charges the LV battery. This bidirectional dc–dc converter is operated within wide voltage ranges:

1) HV port voltage V_1: $240\,\mathrm{V} \leq V_1 \leq 450\,\mathrm{V}$, nominal voltage: $340\,\mathrm{V}$;
2) LV port voltage V_2: $11\,\mathrm{V} \leq V_2 \leq 16\,\mathrm{V}$,[1] nominal voltage: $12\,\mathrm{V}$.

The rated power is $2\,\mathrm{kW}$ within the entire voltage range. For this application the DAB converter topology [see Fig. 1(a)] [2], [3] is selected in [4] due to the low number of passive components and due to its soft-switching properties. It facilitates a high switching frequency and therefore a highly compact converter is feasible [5].

Current research on the DAB converter mainly focuses on four subjects listed below.

1) *Applications of DAB Converters:* to enable bidirectional power transfer between a HV drive train and the LV bus of fuel cell vehicles, hybrid electric vehicles, and electric vehicles [4], [6]; to store electric energy in ultracapacitors in aircraft systems [7].
2) *Characteristics of the DAB in Steady State Operation:* calculation of the impact of dead time intervals and semiconductor losses on the power transferred [8]; converter operation at low power levels [9]; accurate prediction of the power losses of the DAB [4].

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The authors are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zurich, Switzerland (e-mail: krismer@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

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[1] According to [1], V_2 may be as low as 8.5 V. The proposed DAB converter can be operated with $V_2 < 11\,\mathrm{V}$; however, the LV port current of the given converter is limited to 200 A.

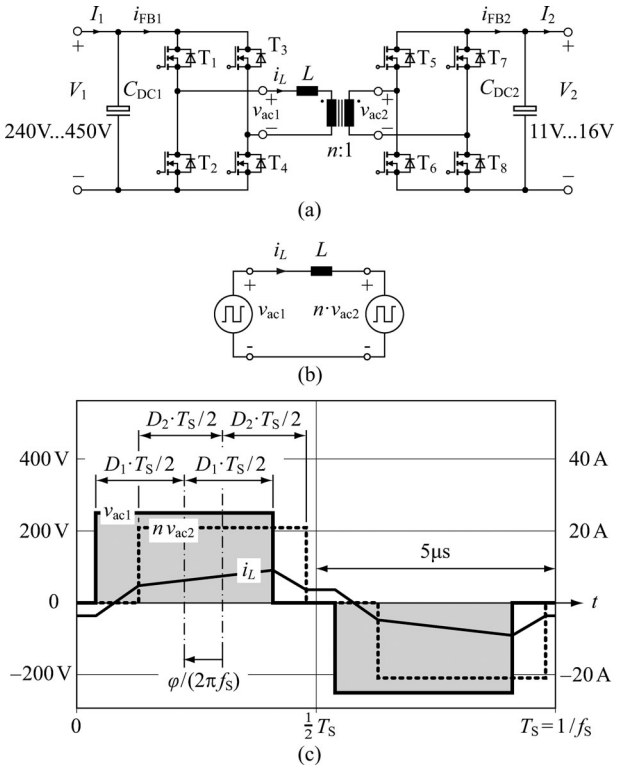

Fig. 1. (a) DAB converter topology; (b) employed lossless electrical DAB model; (c) general waveforms of v_{ac1}, v_{ac2}, and i_L used to define D_1, D_2, and φ; the waveforms are calculated for $V_1 = 250\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$, $D_1 = 0.37$, $D_2 = 0.35$, $\varphi = 0.5\,\mathrm{rad}$, $L = 26.7\,\mu\mathrm{H}$, and $n = 19$.

3) *Modeling of the dynamic converter characteristics and converter control:* derivation of an accurate small signal model of the DAB inclusive EMI filter dynamics [10]; development of a nonlinear control model, which considers the impact of parasitic effects (e.g., dead time) on the dynamic converter properties [11]; investigation of the impact of the employed modulation scheme on the dynamic converter properties [12].
4) *Modulation schemes:* novel modulation schemes, which facilitate increased converter efficiency and/or power density of the DAB converter [13]–[23].

Due to the general demand for high converter efficiency and/or power density, research on improved modulation schemes is particularly prominent.

The first modulation scheme presented in [2], [3] operates the full bridges of the DAB with maximum duty cycles, $D_1 = D_2 = 0.5$, and solely adjusts the phase angle φ between v_{ac1} and v_{ac2} in order to achieve the required power transfer [see Fig. 1(c) defines D_1, D_2, and φ].[2] This modulation scheme, termed conventional phase shift modulation (CPM), thus facilitates simple control of the DAB. Moreover, high converter efficiency is achieved at rated power and for $V_1 \approx nV_2$ [13]. CPM, however, causes considerably increased rms currents in the inductor, the transformer, and the switches for $V_1 \ll nV_2$ or $V_1 \gg nV_2$ (in particular at low power levels), which generates increased losses and reduces the efficiency of the DAB, there [14].

Numerous alternative modulation schemes have been proposed in literature in order to achieve increased efficiency and/or power density of the DAB converter [13]–[23]. The proposed modulation schemes can be classified into the two groups listed below.

1) Some of the proposed modulation schemes apply:

$$D_1 = 0.5 \wedge 0 \le D_2 \le 0.5 \,\forall\, nV_2/V_1 \le 1 \text{ or}$$
$$D_2 = 0.5 \wedge 0 \le D_1 \le 0.5 \,\forall\, nV_2/V_1 > 1. \quad (1)$$

2) The remaining modulation schemes use:

$$0 \le D_1 < 0.5 \wedge 0 \le D_2 < 0.5. \quad (2)$$

The modulation schemes summarized with (1) gain one degree of freedom compared to CPM by either changing D_1 or D_2, which is most often used to extend the converter's operating range where low switching losses occur (ZVS range of the DAB) [15]. A possible selection of D_1 or D_2, useful to achieve an increased ZVS range, is given in [16]. Optimal D_1 or D_2 are calculated in [17] with respect to maximum converter efficiency (on the assumption of a predefined converter loss model) or in [18] with respect to minimum reactive inductor power. However, no closed-form solutions for optimal D_1 and D_2 are given.

The modulation schemes specified with (2) facilitate the highest possible degree of freedom regarding the search toward an optimal modulation scheme, provided that a constant switching frequency is used. As a consequence, analytical investigations, e.g., the calculation of D_1 and D_2 with respect to maximum converter efficiency, become considerably more complex than for the modulation schemes defined with (1) [19]. D_1 and D_2 are thus often calculated with respect to a particular waveform of the inductor current i_L. With the use of triangle-shaped inductor currents, improved low-load efficiency is demonstrated in [20] (as compared to CPM); however, limited voltage ranges apply for V_1 and V_2. This restriction has been eliminated with the introduction of trapezoidal-shaped inductor currents [14], [21]. The best choice between either CPM, triangular inductor current, or trapezoidal inductor current, with respect to high-converter efficiency, is presented in [13]. There, however, no new modulation schemes are considered, whereas this paper describes a new modulation scheme, which outperforms three modulation schemes regarded in [13] with respect to the rms transformer currents within given limits of the output power. In a different approach, in [22], a combination of the modulation schemes given with (1) and (2) is proposed and simple solutions are given for D_1 and D_2, which enables ZVS within a wide range of operation in order to achieve increased converter efficiency. In [23] an analytic approach is presented, which focusses on the reduction of reactive converter power; a possible selection of the control parameters is presented in [12]. With this,

[2]The duty cycles are defined as the durations of the positive active time intervals divided by T_S, e.g., if T_1 is the duration of the time interval with $v_{ac1}(t)$ being equal to $+V_1$ then $D_1 = T_1/T_S$. The phase shift, φ, is measured between the center points of the positive active time intervals of v_{ac1} and v_{ac2}. It can be shown that the sign of φ determines the power transfer direction with this definition, e.g., $\varphi > 0$ causes a power transfer from the HV port to the LV port.

however, considerably high rms currents result, which is shown in Table IV (see Section III-D).

So far, all modulation schemes presented are either restricted to the modulation schemes summarized with (1) or are not optimized with respect to the converter losses. In particular, no closed-form solutions for optimal modulation parameters D_1, D_2, and φ exist.

This paper presents closed-form solutions for D_1, D_2, and φ of a new modulation scheme, which selects the specific operating mode out of all possible operating modes that generates the minimum inductor rms current at a given operating point; this facilitates minimum conduction and copper losses (see Section II-A).

In Section II, a simplified model of the DAB converter is presented and all possible operating modes of the DAB are detailed. The expressions given in Section II facilitate the calculation of optimal control parameters $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ_{opt}, as presented in Section III. In Section III-A the results obtained from a numerical optimization are analyzed in detail in order to enable the derivation of the expressions for optimal control parameters $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ_{opt}. Section III-B summarizes the results obtained for $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ_{opt}. Section IV focusses on the DAB hardware prototype employed; the actual implementation of the optimal modulation scheme is discussed in Section IV-A and measured efficiency results, used to validate the achieved improvements as compared to CPM, are presented in Section IV-B.

II. DAB Model and Operating Modes

The DAB converter contains two voltage-sourced full bridge circuits, which apply the ac voltages $v_{\mathrm{ac1}}(t)$ and $v_{\mathrm{ac2}}(t)$ to the inductor L and the HF transformer. On the assumption of ideal components, the lossless electrical converter model depicted in Fig. 1(b) can be used to investigate the DAB converter; there, the full bridges and the HF transformer are replaced by the respective voltage sources v_{ac1} and $n\,v_{\mathrm{ac2}}$.

A. DAB Conduction Losses

The lossless model of the DAB [see Fig. 1(b)] assumes a negligible magnetizing rms current I_{m} of the HF transformer, i.e., $I_{\mathrm{m}} \ll I_L$ (with I_{m} being referred to side 1). This is typically given for magnetic transformer cores. Moreover, the impact of additional HF losses, caused by current harmonics, is neglected. Both assumptions are most often used for investigations of the DAB converter, e.g., in [2], [17], [24], and allow for a practically reasonable estimate of I_L.

Based on these assumptions and according to [4], the total conduction losses of all MOSFETs are

$$P_{\mathrm{cond}} = 4R_{\mathrm{DS(on),HV}}\left(\frac{I_L}{\sqrt{2}}\right)^2 + 4n^2R_{\mathrm{DS(on),LV}}\left(\frac{I_L}{\sqrt{2}}\right)^2 \propto I_L^2 \tag{3}$$

($R_{\mathrm{DS(on),HV}}$ denotes the on-state resistances of the MOSFETs T_1, T_2, T_3, and T_4 and $R_{\mathrm{DS(on),LV}}$ denotes the on-state resistances of the MOSFETs T_5, T_6, T_7, and T_8). The copper losses generated in the inductor windings and in the transformer windings are

$$P_{\mathrm{cu}} = R_L(f_{\mathrm{S}})I_L^2 + R_{\mathrm{tr,HV}}(f_{\mathrm{S}})I_L^2 + n^2R_{\mathrm{tr,LV}}(f_{\mathrm{S}})I_L^2 \propto I_L^2 \tag{4}$$

(R_L: ac resistance of the inductor, $R_{\mathrm{tr,HV}}$: ac resistance of the HV winding of the transformer, $R_{\mathrm{tr,LV}}$: ac resistance of the LV winding of the transformer; all ac resistances are determined at the switching frequency).

According to (3) and (4), the conduction and copper losses generated in the DAB converter shown in Fig. 1(a) are proportional to the square of the inductor rms current, I_L^2. As a consequence, minimum I_L leads to minimum conduction and copper losses.

B. Operating Modes of the DAB

The two full bridge circuits employed can generate 12 different voltage patterns, regarding the different sequences of rising and falling edges of v_{ac1} and v_{ac2}; Fig. 2 depicts examples for all of these 12 patterns, for discrete phase angles $\varphi = 0,\ 45°,\ 90°,\ 135° \ldots -90°,\ -45°$, and for selected duty cycles D_1 and D_2. With respect to the search toward the modulation scheme with minimum inductor rms current I_L; however, only the patterns 1a, 1b, 2, 3b, 7b, and 8 are considered since the remaining six patterns, 3a, 4, 5a, 5b, 6, and 7a, lead to an increased inductor rms current and do not result in a higher DAB power transfer capability. Patterns 3a and 7a obviously cause the rms current value of i_L to increase, e.g., regarding Fig. 2(c): the transferred power remains constant if the duration of the time interval $t_1 - t_2$ changes; however, the rms value I_L becomes smaller for decreasing $t_1 - t_2$, since the current during $t_1 < t < t_2$ considerably increases the total rms current. The remaining patterns 4, 5a, 5b, and 6 employ $90° < |\varphi| < 180°$; this also causes unnecessarily high rms currents I_L. The fundamental frequency approach, often used to investigate the DAB (e.g., in [21]), can be used to analyze this property of the DAB. The normalized fundamental frequency components of $v_{\mathrm{AC1}}(t)$, $v_{\mathrm{AC2}}(t)$, and $i_L(t)$ are

$$\overline{V}_{1,\sim} = 4\overline{V}_1\sin(\pi D_1)/\pi \tag{5}$$

$$\overline{V}_{2,\sim} = 4\overline{V}_2\sin(\pi D_2)\mathrm{e}^{-\mathrm{j}\varphi}/\pi \tag{6}$$

$$\overline{I}_{L,\sim} = \frac{\overline{V}_{1,\sim} - \overline{V}_{2,\sim}}{\mathrm{j}}. \tag{7}$$

The active power,

$$\overline{P} = \mathrm{Re}(\overline{V}_{1,\sim}\overline{I}^*_{L,\sim}) = \mathrm{Re}(\overline{V}_{2,\sim}\overline{I}^*_{L,\sim}) = \sin(\varphi)|\overline{V_{1,\sim}}||\overline{V_{2,\sim}}| \tag{8}$$

is proportional to $\sin(\varphi)$ and thus shows a maximum for $|\varphi| = 90°$. The rms value of the fundamental component

$$|\overline{I}_{L,\sim}|^2 = |\overline{V_{1,\sim}}|^2 + |\overline{V_{2,\sim}}|^2 - 2\cos(\varphi)|\overline{V_{1,\sim}}||\overline{V_{2,\sim}}| \tag{9}$$

however, is minimal for $\varphi = 0$ and increases for increasing $|\varphi|$. Thus, $90° < |\varphi| < 180°$ would cause a reduced power transfer and a high rms current $|\overline{I}_{L,\sim}|$.

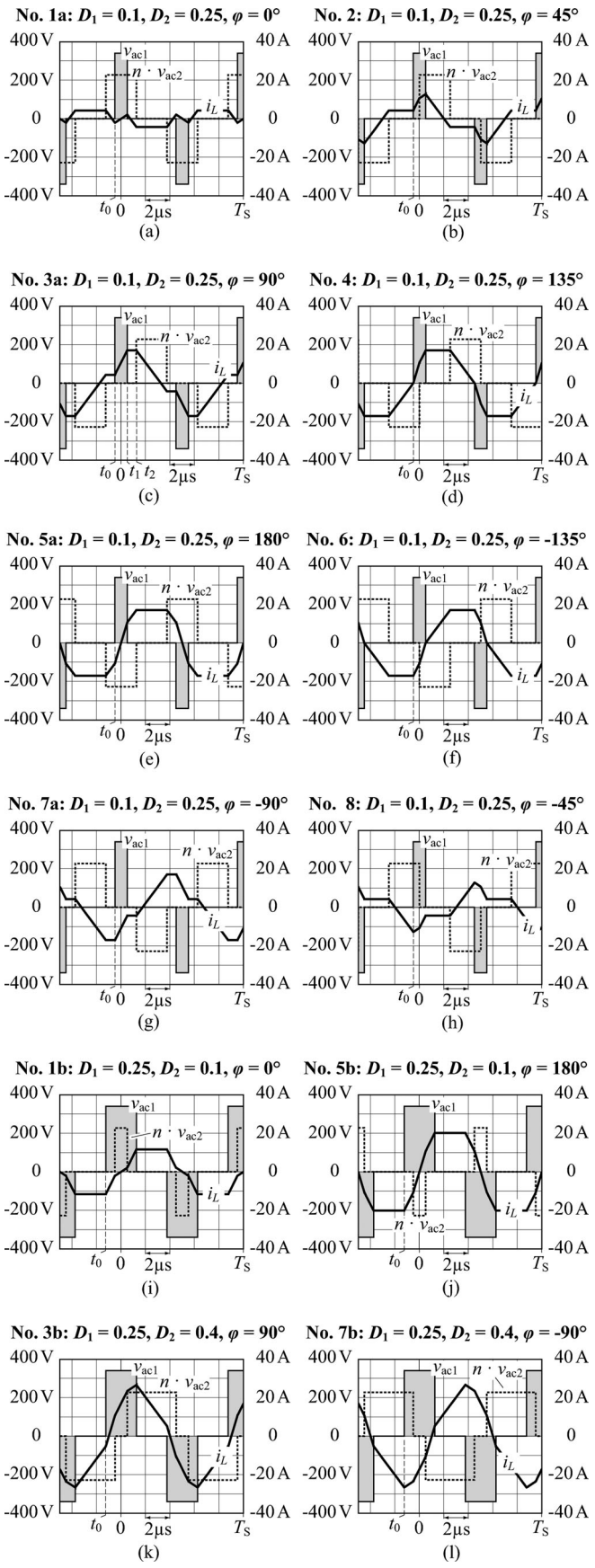

Fig. 2. Twelve basic voltage patterns generated with the two full bridges; $V_1 = 340\,\mathrm{V}$, $V_2 = 12\,\mathrm{V}$, $L = 26.7\,\mu\mathrm{H}$, $n = 19$, and $f_\mathrm{S} = 100\,\mathrm{kHz}$.

TABLE I
CONTROL PARAMETER RELATIONS FOR ACHIEVING THE RESPECTIVE VOLTAGE PATTERNS

Pattern	*Condition*
1a	$D_1 - D_2 < \varphi_{1a}/\pi < -D_1 + D_2$
1b	$-D_1 + D_2 < \varphi_{1b}/\pi < \quad D_1 - D_2$
2	$\lvert D_1 - D_2\rvert < \quad \varphi_2/\pi < \min\left[D_1 + D_2, 1 - (D_1 + D_2)\right]$
8	$\lvert D_1 - D_2\rvert < -\varphi_8/\pi < \min\left[D_1 + D_2, 1 - (D_1 + D_2)\right]$
3b	$1 - (D_1 + D_2) < \quad \varphi_{3b}/\pi < D_1 + D_2$
7b	$1 - (D_1 + D_2) < -\varphi_{7b}/\pi < D_1 + D_2$

TABLE II
REQUIRED PHASE SHIFT ANGLES φ FOR A GIVEN POWER $\overline{P}$

Pattern	φ
1a	$\varphi_{1a} = \frac{\overline{P}}{2D_1\overline{V}_1\overline{V}_2}$
1b	$\varphi_{1b} = \frac{\overline{P}}{2D_2\overline{V}_1\overline{V}_2}$
2	$\varphi_2 = \pi\left(D_1 + D_2 - 2\sqrt{D_1D_2 - \frac{\overline{P}}{2\pi\overline{V}_1\overline{V}_2}}\right)$
8	$\varphi_8 = -\pi\left(D_1 + D_2 - 2\sqrt{D_1D_2 + \frac{\overline{P}}{2\pi\overline{V}_1\overline{V}_2}}\right)$
3b	$\varphi_{3b} = \pi\left[\frac{1}{2} - \sqrt{D_1(1-D_1) + D_2(1-D_2) - \frac{1}{4} - \frac{\overline{P}}{\pi\overline{V}_1\overline{V}_2}}\right]$
7b	$\varphi_{7b} = -\pi\left[\frac{1}{2} - \sqrt{D_1(1-D_1) + D_2(1-D_2) - \frac{1}{4} + \frac{\overline{P}}{\pi\overline{V}_1\overline{V}_2}}\right]$

The voltage pattern, which is active for a given set of control parameters D_1, D_2, and φ, is determined using the conditions listed in Table I (most of these conditions are presented in [22]; there, however, the control parameters are defined differently).

Table II lists the expressions used to calculate the phase angles, φ_{1a}, φ_{1b}, φ_2, φ_{3b}, φ_{7b}, and φ_8, at a certain power level $\overline{P}$, for given operating voltages $\overline{V_1}$, $\overline{V_2}$, and for the duty cycles D_1, D_2. The calculation of these expressions can be divided into the three steps given below.

1) The steady-state value of the inductor current, $\bar{i}_L(t_0)$, needs to be calculated at a certain instant, e.g., at $t = t_0$ in Fig. 2; the calculation of this steady state value assumes that the inductor current repeats with reverse sign after each half cycle, i.e., $\bar{i}_L(t_0) = -\bar{i}_L(t_0 + T_\mathrm{S}/2)$.
2) The average port current,

$$\overline{I}_{1,\mathrm{avg}} = \frac{2}{T_\mathrm{S}}\int_{t_0}^{t_0+T_\mathrm{S}/2} \bar{i}_{\mathrm{FB1}}(t)\mathrm{d}t \tag{10}$$

and the power $\overline{P} = \overline{P}_1 = \overline{V}_1\overline{I}_{1,\mathrm{avg}}$ are calculated in a second step.
3) $\overline{P}$ needs to be reformulated with respect to φ in a last step.

An example of this calculation is presented in [24] for the three-phase DAB; however, the calculation principle is the same for the single-phase DAB.

TABLE III
EXPRESSIONS FOR THE INDUCTOR RMS CURRENT $\overline{I}_L$

Seq.	*Normalized inductor rms current* $\overline{I}_L$
All	$\overline{I}_L = \pi \sqrt{D_1^2 \overline{V}_1^2 \left(1 - \frac{4}{3} D_1\right) + D_2^2 \overline{V}_2^2 \left(1 - \frac{4}{3} D_2\right) + \frac{\overline{V}_1 \overline{V}_2}{3} e_{\mathrm{rms}}}$
1a	$e_{\mathrm{rms}} = 6 D_1 \left[\frac{\varphi^2}{\pi^2} + \left(D_2 \left(D_2 - 1\right) + \frac{D_1^2}{3}\right)\right]$
1b	$e_{\mathrm{rms}} = 6 D_2 \left[\frac{\varphi^2}{\pi^2} + \left(D_1 \left(D_1 - 1\right) + \frac{D_2^2}{3}\right)\right]$
2, 8	$e_{\mathrm{rms}} = D_1^3 + 3 D_1^2 \left(D_2 - \frac{\lvert\varphi\rvert}{\pi}\right) + \left(D_2 - \frac{\lvert\varphi\rvert}{\pi}\right)^3 + 3 D_1 \left[\frac{\varphi^2}{\pi^2} - D_2 \left(2 - \frac{2\lvert\varphi\rvert}{\pi} - D_2\right)\right]$
3b, 7b	$e_{\mathrm{rms}} = \left(1 - \frac{2\lvert\varphi\rvert}{\pi}\right) \left\{1 - \frac{\lvert\varphi\rvert}{\pi} + \frac{\varphi^2}{\pi^2} - 3 \left[D_1 \left(1 - D_1\right) + D_2 \left(1 - D_2\right)\right]\right\}$

The interim value e_{rms} is needed to evaluate the expression given in the first line, under "All"; e_{rms} depends on the pattern number.

The implemented algorithm, which is used to calculate the rms current $\overline{I}_L$ for a given set of input parameters $\overline{V}_1$, $\overline{V}_2$, $\overline{P}$, D_1, and D_2, first calculates all phase angles of Table II and then evaluates the conditions listed in Table I in order to determine the active voltage pattern (if a complex phase angle results then the respective voltage pattern is disregarded). It can be shown that only a single pattern is valid at a certain operating point, i.e., ambiguities are avoided. The active voltage pattern determines the phase angle φ,

$$\varphi = \begin{cases} \varphi_{1\mathrm{a}} & \text{if pattern 1a is active} \\ \varphi_{1\mathrm{b}} & \text{if pattern 1b is active} \\ \varphi_{2} & \text{if pattern 2 is active} \\ \varphi_{3\mathrm{b}} & \text{if pattern 3b is active} \\ \varphi_{7\mathrm{b}} & \text{if pattern 7b is active} \\ \varphi_{8} & \text{if pattern 8 is active.} \end{cases} \tag{11}$$

The normalized inductor rms current, $\overline{I}_L$, which occurs at the given operating point and for given D_1, D_2, and φ, is finally calculated with Table III, using the expression that corresponds to the active voltage pattern determined before. The calculation of $\overline{I}_L$,

$$\overline{I}_L^2 = \frac{2}{T_{\mathrm{S}}} \int_{t_0}^{t_0 + T_{\mathrm{S}}/2} \overline{i}_L^2(t) \mathrm{d}t \tag{12}$$

is similar to the calculation of $\overline{I}_{1,\mathrm{avg}}$ discussed earlier.

III. OPTIMAL MODULATION SCHEME

The calculation of the optimal control parameters, $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ_{opt}, takes the complete operating range of the DAB into account, which is limited according to

$$V_1 > 0 \ \wedge \ V_2 > 0 \ \wedge \ -P_{\max} \le P \le P_{\max}. \tag{13}$$

It can be shown that the maximum power transfer capability of the DAB, $P_{\max}$, is achieved with CPM at $\varphi = \pi/2$:

$$\overline{P}_{\max} = \frac{\pi \overline{V}_1 \overline{V}_2}{4}, \quad P_{\max} = \frac{n V_1 V_2}{8 f_{\mathrm{S}} L}. \tag{14}$$

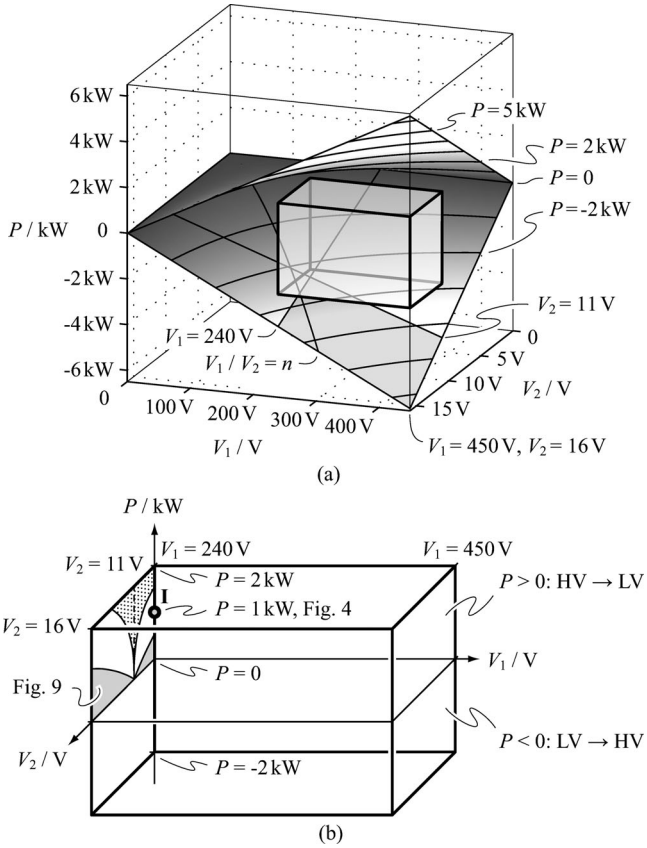

Fig. 3. (a) Volume between the upper and the lower surfaces, calculated with (13) and (14), defines the complete operating range of the DAB with $n = 19$ and $L = 26.7\,\mu$H; (b) operating range of the DAB converter specified in Section I, i.e., $240\,\mathrm{V} \le V_1 \le 450\,\mathrm{V}$, $11\,\mathrm{V} \le V_2 \le 16\,\mathrm{V}$, and $-2\,\mathrm{kW} \le P \le 2\,\mathrm{kW}$, defines a cubical shaped volume. The operating point I, $V_1 = 240\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$, and $P = 1\,\mathrm{kW}$, is used to exemplify the optimization procedure used in Section III. The surface defined with $V_1 = 240\,\mathrm{V}$, $11\,\mathrm{V} \le V_2 \le 16\,\mathrm{V}$, $-2\,\mathrm{kW} \le P \le 2\,\mathrm{kW}$ depicts the different operating modes of the DAB needed to achieve minimum inductor rms current (cf., Fig. 9). The results presented for $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ_{opt} (see Section III-B) facilitate minimum inductor rms current within the complete operating range of the DAB.

The sign of P denotes the direction of the power transfer:

$$P > 0 : \mathrm{HV} \rightarrow \mathrm{LV}, \qquad P < 0 : \mathrm{LV} \rightarrow \mathrm{HV}. \tag{15}$$

Fig. 3(a) depicts the surfaces $P_{\max}(V_1, V_2)$ and $-P_{\max}(V_1, V_2)$ calculated for the DAB used ($n = 19$, $L = 26.7\,\mu$H; see Section IV-B). All operating points possible with the DAB are located inside these two surfaces. Furthermore, the operating range specified in Section I, i.e., $240\,\mathrm{V} \le V_1 \le 450\,\mathrm{V}$, $11\,\mathrm{V} \le V_2 \le 16\,\mathrm{V}$, and $-2\,\mathrm{kW} \le P \le 2\,\mathrm{kW}$, defines a cube-shaped volume, which is completely inside the volume of all possible operating points.

The operating point $V_1 = 240\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$, and $P = 1\,\mathrm{kW}$, marked with I in Fig. 3(b), is used to exemplify the optimization procedure employed. Different values for D_1 and D_2 can be used to achieve the designated power transfer at the given port voltages; the different voltage patterns that are active for different duty cycles D_1 and D_2 (calculated with the use of Table II and Table I) are shown in Fig. 4(a). Fig. 4(a) also shows that the

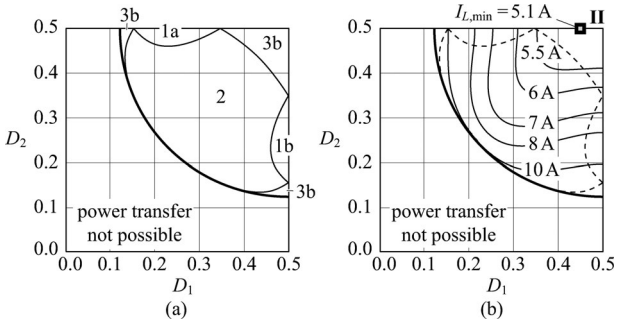

Fig. 4. (a) Employed voltage patterns and (b) inductor rms currents at $V_1 = 240\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$, and $P = 1\,\mathrm{kW}$ [operating point **I** in Fig. 3(b)], plotted against D_1 and D_2; at $D_1 = 0.45$ and $D_2 = 0.5$ (marked with II) minimum inductor rms current, $I_{L,\min} = 5.1\,\mathrm{A}$ is achieved. The required power transfer cannot be accomplished if D_1 and D_2 fall below a certain limit. DAB parameters: $n = 19$, $L = 26.7\,\mu\mathrm{H}$, $f_\mathrm{S} = 100\,\mathrm{kHz}$.

required power transfer cannot be accomplished if D_1 and /or D_2 fall below a certain limit. Fig. 4(b) depicts the inductor rms currents $I_L(D_1, D_2)$ at $V_1 = 240\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$, and $P = 1\,\mathrm{kW}$, calculated with the expressions given in Table III. The calculated surface $I_L(D_1, D_2)$ shows a single minimum, $I_{L,\min} = 5.1A$, at $D_{1,\mathrm{opt}} = 0.45$ and $D_{2,\mathrm{opt}} = 0.5$ [marked with II in Fig. 4(b)].

Thus, the analytic expressions for $\overline{I}_L$ facilitate the calculation of optimal control parameters with respect to minimal $\overline{I}_L$ within $0 \le D_1 \le 0.5$ and $0 \le D_2 \le 0.5$ and for a given operating point, i.e., for constant $\overline{V}_1$, $\overline{V}_2$, and $\overline{P}$:

$$\overline{I}_{L,\min} = \min[\overline{I}_L(\overline{V}_1, \overline{V_2}, \overline{P}, D_1, D_2, \varphi(\overline{V}_1, \overline{V_2}, \overline{P}, D_1, D_2))] \quad \forall \quad 0 \le D_1 \le 0.5 \wedge 0 \le D_2 \le 0.5. \tag{16}$$

The phase angle φ is adjusted according to the expressions listed in Table II and (11) in order to maintain a constant power $\overline{P}$.

Analytical solutions for the optimal control parameters $D_{1,\mathrm{opt}}, D_{2,\mathrm{opt}}$, and φ_opt are not directly feasible and a numerical minimum search is used to calculate $D_{1,\mathrm{opt}}, D_{2,\mathrm{opt}}$, and φ_opt in a first step. A close inspection of the results obtained from the numerical minimum search, detailed in Section III-A, reveals that overall three different modulation strategies are required to achieve minimal I_L within the complete operating range of the DAB. These three modulation strategies and closed-form solutions for $D_{1,\mathrm{opt}}, D_{2,\mathrm{opt}}$, and φ_opt are presented in Section III-B.

A. Numerical Optimization with Respect to Minimum I_L

In a first step, different operating points have been analyzed in order to find $D_{1,\mathrm{opt}}$ and $D_{2,\mathrm{opt}}$ within wide voltage and power ranges. The results of this numerical search are summarized below.[3]

1) Optimal Modulation at Low Power Levels: Fig. 5(a) depicts the resulting values of I_L at a relatively low power level

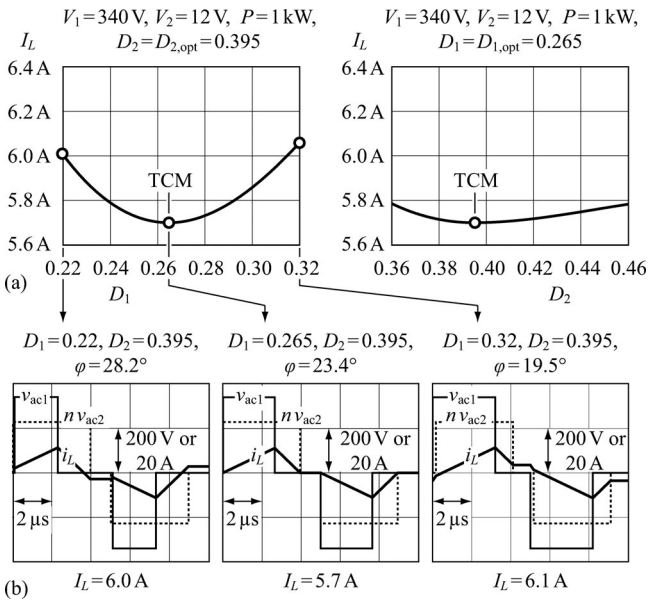

Fig. 5. (a) Values of I_L close to its minimum at $D_{1,\mathrm{opt}} = 0.265$, $D_{2,\mathrm{opt}} = 0.395$ ($V_1 = 340\,\mathrm{V}$, $V_2 = 12\,\mathrm{V}$, $P = 1\,\mathrm{kW}$, $n = 19$, $L = 26.7\,\mu\mathrm{H}$, and $f_\mathrm{S} = 100\,\mathrm{kHz}$). Minimum I_L is achieved with TCM (on the assumption that φ is adjusted in order to achieve constant power transfer). (b) Voltage and current waveforms related to the three operating points marked in Fig. 5(a) to illustrate the impact of the change of D_1 on the converter waveforms. Obviously, the current during the freewheeling time interval increases, which causes the total rms current I_L to increase.

of $P = 1\,\mathrm{kW}$ at $V_1 = 340\,\mathrm{V}$ and $V_2 = 12\,\mathrm{V}$, calculated for different D_1 and D_2 (φ is adjusted in order to maintain a constant power transfer). Minimum I_L is achieved at $D_{1,\mathrm{opt}} = 0.265$ and $D_{2,\mathrm{opt}} = 0.395$, which leads to a triangular transformer current [see Fig. 5(b)]. Based on the inspection of numerous different operating points it has been found that the *triangular current mode modulation (TCM)* scheme presented in [21] yields minimal I_L at low power levels.

Fig. 6(a) depicts typical waveforms of $v_{\mathrm{ac}1}$, $v_{\mathrm{ac}2}$, and i_L. There, the shape of the inductor current is triangular during $0 < t < t_2$ and i_L is zero during the subsequent time interval $t_2 < t < T_\mathrm{S}/2$. TCM can be realized with pattern 2 [HV $\rightarrow$ LV, Fig. 2(b)] or pattern 8 [LV $\rightarrow$ HV, Fig. 2(h)].

The two reasons for TCM being optimal with respect to minimum I_L are

1) A full bridge circuit only transfers power between its dc port and the HF transformer if it remains in the active state, i.e., for $v_{\mathrm{ac}1} = \pm V_1$ on the HV side and for $v_{\mathrm{ac}2} = \pm V_2$ on the LV side. Thus, both full bridges should remain in their active states for as long as possible in order to transfer as much active power as possible with as low currents as possible.
2) The optimal modulation scheme needs to minimize circulating inductor currents in order to achieve low rms inductor currents. Thus, the instantaneous powers p_1 and p_2 generated by each full bridge should be positive:

$$p_1(t) = v_{\mathrm{ac}1}(t) i_L(t) \ge 0 \ \vee \ p_2(t) = v_{\mathrm{ac}2}(t) i_L(t) \ge 0. \tag{17}$$

[3]The presented results have been successfully tested for $n = 19$ and $L = 26.7\,\mu\mathrm{H}$ and within $200\,\mathrm{V} \le V_1 \le 500\,\mathrm{V}$, $11\,\mathrm{V} \le V_2 \le 26\,\mathrm{V}$, and $20W \le P \le 2\,\mathrm{kW}$ for $11 \times 11 \times 11 = 1331$ different operating points. The employed input data array uses equally spaced voltage and power values. Three different search algorithms have been used to test the results: Nelder–Mead, differential evolution, and random search.

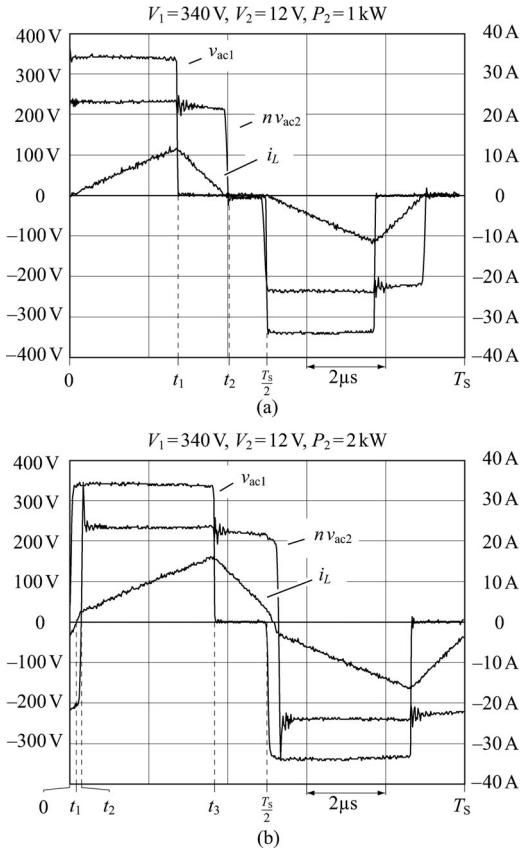

Fig. 6. Measured voltage and current waveforms obtained with the optimal modulation scheme for (a) $V_1 = 340\,\mathrm{V}, V_2 = 12\,\mathrm{V}, P_2 = 1\,\mathrm{kW}$ and (b) $V_1 = 340\,\mathrm{V}, V_2 = 12\,\mathrm{V}, P_2 = 2\,\mathrm{kW}$; $n = 19$, $L = 26.7\,\mu\mathrm{H}$, and $f_\mathrm{S} = 100\,\mathrm{kHz}$.

TCM satisfies both items listed earlier. However, a reduced duration of its active time interval, i.e., $D_2 < D_1$ in Fig. 6(a), is unavoidable, since the slopes $\mathrm{d}i_L/\mathrm{d}t$ are given for given port voltages V_1, V_2 and given hardware parameters n and L of the DAB. Thus, TCM yields minimum I_L, even though $i_L(t)$ shows discontinuous characteristics (see Fig. 5). A further reduction of I_L could be achieved by increasing L or by increasing f_S. The adaptation of L to the actual operating point; however, is difficult to implement and a variable switching frequency is often undesirable.

The closed-form expressions for D_1 and D_2 of TCM are known [21] and are given in Section III-B1.

2) Optimal Modulation at Medium Power Levels: The maximum power feasible with TCM is exceeded at a certain power level [21]; this power level is termed $\overline{P}_{\triangle,\max}$ and is given with (22) in this paper. A possible extension to higher power operation is the trapezoidal current mode modulation scheme presented in [21]. There, negative instantaneous powers p_1 and p_2 are avoided. The results obtained from the numerical optimization, however, suggest either pattern 3b (power is transferred from the HV port to the LV port) or pattern 7b (LV port to HV port) to be used, instead. The numerical optimization procedure further selects $D_{1,\mathrm{opt}}$ or $D_{2,\mathrm{opt}}$ equal to 0.5, depending on the ratio $V_1/(nV_2)$: $D_{1,\mathrm{opt}} = 0.5\ \forall\ V_1 \le nV_2$ and $D_{2,\mathrm{opt}} = 0.5\ \forall\ V_1 \ge nV_2$. Fig. 6(b) shows a typical i_L time behaviour corresponding to this modulation scheme and Fig. 7 shows the resulting values of I_L for D_1 and D_2 around the optimum for $V_1 = 340\,\mathrm{V}$, $V_2 = 12\,\mathrm{V}$, $P = 2\,\mathrm{kW}$. The characteristics of $I_L(D_1, D_2)$ is relatively flat and thus, rms currents close to the minimum are still achieved if D_1 and D_2 are selected within some range around $D_{1,\mathrm{opt}}$ and $D_{2,\mathrm{opt}}$.

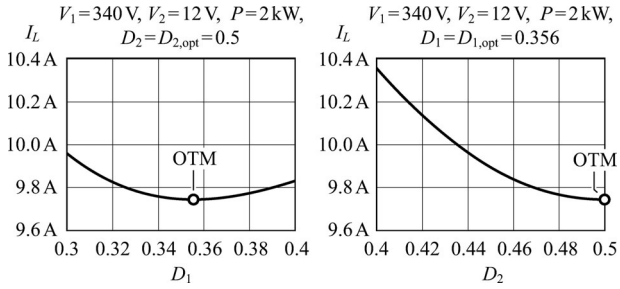

Fig. 7. Values of I_L close to its minimum at medium power levels ($V_1 = 340\,\mathrm{V}$, $V_2 = 12\,\mathrm{V}$, $P = 2\,\mathrm{kW}$, $n = 19$, $L = 26.7\,\mu\mathrm{H}$, and $f_\mathrm{S} = 100\,\mathrm{kHz}$). Minimum I_L is achieved with OTM.

Thus, according to the results obtained from the numerical optimization, minimum inductor rms current is achieved at medium power levels, $|\overline{P}| > \overline{P}_{\triangle,\max}$, if the duration of the active time interval of one full bridge is maximal, i.e., $D_1 = 0.5$ or $D_2 = 0.5$. With this, however, negative instantaneous powers p_1 and p_2 must be accepted, e.g., in Fig. 6(b), p_1 is negative during $0 < t < t_1$ and p_2 is negative during $t_1 < t < t_2$.

The modulation parameters needed for this modulation scheme, termed *optimal transition mode modulation (OTM)*, are obtained from

$$\text{mode 3b, } V_1 \ge nV_2 : \frac{\mathrm{d}\left(I_L|_{D_2=0.5}\right)}{\mathrm{d}D_1} = 0 \Leftrightarrow D_1 = D_{1,\mathrm{opt}} \tag{18}$$

$$\text{mode 3b, } V_1 \le nV_2 : \frac{\mathrm{d}\left(I_L|_{D_1=0.5}\right)}{\mathrm{d}D_2} = 0 \Leftrightarrow D_2 = D_{2,\mathrm{opt}} \tag{19}$$

for power being transferred from the HV port to the LV port. If power is transferred from the LV port to the HV port then mode 3b needs to be replaced by mode 7b in (18) and (19).

3) Optimal Modulation at High Power Levels: At high power levels, the duty cycle $D_{1,\mathrm{opt}}$ or $D_{2,\mathrm{opt}}$, calculated with (18) or (19), exceeds the value 0.5. There the numerical optimization procedure selects $D_{1,\mathrm{opt}} = D_{2,\mathrm{opt}} = 0.5$, i.e., *CPM*. Fig. 8 shows the resulting values of I_L for D_1 and D_2 around the optimum. The characteristics of $I_L(D_1, D_2)$ is relatively flat and thus, rms currents close to the minimum are still achieved if D_1 and D_2 are selected within some range around $D_{1,\mathrm{opt}}$ and $D_{2,\mathrm{opt}}$. However, I_L starts to increase rapidly if D_1 and /or D_2 fall below a certain limit (e.g., $D_1 < 0.42$ in Fig. 8), since the respective phase angle φ, required to maintain a constant power transfer, approaches $\pi/2$.

B. Closed-Form Solutions for $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ_opt

For given $\overline{V}_1$ and $\overline{V}_2$ the power $\overline{P}$ determines the actual modulation scheme needed to obtained minimum I_L:

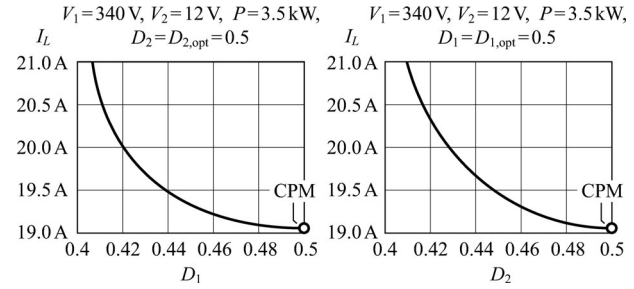

Fig. 8. Values of I_L close to its minimum at high power levels ($V_1 = 340\,\mathrm{V}$, $V_2 = 12\,\mathrm{V}$, $P = 2.6\,\mathrm{kW}$, $n = 19$, $L = 26.7\,\mu\mathrm{H}$, and $f_\mathrm{S} = 100\,\mathrm{kHz}$). Minimum I_L is achieved with CPM.

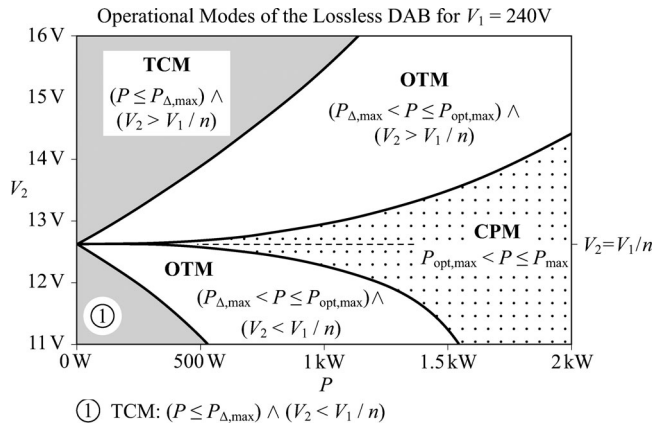

Fig. 9. DAB operating modes for $V_1 = 240\,\mathrm{V}$, different voltages V_2, and positive output power levels P, $n = 19$, and $L = 26.7\,\mu\mathrm{H}$; cf., Fig. 3(b). This Figure is mirrored with respect to the P-axis if negative power levels, $P < 0$, are used.

1) TCM for $|\overline{P}| \le \overline{P}_{\triangle,\max}$: (21), [21];
2) OTM for $\overline{P}_{\triangle,\max} < |\overline{P}| \le \overline{P}_{\mathrm{opt},\max}$: (23), (24);
3) CPM for $\overline{P}_{\mathrm{opt},\max} < |\overline{P}| \le \overline{P}_{\max}$: (26).

The expressions needed to calculate $\overline{P}_{\triangle,\max}$ and $\overline{P}_{\mathrm{opt},\max}$ are given in Sections III-B1 and III-B2, respectively; $\overline{P}_{\max}$ is defined with (14). Fig. 9 depicts the modulation schemes employed for $V_1 = 240\,\mathrm{V}$, different voltages V_2, and different output power levels P for the DAB converter used ($n = 19$, $L = 26.7\,\mu\mathrm{H}$, $f_\mathrm{S} = 100\,\mathrm{kHz}$).

Due to the symmetry of the converter model depicted in Fig. 1(b), similar expressions result for $\overline{V}_1 > \overline{V}_2$ and for $\overline{V}_1 < \overline{V}_2$. In order to reduce the number of equations needed to fully describe the optimal modulation scheme, $\overline{V}_1$, $\overline{V}_2$, $D_{1,\mathrm{opt}}$, and $D_{2,\mathrm{opt}}$ are replaced by $\overline{V}_\mathrm{A}$, $\overline{V}_\mathrm{B}$, D_A, and D_B according to

$$\begin{aligned}&\left[\overline{V}_\mathrm{A}\ \overline{V}_\mathrm{B}\ D_\mathrm{A}\ D_\mathrm{B}\right]^\mathrm{T}\\ &= \begin{cases}\left[\overline{V}_1\ \overline{V}_2\ D_{1,\mathrm{opt}}\ D_{2,\mathrm{opt}}\right]^\mathrm{T} & \forall\ \overline{V}_1 \le \overline{V}_2\\ \left[\overline{V}_2\ \overline{V}_1\ D_{2,\mathrm{opt}}\ D_{1,\mathrm{opt}}\right]^\mathrm{T} & \forall\ \overline{V}_1 > \overline{V}_2.\end{cases}\end{aligned} \tag{20}$$

With this simple transformation $\overline{V}_\mathrm{A} \le \overline{V}_\mathrm{B}$ always applies.

Fig. 10 summarizes the complete procedure used to calculate $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ. This flow chart is in close accordance to the discussions given in Sections III-B1, III-B2, and III-B3, below.

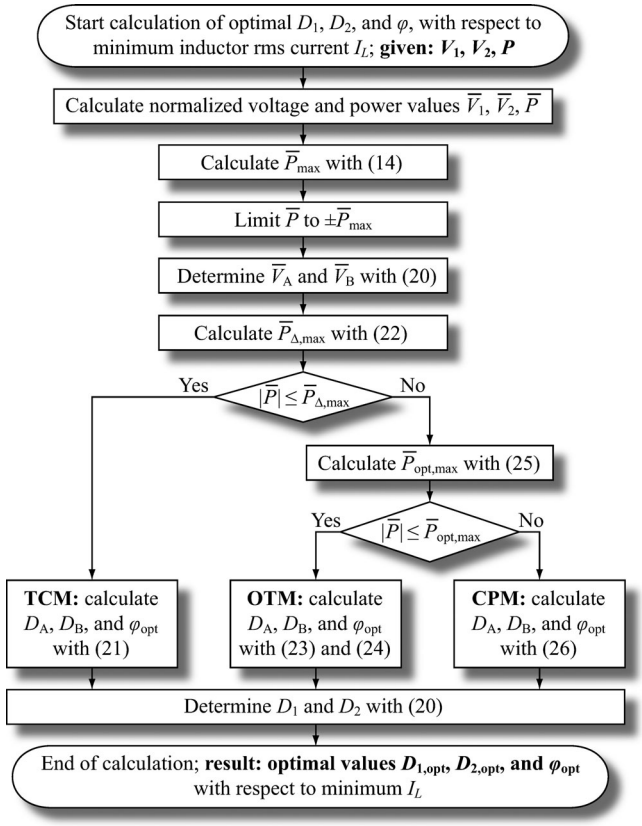

Fig. 10. Procedure to calculate the optimal control parameters using closed-form expressions for $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ.

1) Low Power; Triangular Current Mode Modulation (TCM): TCM is extensively discussed in [21], typical waveforms of v_{ac1}, v_{ac2}, and i_L are depicted in Fig. 6(a). The respective inductor current can be divided into 2 time intervals: an active time interval, characterized by a triangular shape of $i_L(t)$, and a freewheeling time interval with $i_L(t) = 0$ [e.g., $0 < t < t_2$ and $t_2 < t < T_\mathrm{S}/2$ in Fig. 6(a), respectively]. The expressions needed to calculate the respective modulation parameters are

$$\left.\begin{aligned}\varphi_\mathrm{opt} &= \pi\,\mathrm{sgn}(\overline{P})\sqrt{\frac{\overline{V}_\mathrm{B}-\overline{V}_\mathrm{A}}{2\overline{V}_\mathrm{A}^2\,\overline{V}_\mathrm{B}}\,\frac{|\overline{P}|}{\pi}}\\ D_\mathrm{A} &= \frac{|\varphi_\mathrm{opt}|}{\pi}\,\frac{\overline{V}_\mathrm{B}}{\overline{V}_\mathrm{B}-\overline{V}_\mathrm{A}}\\ D_\mathrm{B} &= \frac{|\varphi_\mathrm{opt}|}{\pi}\,\frac{\overline{V}_\mathrm{A}}{\overline{V}_\mathrm{B}-\overline{V}_\mathrm{A}}\end{aligned}\right\}\ \forall\ |\overline{P}| \le \overline{P}_{\triangle,\max}. \tag{21}$$

The duration of the freewheeling time interval decreases with increasing $\overline{P}$ and becomes zero at the maximum possible output power of TCM:

$$\overline{P}_{\triangle,\max} = \frac{\pi}{2}\,\frac{\overline{V}_\mathrm{A}^2\,(\overline{V}_\mathrm{B}-\overline{V}_\mathrm{A})}{\overline{V}_\mathrm{B}}. \tag{22}$$

2) Medium Power; Optimal Transition Mode Modulation (OTM): $D_\mathrm{A} = 0.5$ and a large expression for D_B result from (19) for power levels $|\overline{P}|$ between $\overline{P}_{\triangle,\max}$ and $\overline{P}_{\mathrm{opt},\max}$

($e_1 \ \ldots \ e_8$ denote interim values): [4]

$$
\begin{aligned}
e_1 &= -\frac{2\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2}{\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2} \\
e_2 &= \frac{\overline{V}_{\mathrm{A}}^3 \overline{V}_{\mathrm{B}} + \frac{|\overline{P}|}{\pi}\left(\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)}{\overline{V}_{\mathrm{A}}^3 \overline{V}_{\mathrm{B}} + \overline{V}_{\mathrm{A}} \overline{V}_{\mathrm{B}}^3} \\
e_3 &= 8\overline{V}_{\mathrm{A}}^7 \overline{V}_{\mathrm{B}}^5 - 64\frac{|\overline{P}|^3}{\pi^3}\left(\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)^3 \\
&\quad - \frac{|\overline{P}|}{\pi}\overline{V}_{\mathrm{A}}^4 \overline{V}_{\mathrm{B}}^2 \left(4\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)\left(4\overline{V}_{\mathrm{A}}^2 + 13\overline{V}_{\mathrm{B}}^2\right) \\
&\quad + 16\frac{\overline{P}^2}{\pi^2}\overline{V}_{\mathrm{A}}\left(\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)^2\left(4\overline{V}_{\mathrm{A}}^2 \overline{V}_{\mathrm{B}} + \overline{V}_{\mathrm{B}}^3\right) \\
e_4 &= 8\overline{V}_{\mathrm{A}}^9 \overline{V}_{\mathrm{B}}^3 - 8\frac{|\overline{P}|^3}{\pi^3}\left(8\overline{V}_{\mathrm{A}}^2 - \overline{V}_{\mathrm{B}}^2\right)\left(\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)^2 \\
&\quad - 12\frac{|\overline{P}|}{\pi}\overline{V}_{\mathrm{A}}^6 \overline{V}_{\mathrm{B}}^2\left(4\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right) \\
&\quad + 3\frac{\overline{P}^2}{\pi^2}\overline{V}_{\mathrm{A}}^3 \overline{V}_{\mathrm{B}}\left(4\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)\left(8\overline{V}_{\mathrm{A}}^2 + 5\overline{V}_{\mathrm{B}}^2\right) \\
&\quad + \left(\frac{3|\overline{P}|}{\pi}\right)^{\frac{3}{2}} \overline{V}_{\mathrm{A}}\overline{V}_{\mathrm{B}}^2\sqrt{e_3} \\
e_5 &= \left\{2\overline{V}_{\mathrm{A}}^6 \overline{V}_{\mathrm{B}}^2 + 2\frac{|\overline{P}|}{\pi}\left(4\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)\left[\frac{|\overline{P}|}{\pi}\left(\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)\right.\right. \\
&\quad \left.\left. - \overline{V}_{\mathrm{A}}^3 \overline{V}_{\mathrm{B}}\right]\right\}\left[3\overline{V}_{\mathrm{A}}\overline{V}_{\mathrm{B}}\left(\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)(e_4)^{\frac{1}{3}}\right]^{-1} \\
e_6 &= \frac{4\left(\overline{V}_{\mathrm{A}}^3 \overline{V}_{\mathrm{B}}^2 + 2\overline{V}_{\mathrm{A}}^5\right) + 4\frac{|\overline{P}|}{\pi}\left(\overline{V}_{\mathrm{A}}^2 \overline{V}_{\mathrm{B}} + \overline{V}_{\mathrm{B}}^3\right)}{\overline{V}_{\mathrm{A}}\left(\overline{V}_{\mathrm{A}}^2 + \overline{V}_{\mathrm{B}}^2\right)^2} \\
e_7 &= \frac{(e_4)^{\frac{1}{3}}}{6\overline{V}_{\mathrm{A}}^3 \overline{V}_{\mathrm{B}} + 6\overline{V}_{\mathrm{A}}\overline{V}_{\mathrm{B}}^3} + \frac{e_1^2}{4} - \frac{2e_2}{3} + e_5 \\
e_8 &= \frac{1}{4}\left(\frac{-e_1^3 - e_6}{\sqrt{e_7}} + 3e_1^2 - 8e_2 - 4e_7\right)
\end{aligned}
$$

$$
\left.
\begin{aligned}
D_{\mathrm{A}} &= \frac{1}{2} \\
D_{\mathrm{B}} &= \frac{1}{4}\left(2\sqrt{e_7} - 2\sqrt{e_8} - e_1\right)
\end{aligned}
\right\} \forall\, \overline{P}_{\triangle,\max} < |\overline{P}| < \overline{P}_{\mathrm{opt,max}}. \tag{23}
$$

[4] According to Section III-A and Fig. 4 OTM uses either mode 3b or mode 7b. Moreover, $D_1 = 0.5$ or $D_2 = 0.5$ applies. Result (23) is thus obtained together with (20) by differentiating $\overline{I}_L$ (using e_{RMS} of the last entry of Table III and $D_1 = 0.5$) with respect to D_2 and by equating this expression to zero. The resulting equation then needs to be reformulated with respect to D_2, which is a rather extensive calculation and has been carried out with a software tool, e.g., Mathematica or Maple.

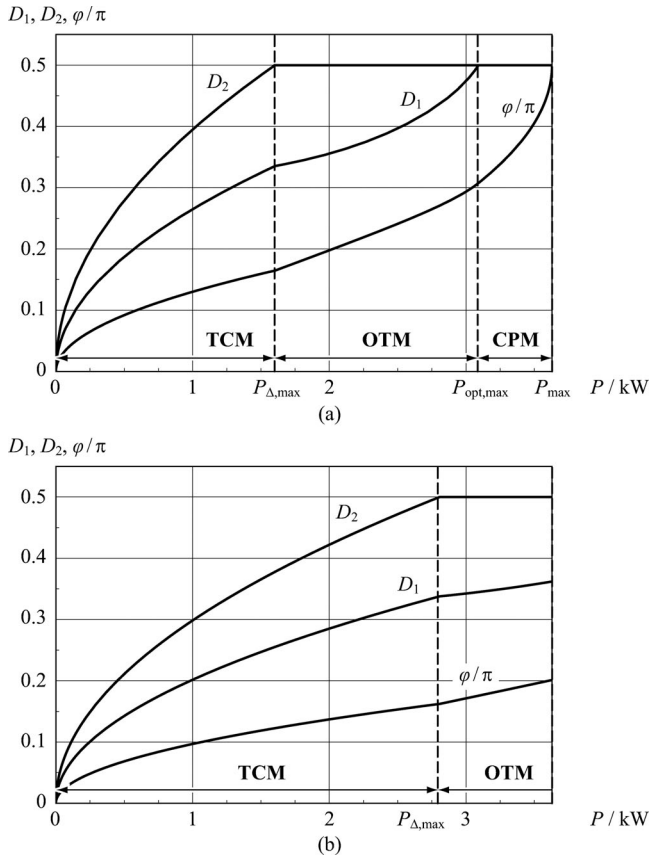

Fig. 11. (a) Optimal control parameters $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ_{opt}, which minimize the inductor rms current for $V_1 = 340\,\mathrm{V}$ and $V_2 = 12\,\mathrm{V}$: TCM is optimal at low power levels and CPM is optimal at high power levels. OTM minimizes the inductor rms current at medium power levels. (b) $D_{1,\mathrm{opt}}$, $D_{2,\mathrm{opt}}$, and φ_{opt} for $V_1 = 450\,\mathrm{V}$ and $V_2 = 16\,\mathrm{V}$: again, TCM is optimal at power levels considerably lower than $P_{\max}$ ($P_{\max} = 6.4\,\mathrm{kW}$ at $V_1 = 450\,\mathrm{V}$ and $V_2 = 16\,\mathrm{V}$); however, due to the increased port voltage levels, $P_{\triangle,\max}$ is equal to $2.8\,\mathrm{kW}$ and thus, TCM is employed at rated power ($P = 2\,\mathrm{kW}$). DAB parameters: $n = 19$, $L = 26.7\,\mu\mathrm{H}$, $f_{\mathrm{S}} = 100\,\mathrm{kHz}$.

The respective phase angle is calculated according to Table II:

$$
\begin{aligned}
\varphi_{\mathrm{opt}} &= \pi\,\mathrm{sgn}(\overline{P}) \\
&\cdot \left[\frac{1}{2} - \sqrt{D_{\mathrm{A}}\left(1 - D_{\mathrm{A}}\right) + D_{\mathrm{B}}\left(1 - D_{\mathrm{B}}\right) - \frac{1}{4} - \frac{|\overline{P}|}{\pi\overline{V}_{\mathrm{A}}\overline{V}_{\mathrm{B}}}}\right].
\end{aligned} \tag{24}
$$

The duty cycle D_{B} increases with increasing $\overline{P}$ and reaches $D_{\mathrm{B}} = 0.5$ at $\overline{P}_{\mathrm{opt,max}}$. However, no closed-form solution has been found for $\overline{P}_{\mathrm{opt,max}}$; therefore, a numerical solver is used to determine $\overline{P}_{\mathrm{opt,max}}$:

$$
\begin{aligned}
\overline{P}_{\mathrm{opt,max}} :\ D_{\mathrm{B}}(\overline{P}_{\mathrm{opt,max}}) &= \frac{1}{2} \ \wedge\ \overline{P}_{\triangle,\max} \\
&< \overline{P}_{\mathrm{opt,max}} \leq \overline{P}_{\max}
\end{aligned} \tag{25}
$$

whereas the values $\overline{P}_{\triangle,\max}$ and $\overline{P}_{\max}$ define upper and lower limits used for the numerical solver algorithm. The value of $\overline{P}_{\mathrm{opt,max}}$ depends on $\overline{V}_1$ and $\overline{V}_2$ (cf., Fig. 9). The calculation of P can also be described based on Fig. 11(a) (there, $D_1 = D_{\mathrm{B}}$ applies): starting at $P = P_{\triangle,\max}$ the value of D_1 increases

with increasing P and eventually reaches $D_1 = 0.5$. There, $P = P_{\mathrm{opt,max}}$ applies.

3) High Power; CPM: CPM is used at high power levels. The respective modulation parameters are

$$\left.\begin{aligned} \varphi_{\mathrm{opt}} &= \pi\,\mathrm{sgn}(\overline{P})\left[\frac{1}{2} - \sqrt{\frac{1}{4} - \frac{|\overline{P}|}{\pi \overline{V}_{\mathrm{A}} \overline{V}_{\mathrm{B}}}}\right] \\ D_{\mathrm{A}} &= \frac{1}{2} \\ D_{\mathrm{B}} &= \frac{1}{2} \end{aligned}\right\} \quad \forall\, \overline{P}_{\mathrm{opt,max}} < |\overline{P}| \wedge |\overline{P}| \leq \overline{P}_{\max}. \quad (26)$$

In order to avoid complex values for φ_{opt}, $\overline{P}$ needs to be limited to $\overline{P}_{\max}\,\mathrm{sgn}(\overline{P})$, whereas $\overline{P}_{\max}$ is given with (14). Moreover, (14) limits the inductance L of a DAB converter with a maximum rated power $P_{\max}$ according to

$$L \leq \frac{\min(V_1)\min(n\,V_2)}{8 f_{\mathrm{S}} P_{\max}}. \quad (27)$$

C. Example for $V_1 = 340\,\mathrm{V}$ and $V_2 = 12\,\mathrm{V}$

Fig. 11(a) depicts D_1, D_2, and φ at $V_1 = 340\,\mathrm{V}$, $V_2 = 12\,\mathrm{V}$, and for different power levels. Reduced duty cycle values $D_1 < 0.5$ and $D_2 < 0.5$ result for $P < P_{\triangle,\max}$; the duty cycle D_2 becomes equal to 0.5 at $P = P_{\triangle,\max}$. OTM is used within $P_{\triangle,\max} < P \leq P_{\mathrm{opt,max}}$, i.e., D_1 is calculated with (23). At power levels exceeding $P_{\mathrm{opt,max}}$, CPM is used ($D_1 = D_2 = 0.5$). The given equations facilitate continuous characteristics of D_1, D_2, and φ. It is important to note that the actual values of $P_{\triangle,\max}$, $P_{\mathrm{opt,max}}$, and $P_{\max}$, needed to distinguish between low, medium, and high power levels, depend on V_1 and V_2; e.g., for $V_1 = 450\,\mathrm{V}$ and $V_2 = 16\,\mathrm{V}$, depicted in Fig. 11(b), TCM is employed at rated power, $P = 2\,\mathrm{kW}$, since $P_{\triangle,\max}$ is equal to $2.8\,\mathrm{kW}$, there.

D. Theoretical Results

Fig. 12 shows different inductor rms currents I_L, calculated according to the expressions listed in Table III. Fig. 12(a) depicts I_L for CPM at $P = 1\,\mathrm{kW}$: at $V_1 = 450\,\mathrm{V}$ and $V_2 = 11\,\mathrm{V}$ a maximum rms current of $13.5\,\mathrm{A}$ results. The optimal modulation scheme reduces the maximum rms current to $6.7\,\mathrm{A}$ [see Fig. 12(b): $V_1 = 450\,\mathrm{V}$ and $V_2 = 11\,\mathrm{V}$]: as a consequence, the conduction losses, which are proportional to I_L^2 for the given converter, are reduced by 75%.

Similar results are obtained at rated power, $P = 2\,\mathrm{kW}$: with CPM the maximum inductor rms current is 14.9 A at $V_1 = 450\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$ [see Fig. 12(c)], whereas the optimal modulation scheme achieves a maximum I_L of 11.3 A at $V_1 = 450\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$ [see Fig. 12(d)]. The optimized modulation scheme thus facilitates a 42% reduction of the maximum conduction losses at rated power.

Table IV compares the rms currents I_L achieved with recently published modulation schemes for different operating points.

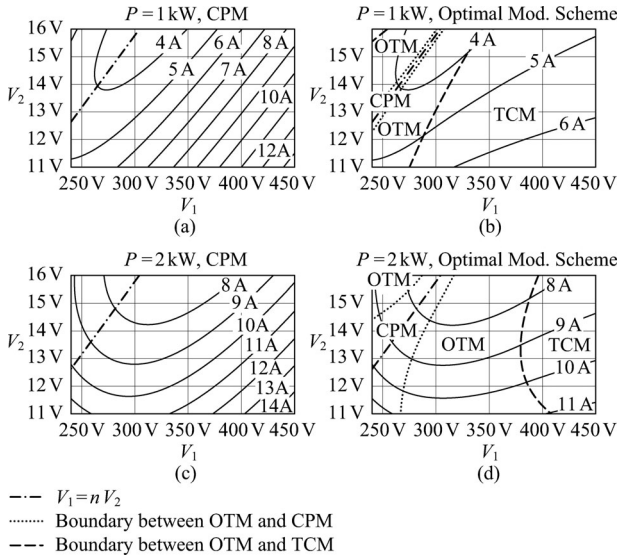

Fig. 12. Inductor rms currents, I_L, calculated with the expressions listed in Table III; (a) $P = 1\,\mathrm{kW}$, CPM; (b) $P = 1\,\mathrm{kW}$, optimal modulation scheme; (c) $P = 2\,\mathrm{kW}$, CPM; (d) $P = 2\,\mathrm{kW}$, optimal modulation scheme; considered hardware parameters: $n = 19$, $L = 26.7\,\mu\mathrm{H}$, and $f_{\mathrm{S}} = 100\,\mathrm{kHz}$.

Obviously, the dual-phase-shift control presented in [12], [23] causes comparably high rms currents, in particular at low-load conditions. This is mainly due to the selected phase angle of $\varphi = \pi/2$. Considerably reduced rms currents result with the modulation schemes presented in [22]: these modulation schemes are based on practical and intuitive considerations; still, D_1 and D_2 are close to the optimal values presented in this paper and thus almost the minimum values of I_L are achieved.[5] This is due to the fact that $I_L(D_1, D_2)$ shows a flat characteristics, i.e., I_L is close to its minimum for control parameters close to the optimum control parameters (cf., Figs. 7 and 8).

IV. Experimental Results

A. Practical Implementation

1) Digital Control Concept: Fig. 13 depicts the cascaded control structure employed to control V_2, i.e., for power being transferred from the HV port to the LV port. In the inner control loop, a current controller (PI-controller) controls the dc current I_1 and the modulator determines the control parameters needed for the DAB to generate the set current $I_{1,\mathrm{mod}}$ and the set power $P_{\mathrm{mod}} = V_{1,\mathrm{f}}\, I_{1,\mathrm{mod}}$. The outer control loop contains the voltage controller (PI-controller), which sets the output voltage V_2. Digital moving average filters are used to remove noise from V_1, V_2, and I_1. The realized DAB converter employs a single dc current sensor that measures I_1; the voltage controller, however, provides the value of the dc current needed at the LV port, $I_{2,\mathrm{ref}}$. Therefore, the additional arithmetic block shown in Fig. 13 is required to determine $I_{1,\mathrm{ref}} \approx I_{2,\mathrm{ref}} V_2 / V_1$ (on the assumptions of a lossless converter and slowly varying dc port voltages, i.e.,

[5] In the lower power regime TCM is proposed in [22] and thus, minimum I_L is achieved, there.

TABLE IV
RMS CURRENTS ACHIEVED WITH RECENTLY PUBLISHED MODULATION SCHEMES

Operating point (V_1, V_2, P)	*Control variables according to the cited literature*	*Respective D_1, D_2, and φ, according to Fig. 1(c)*	I_L	*Rel. difference to minimum I_L*
Dual-phase-shift (DPS) control [12], [23], $D_1 = 0.5$ (important: D_1 and D_2 defined in Fig. 2 in [12] are different to D_1 and D_2 used in this paper)				
300 V, 16 V, 2 kW	$D_1 = 0.5$, $D_2 = 0.484$	$\varphi = \pi/2$, $D_1 = 0.242$, $D_2 = 0.242$	$I_L = 15.9$ A	118%
300 V, 16 V, 500 W	$D_1 = 0.5$, $D_2 = 0.242$	$\varphi = \pi/2$, $D_1 = 0.121$, $D_2 = 0.121$	$I_L = 8.86$ A	420%
300 V, 11 V, 2 kW	$D_1 = 0.5$, $D_2 = 0.601$	$\varphi = \pi/2$, $D_1 = 0.300$, $D_2 = 0.300$	$I_L = 15.9$ A	51%
300 V, 11 V, 500 W	$D_1 = 0.5$, $D_2 = 0.292$	$\varphi = \pi/2$, $D_1 = 0.146$, $D_2 = 0.146$	$I_L = 8.97$ A	159%
300 V, 11 V, 2.68 kW	$D_1 = 0.5$, $D_2 = 0.791$	$\varphi = \pi/2$, $D_1 = 0.396$, $D_2 = 0.396$	$I_L = 18.6$ A	22%
Single H-Bridge PWM [22]				
300 V, 16 V, 2 kW	$\alpha_p = 0$, $\alpha_s = 0.041$, $\phi_f = 0.426$	$\varphi = 0.426$, $D_1 = 0.5$, $D_2 = 0.493$	$I_L = 7.31$ A	0.0%
300 V, 16 V, 500 W	$\alpha_p = 0$, $\alpha_s = 0.041$, $\phi_f = 0.095$	$\varphi = 0.095$, $D_1 = 0.5$, $D_2 = 0.493$	$I_L = 1.70$ A	0.0%
300 V, 11 V, 2 kW	$\alpha_p = 0.953$, $\alpha_s = 0$, $\phi_f = 0.823$	$\varphi = 0.823$, $D_1 = 0.348$, $D_2 = 0.5$	$I_L = 10.7$ A	1.4%
300 V, 11 V, 500 W	$\alpha_p = 0.953$, $\alpha_s = 0$, $\phi_f = 0.192$	$\varphi = 0.192$, $D_1 = 0.348$, $D_2 = 0.5$	$I_L = 4.18$ A	21%
300 V, 11 V, 2.68 kW	cannot be achieved with this modulation scheme			
Simultaneous Dual PWM of DAB, Composite Scheme [22]				
300 V, 16 V, 2 kW	$\alpha_p = 0$, $\alpha_s = 0.031$, $\phi_f = 0.426$	$\varphi = 0.426$, $D_1 = 0.5$, $D_2 = 0.495$	$I_L = 7.31$ A	0.0%
300 V, 16 V, 500 W	$\alpha_p = 0$, $\alpha_s = 0.039$, $\phi_f = 0.095$	$\varphi = 0.095$, $D_1 = 0.5$, $D_2 = 0.494$	$I_L = 1.70$ A	0.0%
300 V, 11 V, 2 kW	$\alpha_p = 0.708$, $\alpha_s = 0$, $\phi_f = 0.758$	$\varphi = 0.758$, $D_1 = 0.387$, $D_2 = 0.5$	$I_L = 10.6$ A	0.14%
300 V, 11 V, 500 W	$\alpha_p = 1.752$, $\alpha_s = 1.147$, $\phi_f = 0.302$	$\varphi = 0.302$, $D_1 = 0.221$, $D_2 = 0.317$	$I_L = 3.47$ A	0.0%
300 V, 11 V, 2.68 kW	$\alpha_p = 0.370$, $\alpha_s = 0$, $\phi_f = 1.146$	$\varphi = 1.146$, $D_1 = 0.441$, $D_2 = 0.5$	$I_L = 15.4$ A	0.94%

The operating points are selected such that the comparison considers $V_1 \approx nV_2$, $V_1 > nV_2$, and different power levels ($n = 19$, $L = 26.7\,\mu$H).

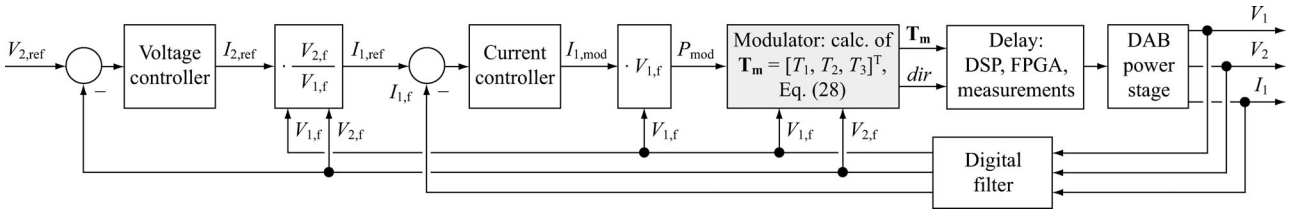

Fig. 13. Employed control structure including voltage and current control loops for power transfer from the LV to the HV port as well as the modulator function which calculates the required timing signals, $\mathbf{T_m} = [T_1,\ T_2,\ T_3]^{\mathrm{T}}$ [T_1, T_2, and T_3 are calculated with (28)]. Voltage and current controllers and the modulator reside in the DSP; the FPGA generates the gate signals for the MOSFETs of the DAB.

$V_1 \approx V_{1,\mathrm{f}}$ and $V_2 \approx V_{2,\mathrm{f}}$).[6] Details regarding the control of the employed DAB are presented in [10].

A DSP runs the voltage and current controllers, interfaces to current and voltage measurement peripherals (A/D converters), monitors overcurrent and overvoltage conditions in order to ensure safe converter operation, and communicates with a control pc, which is used to start and stop the DAB converter and to adjust the output voltage. The DSP as well calculates the control parameters, φ, D_1, and D_2, and interfaces to an FPGA that generates the dedicated gate signals. The employed gate signal generation unit, presented in Section IV-A3, requires the timing parameter vector $\mathbf{T_m} = [T_1, T_2, T_3]^{\mathrm{T}}$:

$$\varphi > 0: T_1 = \frac{D_1 - D_2 + \varphi/\pi}{2f_{\mathrm{S}}}, \quad T_2 = \frac{D_1}{f_{\mathrm{S}}}, \quad T_3 = \frac{D_2}{f_{\mathrm{S}}};$$
$$\varphi < 0: T_1 = \frac{D_2 - D_1 - \varphi/\pi}{2f_{\mathrm{S}}}, \quad T_2 = \frac{D_2}{f_{\mathrm{S}}}, \quad T_3 = \frac{D_1}{f_{\mathrm{S}}}. \tag{28}$$

[6]If power is transferred from the LV port to the HV port, the shown voltage controller needs to control V_1. In that case the arithmetic block connected in series to the voltage controller is not required, since the respective voltage controller directly outputs $I_{1,\mathrm{ref}}$.

The variable dir determines the direction of power transfer (it can be shown that the sign of P is equal to the sign of φ):

$$dir = \mathrm{sgn}(P_{\mathrm{mod}}) = \mathrm{sgn}(\varphi) = \begin{cases} +1: & \mathrm{HV} \rightarrow \mathrm{LV} \\ -1: & \mathrm{LV} \rightarrow \mathrm{HV}. \end{cases} \tag{29}$$

The employed DSP is a TMS320F2808 operated with a clock frequency of 100 MHz; the software is implemented in the computer language C. For the FPGA, the device LCMXO2280, operated with a clock frequency of 100 MHz, is employed; the hardware description language VHDL is used to program the FPGA.

2) On-line Calculation of the Modulation Parameters: The calculation of (23) and (25) requires elaborate calculations in order to determine the three-control parameters φ_{opt}, $D_{1,\mathrm{opt}}$, and $D_{2,\mathrm{opt}}$. With the given computational power of the DSP, on-line parameter calculation is not feasible. In order to still run the discussed optimal modulation method, the respective control parameters are calculated off-line for a set of basic values and stored in a table on the DSP. The controller software then uses linear interpolation to approximately determine the actual control parameter values.

Each control parameter depends on the current operating point, characterized by $V_{1,\mathrm{f}}$, $V_{2,\mathrm{f}}$, and P_{mod}: $\varphi_{\mathrm{opt}}(V_{1,\mathrm{f}}, V_{2,\mathrm{f}}, P_{\mathrm{mod}})$, $D_{1,\mathrm{opt}}(V_{1,\mathrm{f}}, V_{2,\mathrm{f}}, P_{\mathrm{mod}})$, and $D_{2,\mathrm{opt}}(V_{1,\mathrm{f}}, V_{2,\mathrm{f}}, P_{\mathrm{mod}})$.

TABLE V
POWER ERROR BY REASON OF THE LINEAR INTERPOLATION

$\max\|e_P\|$	Arithmetic mean of $\|e_P\|$	$\max\|e_{P,\mathrm{r}}\|$	Arithmetic mean of $\|e_{P,\mathrm{r}}\|$
CPM:			
44 W	2.7 W	1.8%	0.21%
Optimal modulation scheme:			
44 W	5.2 W	6.6%	0.68%

The error values are calculated according to (39) and (40), whereas the calculation of the relative error excludes zero power.

Consequently, a 3-D table is required for every control parameter to store the basic values and to facilitate the subsequent linear function interpolation. The employed interpolation algorithm is detailed in [25].

The currently used tables employ 16 basic values $V_{1,k}$ and $V_{2,l}$,

$$V_{1,k} = V_{1,\min} + k\frac{V_{1,\max} - V_{1,\min}}{15}, \quad k \in \mathbb{N}_0 \wedge k \leq 15 \quad (30)$$

$$V_{2,l} = V_{2,\min} + l\frac{V_{2,\max} - V_{2,\min}}{15}, \quad l \in \mathbb{N}_0 \wedge l \leq 15 \quad (31)$$

and 32 values P_m,

$$P_m = -P_{0,\max} + m\frac{2P_{0,\max}}{31}, \quad m \in \mathbb{N}_0 \wedge m \leq 31. \quad (32)$$

The tables are calculated for a slightly enlarged operating range in order to avoid extrapolation during transient operation:

$$V_{1,\min} = 200\,\mathrm{V}, \quad V_{1,\max} = 490\,\mathrm{V} \quad (33)$$

$$V_{2,\min} = 10\,\mathrm{V}, \quad V_{2,\max} = 17\,\mathrm{V} \quad (34)$$

$$P_{0,\max} = 2.5\,\mathrm{kW}. \quad (35)$$

In total, the tables for D_1, D_2, and φ require $3 \times 16^2 \times 32 = 24576$ memory cells; this fits into the on-chip flash memory of the TMS320F2808.

Depending on the operating point, the transferred power may deviate from the set power by reason of the linear interpolation. The maximum power errors occur approximately in the middle between eight adjacent basic values and therefore

$$V_{1,\mathrm{e},k} = \frac{V_{1,k} + V_{1,k+1}}{2}, \quad k \in \mathbb{N}_0 \wedge 0 \leq k < 15 \quad (36)$$

$$V_{2,\mathrm{e},l} = \frac{V_{2,l} + V_{2,l+1}}{2}, \quad l \in \mathbb{N}_0 \wedge 0 \leq l < 15, \text{ and} \quad (37)$$

$$P_{\mathrm{e},m} = \frac{P_{\mathrm{e},m} + P_{\mathrm{e},m+1}}{2}, \quad m \in \mathbb{N}_0 \wedge 0 \leq m < 31 \quad (38)$$

are considered in order to calculate the absolute and relative errors:

$$e_P(V_{1,\mathrm{e},k}, V_{2,\mathrm{e},l}, P_{\mathrm{e},m}) = P - P_{\mathrm{i}}(V_{1,\mathrm{e},k}, V_{2,\mathrm{e},l}, P_{\mathrm{e},m}) \quad (39)$$

$$e_{P,\mathrm{r}}(V_{1,\mathrm{e},k}, V_{2,\mathrm{e},l}, P_{\mathrm{e},m}) = \frac{e_P(V_{1,\mathrm{e},k}, V_{2,\mathrm{e},l}, P_{\mathrm{e},m})}{P} \quad (40)$$

(P_{i} denotes the power calculated with the interpolated control parameters determined at $V_{1,\mathrm{e},k}$, $V_{2,\mathrm{e},l}$, and $P_{\mathrm{e},m}$; the calculation of the relative error excludes zero power). Table V summarizes the errors calculated for the different modulation schemes. The maximum absolute error is 44 W; with the optimal modulation scheme, a maximum relative error of 6.6% occurs. The error due to the linear interpolation causes an error in the output current if the DAB is operated open loop. With the use of a current controller, as shown in Fig. 13, $I_{1,\mathrm{mod}}$ and P_{mod} are adjusted such that the difference between the reference current and the measured current becomes smaller; a PI current controller eliminates the steady state difference between I_1 and $I_{1,\mathrm{ref}}$.

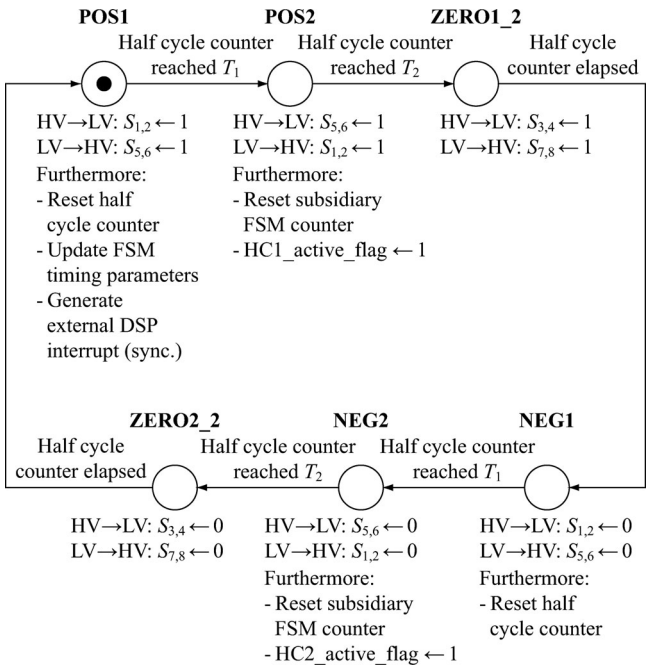

Fig. 14. Master state machine: employed for the DAB to control three out of four half-bridge state machines (see Fig. 16). The fourth half-bridge is controlled with the additional state machine depicted in Fig. 15, since those particular switching commands may occur after the half cycle has elapsed, e.g., in Fig. 6(b). It is important to note, that the assignments related to each state are only performed at the instant the FSM enters the respective state.

3) Flexible Gate Signal Generation Unit: The voltage patterns required for the different modulation schemes demand for a highly flexible gate signal generation unit. The gate signal generation is therefore performed with finite state machines (FSMs) being executed in an FPGA; this approach allows for very high flexibility regarding the generation of different gate signal pulse patterns.

The gate signal generation unit consists of six different state machines: the master FSM (see Fig. 14) and its supporting subsidiary FSM (see Fig. 15) control for subordinate FSMs which in turn generate the gate signals (see Fig. 16).

Let us assume, that the state "POS1" of the master FSM becomes active with the configured direction of power transfer being "HV → LV." The FPGA thus resets the half cycle counter (required in order to detect the end of the half cycle), updates the FSM timing parameters, and generates an external DSP interrupt to synchronize the digital control part implemented on the DSP to the gate signal generation unit. It further sets the switch signal $S_{1,2}$ to 1 which triggers the half bridge FSM assigned to T_1 and T_2 (see Fig. 16 with $i = 1$ and $j = 2$). At

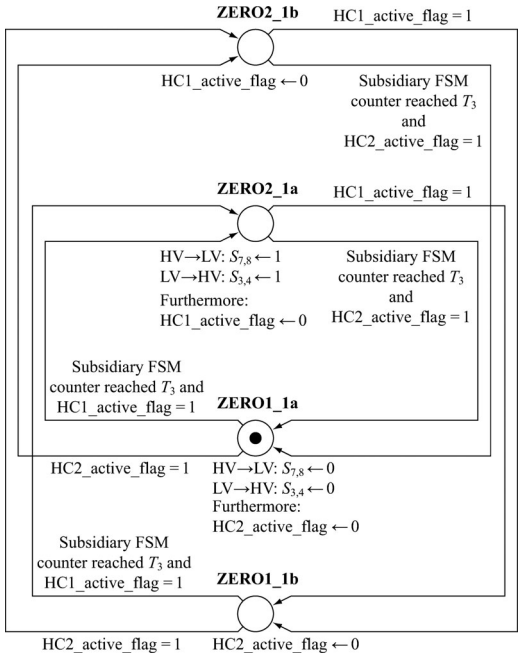

Fig. 15. Subsidiary part of the master state machine depicted in Fig. 14; controls the state machine of the fourth half-bridge (HV → LV: T_7, T_8; LV → HV: T_3, T_4). This additional state machine is required, since the switching action of the fourth half-bridge may occur after the half-cycle in the master state machine has elapsed. Therefore, the control of the fourth half-bridge needs to be decoupled from the master state machine [e.g., to generate the waveform shown in Fig. 6(b)]. The state machine uses the variables HC1_active_flag and HC2_active_flag to prevent failure modes during unsteady converter operation.

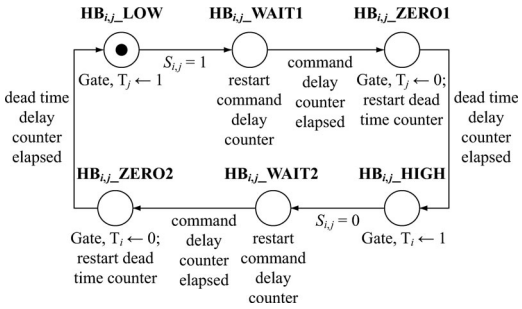

Fig. 16. State machine $\mathrm{HB}_{i,j}$ employed to generate the gate signals of a single half bridge (inclusive command delay and dead time interval generation). The indices i and j denote the indices of the MOSFETs' reference designators given in Fig. 1). The FPGA runs four of these state machines, i.e., $\mathrm{HB}_{1,2}$, $\mathrm{HB}_{3,4}$, $\mathrm{HB}_{5,6}$, and $\mathrm{HB}_{7,8}$, in parallel.

the time the half cycle counter reaches the value T_1, the master FSM changes its state to "POS2," triggers the half-bridge FSM assigned to T_5 and T_6, and resets an independent counter used to control the subsidiary FSM (see Fig. 15). In order to avoid an erroneous switching sequence, a flag indicating the current half cycle, HC1_active_flag, is set (see Fig. 14). As soon as the half-cycle counter reaches the value T_2, the half-bridge FSM assigned to T_3 and T_4 is triggered. The master state machine starts with the second half-cycle at the instant the half-cycle counter reaches the value $T_\mathrm{S}/2$.

The use of the independent subsidiary state machine enables the time T_3 to range from 0 to $T_\mathrm{S}/2$. With the extension to both power transfer directions, as shown in Fig. 14 and Fig. 15, the proposed architecture allows us to reproduce all required voltage patterns needed to realize the optimal modulation scheme.

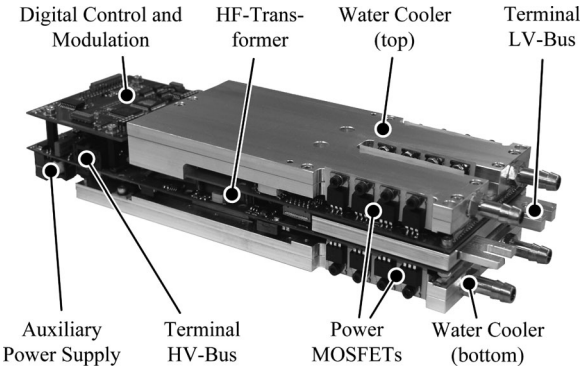

Fig. 17. 2 kW automotive DAB converter ($273\,\mathrm{mm} \times 90\,\mathrm{mm} \times 53\,\mathrm{mm}$); rated voltage transfer ratio: $V_1 = 340\,\mathrm{V}$ and $V_2 = 12\,\mathrm{V}$.

The use of independent state machines for each half bridge finally allows for the switching signals $S_{i,j}$ to be delayed individually in order to compensate for different switching time delays caused by the semiconductor switches.

B. Experimental Results

The experimental results are obtained from the DAB hardware prototype depicted in Fig. 17. This DAB is realized for an automotive application and enables bidirectional power transfer between the HV power train and the LV dc bus (LV battery, LV ancillary loads) of a fuel cell car [1], [4]. Its voltage and power ratings are given in Section I and its basic technical data are listed below.

1) PCB: four layer PCB, 200 μm copper on each layer.
2) LV side:
   a) Dc capacitor: 96 × 10 μF/25 V/X5R in parallel,
   b) Switches: 8 × IRF2804 in parallel.
3) HV side:
   a) Dc capacitor: 6 × 470 nF/630 V in parallel.
   b) Switches: SPW47N60CFD (CoolMOS).
4) Transformer core: two planar E58 cores.
5) Transformer turns ratio and DAB converter inductance: $n = 19$: 1, L = 26.7 μH.
6) Switching frequency: f_S =100 kHz.

The switching frequency is selected in order to obtain a highly compact converter and n and L are determined with respect to maximum converter efficiency and for CPM being used [26]; the design procedure, e.g., as presented in [26]–[28], is beyond the scope of this paper. Moreover, the DAB could be operated more efficiently with the optimal modulation scheme if different values of n and L would be used [26]. However, for the measurements solely $n = 19$ and $L = 26.7\,\mu$H have been used in order to allow for a meaningful comparison.

The efficiency results obtained with this hardware prototype are used to illustrate the improvements achieved with the optimal modulation scheme compared to CPM. The efficiency measurement includes conduction and switching losses of the semiconductor switches, copper and core losses of the HF transformer and the DAB inductor, and the power needed for the gate

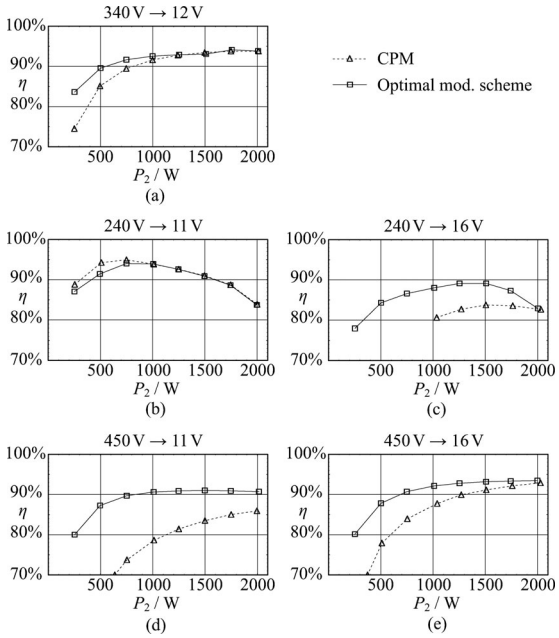

Fig. 18. Converter efficiencies measured for CPM (△) and for the optimal modulation scheme detailed in Section III (□): (a) $V_1 = 340\,\mathrm{V}$, $V_2 = 12\,\mathrm{V}$, (b) $V_1 = 240\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$, (c) $V_1 = 240\,\mathrm{V}$, $V_2 = 16\,\mathrm{V}$, (d) $V_1 = 450\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$, and (e) $V_1 = 450\,\mathrm{V}$, $V_2 = 16\,\mathrm{V}$; power is transferred from the HV port to the LV port; employed DAB converter: $n = 19$ and $L = 26.7\,\mu\mathrm{H}$; the efficiency measurement is carried out at an ambient temperature of $T_\mathrm{A} = 25\,^\circ\mathrm{C}$.

drivers and for the digital control platform.[7] Fig. 18 depicts the efficiencies measured at different operating voltages V_1 and V_2, different output power levels P_2, and for power being transferred to the LV port; dashed lines mark CPM operation, solid lines mark the operation with the optimal modulation scheme (all efficiencies have been measured at room temperature, $T_\mathrm{A} = 25\,^\circ\mathrm{C}$).

The overview of the different operating modes employed for the optimal modulation scheme (see Fig. 9) reveals that TCM and OTM are typically employed for $V_1/(nV_2) \ll 1$ or $V_1/(nV_2) \gg 1$ and at low-power levels; CPM is the optimal choice at $V_1/(nV_2) \approx 1$. Thus, considerably increased converter efficiency is observed in Fig. 18 for $V_1/(nV_2) \ll 1$ or $V_1/(nV_2) \gg 1$, e.g., in Fig. 18(c) $[V_1/(nV_2) = 0.79]$ or Fig. 18(d) $[V_1/(nV_2) = 2.2]$, respectively. Moreover, the efficiency increases for most operating voltages at reduced power levels, i.e., $P_2 < 1.5\,\mathrm{kW}$ in Fig. 18. However, operation with CPM may lead to a higher efficiency at certain operating points, e.g., at $P_2 = 500\,\mathrm{W}$ in Fig. 18(b), since the presented optimal modulation scheme disregards loss components other than conduction and copper losses (e.g., switching losses).

The efficiency of the converter drops to values below 85% at rated power and at two operating voltages:

1) $V_1 = 240\,\mathrm{V}$, $V_2 = 11\,\mathrm{V}$, and $P_2 = 2\,\mathrm{kW}$ [see Fig. 18(c)]: at minimum input and output voltages a large phase angle is required and therefore I_L is comparably large. This could be avoided by reducing L, which, however, causes an increase of I_L for most other operating points.
2) $V_1 = 240\,\mathrm{V}$, $V_2 = 16\,\mathrm{V}$, and $P_2 = 2\,\mathrm{kW}$ [see Fig. 18(e)]: there, the LV full bridge generates high switching losses, which is not considered by the presented modulation scheme. Possible improvements are discussed in [26].

[7]The use of reduced duty cycles $D_1 < 0.5$ and $D_2 < 0.5$ facilitates a reduction of the transformer's and the inductor's core losses [22]. Thus, the optimal modulation scheme achieves a reduction of the transformer's and the inductor's core losses at low power levels when compared to CPM.

V. Conclusion

This paper presents the general closed-form solutions for the modulation parameters D_1, D_2, and φ of an optimal modulation scheme, which achieves minimum inductor and transformer rms currents for a DAB converter. As a consequence, minimal conduction and copper losses are achieved. The given closed-form expressions can be directly used for a given DAB converter. The presented modulation scheme is thus useful during the first stage of a systematic design process of the DAB converter, to determine the current and voltage stresses of the converter's power components, and facilitates the design and /or selection of most suitable power components. In this context a converter model, e.g., according to [4], [29], needs to be implemented in order to predict the different component losses and to dimension the heat sink. In a final step optimal values of n and L (e.g., with respect to maximum average efficiency) may be determined using the design procedure presented in [26].

The practical value of this modulation scheme is demonstrated for a bidirectional, automotive DAB converter with a low voltage/high current port and a rated power of $2\,\mathrm{kW}$: the converter efficiency is measured for the conventional CPM and the optimal modulation strategy at different operating points. The efficiency considerably increases for most operating voltages at reduced output power levels, $P < 1.5\,\mathrm{kW}$. The achieved improvement is most distinct at $V_1 = 450\,\mathrm{V}$ and $V_2 = 11\,\mathrm{V}$: there, the efficiency increases from 78.6% to 90.6% at $1\,\mathrm{kW}$ output power and from 85.9% to 90.7% at $2\,\mathrm{kW}$ output power. The optimal modulation scheme is thus most useful for DAB converters which are operated within wide input and output voltage ranges.

The proposed modulation scheme is optimal with respect to minimal inductor rms current. Even though, the presented optimization procedure does not consider the switching properties of the DAB, it can be shown that ZVS is achieved for medium and high power levels, $|\overline{P}| > \overline{P}_{\triangle,\max}$. At low power levels, however, switching operations with zero inductor current, i.e., $i_L = 0$, cause increased switching losses on the HV side [4], [26]. Thus, future investigations may focus on the properties of this modulation scheme regarding switching losses and possible improvements with respect to the extension of the ZVS operating range.

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Florian Krismer (S'05) received the M.Sc. degree (Hons) from the University of Technology Vienna, Vienna, Austria, in 2004 and the Ph.D. degree from the Power Electronic Systems Laboratory (PES), Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland, in 2011.

He is currently a Postdoctoral Fellow at PES. His research interests include the analysis, design, and optimization of high-current and high-frequency power converters.

Johann W. Kolar (S'89–M'91–SM'04–F'10) received the M.Sc. and Ph.D. degrees (*summa cum laude*/*promotio sub auspiciis praesidentis rei publicae*) from the University of Technology Vienna, Vienna, Austria.

He is currently a Full Professor of Power Electronics at the Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland, and the Chair of the ETH Power Electronic Systems Laboratory. He has proposed numerous novel converter topologies and modulation/control concepts, e.g., the VIENNA rectifier, the Swiss rectifier, and the three-phase ac–ac sparse matrix converter. In this context, he has published more than 400 scientific papers and has filed more than 80 patents. His current research interests include ac–ac and ac–dc converter topologies with low effects on the mains, solid-state transformers for smart microgrids, ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC and GaN), power supply on chip systems, multidomain/scale modeling/simulation and multiobjective optimization, pulsed power, and ultra-high speed and bearingless motors.

He has received numerous Best Paper Awards of IEEE Transactions and IEEE Conferences and initiated and/or is the founder/co-founder of four ETH Spin-off companies. He is a member of the Steering Committees of several leading international conferences in the field and serves as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, the *Journal of Power Electronics of the Korean Institute of Power Electronics* and as an Editorial Advisory Board Member of the *IEEJ Transactions on Electrical and Electronic Engineering*.