Power Electronic Systems
Laboratory

IEEE Transactions on Power Electronics, Vol. 28, No. s2, pp. 899-907, February 2013

Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications

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Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications

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***Abstract*—The demand for lightweight converters with high control performance and low acoustic noise led to an increase in switching frequencies of hard switched two-level low-voltage 3-phase converters over the last years. For high switching frequencies, converter efficiency suffers and can be kept high only by employing cost intensive switch technology such as SiC diodes or CoolMOS switches; therefore, conventional IGBT technology still prevails. In this paper, the alternative of using three-level converters for low-voltage applications is addressed. The performance and the competitiveness of the three-level T-type converter ($3LT^2C$) is analyzed in detail and underlined with a hardware prototype. The $3LT^2C$ basically combines the positive aspects of the two-level converter such as low conduction losses, small part count and a simple operation principle with the advantages of the three-level converter such as low switching losses and superior output voltage quality. It is, therefore, considered to be a real alternative to two-level converters for certain low-voltage applications.**

***Index Terms*—High efficiency, three-level converter, T-type converter.**

I. Introduction

EFFICIENT energy conversion in the low-voltage range has gained more and more attention. Applications such as photovoltaic grid inverters, PFC rectifiers, and automotive inverter systems demand for an outstanding efficiency at low costs. In order to have small and cheap passive components, the switching frequency is often increased to medium values of 12–25 kHz, what leads to higher switching losses and lower system efficiency. Additionally, acoustic noise can be a problem in residential applications. The switching frequency has to be increased above the audible range of 20 kHz if cost intensive measures for attenuating acoustic noise should be avoided.

In high-speed drives and in aircraft applications fundamental output frequencies of up to 1 kHz are common and high control bandwidths are required. Here, the switching frequency can be increased up to 50 kHz in order to obtain acceptable waveforms and control performance. Again, the efficiency suffers and bulky cooling systems are necessary.

Manuscript received March 29, 2012; revised May 15, 2012; accepted May 26, 2012. Date of current version September 27, 2012. Recommended for publication by Associate Editor Dr. P. Barbosa.

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Digital Object Identifier 10.1109/TPEL.2012.2203151

The IGBT based two-level topology is still the standard industry solution to meet the requirements of the applications described. Alternative solutions have difficulties to gain market share due to their increased complexity and costs. Potential energy savings achieved with a different converter topology can only convince the customer if the initial costs are not too high and the investment may give a good return.

Previous work showed that multilevel topologies have a very flat dependence of the converter efficiency on the switching frequency [1], [2]. If a standard two-level voltage source converter (VSC) built with 1200-V IGBTs is compared to a three-level neutral point clamped (NPC) converter built with 600-V devices, the efficiency of the three-level converter can be better if the switching frequency is higher than 10 kHz.

In this paper, the competitiveness of the three-level T-type converter ($3LT^2C$) [3]–[8] for low-voltage applications is analyzed. Compared to the three-level NPC topology [4], the T-type employs an active bidirectional switch to the dc-link voltage midpoint and gets along with two diodes less per bridge leg. It is an alternative to more complex three-level topologies such as active neutral point clamped converters [9]–[11] or split-inductor converters [12], [13]. The $3LT^2C$ basically combines the positive aspects of the two-level converter such as low conduction losses, small part count and a simple operation principle with the advantages of the three-level converter such as low switching losses and superior output voltage quality.

A discussion on the possible switch configurations, the commutation steps and the available modulation schemes is given in Section II. The main differences and advantages compared to the three-level NPC topology are highlighted. The impact of the combination of different switch types on the switching losses is investigated. The converter efficiency is calculated with a generic approach considering the temperature dependence of the loss components.

It will be shown that the semiconductor losses of the $3LT^2C$ are decreased and distributed over several devices. This leads only to a small increase in the junction temperature and allows for choosing smaller semiconductor chip sizes or for keeping high efficiency and high reliability.

In Section III, the calculated efficiency is proved with measurements on a 99 % efficient, 10-kW hardware prototype of the $3LT^2C$. The hardware prototype has the ability to change its switching frequency and to switch between two-level and three-level modulation during operation. Accordingly, the impact on the losses of passive components such as the load machine or the EMI filter can directly be evaluated.

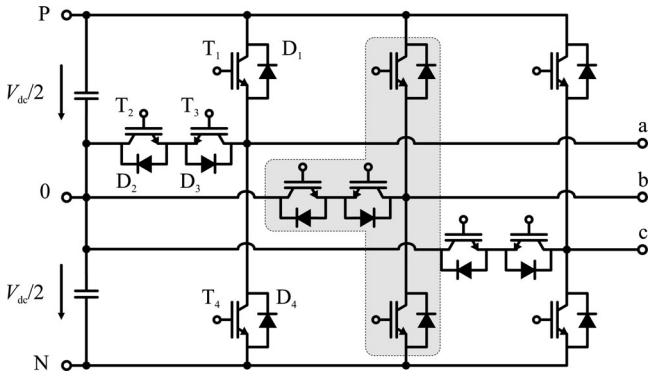

Fig. 1. Schematic of the three-level T-type topology. The conventional two-level VSC topology is extended with an active, bidirectional switch to the dc-link midpoint. A single-bridge leg of the T-type VSC resembles the shape of the rotated character "T", accordingly the topology is denominated as T-type topology.

A comparison of the achievable converter efficiency of the two-level VSC, the 3LT^{2}C, and the three-level NPC converter is given in Section IV. Due to the low conduction losses and the low switching losses of the 3LT^{2}C, the efficiency is very high especially for medium switching frequencies (8–24 kHz) often used in industry. This is achieved without employing SiC devices which can be very expensive if chip sizes leading to comparable conduction losses are chosen.

The 3LT^{2}C is considered to be a real alternative to two-level converters for low-voltage applications, where a higher switching frequency and high efficiency is a key target.

II. The T-Type Topology

The basic topology of the 3LT^{2}C is depicted in Fig. 1. The conventional two-level VSC topology is extended with an active, bidirectional switch to the dc-link midpoint.

For low-voltage applications (e.g., $V_{\rm dc} = 650$-V), the high-side and the low-side switches ($\rm T_1/D_1$ and $\rm T_4/D_4$) would usually be implemented with 1200-V IGBTs/diodes as the full dc-link voltage has to be blocked. Differently, the bidirectional switch to the dc-link midpoint has to block only half of the dc-link voltage. It can be implemented with devices having a lower voltage rating, in the case at hand two 600-V IGBTs including antiparallel diodes are used [cf., Fig. 2(a)]. Due to the reduced blocking voltage, the middle switch shows very low switching losses and acceptable conduction losses, although there are two devices connected in series.

Contrary to the three-level NPC topology, there is no series connection of devices that has to block the whole dc-link voltage $V_{\rm dc}$. For the NPC topology, switching transitions directly from the positive (P) to the negative (N) dc-link voltage level and vice versa are usually omitted as there might occur an uneven share of the voltage to be blocked in the transient case when both IGBTs connected in series turn off at the same time. This undesirable effect cannot occur in the T-type topology. It is not necessary to implement low-level routines which prevent such transitions or ensure a transient voltage balancing among series connected IGBTs.

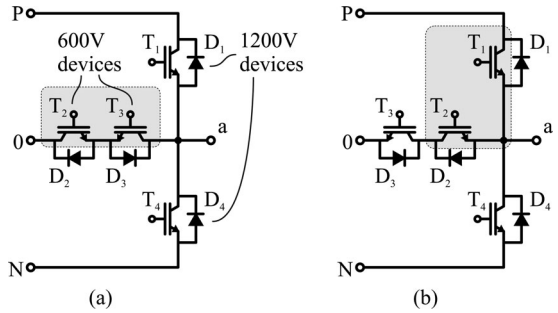

Fig. 2. Bidirectional switch to the midpoint can be implemented with two IGBTs in (a) common emitter configuration or (b) in common collector configuration.

An additional benefit related to using single 1200-V devices to block the full dc-link voltage are reduced conduction losses, if bipolar devices are considered. Whenever the output is connected to (P) or (N), the forward voltage drop of only one device occurs, contrary to the NPC topology where always two devices are connected in series. The conduction losses are considerably reduced making the 3LT^{2}C an interesting choice even for low swichting frequencies.

Historically, the three-level NPC topology was developed for medium-voltage applications. There, it was necessary to place devices in series due to the limited voltage blocking capability of the available devices. The drawback of the increased conduction losses due to the series connected bipolar devices was outperformed by the gain in voltage handling capability and the directly related gain in power handling capability. Contrary, for low-voltage applications, this benefit is invalid. The available devices have sufficient voltage ratings and fast switching speeds; therefore, it is not necessary to connect devices in series. An increased output power is achieved with increased phase currents. The conduction losses are an important factor limiting the power range and should be kept as small as possible. Therefore, the T-type topology is the better choice for low-voltage applications based on bipolar devices.

The T-type topology is also used in medium-voltage applications [14], [15] where it is known as neutral point piloted (NPP) converter or transistor clamped converter (TCC). For medium-voltage applications, the voltage blocking capability of a single device is not sufficient to block the full dc-link voltage. Each of the switches $\rm T_1$ and $\rm T_4$ has to be replaced by a series connection of two IGBTs. Special active gate drive units are necessary for transient and steady-state voltage balancing [16], [17]. The implementation effort is increased considerably and the conduction losses increase due the series connection of bipolar devices. Therefore, this configuration is not recommended for low-voltage applications.

A. Switch Configuration

There are basically two ways the two 600-V IGBTs can be configured to form a bidirectional switch, either in common emitter configuration or in common collector configuration.

The common emitter configuration [cf., Fig. 2(a)] would require one additional isolated gate drive supply voltage for each

TABLE I
SWITCHING STATES

State	V_{out}	T_1	T_2	T_3	T_4
P	$+V_{dc}/2$	on	on	off	off
0	0	off	on	on	off
N	$-V_{dc}/2$	off	off	on	on

bridge leg, summing up to three additional gate drive supplies compared to the two-level VSC topology.

This number can be reduced even more if a common collector configuration [cf., Fig. 2(b)] is used. T_2 shares now a common emitter with the high-side switch T_1 and can be supplied with the isolated gate drive voltage of T_1. The emitter of the second 600-V IGBT is connected to the midpoint voltage level. If the 3-phase topology is considered, all three IGBTs $T_{3,a,b,c}$ share a common emitter, and therefore only one isolated gate drive supply is necessary. In total, the complete T-type topology can be implemented with only one additional isolated gate drive supply compared to the two-level topology.

The necessary power rating of the isolated gate drive supply of the high-side switch T_1 is not increased if the gate charges of the 600 and the 1200-V IGBT are approximately equal. Because of the implemented commutation and modulation strategy T_1 and T_2 are newer switched both in the same modulation cycle what will be shown in the next section.

It is still necessary to implement six additional gate drive ICs and six additional digital isolators for the switch signals which will increase the costs slightly. Compared to the three-level NPC topology the removal of the clamping diodes reduces the necessary diodes from 18 to 12. Furthermore, the reduction of the additional isolated gate drive supplies from six to one is a clear improvement and can drive the costs down.

B. Commutation

The switch commutation has to be considered in detail for the 3LT^{2}C. Basically, the output of a bridge leg can be connected to the positive (P), neutral (0), or the negative (N) dc-link voltage level as can be seen in Fig. 3. The positive voltage level, for instance, could be achieved by closing T_1, the neutral level by closing T_2 and T_3, and the negative level by closing T_4 for both current directions. However, this strategy would require a current-dependent commutation sequence. Fortunately, there is a simpler commutation strategy which works independently of the current direction.

If we close not only T_1, but T_1 and T_2 for the positive voltage level, T_2 and T_3 for the neutral, and T_3 and T_4 for the negative voltage level, the current commutates naturally to the correct branch independent of the current direction. Table I describes which switches are closed to achieve the desired output voltage. A simple turn-on delay for all switches is sufficient to prevent a dc-link short circuit. If these switch signals are used, the modulation is identical to the three-level NPC topology modulation.

As an example we consider Fig. 3(a), where the output phase is connected to the positive (P) voltage level (T_1 and T_2 are closed) for positive output current. In order to commutate to the neutral level (0), T_1 is opened and after the turn-on delay T_3 is closed additionally. During the turn-off of T_1, the current naturally commutates over T_2 and D_3 to the neutral level. For a negative phase current [cf., Fig. 3(b)], the current commutates to the neutral after T_3 is closed.

If we switch back from (0) to (P), first T_3 is opened and after the turn-on delay T_1 is closed. For a positive phase current [cf., Fig. 3(c)] during turn-off of T_3, the current continues flowing through D_3 and commutates to the positive voltage level after the turn-on of T_1. For a negative phase current [cf., Fig. 3(d)], the current commutates to D_1 during turn-off of T_3. This principle works for all remaining switching transitions.

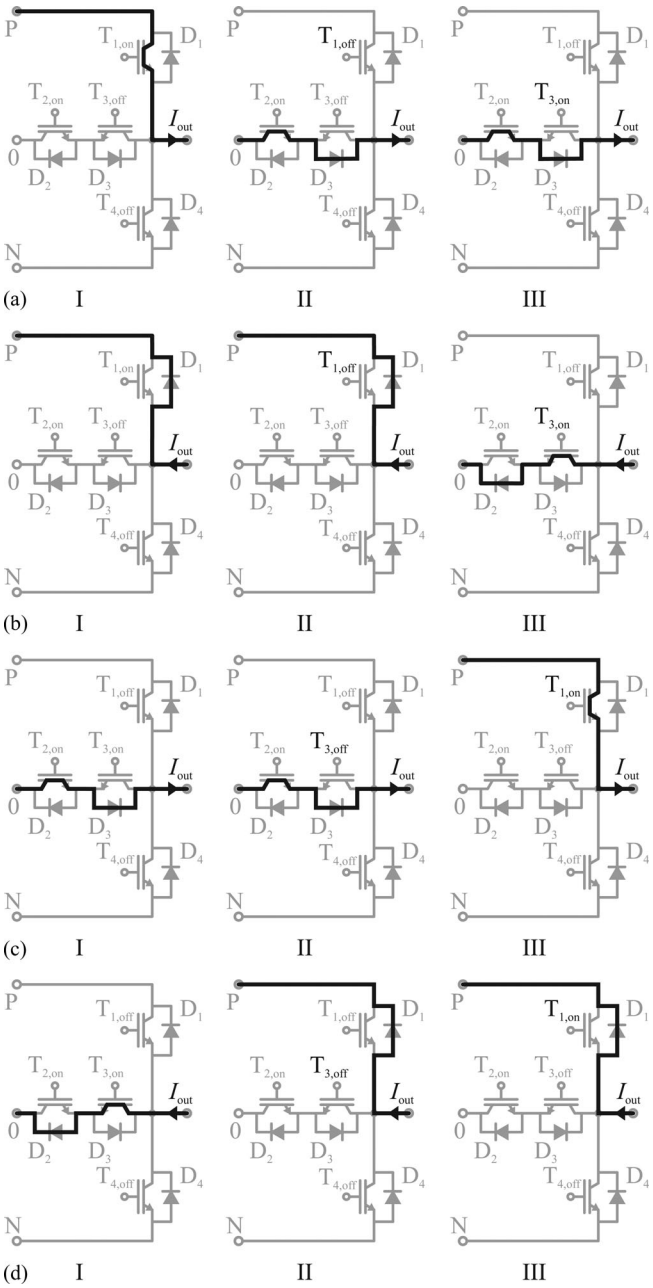

Fig. 3. Current commutation during switching transition (P → 0) for (a) positive and (b) negative output current. Current commutation during switching transition (0 → P) for (c) positive and (d) negative output current.

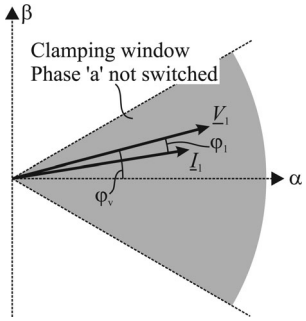

Fig. 4. Space-vector diagram showing the implemented clamping window.

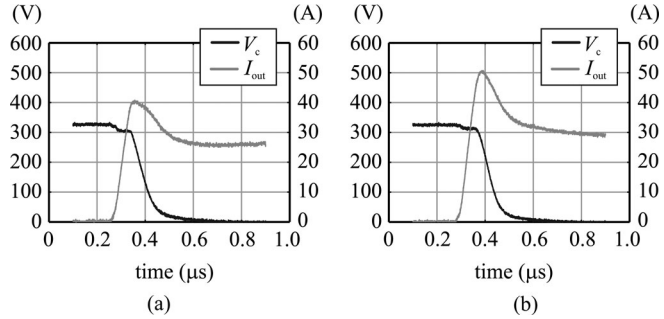

Fig. 5. Recorded turn-on switching transients of T_1 for $V_\mathrm{c} = 325\,\mathrm{V}$, $I_\mathrm{out} = 25\,\mathrm{A}$, $T_\mathrm{j} = 125\,^\circ\mathrm{C}$. (a) Commutating diode is rated for 600 V. (b) Commutating diode is rated for $1200V$.

The direct transition from (N) to (P) and vice versa is avoided by the implemented space-vector modulation and occurs only at sector borders. Although the transition is not a problem for the 3LT^{2}C, it produces additional losses in the 600-V diodes. A reverse recovery current pulse flows to the neutral voltage level because of the blocking voltage change from $-V_\mathrm{dc}/2$ to $+V_\mathrm{dc}/2$ over D_2 and D_3. This reverse recovery current produces additional losses in the diodes.

By omitting direct transitions from (N) to (P) and vice versa, the IGBTs T_1 and T_2 are not switched in the same modulation cycle. Therefore, as already mentioned in Section II-A, the necessary power rating of the isolated gate drive supply of the high-side switch T_1 is not increased if it is used to additionally power the gate drive unit of T_2.

C. Modulation

The modulation strategies known from the three-level NPC converter can also be applied to the 3LT^{2}C. The modulation strategy is an important point for the converter efficiency [18]. Either space-vector-based modulation strategies [19] or phase-oriented pulse-width modulation (PWM) [20], [21] can be used.

A space-vector modulation scheme with switching loss optimal clamping described in [19] is used in this paper. The output phase with the momentary highest current is not switched over an electrical angle of 60° (discontinuous PWM) what reduces the switching losses. A fixed clamping window around $\varphi_\mathrm{v} = -30^\circ \ldots 30^\circ$ is implemented ideally fitting a current to voltage displacement angle of $\varphi_1 = 0^\circ$ (cf., Fig. 4).

An issue related to the adopted optimal clamping space-vector modulation is that the dc-link capacitors are loaded in an alternating fashion with three times the fundamental frequency. Therefore, a certain dc-link voltage unbalance occurs periodically. The space-vector modulation can be adopted to account for this voltage unbalance according to [22]. The compensation ensures that the output voltage is generated correctly, although the link is not exactly balanced.

D. Determination of the Switching Losses

The 3LT^{2}C is built with mixed semiconductor technology. 600-V IGBTs and diodes are combined with 1200-V IGBTs and diodes. It would be inadequate to assume that the datasheet switching losses with simple scaling to the commutation voltage would be accurate enough to determine the switching losses of the 3LT^{2}C. The turn-on switching loss energy of the 1200-V IGBT will be lower if the commutating diode is only 600 V rated with considerably lower reverse recovery charge. The current overshoot during turn-on of T_1 is considerably reduced if the commutating diode is 600 V rated [cf., Fig. 5(a)] compared to the case where the commutating diode is rated for 1200 V [cf., Fig. 5(b)]. In the same manner, the 600-V device turn-on loss energy will be higher if the commutating diode is 1200 V rated.

TABLE II
SWITCHING LOSS ENERGIES

Switching Transition	Switching loss energies
$I_{out} \geq 0$	
$P \rightarrow 0$	$E_{\mathrm{T1,off}}$, $E_{\mathrm{D3,on}}$
$0 \rightarrow P$	$E_{\mathrm{T1,on}}$, $E_{\mathrm{D3,off}}$
$N \rightarrow 0$	$E_{\mathrm{T2,on}}$, $E_{\mathrm{D4,off}}$
$0 \rightarrow N$	$E_{\mathrm{T2,off}}$, $E_{\mathrm{D4,on}}$
$I_{out} < 0$	
$P \rightarrow 0$	$E_{\mathrm{T3,on}}$, $E_{\mathrm{D1,off}}$
$0 \rightarrow P$	$E_{\mathrm{T3,off}}$, $E_{\mathrm{D1,on}}$
$N \rightarrow 0$	$E_{\mathrm{T4,off}}$, $E_{\mathrm{D2,on}}$
$0 \rightarrow N$	$E_{\mathrm{T4,on}}$, $E_{\mathrm{D2,off}}$

In order to determine in which device switching losses occur depending on the switching transition and of what value these losses are, switching transients have been recorded directly at the 3LT^{2}C prototype over a range of commutation voltages, currents and temperatures. Passive voltage probes and passive ac current transformers directly mounted to the pins of the implemented discrete TO-247 packages enabled an accurate measurement with a minimum influence on the commutation inductance. The 3LT^{2}C prototype (cf., Section III) was built with the following devices:

1) Infineon IGBT 1200 V, 40 A IKW40T120;
2) Infineon IGBT 600 V, 50 A IKW50N60T.

Switching losses occur in different semiconductors depending on the switching transition and the direction of the output current. It is important to analyze the commutation process in detail for every switching transition in order to find what devices obtain turn-on and turn-off losses as well as diode reverse-recovery losses. Table II summarizes the results. The direct transition from (P) to (N) and vice versa is omitted by the implemented space-vector modulation.

TABLE III
MEASURED SWITCHING LOSS ENERGIES FOR $V_c = 325\,\mathrm{V}, I_{out} = 25\,\mathrm{A}$, AND $T_j = 125\,^\circ\mathrm{C}$

Energy	Measurement	Datasheet	Difference
$E_{T1,on}$	1.20 mJ	1.58 mJ	−24 %
$E_{T1,off}$	1.59 mJ	1.68 mJ	−5 %
$E_{D1,on}$	0.17 mJ		
$E_{D1,off}$	1.13 mJ	1.12 mJ	+1 %
$E_{T3,on}$	1.26 mJ	0.65 mJ	+94 %
$E_{T3,off}$	0.72 mJ	0.68 mJ	+6 %
$E_{D3,on}$	0.06 mJ		
$E_{D3,off}$	0.34 mJ	0.41 mJ	−17 %

Due to the symmetry of the circuit, the turn-on and turn-off energies of both 600-V devices are equal under the same conditions (i.e., $E_{T2,on} = E_{T3,on}$, $E_{T2,off} = E_{T3,off}$, $E_{D2,off} = E_{D3,off}$, and $E_{D2,on} = E_{D3,on}$). For the same reason, this holds also for the 1200-V devices (i.e., $E_{T1,on} = E_{T4,on}$, $E_{T1,off} = E_{T4,off}$, $E_{D1,off} = E_{D4,off}$, and $E_{D1,on} = E_{D4,on}$).

In Table III, the measured switching loss energies and the deviation from the datasheet values are summarized. It can be seen that the 1200-V IGBT turn-on energy is 24% lower and the 600-V IGBT turn-on energy is 94% higher than the datasheet values. The switching losses will still be lower than for the two-level VSC because the commutation voltage is only $V_{dc}/2$. The datasheet switching loss energies have been linearly interpolated to a commutation voltage of $V_c = 325\,\mathrm{V}$, a phase current of $I_{out} = 25\,\mathrm{A}$ and a junction temperature of $T_j = 125\,^\circ\mathrm{C}$ for this comparison. The datasheet diode turn-off loss energy was calculated from the given reverse recovery charge. The diode turn-on losses are very small and are usually not given in the datasheet.

E. Calculation of the Converter Efficiency

In order to calculate the operating point dependent 3LT^{2}C efficiency, an algorithm described in [2] was used and slightly adapted. The calculation incorporates the space-vector modulation such that the impact of optimal clamping is considered correctly.

The complete algorithm was extended to work with nonlinear approximations for the switching and the conduction losses. Additionally, the junction temperature of each device was considered in the loss calculation. The efficiency of the 3LT^{2}C prototype is expected to be in the range of 99%, and therefore the junction temperatures of the semicondcutor devices will be rather low. As the loss components are dependent on the temperature, neglecting this dependence could lead to wrong predictions of the achievable efficiency.

Models describing the current and voltage dependencies of the switching losses and the conduction losses have to be provided to the algorithm.

The switching loss energies have been approximated with (1) (cf., [23]). The coefficients are determined with a least-squares fit using the measurement data

$$E_{sw}(V,I) = k_1 \cdot V \cdot I + k_2 \cdot V \cdot I^2 + k_3 \cdot V^2 + k_4 \cdot V^2 \cdot I + k_5 \cdot V^2 \cdot I^2. \quad (1)$$

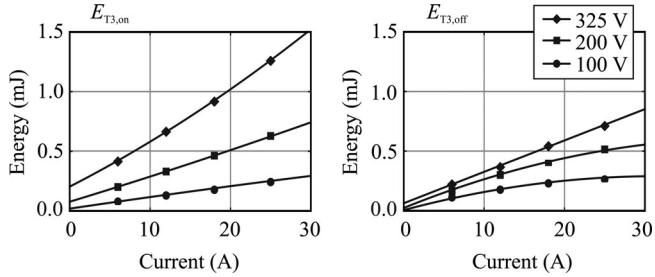

Fig. 6. Measured turn-on and turn-off energies of the 600-V IGBT at $T_j = 125\,^\circ\mathrm{C}$ and their curve-fitted approximation.

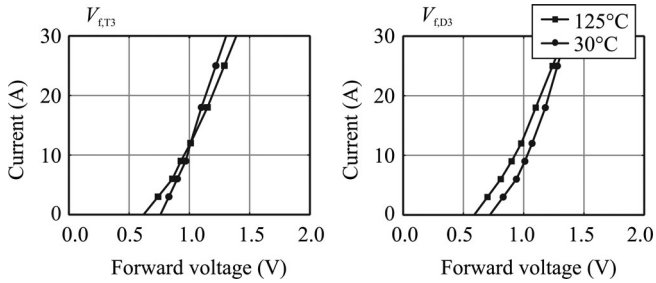

Fig. 7. Measured forward voltage drop of the 600-V IGBT and diode for two different junction temperatures.

As an example, the determined turn-on and turn-off loss energies and the fitted curves of the 600-V IGBT are depicted in Fig. 6. The switching losses increase with higher junction temperature and have been experimentally measured at three different temperatures $T_j = \{30\,^\circ\mathrm{C}, 80\,^\circ\mathrm{C}, 125\,^\circ\mathrm{C}\}$. In between these temperatures, piecewise linear interpolation is used for the calculation.

Also the conduction losses of each semiconductor device were determined experimentally. The forward voltage drop of the devices has been measured for several currents and junction temperatures. The self-heating effect of the semiconductor during the measurement is negligible because of the small duration ($T_p < 2$ms) of the applied current pulses. The current-dependent conduction-loss model was simply constructed with piecewise linear interpolation in between the experimental data points. The measured forward characterisics of the 600-V IGBT and diode are depicted in Fig. 7 for two different junction temperatures. The typical temperature dependence can be observed. The forward voltage decreases and the differential resistance increases with higher junction temperature.

Using these models, it is possible to calculate the losses over a fundamental period in each semiconductor device. A simple thermal model was included in the calculation in order to determine the mean junction temperatures and adapt the loss models. The thermal model consists of an heatsink with forced air cooling ($R_{sa} = 0.17\,\mathrm{K/W}$), an isolation foil ($R_{cs} = 0.51\,\mathrm{K/W}$) for each discrete device and the thermal resistances of the semiconductors given in the datasheet ($R_{jc,T1} = 0.45\,\mathrm{K/W}$, $R_{jc,D1} = 0.81\,\mathrm{K/W}$, $R_{jc,T2} = 0.45\,\mathrm{K/W}$ and $R_{jc,D2} = 0.8\,\mathrm{K/W}$). The junction temperatures converge to their final value after a few iterations of the loss calculation algorithm.

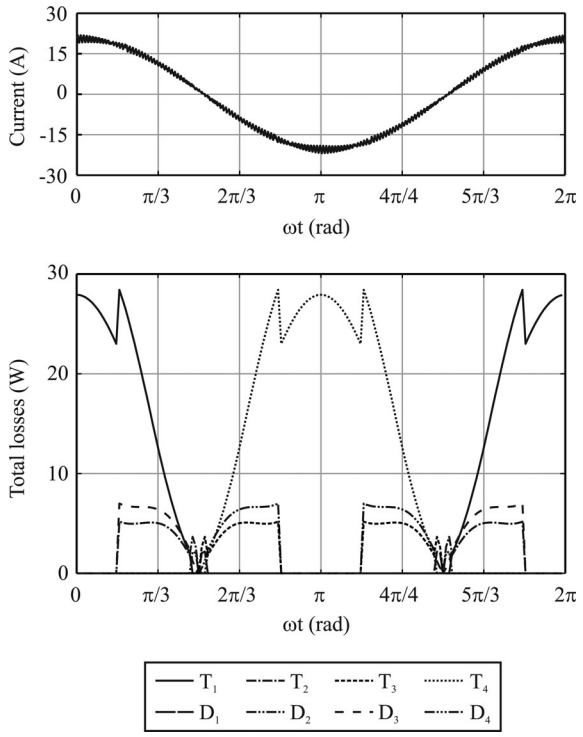

Fig. 8. Semiconductor loss distribution over an output voltage period at $\hat{V}_1 = 325\,\mathrm{V}, \hat{I}_1 = 20.5\,\mathrm{A}, \varphi_1 = 0°,$ and $f_\mathrm{s} = 8\,\mathrm{kHz}$.

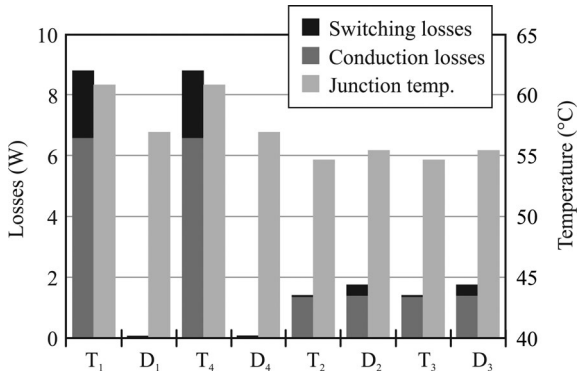

Fig. 9. Mean loss distribution in the semiconductor devices and corresponding junction temperatures for inverter operation ($\hat{V}_1 = 325\,\mathrm{V}, \hat{I}_1 = 20.5\,\mathrm{A}, \varphi_1 = 0°, f_\mathrm{s} = 8\,\mathrm{kHz},$ and $T_\mathrm{amb} = 40\,°\mathrm{C}$).

The combined switching and conduction losses over an output fundamental period are depicted in Fig. 8 for inverter operation at the nominal output power of $P_\mathrm{out} = 10\,\mathrm{kW}$. The characteristic reduction of losses over an electrical angle of $60°$ around the maximum current peak due to the implemented loss optimal clamping scheme can be seen.

Finally, the average losses in each semiconductor device of the 3LT^{2}C can be calculated. Fig. 9 shows the mean conduction and switching losses in each device. Generally, the 3LT^{2}C obtains very low losses for a wide range of switching frequencies. The conduction losses are comparable with the two-level converter, but the switching losses are further reduced because the commutation voltage is only $V_\mathrm{dc}/2$.

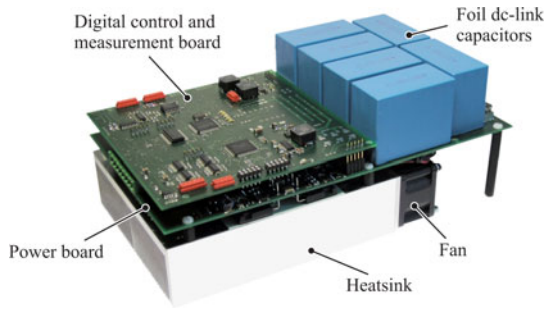

Fig. 10. Prototype of the 3LT^{2}C.

TABLE IV
PARAMETERS OF THE 3LT^{2}C

Parameter	Variable	Value
Nominal output power	P_n	$10\,\mathrm{kW}$
Nominal efficiency	η_n	$99.0\,\%$
Switching frequency	f_s	$8\,\mathrm{kHz}$
DC-link voltage	V_dc	$650\,\mathrm{V}$
DC-link capacitance	C_dc	$2 \times 240\,\mu\mathrm{F}$ in series
Volume	V	$3\,\mathrm{dm}^3$
Weight	m	$2\,\mathrm{kg}$
Power density	ρ	$3.3\,\mathrm{kW/dm}^3$
Power weight	σ	$5\,\mathrm{kW/kg}$

Similarly to the three-level NPC topology, the loss distribution is strongly dependent on the operating point. For inverter operation, the diodes D_1 and D_4 obtain only negligible losses, whereas for rectifier operation the IGBTs T_1 and T_4 are nearly not loaded. This distinct loss distribution profile enables to optimize a T-type bridge-leg module for certain applications such as solar inverters or PFC rectifiers (cf., [24]). The semiconductor chip area of the lightly loaded devices can be decreased to a minimum what saves costs.

Due to the low semiconductor losses, the junction temperatures of the devices are only about $60\,°\mathrm{C}$ for an ambient temperature of $T_\mathrm{amb} = 40\,°\mathrm{C}$. The switching frequency can be increased without problems up to $f_\mathrm{s} = 50\,\mathrm{kHz}$ if converter efficiency is not a key target. Otherwise, the reliability of the semiconductor devices increases due to the decreased junction temperatures and the small thermal cycling.

III. THE 3LT^{2}C PROTOTYPE

The key performance data of the 3LT^{2}C prototype (cf., Fig. 10) are summarized in Table IV. The converter is designed for an output power of $10\,\mathrm{kW}$ and allows the switching frequency to be set in a range from 4 to $24\,\mathrm{kHz}$. At the nominal switching frequency of $8\,\mathrm{kHz}$, the converter reaches a pure semiconductor efficiency of 99 %. Digital control, gate drive circuits, and forced air cooling consume $20W$ in addition. The power density is given with $3.3\,\mathrm{kW/dm}^3$.

The converter is controlled with a digital signal processing board consisting of a $100\,\mathrm{Mhz}$ DSP from TI (TMS320F2808) and a FPGA from Lattice (LCMXO2280) as well as filtering and amplification circuitry. The control board is mounted on top of the power board which holds the gate drive circuits and the power semiconductors.

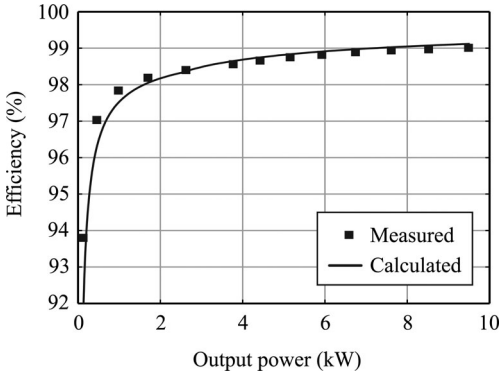

Fig. 11. Calculated and measured efficiency of the 3LT^{2}C prototype supplying a *RL* load ($R = 20\,\Omega, L = 2.5\,\mathrm{mH}$).

An important feature of the prototype is the ability to change the switching frequency during operation. Also the output voltage can be switched between two-level and three-level modulations during operation what allows an investigation of the impact on the losses occuring in the load machine without stopping the machine and changing its thermal conditions. An analysis showing the positive impact of the three-level output voltage waveform on the harmonic machine losses was presented in [25]. The harmonic machine losses can be reduced approximately by a factor of 4 compared to standard two-level operation.

The efficiency of the 3LT^{2}C has been measured with a Yokogawa WT3000 precision power analyzer (basic power accuracy of 0.02%). The measurements were conducted with a fixed RL-load ($R = 20\,\Omega, L = 2.5\,\mathrm{mH}$) and the output voltage was increased in small steps. The clamping interval was set to a symmetric clamping around 0° in order to match the small current displacement angle φ_1 resulting from the mainly resistive *RL* load.

Fig. 11 shows the measured and the calculated efficiency over the output power. The initial efficiency calculation resulted in a slightly higher efficiency than measured. Further measurements revealed additional loss components caused by cabling resistances (due to technical reasons, a four-wire measurement was not possible) and contact resistances of the implemented screw clamps at the power terminals of the converter. Although these loss components are very small ($P_{\mathrm{cable}} = 12.8\,\mathrm{W}$ and $P_{\mathrm{screw}} = 13.8\,\mathrm{W}$ at the nominal output power), the influence is not negligible if such high efficiencies are measured. If these additional losses are included, calculation and measurement show a very good agreement.

IV. Efficiency Comparison

In this section, the efficiency of the 3LT^{2}C is compared with the standard two-level VSC and the three-level NPC topology. A reasonable switching frequency range of $f_{\mathrm{s}} = 4$–$48\,\mathrm{kHz}$ is chosen for the comparison.

In Fig. 12 the efficiency for inverter and rectifier operation of the 3LT^{2}C, the two-level VSC with 1200-V IKW40T120 and the three-level NPC with 600-V IKW50N60T switches are depicted. For the calculation of the two-level and the three-level NPC efficiency, the same algorithm accounting for the loss optimal space-vector modulation is used.

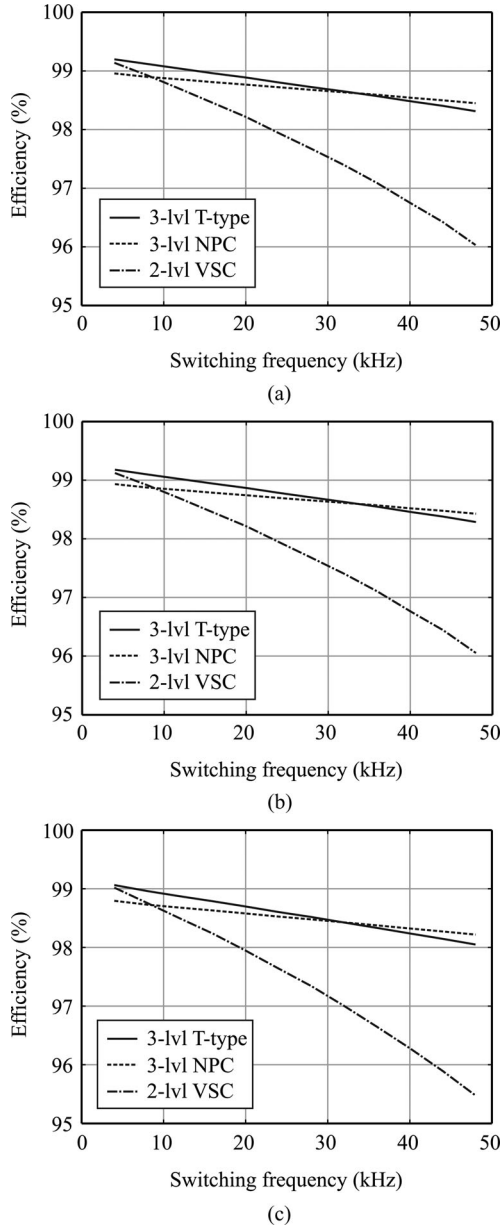

Fig. 12. Calculated efficiency comparison for $S_{\mathrm{out}} = 10\,\mathrm{kVA}$, $\hat{V}_1 = 325\,\mathrm{V}$, $\hat{I}_1 = 20.5\,\mathrm{A}$. (a) Inverter operation with $\varphi_1 = 0^\circ$, (b) rectifier operation with $\varphi_1 = 180^\circ$, and (c) inverter operation with load machine ($\varphi_1 = 30^\circ$). Switch types: Infineon IKW40T120 and IKW50N60T.

The same thermal model as described in Section II-E is used for all topologies. The performance of the heatsink had to be improved in order to get reasonable junction temperatures for the two-level converter at high switching frequencies. The resulting thermal resistance is given with $R_{\mathrm{sa}} = 0.12\,\mathrm{K/W}$ and is used for all topologies.

The temperature-dependent conduction loss models described in Section II-E are used for the calculation. The switching loss models have been adapted slightly in order to have the same data basis for the comparison of the three different

topologies. Instead of using the nonlinear model described in Section II-E, the switching loss energies were scaled linearly with the commutation voltage and the switched current. The temperature dependence of the switching losses is still included.

The only additional loss components included for all converters are due to the contact resistances of the screw clamps ($R_{\mathrm{screw}} = 14.5\,\mathrm{m\Omega}$). The cabling losses have been removed as they are dependent on the measurement setup.

The efficiency of the T-type converter is outstanding for medium switching frequencies from 4 to $30\,\mathrm{kHz}$ (cf., Fig. 12). The main benefit of the T-type topology comes from the reduced switching losses because the commutation voltage of the 1200-V devices is only $325\,\mathrm{V}$ instead of $650\,\mathrm{V}$ in the two-level VSC. Compared to the three-level NPC topology the conduction losses are lower because of only two devices being in series in the current path. The difference between inverter operation [cf., Fig. 12(a)] and rectifier operation [cf., Fig. 12(b)] is very small. If the load is partly inductive such as an induction machine, the loss optimal clamping interval can be adapted for all three topologies. Fig. 12(c) shows the achievable efficiencies for a current displacement angle $\varphi_1 = 30^\circ$ with a matched clamping interval.

For a switching frequency above $30\,\mathrm{kHz}$, the three-level NPC topology is superior. As the efficiency curves of the three-level NPC and the T-type topology are very flat, the switching frequency at which both topologies have equal efficiency is very sensitive to variations of the semiconductor properties such as conduction and switching losses. If the dc-link voltage is increased, the cross-over point is at a lower switching frequency because the switching losses of the T-type topology become more important.

The application area of the three-level NPC topology is limited to special applications, where exceptionally high switching frequencies are necessary and where the increased costs due to the number of necessary semiconductors and gate drive units can be justified. For all other low-voltage applications the 3LT^{2}C is the better choice if efficiency and costs are important. Naturally, for medium-voltage applications, the three-level NPC topology has its advantages and cannot be replaced by the 3LT^{2}C.

V. Conclusion

In this paper, the 3LT^{2}C for high-efficiency low-voltage applications was presented. It is an alternative to the two-level VSC for medium switching frequency applications and is very efficient in the range of 4–30 kHz. The main advantage comes from the halved commutation voltage which reduces the switching losses compared to the two-level topology. The conduction losses do not change considerably.

The implementation of the bidirectional switch to the midpoint of the dc-link with two antiserial 600-V IGBTs in common-emitter or common-collector configuration was discussed and benefits concerning the additional isolated gate drive supplies have been shown for the common-collector configuration. A simple commutation scheme which is independent on the current direction was presented.

The losses of the 3LT^{2}C were calculated with an algorithm considering the loss optimal clamping scheme and the temperature dependence of the loss components. The predicted efficiency of 99% was proved with measurements on a 10-kW prototype of the 3LT^{2}C.

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