Power Electronic Systems
Laboratory

Proceedings of the International Conference of Integrated Power Electronics Systems (CIPS 2012), Nuremberg, Germany, March 6-8, 2012

Comparative Evaluation of Individual and Coupled Inductor Arrangements for Input Filters of PV Inverter Systems

B. Cougo,
T. Friedli,
D. O. Boillat,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Comparative Evaluation of Individual and Coupled Inductor Arrangements for Input Filters of PV Inverter Systems

Bernardo Cougo, Thomas Friedli, David O. Boillat and Johann W. Kolar, ETH Zurich, Power Electronic Systems Laboratory, Zurich, Switzerland.

Abstract

Photovoltaic systems (PV) of higher power are connected to the grid through three-phase inverters via output filters which are designed to limit Electromagnetic Interference (EMI), in order to comply with international standards. With the purpose of reducing the volume of this converter, this paper evaluates 3 configurations of bridge legs and output magnetic components and identifies the most compact options for a system of 10kVA. A single bridge leg and two interleaved bridge legs with coupled or uncoupled inductors are considered in the comparison. Switching frequency and total silicon area are fixed and the volume of the passive components and the heatsink are evaluated as well as the system efficiency. The analysis developed in this paper show that the configuration with interleaved bridge legs and coupled inductors has a total volume close to 70% when compared to the configuration with interleaved bridge legs and uncoupled inductors, but it has a similar total volume when compared to the configuration with a single bridge leg. Although it is reported in the literature that systems with coupled inductors usually have a lower volume, the case at hand has the output filters designed to comply with EMI standards and it will be shown that, like this, the volume reduction of magnetic components provided by coupled inductors is compensated by the increase on the volume of capacitors.

1 Introduction

In modern power electronics, the design of high frequency power converters and associated filters is mainly determined by a trade-off between different characteristics, such as power density, efficiency, price and other performances. In PV applications, converters transferring the energy from solar panels to the mains have to fulfill EMI standards concerning the level of harmonics in the output voltage, as e.g. Class A and Class B limits from CISPR [1]. These standards directly influence the size of output differential- and common-mode filters.

Classical three-phase converters for PV applications usually make use of a single bridge leg per phase. However, depending on the current rating and availability of switches, more than one bridge might be used per phase. Interleaving the switching signals of paralleled legs increases the apparent frequency of the output current and as a consequence the filter size can be reduced if the maximum output voltage or current ripple is fixed.

Bridge legs can be connected through either coupled or uncoupled inductors. Coupled inductors, also called InterCell Transformers (ICT), have the advantage of decreasing the current ripple in each paralleled leg and, as a consequence, reducing high frequency conduction losses in the magnetic components, contributing to reduce the total size of the converter [2,3].

In this paper, 3 different configurations of a 10kVA three-phase inverter (cf. **Fig. 1**) will be evaluated and optimized with respect to the volume. Given the connection of the central point of the DC bus of the converter to the neutral point of the mains, the analysis will be made for only one single-phase two-level system of 3.33kVA. A switching frequency of 16kHz is chosen so the converter has low audible noise and still a reasonably high efficiency.

For a representative comparison, the steps to design the converters will be as follows:

1 – The required silicon area is determined as shown in [4] considering the configuration with a single bridge leg, for a maximum average junction temperature of 125°C in each component. The same silicon area is then used in the other configurations.

2 – Semiconductors losses are calculated and the required heatsink volumes are evaluated for the same *Cooling System Performance Index* CSPI, i.e. for assuming a certain thermal conductance per heatsink volume [5].

3 – Inductances and capacitances of the output filters are calculated. This paper only deals with the differential-mode filter. Due to the low switching frequency, a 2nd order filter is sufficient for achieving the required attenuation in the output voltage harmonics to comply with EMI standards.

4 – The volume of the filter capacitors is calculated based on commercial capacitors. Coupled and uncoupled inductors are designed/optimized for minimum boxed volume.

2 Compared Configurations

The specifications common to the three converters are shown in **Tab. 1**. The 3 configurations considered in the comparison are shown in **Fig. 1**.

- Configuration 1 (**Fig. 1a**): One single leg with a single inductor.
- Configuration 2 (**Fig. 1b**): Two paralleled legs with interleaved switching signals, connected through (uncoupled) regular inductors.
- Configuration 3 (**Fig. 1c**): Two paralleled legs with interleaved switching signals, connected through an ICT, and with a regular filter inductor.

ISBN 978-3-8007-3414-6

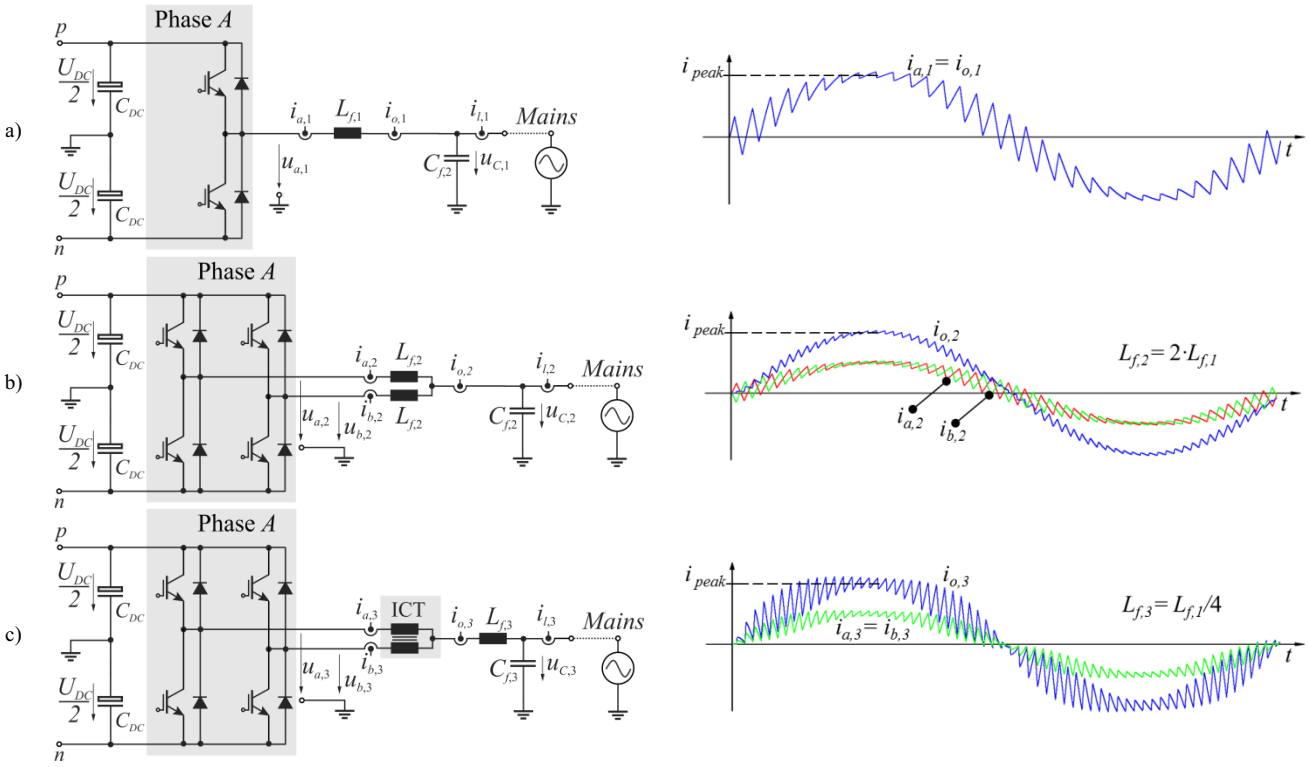

Fig. 1 Converters considered in the comparison: a) Single bridge leg (Config. 1); b) Interleaved bridge legs with regular inductors (Config. 2); c) Interleaved bridge legs with ICT (Config. 3). Furthermore shown: Typical current waveforms of the converters. All configurations present the same relative current ripple at the output of a bridge leg.

Output power (single-phase)	3.33kVA
DC bus voltage, U_{DC}	700V
Output voltage (*rms* value), u_l	230V
Peak output current, $\hat{\imath}_l$	20.5A
Switching frequency, f_s	16kHz
Maximum relative current ripple (peak value) in a leg	20% of peak current of the leg

Tab. 1 Parameters of the designed converters.

Current waveforms associated to each configuration are also shown in **Fig. 1**. In this figure, each configuration has the same relative ripple of ±35% of the peak value of the low frequency current of a bridge leg; and the switching frequency of each leg is set to 1.6kHz. These values are different from **Tab. 1** and were chosen for a clear graphical representation of the characteristics of the considered configurations.

Fig. 1b shows that the leg currents $i_{a,2}$ and $i_{b,2}$ are interleaved and the resulting current $i_{o,2}$ has twice the low frequency content of each leg. However, the maximum ripple of $i_{o,2}$ is half the maximum ripple of each leg. Also the frequency of the ripple of $i_{o,2}$ is twice the switching frequency.

If the high frequency voltage over the output capacitor has low ripple, the instantaneous peak-to-peak current ripple in each leg of the interleaved converter of **Fig. 1b** can be calculated as for a single bridge as

$$\Delta i_{a,2} = \frac{\alpha \cdot (1-\alpha) \cdot U_{DC}}{L_{f,2} \cdot f_s} \qquad (1)$$

where α is the instantaneous duty cycle and $L_{f,2}$ is the inductance in each leg of the converter.

The instantaneous peak-to-peak current ripple of $i_{o,2}$ then results as

$$\Delta i_{o,2} = \frac{\alpha' \cdot (1-\alpha') \cdot U_{DC}}{2 \cdot L_{f,2} \cdot f_s} \qquad (2)$$

where α' is an equivalent duty cycle defined below:

$$\alpha' = 2\alpha \quad \text{if} \quad 0 \le \alpha \le 0.5 \quad \text{and}$$
$$\alpha' = 2\alpha - 1 \quad \text{if} \quad 0.5 < \alpha \le 1 \quad . \qquad (3)$$

For the converter of **Fig. 1c**, an ICT is used to magnetically couple both legs. Like this, although different voltages are applied to the windings, the currents of the legs are forced to be the same, if the number of turns of each winding is the same. Explanation on the operation of coupled inductors (ICT) can be found in [6]. According to [6], the current ripple in the inductor $L_{f,3}$ can be calculated as

$$\Delta i_{o,3} = \frac{\alpha' \cdot (1-\alpha') \cdot U_{DC}}{L_{f,3} \cdot f_s} \qquad (4)$$

and the current ripple in the ICT windings is half of the ripple calculated in Eq. (4).

With Eqs. (1) to (4), one can conclude that if the absolute values of the maximum amplitudes of the current ripples in the output of the magnetic components are the same ($\Delta i_{o,1}=\Delta i_{o,2}=\Delta i_{o,3}$), then the relation between the inductances is $L_{f,1}= 2L_{f,2}= 4L_{f,3}$.

If the relative amplitude of the current ripples in each bridge leg is the same ($\Delta i_{a,1}/\hat{\imath}_{a,1}=\Delta i_{a,2}/\hat{\imath}_{a,2}=\Delta i_{a,3}/\hat{\imath}_{a,3}$), then the relation between the inductances is $L_{f,1}= L_{f,2}/2= 4L_{f,3}$.

In any case, Configuration 3 presents a lower inductance than the others, which results in smaller magnetic devices, as will be seen in **Section 4**.

ISBN 978-3-8007-3414-6

3 System Design

3.1 Silicon area and losses

The main idea of the design is to adapt the silicon area of transistors and diodes such that the average junction temperature of each component is 125°C. The procedure is shown in [4] and the data used for the silicon losses and thermal models are adapted from Infineon Trench and Field Stop 1200V IGBT4. The thermal model considers a fixed heatsink temperature of 80°C.

For the single bridge configuration and specifications of **Tab. 1**, the minimum required area for the 6 transistors (considering the 3–phase system) is 177mm^2 and for the 6 diodes 74mm^2. The total semiconductor losses (P_{tot}) are 317W.

The same silicon areas as for configuration 1 were considered for the calculation of the losses and the temperatures of the converters in configurations 2 and 3. Thus, since these configurations have 12 transistors and 12 diodes each, the area of each component is half the corresponding area in configuration 1. In the model shown in [4], switching and conduction losses do not significantly change with the area. Like this, since only half the current is conducted in each component of configurations 2 and 3, similar losses are calculated when compared to configuration 1; a total loss (P_{tot}) of 328W is calculated for each configuration (2 or 3). However, given that the thermal resistance from the junction to the heatsink is inversely proportional to $A_s^{0.88}$ (where A_s is the silicon area), the junction temperature of the transistors and diodes for configurations 2 and 3 is 122°C which is about the same as for configuration 1 (125°C).

3.2 Heatsink volume

With the total losses and heatsink temperatures (T_{HS}) given in the last section, one can calculate the required thermal resistance of the heatsink as

$$Rth_{HS} = \frac{(T_{HS} - T_{amb})}{P_{tot}} \tag{5}$$

where T_{amb} is the ambient temperature, which is considered to be 45°C. For a typical aluminium heatsink with Cooling System Performance Index *CSPI* (defined in [5]) equal to 17.88mW/K·cm^3, the heatsink volume results as

$$Vol_{HS} = (CSPI \cdot Rth_{HS})^{-1} \quad . \tag{6}$$

3.3 Inductance and Capacitance Calculation

The LC filter in the output of the converter has to limit the EMI injected into the mains and the current ripple in the bridge legs. Typically, two LC filter stages are employed, however for the sake of a clearer representation, only a single-stage filter is considered here.

Since the magnetic components are usually the bulkiest and most expensive parts of the filter, it is usually designed to have the lowest possible inductance. This inductance is then calculated considering the maximum allowed amplitude of the ripple in the bridge legs, which was chosen to be 20% of the peak current in each leg, for facilitating a correct measurement of these currents by the converter control. With this requirement and using Eqs. (1) to (4), the inductances values are

$$L_{f,1} = \frac{U_{DC}}{8 \cdot f_s \cdot 0.2 \cdot \hat{i}_l} \;,\; L_{f,2} = 2 \cdot L_{f,1} \;,\; L_{f,3} = \frac{L_{f,1}}{4} \,. \tag{7}$$

For these values, the same relative maximum current ripple is obtained in each bridge leg, however the maximum amplitude of the current ripple in the output of the magnetic component (which will mainly flow through the filter capacitor), will be only the same for configurations 1 and 3, but will be 4 times smaller for configuration 2.

3.3.1 Capacitance calculation considering EMI standards

Measurement of voltage noise injected into the mains is made using a line impedance stabilization network (LISN, defined in [7]), which is connected between the mains and the converter. The voltage measured at the LISN output, which is practically the high frequency component of the filter capacitor voltage, is read by the EMI Test Receiver, which processes this noise according to [8]. The output of this circuit is compared to the limits defined by the standards.

The capacitor is designed such that the output of the EMI Receiver stays below the limits. The design adopted here is based on the assumption that *rms* value of the voltage harmonics at the LISN (U_{LISN}) output is an adequate measure for the estimation of the output of the EMI Test Receiver. It is shown in [9] that when making this consideration, the error in the estimation is less than 6.7dB. The main idea of the design is that all the harmonics in the output of bridge legs ($U_{h,rms}$) can be considered to be concentrated at the switching frequency. The EMI Test Receiver, which measures noises starting from 150kHz, will measure a signal *m* times smaller than $U_{h,rms}$, where *m* is the rank of the first harmonic after 150kHz. The difference between the measured value and the value of the EMI standards at this frequency defines the required attenuation of the output filter. This is schematically shown in **Fig. 2**. The design procedure is divided into four steps, which are explained below.

Step 1) Simulation or calculation of the harmonic voltage ($U_{h,rms}$) at the output of the converter: For complex systems, the output voltage u_o of the converter can be simulated and may be processed by software in order to eliminate the voltage at the fundamental frequency (U_{fund}) and to calculate only the *rms* value of the harmonics. However, for inverters, the *rms* value of the harmonics can be calculated analytically as

$$U_{h,rms} = \sqrt{U_{o,rms}^2 - U_{fund,rms}^2} \quad . \tag{8}$$

Since the voltage at the output of a bridge leg is a rectangular waveform with amplitudes $-U_{DC}/2$ and $+U_{DC}/2$, its *rms* value is always equal to $U_{DC}/2$, independent of the modulation. The *rms* value of the fundamental depends on the modulation index (*M*), and like this Eq. (8) becomes

$$U_{h,rms} = \frac{U_{DC}}{2}\sqrt{1 - \frac{M^2}{2}} \quad . \tag{9}$$

The result of Eq. (9) is valid for configuration 1, where only a single bridge is employed. When interleaved bridge legs are considered, since the output voltages of the two bridges are connected through coupled or uncoupled inductors, the voltage in the output capacitor is related to the average of the voltages at the output of both bridge legs. Since these voltages are inter-

ISBN 978-3-8007-3414-6

leaved (180° phase shift), the equivalent average voltage (U_{oeq}) is a three-level voltage at twice the switching frequency, with values 0 and $+U_{DC}/2$ when the converters duty cycle is greater than 0.5 (α>0.5) and 0 and $-U_{DC}/2$ when α<0.5. The fundamental of U_{eq} is the same as $U_{o,rms}$ shown in Eq. (8), however the total *rms* voltage is not and it can be analytically calculated as

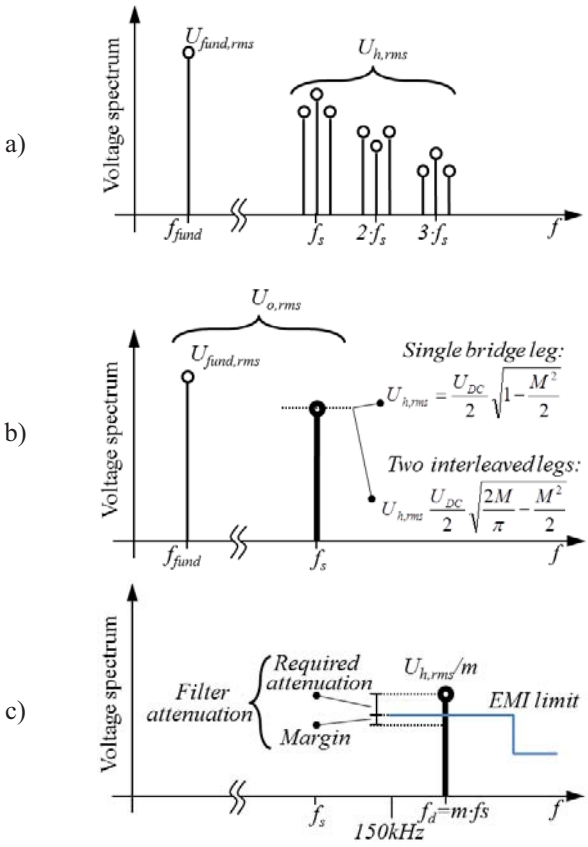

Fig. 2 Main idea of harmonic voltage estimation and filtering requirements. Estimating the total harmonic *rms* voltage in a) and considering it to be concentrated only at the switching frequency as in b). c) The harmonic content at the design frequency f_d is estimated, and the filtering requirements are calculated regarding EMI standards.

$$U_{oeq,rms}^2 = \frac{1}{T}\cdot\int_0^T U_{eq}^2(t)\mathrm{d}t = \\ = \frac{1}{T}\cdot\int_0^{T/2}\left(\frac{U_{DC}}{2}\right)^2 M\sin(2\pi ft)\mathrm{d}t + \\ + \frac{1}{T}\int_{T/2}^{T} -\left(\frac{U_{DC}}{2}\right)^2 M\sin(2\pi ft)\mathrm{d}t = \left(\frac{U_{DC}}{2}\right)^2\frac{2M}{\pi}. \quad (10)$$

The *rms* value of the harmonics for the interleaved converter then results as

$$U_{eqh,rms} = \frac{U_{DC}}{2}\sqrt{\frac{2M}{\pi}-\frac{M^2}{2}} \quad . \quad (11)$$

Eqs. (9) and (11) are graphically shown in **Fig. 3**, normalized to $U_{DC}/2$. Note that interleaved bridge legs generate lower harmonic voltage than a single bridge leg, and the ratio is close to 2 for a wide range of modulation indexes. However, in the interleaved case, the harmonics are generated at twice the switching frequency. It means that the harmonic voltage considered at the design frequency (which will be explained in the next steps) is attenuated two times less than for the case of a single bridge leg. The required filter attenuation for all configurations therefore is about the same.

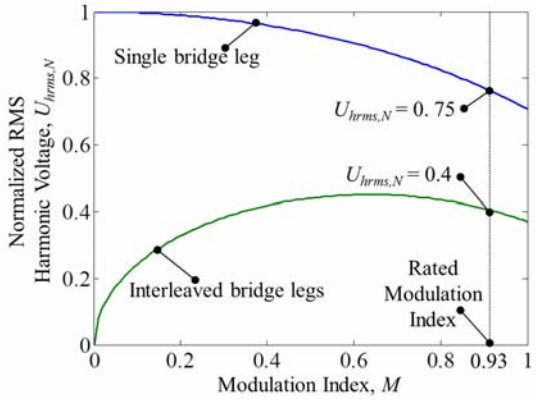

Fig. 3 Harmonic voltage (*rms* value) at the output of a single bridge leg and for two interleaved bridge legs versus the modulation index. Values are normalized to $U_{DC}/2$.

Step 2) Definition of the rank m of the first harmonic after 150kHz, which is at f_d (design frequency): For a switching frequency of 16kHz, f_d = 160kHz. The rank m is different for a single bridge and for interleaved bridge legs; and the corresponding values are

$$m = f_d / f_s \quad \text{and} \quad m = f_d / (2\cdot f_s) \ , \quad (12)$$

respectively. The voltage at the frequency f_d at the EMI Receiver can be estimated, if no filter is considered:

$$U_{est}(f_d)[dB\cdot\mu V] = 20\cdot\log\left(\frac{10^6\cdot U_{hrms}}{m}\right). \quad (13)$$

Step 3) Calculation of the required attenuation (*Att*) provided by the filter: To comply with EMI standards, the filter attenuation has to be

$$Att(f_d)[dB] = U_{est}(f_d)[dB\cdot\mu V] \\ - Limit(f_d)[dB\cdot\mu V] + Margin[dB\cdot\mu V] \quad (14)$$

where *Limit* value is extracted from the noise limit curve defined in the EMI standard curve at the design frequency (equal to 79dB·µV for Class A EMI standard for quasi-peak detection, at 160kHz) and *Margin* is defined considering inaccuracies of the applied method. For this work *Margin* is set to 10dB·µV which results in the required filter attenuations as shown below.

Configuration 1: $Att(f_d)$[dB] = 79.4dB.

Configuration 2 and 3: $Att(f_d)$[dB] = 79.9dB.

As mentioned in *Step 1*, the required attenuations for a single bridge leg and two interleaved legs are similar although they have the harmonic voltage concentrated in different frequencies.

Step 4) Calculation of the required filter capacitance: The value of capacitance to achieve the required filter attenuation (*Att*) can be calculated based on the transfer function of a 2nd order filter.

$$C = \frac{1+Att^{-1}}{4\cdot\pi^2\cdot f_d^2\cdot L} \quad (15)$$

where L depends on which configuration is considered:

ISBN 978-3-8007-3414-6

Configuration 1: $L = L_{f,1}$
Configuration 2: $L = L_{f,2}/2$
Configuration 3: $L = L_{f,3}$.

3.4 Capacitor, Inductor and ICT Volume Calculation

As typically used in EMI filter design, X2 MKP film capacitors from EPCOS with a rated voltage of 305V_{rms} were selected. The capacitors volume can be calculated using the average capacitance density extracted from the manufacturer's datasheet. This value is equal to 0.18µF/cm^3.

The ICTs and inductors were optimized for minimum volume according to the procedure shown in the flow-chart of **Fig. 4**. Since the main objective of the design is to reduce the boxed volume of the magnetic components, the ICT and inductor structures of **Fig. 5** were considered. Windings are composed of copper foil conductors which provide high utilization of the core window and low copper losses at higher frequencies. The core material is chosen to be Nanocrystalline Vitroperm 500F from VacuumSchmelze, given its low specific losses at high frequencies and high saturation flux density (close to 1T).

Geometric parameters which had their values changed during optimization are: conductor thickness and width, core leg width and depth and the number of turns. Optimization constraints were defined as follows: maximum temperature rise (T_{lim}) equal to 40°C and maximum flux density (B_{max}) in the core equal to 0.8T. The calculations performed in the optimization algorithm are briefly described below.

3.5 Core losses and maximum flux density

In an inductor, the flux density B_{ind} inside the core is proportional to the current i_{ind} flowing in the windings,

$$B_{ind}(t) = \frac{L \cdot i_{ind}(t)}{A_c \cdot N} \quad , \tag{16}$$

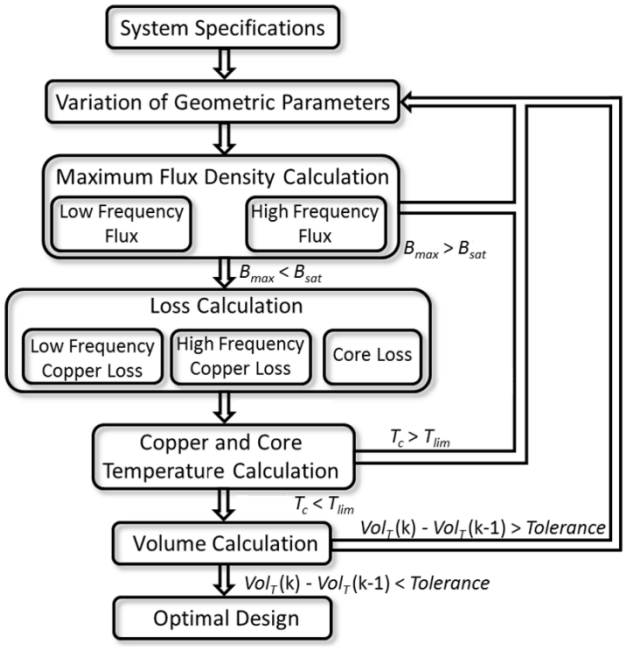

Fig. 4 Design flow-chart of the ICT and inductor.

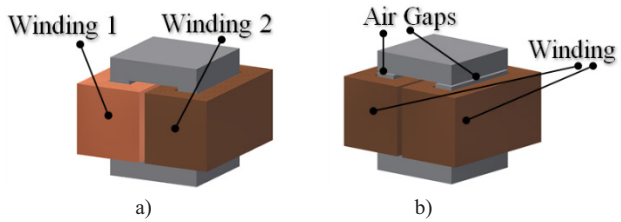

Fig. 5 Structure of a) ICT and b) inductor used in the optimization procedure.

where A_c is the core cross section, N is the number of turns and L is the inductance. With this equation, one can calculate the maximum flux density and the high frequency flux [together with Eqs. (1) to (4)] to estimate the core losses.

In an ICT, the low frequency flux is inversely proportional to the leakage inductance [6] which is neglected in the case at hand. However, the high frequency flux depends on the difference between the voltages applied to the windings [6], and the peak value B_p can be calculated as

$$B_p = \frac{\alpha \cdot (1-\alpha) \cdot U_{DC}}{2 \cdot N \cdot f_s \cdot A_c} \quad . \tag{17}$$

In an inverter, the duty cycle changes at each switching period, thus a precise way to calculate core losses is to use Eq. (17) to calculate the peak flux density waveform for each switching period and the corresponding losses according to Eq. (18), and then average all these values in a period of the mains. An approximate calculation of the core losses in a nanocrystalline core in each switching period can be based on the Steinmetz equation, which determines the core loss density,

$$P_v = k \cdot f_s^{\,a} \cdot B_p^{\,\beta} \quad . \tag{18}$$

Coefficients k, a and β are specific for each magnetic material and they vary mainly with the frequency and temperature. The coefficients for the nanocrystalline material, at 100°C, are: a = 1.3, β = 2.07 and $k = 4.04 \cdot 10^{-5}$ (loss density is given in kW/m^3).

3.6 Copper losses

Given the size of the magnetic devices, low frequency copper losses can be calculated using the DC resistance of the windings. However, the current ripple generates high frequency copper losses which can only be approximated by analytical calculations. This work has used the formulas developed by Dowell [10] to calculate the AC resistance R_{ACm} at a given frequency.

Copper losses have to be calculated for each switching period given that the ripple amplitude and waveform change with the duty cycle [Eqs. (1) to (4)]. Additionally, the current ripple is mainly triangular which means that it contains several harmonics. Each harmonic frequency has a corresponding AC resistance. Therefore, the AC resistance has to be calculated not only for the switching frequency (in the case of an inductor) or for twice the switching frequency (in the case of the ICT), but also for all the important harmonics. Total copper losses can be calculated according to the following equation:

$$P_c = R_{DC} \cdot I_{LF,rms}^{\,2} + \sum_{m=1}^{\infty} R_{ACm} \cdot I_{m,rms}^{\,2} \tag{19}$$

where $I_{LF,rms}$ is the *rms* value of the current at the fundamental frequency (50Hz) and $I_{m,rms}$ is the *rms* value of the m^{th} harmonic of the high frequency current flowing through the windings.

ISBN 978-3-8007-3414-6

Although this approach may result in some inaccuracies on the AC copper loss calculation, the inductor and ICT designs remain largely unchanged since low frequency copper losses are dominating.

3.7 Thermal calculation

After calculating the copper and the core losses, the ICT and inductor temperatures must be estimated. Since the components show a low volume (and thus have a high surface to volume ratio), no active cooling is necessary to achieve high values of power density. A simple model considering a unique temperature for the whole magnetic component is used. The total heat exchange area (S_{exc}) of the magnetic component is calculated considering all copper and core surfaces which are in direct contact with the air. This is used to calculate the overall temperature rise (T_c) of the magnetic component according to

$$T_c = \frac{P_t}{S_{exc} \cdot H_{exc}} \quad , \tag{20}$$

where P_t is the total losses dissipated by the magnetic component and H_{exc} is a thermal exchange coefficient which takes into account natural convection and radiation effects at high temperatures. This coefficient is usually between 5 and 15W/m^2·K [11] and here it is considered equal to 12W/m^2·K given the high core temperature.

4 Results

The main results of the system design for all configurations are compiled in **Tab. 2**. The total volume accounts for the volume of the heatsink, the capacitors and all magnetic components (individual inductors and ICTs).

Parameter	Config. 1	Config. 2	Config. 3
Si area (mm^2)	251	251	251
Si losses (W)	317	328	328
Heatsink vol. (cm^3)	502	493	493
$L_{f,x}$ (mH)	1.33	2.66	0.33
$C_{f,x}$ (µF)	6.94	7.36	29.5
Inductor vol. (cm^3)	978	1716	292
ICT vol. (cm^3)	-	-	303
Capacitor vol. (cm^3)	117	123	490
(L + C) losses (W)	69.1	91.0	46.5
Total vol. (cm^3)	1597	2300	1578
Power dens. (kW/dm^3)	6.27	4.35	6.34
Efficiency	0.963	0.960	0.964

Tab. 2 System design results for configurations 1, 2 and 3. Volumes and losses are given for a total of three-phases. Row "Total vol. (cm^3)" accounts for the volume of the heatsink, the capacitors and all magnetic components.

4.1 Filter design method verification

Simulations of the three configurations were performed for filter component values according to **Tab. 2**. The simulated output voltage ($u_{c,x}$) of each configuration was fed into a EMI Test Receiver simulator and the resulting curves are shown in **Fig. 6**. The output signals of the EMI Test Receiver simulator are for all configurations at least 7dB below the CISPR Class A limit [1] at the design frequency (160kHz). This difference is smaller than the 10dB *Margin* used in the design and higher than 4dB, which is the difference between the *Margin* (10dB) and the maximum error (6dB) calculated by using the filter design approach [9]. This verifies the accuracy of the method.

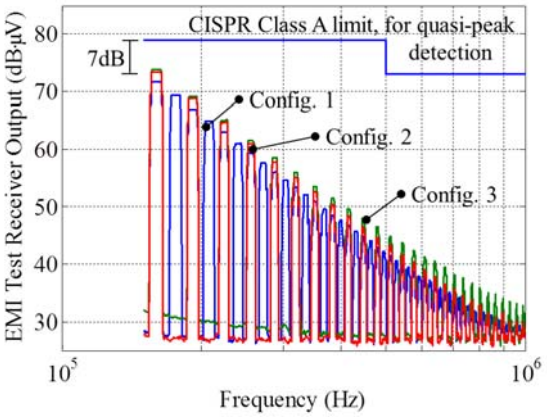

Fig. 6 Output of EMI Test Receiver simulator for the 3 configurations. The maximum noise (at 160kHz) is 7dB below the CISPR Class A limit.

4.2 Converter comparison

Tab. 2 shows that configurations 1 and 3 have very similar total volume and losses, although the distribution of the volumes are different among the components, as illustrated in **Fig. 7a** and **Fig. 7b**. The design criterion of same relative current ripple in the bridge legs forces the inductance of configuration 3 to be 4 times smaller than the one of configuration 1 but the total volume of the magnetic components is only 1.5 times smaller, given that configuration 3 uses an extra ICT (when compared to configuration 1).

Configuration 2 has two inductors with twice the inductance of configuration 1, but carrying half the current. Although the stored energy in the inductors is the same for these two configurations, building 2 inductors naturally leads to higher volumes (75% higher in this case).

All the configurations require about the same attenuation, as shown in **Section 3.3**. Thus, since configuration 3 has 4 times less inductance than configuration 1, it has about 4 times higher capacitance. For the given inductor and capacitor technologies, the increase in the capacitance volume in configuration 3 compensates the reduction of magnetic component volume when compared to configuration 1.

If the converter would be allowed to switch at frequencies in the audible range, the total volume of configurations 1 and 3 would be different as shown in **Fig. 8**. The whole converter design was performed for different frequencies but the same constraints as before. **Fig. 8** shows the efficiency and the power density calculated for frequencies from 6 to 32kHz, in 1kHz steps. The steps of the curves shown in this figure are due to the step in the required capacitance values given that the rank m of the harmonic considered in the filter design (at frequency f_d) is changed when different switching frequencies are considered. For this reason, the steps are more pronounced in the curve related to configuration 3, since it always requires a higher capacitance than configuration 1.

ISBN 978-3-8007-3414-6

Note that for minimum volume (and maximum power density), the optimal switching frequency for configuration 1 is equal to 16kHz while it is equal to 12kHz for configuration 3. At the optimal switching frequency, configuration 3 presents a total volume and losses around 14% smaller than that of configuration 1. At the optimal switching frequency, if the volume of configuration 3 is scaled to the volume of configuration 1, configuration 3 could provide about 11% more power than configuration 1.
Switching losses and the heatsink volume are decreased with the switching frequency reduction. The inductor and ICT volumes increase due to the current ripple criterion and the capacitor volume decreases due to EMI limit criterion. Thus, at the optimal frequency, the total magnetic components volume is similar to the sum of the capacitors and heatsink volumes, as it can be seen in **Fig. 7c**, where the volume of the components of configuration 3 is illustrated for the optimal switching frequency (12kHz).

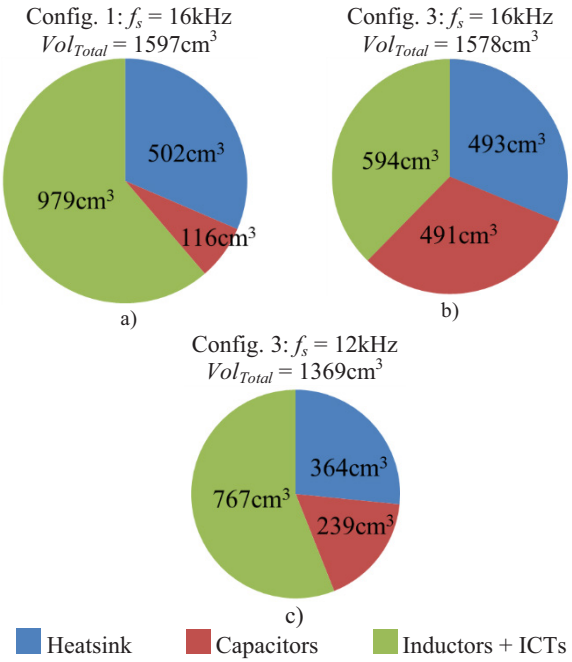

Fig. 7 Volume of each main part of the designed systems for the nominal switching frequency [for a) configuration 1 and b) configuration 3], and for the optimal switching frequency reducing the total volume [for c) Configuration 3].

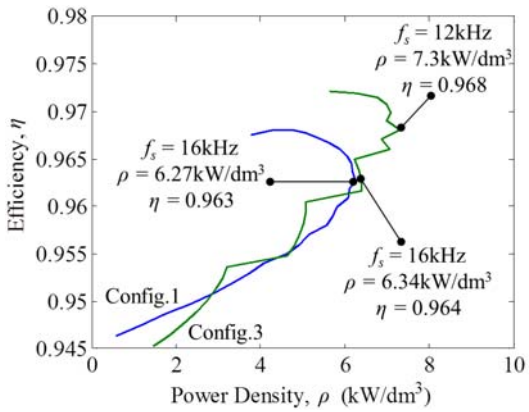

Fig. 8 Efficiency versus power density of the systems of configuration 1 and 3, for a frequency variation from 6 to 32kHz.

4.3 Discussion

References [2,3,12] show that converters with interleaved bridge legs have several advantages if using ICTs instead of regular inductors, e.g. low current ripple in the bridge legs and reduction of the total magnetic component size. The latter is observed in the comparison presented in this paper. References [2,12] also report a significant reduction on the magnetic component weight if a single bridge leg with inductor is replaced by two or more interleaved bridge legs with ICTs.
For the results shown in **Tab. 2**, this also could be noted since the magnetic components of configuration 3 have about 60% of the size of the inductors of configuration 1. However, higher capacitance is required in configuration 3 for EMI standard compliance and thus the total volume of configurations 1 and 3 are about the same. Configuration 3 could have significant lower volume when compared to configuration 1 at 3 different situations:
1 – Different magnetic materials: Nanocrystalline material used in the comparison has high performance at high frequency and may achieve high saturation flux density. It is also very expensive. For reducing the costs, ferrite could be used, which however would result in a significant larger volume of the inductors and the ICT. In a rough estimation, if a maximum allowed flux density of 0.25T is considered for ferrite, ICT and inductors would be around 3 times bigger than the ones made with nanocrystalline material. Like this, the total volume of configuration 1 would be 28% higher than that of configuration 3, for the same conditions used in the comparison of this paper.
2 – Lower allowed current ripple: Many authors design converters with a maximum relative current ripple lower than ±20% of the low frequency current peak value. For example, [13] considers ±10% in order to have good controllability of the system. If this maximum ripple value would be considered in the systems compared here, inductances would be two times higher and the magnetic component volumes would be about twice. Like this the total volume of configuration 1 would be 19% higher than that of configuration 3.
3 – Different criteria for defining the output filter: In this paper, an EMI standard together with a maximum current ripple in each bridge leg is defining the output filter characteristic. If other criteria are used, e.g., maximum THD or ripple in the output voltage, configuration 3 could have a great advantage. For example, if the same maximum current ripple is considered and if a maximum peak-to-peak voltage ripple of 1% of the output voltage would be allowed over the output capacitor, the capacitance needed for configuration 1 would be equal to 8µF while it would be equal to 4µF for configuration 3 (since the frequency of the current ripple is twice the switching frequency in the interleaved case). Like this the total volume of configuration 1 would be 29% higher than that of configuration 3.

5 Conclusions

The minimization of the output filter inductance is one of the key objectives when designing converters for applications where high compactness is requires. This paper evaluated 3 different configurations of 16kHz/10kVA inverters composed by single or two interleaved bridge legs.

ISBN 978-3-8007-3414-6

Since configuration 1 uses a single bridge leg and configurations 2 and 3 use 2 interleaved bridge legs, the comparison is based on the same total silicon area for each configuration. Thus, approximately the same semiconductor losses and heatsink volume is calculated for all configurations.

The output filter is designed considering two criteria: 1) the same maximum relative current ripple in each bridge leg, which mainly influences the inductor and ICT design; 2) Compliance of the output voltage harmonics with EMI standards, which mainly impacts the size of the output capacitors.

A simplified procedure to guarantee harmonic voltages lower than EMI limits was presented. The method is based on the simulation or calculation of the total *rms* voltage of harmonics at the output of the bridge legs. Here analytical formulas are derived to calculate these voltages for a single bridge leg or two interleaved bridge legs, which turns out to be the same as for a single 3-level bridge leg.

Results show that the simplified procedure to calculate the filter values is effective since the simulated systems presented the harmonic content below the EMI limits, as predicted.

After calculation of the required inductances and capacitances, the capacitor volumes were determined based on available commercial film capacitors. However, inductors and ICTs are not readily found in the market and so these components were optimized for minimum volume, using high performance magnetic material (nanocrystalline).

Optimization results show that configuration 2 (with interleaved bridge legs and regular inductors) requires approximately a 45% higher volume than the other two configurations.

Configurations 1 and 3, respectively the one with a single bridge leg and the one with two interleaved bridge legs and an ICT, presented similar total volumes. However, the first has magnetic components 65% larger than the latter resulting in a more expensive converter.

Finally, the switching frequency of varied for both configurations from 6 to 32kHz and the optimal frequencies were determined. At these frequencies, configuration 3 presented a 14% lower volume and lower losses than configuration 1. This difference could be higher if low cost ferrite cores are used and a lower current ripple is tolerated in the bridge legs.

6 References

[1] *Specification for radio disturbance and immunity measuring apparatus and methods part ii: methods of measurement of disturbance and immunity-publication 16*, CISPR, Geneva, Switzerland, 1999.

[2] T. Meynard, F. Forest, E. Laboure, V. Costan, A. Cuniere, and E. Sarraute, “Monolithic magnetic couplers for interleaved converters with high number of cells,” IEEE CIPS, Naples, Italy, June 2006.

[3] F. Forest, E. Laboure, T. Meynard, V. Smet, “Design and comparison of inductors and intercell transformers for filtering of PWM inverter output,” IEEE Trans. on Power Electron., vol. 24, n. 3, pp. 812-821, Mar. 2009.

[4] M. Schweizer, I. Lizama, T. Friedli, J. W. Kolar, “Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies,” IEEE IECON, Phoenix, USA, November, 2010.

[5] U. Drofenik, J. W. Kolar, “Analyzing the theoretical limits of forced air-cooling by employing advanced composite materials with thermal conductivities > 400W/mK,” IEEE CIPS, Naples, Italy, June 2006.

[6] B. Cougo, “Design and optimization of intercell transformers for parallel multicell converters” PhD dissertation, INP Toulouse, France, 2010.

[7] *Information technology equipment—radio disturbance characteristics—limits and methods of measurement—publication 22*, CISPR, Geneva, Switzerland, 1997.

[8] J. Wang, W. G. Dunford, and K. Mauch, “Analysis of a ripple-free input current boost converter with discontinuous conduction characteristics,” IEEE Trans. Power Electron., vol. 12, n. 4, pp. 684–694, Jul. 1997.

[9] K. Raggl, T. Nussbaumer, J. W. Kolar, “Guideline for a simplified differential-mode EMI filter design,” IEEE Trans. Indust. Electron., vol. 57, n. 3, pp. 1031–1040, Mar. 2010.

[10] P. L. Dowell, “Effect of eddy currents in transformer windings,” Proceedings IEE (UK), vol. 113, n. 8, pp. 1387-1394, 1966.

[11] J. Biela, J. W. Kolar, “Cooling concepts for high power density magnetic devices,” IEEJ/IEEE PCC, Nagoya, Japan, 2007.

[12] B. Cougo, T. Meynard, F. Forest, E. Laboure, “Parallel multicell converters for high current: Design of intercell transformers” IEEE ICIT, Vina del Mar, Chile, 2010.

[13] J. Mühlethaler, M. Schweizer, R. Blattmann, J. W. Kolar, A. Ecklebe, “Optimal design of LCL harmonic filters for three-phase PFC rectifiers,” IEEE IECON, Melbourne, Australia, Nov. 2011.

ISBN 978-3-8007-3414-6