Power Electronic Systems
Laboratory

IEEE Transactions on Power Electronics, Vol. 28, No. 1, pp. 7-13, January 2013

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Letters

Hybrid Active Third-Harmonic Current Injection Mains Interface Concept for DC Distribution Systems

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***Abstract*—This paper presents the design and implementation of a three-phase high power factor mains interface concept appropriate for many power electronic applications such as supplies for dc power distribution systems in telecommunication, electric vehicle battery charging, future more electric aircraft, variable-speed ac drives, and high power lighting systems. The circuit topology comprises a buck-type power factor correction rectifier circuit built by the combination of an active third-harmonic injection rectifier and a series-connected dc–dc buck-type converter. The characteristics of this rectifier topology, including the principles of operation, modulation strategy, suitable control structure, and dimensioning equations, are described in this paper. The feasibility of the presented converter for buck-type rectifier applications is demonstrated by means of a constructed hardware prototype.**

***Index Terms*—Active third-harmonic current injection, buck-type power factor correction converter, rectifier systems.**

I. Introduction

A SUITABLE 400-V dc power distribution architecture for telecom and/or data center applications is shown in Fig. 1 [1]. There, a unidirectional three-phase power factor correction (PFC) rectifier is utilized as mains interface circuit in order to power the telecom equipment at the dc side with controlled voltage, while at the ac side, high-power-factor operation is maintained. If isolation of the dc bus from the PFC rectifier is required for safety reasons, this can be facilitated by an isolated dc–dc converter connected in series, which can additionally be used for voltage regulation.

In the European market with the typical three-phase 400 V (line-to-line rms voltage) ac mains, boost-type PFC rectifiers produce an output voltage (typically 700–800 V) that is too high to directly feed the telecom 400-V dc bus and thus call for a step-down dc–dc converter at their output even if no isolation is required. On the other hand, buck-type PFCs, see Fig. 2, are particularly interesting because they provide a wide output voltage control range, while maintaining PFC capability at the input, enable direct start-up, and allow for current limitation in case of an output short circuit [2].

Recent discussions about three-phase buck-type PFC systems [3]–[6] have identified topologies based on third-harmonic

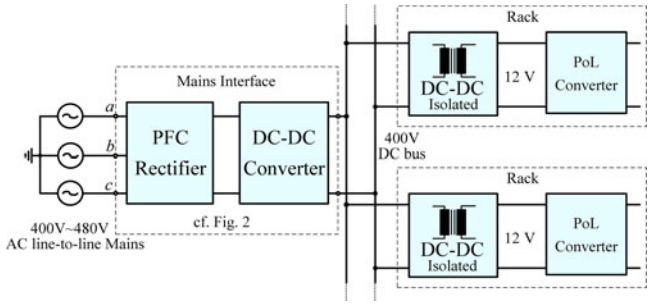

Fig. 1. Possible 400-V dc distribution architecture for telecom and/or data center applications [1].

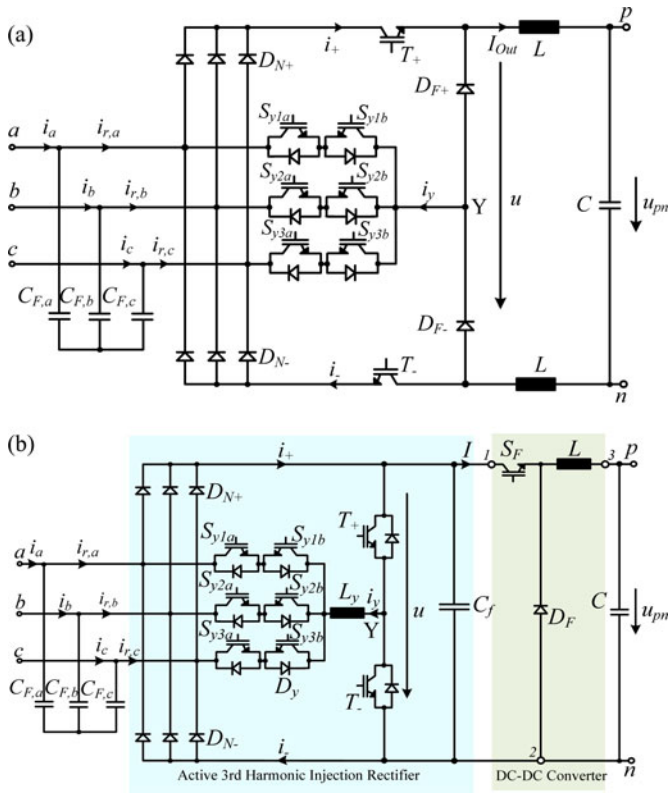

Fig. 2. Basic structure of three-phase buck-type PFC rectifiers employing an active third-harmonic current injection circuit: (a) SR and (b) H3R.

Manuscript received February 16, 2012; revised May 27, 2012; accepted July 15, 2012. Date of current version September 11, 2012. Recommended for publication by Associate Editor R. Ayyanar.

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Digital Object Identifier 10.1109/TPEL.2012.2209897

current injection circuit appropriate for mains interface of dc distribution architectures. The circuit schematic depicted in Fig. 2(a), also referred as the SWISS rectifier (SR), is a remarkable example, as for some operation conditions it can achieve a superior efficiency performance than conventional buck-type structures, i.e., at high switching frequencies. In fact, the main advantage of the SR is not only seen in the higher achievable efficiency but also that the system can be controlled similarly to a dc–dc converter. Accordingly, basic knowledge of the function of a buck-type dc–dc converter and a three-phase passive diode rectifier is sufficient to implement a three-phase PFC rectifier with sinusoidal input currents and a controlled output voltage. For more details about this converter concept, the interested reader is referred to [6] and [7], where this system was comprehensively studied.

Another interesting three-phase buck-type PFC rectifier is depicted in Fig. 2(b) [3], [4]. This circuit, referred to here as hybrid active third-harmonic injection buck-type rectifier (H3R) combines an active current injection electrolytic capacitor-less converter (front-end) with a series-connected dc–dc buck-type converter (back-end). The main advantage of this concept over conventional buck-type PFCs is that only a single power transistor S_F and two line-commuted diodes $D_{N+/-}$ exist in the main current path, which leads to low conduction losses. Additionally, the components in the injection circuit require relatively low current rating devices, i.e., the maximum value of the flowing current is rated half the amplitude of the sinusoidal input current.

The front-end circuit concept of the H3R system was first introduced in late 90s by Jantsch and Verhoeve [8], where three-phase grid-connected photovoltaic inverters without electrolytic capacitor for improved lifetime were proposed. In [3], this topology was implemented as an auxiliary circuit to attenuate the input current harmonics of a conventional diode rectifier-fed inverter having a very small dc-link capacitor. Thus, that system did not provide the full functionality of an output voltage-regulated PFC rectifier and critical operating conditions could damage the system reliability, i.e., problems could occur due to the low energy storage during short-term input voltage interruption or during load variations which would be passed on directly to the mains. Only recently the full potential of the H3R circuit has been investigated (cf., [5]), but no hardware implementation with experimental results validating the proposed circuit analyses has been shown. Additionally, a general guideline for the H3R system design, dealing with some implementation issues, such as a distinct modulation of the current injection circuit providing the required uninterrupted current flow, is still missing in the literature.

In this paper, after the explanation of the structural characteristics as well as the calculation of the relative on-times of the active switches guaranteeing PFC operation of the H3R in Section II, a pulsewidth modulation (PWM)-control method and modulation strategy for robust operation are proposed in Section III. The analytical equations for calculating the stresses of the main semiconductors and passive components with dependence on the input current amplitude and the voltage transfer ratio of the converter as required for the design of the converter are given in Section IV. Finally, a 5-kW hardware prototype is designed to attest the feasibility of the H3R rectifier concept. This system was strategically designed to enable operation as the SR by only performing small changes in the prototype circuit. Therefore, the H3R and SR systems are compared regarding the measured efficiency, current total harmonic distortion (THD), and power factor.

II. HYBRID ACTIVE THIRD-HARMONIC CURRENT INJECTION BUCK-TYPE PFC RECTIFIER

The basic configuration of a three-phase high-power-factor rectifier solution is shown in Fig. 2(b). The front-end converter consists of a three-phase electrolytic capacitor-less line-commuted rectifier combined with an active current injection circuit, which is formed only by a single fast-commuted half-bridge-leg, a phase inductor, and three low-frequency bidirectional switches. Accordingly, this circuit shows a relatively low implementation effort, however, at the expense of a missing output voltage control. The output voltage *u* is now determined directly by the diode bridge rectifier and hence exhibits a six-pulse shape. Therefore, a series-connected dc–dc converter (back-end) is necessary to provide the required dc-bus voltage level regulation and/or dynamic current limitation.

The high-power-factor operation is assured by the back-end converter, which needs to be controlled to demand (fundamental) constant power *P* and no smoothing capacitor of higher capacitance C_f is connected to the dc link. In this case, currents *I* varying in opposite phase to the six-pulse rectifier voltage will be impressed at the output of the front-end converter. This leads to a sinusoidal shape of all mains phase currents after overlaying with the currents of the injection current circuit (i_y, i_+, and i_-).

Although the capacitor C_f can degrade the sinusoidal controllability of the mains currents, a minimum capacitance value is required for proper converter operation. For some conduction states, this component provides the necessary current path for the imposed injection current i_y. This characteristic can be seen in the conduction state depicted in Fig. 3(b) valid for the mains interval [0, 30°] ($u_a > u_b > u_c$). There, the value of C_f should also be selected to limit the rise of the voltage at the output of the diode bridge.

As illustrated in Fig. 3, the implementation of this system with a simple dc–dc buck converter is very attractive as few active switches in the main current path exist (only the single power transistor S_F), leading to low conduction losses, i.e., in particular at high output voltages with a relatively short freewheeling interval. In addition, the negative output voltage terminal is always connected to the mains via a diode of the rectifier. Therefore, no output common-mode (CM) voltage with switching frequency is generated. The implementation effort of the CM EMI filter can thus be reduced as only the parasitic capacitors of the power semiconductors lead to high-frequency CM noise currents.

Note that the buck dc–dc converter unit and the four-quadrant switches can be replaced by other typical power electronic circuits. For example, the line-commutated injection switches could be implemented with an antiparallel connection of reverse

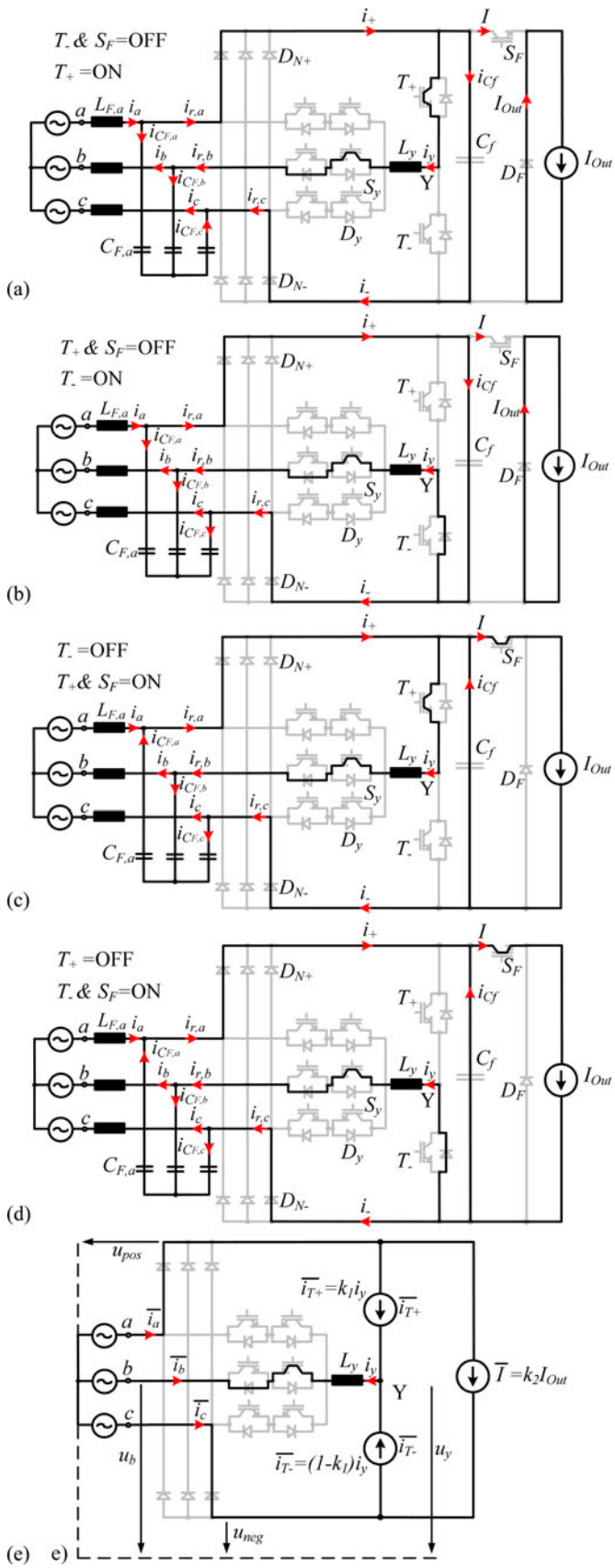

Fig. 3. (a)–(d) Conduction states and (e) equivalent circuit of the rectifier for $u_a > u_b > u_c$.

blocking insulated bipolar transistors (IGBTs) with a low forward voltage drop. Additionally, if converter isolation and/or further voltage level regulation is necessary, another dc–dc converter with galvanic isolation could be used to replace the simple buck-type circuit. A bidirectional implementation can be accomplished by adding discrete IGBTs in parallel to the line diodes $D_{N+/-}$ and fast diode D_F, while an auxiliary fast diode would be required in parallel to S_F [9]. Finally, in applications such as high-power electric vehicle battery charging and variable-speed ac drives, interleaved dc–dc converters, resonant topologies, or multiphase inverters could be advantageously utilized as replacement for the simple dc–dc buck converter.

For proof of the sinusoidal controllability of the mains currents, the four conduction states and equivalent circuit of the H3R circuit valid for the mains interval [0, 30°] ($u_a > u_b > u_c$) are considered for analysis (cf., Fig. 3). Ideally, the rectifier system operates as a symmetric three-phase load of phase conductance G to the mains; therefore, the value of the current to be injected into phase b may be written as

$$i_y = -\bar{i}_b = -Gu_b. \tag{1}$$

The mains frequency voltage drop across the inductor of the current injection circuit can in a first approximation be neglected for the formation of i_y

$$u_L = 0. \tag{2}$$

Accordingly, the voltage formed at the output of the bridge leg will be given by

$$u_y = u_b. \tag{3}$$

If the voltage at the terminal Y is formed according to the relative on-time of the transistor T_+ as k_1 and T_- as $(1-k_1)$, it will result in

$$u_y = k_1 u_a + (1-k_1)\, u_c = k_1 u_{ac} + u_c. \tag{4}$$

For the duty cycle k_1 given by

$$u_{\text{pos}} = \max(u_a, u_b, u_c) \tag{5}$$

$$u_{\text{neg}} = \min(u_a, u_b, u_c) \tag{6}$$

$$k_1 = \frac{-(u_{\text{pos}} + 2u_{\text{neg}})}{u_{\text{pos}} - u_{\text{neg}}} = \frac{u_{bc}}{u_{ac}} \tag{7}$$

the current across T_+ can be calculated as

$$\bar{i}_{T+} = k_1 i_y = -k_1 \bar{i}_b = -k_1 G u_b = -G u_b \frac{u_{bc}}{u_{ac}}. \tag{8}$$

Considering the fundamental input currents that have to be generated at the input

$$\bar{i}_a = Gu_a, \quad \bar{i}_b = Gu_b, \quad \text{and} \quad \bar{i}_c = Gu_c \tag{9}$$

and the current consumption of the constant power load as

$$\bar{I} = k_2 I_{\text{Out}} \quad \text{with} \quad k_2 = \frac{u_{pn}}{u_{\text{pos}} - u_{\text{neg}}} \tag{10}$$

gives

$$\bar{I} = \frac{P}{u_{ac}} = \frac{\bar{i}_a u_{ac} + \bar{i}_b u_{bc}}{u_{ac}} = G\frac{u_a u_{ac} + u_b u_{bc}}{u_{ac}}. \tag{11}$$

TABLE I
MODULATION OF THE CURRENT INJECTION CIRCUIT AND DUTY CYCLE CALCULATION FOR PFC OPERATION (CF., FIG. 4)

Sector	k_1	k_2	S_{y1a}	S_{y1b}	S_{y2a}	S_{y2b}	S_{y3a}	S_{y3b}
0°-30°	u_{bc}/u_{ac}	u_{pn}^*/u_{ac}	0	0	1	1	0	0
30°-60°	u_{bc}/u_{ac}	u_{pn}^*/u_{ac}	0	0	1	1	0	0
60°-90°	u_{ac}/u_{bc}	u_{pn}^*/u_{bc}	1	1	0	0	0	0
90°-120°	u_{ac}/u_{bc}	u_{pn}^*/u_{bc}	1	1	0	0	0	0
120°-150°	u_{ca}/u_{ba}	u_{pn}^*/u_{ba}	0	0	0	0	1	1
150°-180°	u_{ca}/u_{ba}	u_{pn}^*/u_{ba}	0	0	0	0	1	1
180°-210°	u_{ba}/u_{ca}	u_{pn}^*/u_{ca}	0	0	1	1	0	0
210°-240°	u_{ba}/u_{ca}	u_{pn}^*/u_{ca}	0	0	1	1	0	0
240°-270°	u_{ab}/u_{cb}	u_{pn}^*/u_{cb}	1	1	0	0	0	0
270°-300°	u_{ab}/u_{cb}	u_{pn}^*/u_{cb}	1	1	0	0	0	0
300°-330°	u_{cb}/u_{ab}	u_{pn}^*/u_{ab}	0	0	0	0	1	1
330°-360°	u_{cb}/u_{ab}	u_{pn}^*/u_{ab}	0	0	0	0	1	1

The resultant low-frequency current drawn from phase a is therefore proportional to the mains voltage

$$\bar{i}_a = \bar{I} + \bar{i}_{T+} = G u_a . \tag{12}$$

Additionally, the low-frequency current for phase c can be determined using (1), (12), $\bar{i}_a + \bar{i}_b + \bar{i}_c = 0$, and $u_a + u_b + u_c = 0$

$$\bar{i}_c = G u_c . \tag{13}$$

Therefore, sinusoidal shape of all phase currents for the mains interval [0, 30°] ($u_a > u_b > u_c$) has been proven.

Finally, high-power-factor operation and controlled output voltage u_{pn} for all mains sector can be achieved with the relative on-times k_1, $(1-k_1)$ and k_2 of the power transistors T_+/T_- and S_F given in Table I (cf., Fig. 4). These variables are reliant on the instantaneous values of the mains voltages $u_{a,b,c}$ converted to line-to-line quantities and the output voltage reference u^*_{pn}.

III. PWM CONTROL SCHEME

A possible implementation of a control scheme for the H3R circuit is shown in Fig. 5, and consists of two control loops: one for the dc–dc converter, corresponding to the constant-power load, and a second for the injection circuit, controlling the voltage applied across L_y, thus regulating the current injected back into the mains phases.

The modulation of the current injection circuit is performed at low frequency (twice the input frequency, with two 60° conduction periods within a period), following the rectifier input voltages $u_{a,b,c}$ in such a way that the active current injection always occurs into only one mains phase as presented in Table I (cf., Fig. 4). Due to the requirement of uninterrupted current flow through the inductor L_y, while still allowing a dead-time preventing short circuits between the individual phases, the modulation depicted in Fig. 4 is implemented. Auxiliary free-wheeling diodes D_{FW1} and D_{FW2} can also be placed as alternative or supplementary protection to the current injection switches. Ideally, D_{FW1} and D_{FW2} never conduct.

IV. MAIN DESIGN EXPRESSIONS

In this section, the main expressions for designing the H3R rectifier, which models the stresses of the active and passive components, are given. These are functions of the modulation index M, the output voltage u_{pn}, amplitude of the sinusoidal input current $\hat{I}_N$, and output current I_{Out}. There, it is assumed that the rectifiers have a purely sinusoidal phase current shape; ohmic mains behavior, no low-frequency voltage drop across the inductors; and a switching frequency f_P, which is much higher than the mains frequency f_N ($f_P \gg f_N$).

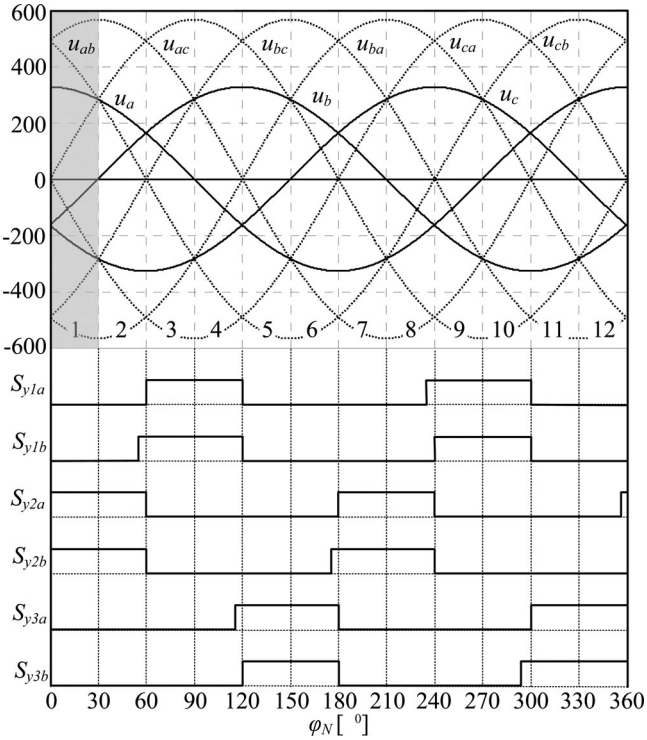

Fig. 4. Mains sectors 1–12 defined by the different relations of the instantaneous values of the mains phase voltages $u_{a,b,c}$ and respective gate signals of the third-harmonic injection circuit switches providing the injection current logic and the required uninterrupted current path for L_y.

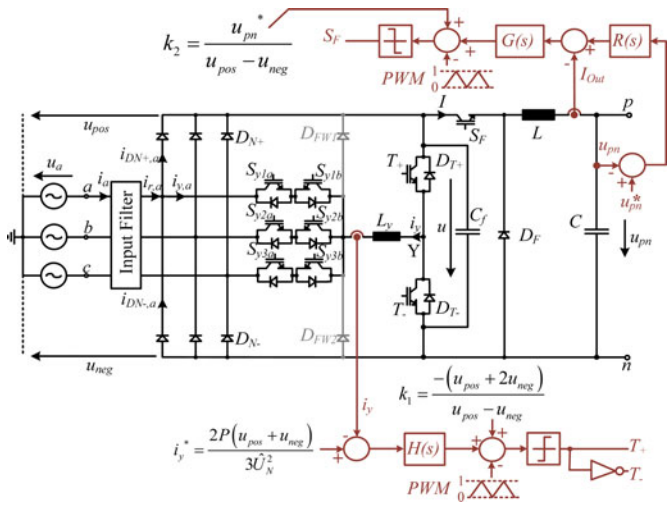

Fig. 5. Control structure for the H3R rectifier. The modulation/on-time of the current injection circuit is given in Table I. $\hat{U}_N$ and u^*_{pn} are the amplitude of the input phase voltage and output voltage reference, respectively.

A. Semiconductor Voltage and Current Stresses

The bidirectional switches S_y and D_y have to block a maximum voltage which corresponds to the 60° sinusoidal progression of the maximum line-to-line input voltage $u_{N,l-l,\max}$

$$u_{N,l-l,\max} = \sqrt{2}\sqrt{3}u_{a,\mathrm{rms},\max} \tag{14}$$

$$u_{Sy,\max} = \frac{\sqrt{3}}{2}u_{N,l-l,\max}. \tag{15}$$

All the remaining semiconductors (T_+, T_-, D_T+, D_T-, D_N+, D_N, S_F, and D_F) have to block the voltage $u_{N,l-l,max}$.

The average and rms currents of the transistors and diodes can be determined as follows:

$$I_{\frac{Dy}{Sy},\mathrm{avg}} = \hat{I}_N\frac{2-\sqrt{3}}{2\pi} \quad \text{and} \quad I_{\frac{Dy}{Sy},\mathrm{rms}} = \hat{I}_N\sqrt{\frac{1}{12}-\frac{\sqrt{3}}{8\pi}} \tag{16}$$

$$I_{DN,\mathrm{avg}} = \hat{I}_N\frac{\sqrt{3}}{2\pi} \quad \text{and} \quad I_{DN,\mathrm{rms}} = \hat{I}_N\sqrt{\frac{1}{6}+\frac{\sqrt{3}}{8\pi}} \tag{17}$$

$$I_{DT,\mathrm{avg}} = \frac{\hat{I}_N}{5\pi}\left(12-6\sqrt{3}\right) \text{ and}$$

$$I_{DT,\mathrm{rms}} = \hat{I}_N\sqrt{\frac{1}{8}+\frac{3\sqrt{3}}{4\pi}\left(\ln\left(\frac{4}{3}\right)-\frac{1}{2}\right)} \tag{18}$$

$$M = \frac{2}{3}\frac{u_{pn}}{\hat{U}_N} \tag{19}$$

$$I_{DF,\mathrm{avg}} = I_{\mathrm{Out}}\left(1+\frac{3\sqrt{3}M}{2\pi}\ln\left(\frac{1}{3}\right)\right) \quad \text{and}$$

$$I_{DF,\mathrm{rms}} = I_{\mathrm{Out}}\sqrt{1+\frac{3\sqrt{3}M}{2\pi}\ln\left(\frac{1}{3}\right)} \tag{20}$$

$$I_{T,\mathrm{avg}} = \frac{3\hat{I}_N}{4\pi}\left(2+\sqrt{3}\ln\left(\frac{1}{3}\right)\right) \text{ and}$$

$$I_{T,\mathrm{rms}} = \hat{I}_N\sqrt{\frac{1}{8}+\frac{3\sqrt{3}}{4\pi}\ln\left(\frac{3}{4}\right)} \tag{21}$$

$$I_{SF,\mathrm{avg}} = \frac{-3\sqrt{3}I_{\mathrm{Out}}M}{2\pi}\ln\left(\frac{1}{3}\right) \text{ and}$$

$$I_{SF,\mathrm{rms}} = I_{\mathrm{Out}}\sqrt{-\frac{3\sqrt{3}M}{2\pi}\ln\left(\frac{1}{3}\right)}. \tag{22}$$

B. Passive Components Stresses

The current flowing through *L* is defined by the full dc (load) current and a current ripple $\Delta i_{L,\mathrm{pp},\max}$ which is limited to a given value, i.e., 25% of I_{Out}. The current stresses across *L* are determined by

$$I_{\mathrm{Out}} = \frac{P}{u_{pn}} \tag{23}$$

$$\Delta i_{L,pp,\max} = \frac{u_{pn}}{Lf_P}\left(1-\frac{\sqrt{3}}{2}M\right) \tag{24}$$

$$i_{L,\mathrm{rms}} = \sqrt{I_{\mathrm{Out}}^2+\frac{\Delta i_{L,pp,\max}^2}{12}} \tag{25}$$

$$L \geq \frac{u_{pn}}{\Delta i_{L,pp,\max}f_P}\left(1-\frac{\sqrt{3}}{2}M\right). \tag{26}$$

The voltage and important current quantities across the current injection inductor L_y are equivalent to

$$u_{Ly} = \sqrt{\frac{3}{2}}u_{N,l-l,\max} \tag{27}$$

$$i_{Ly,\mathrm{pk}} = \frac{\hat{I}_N}{2} \tag{28}$$

$$i_{Ly,\mathrm{rms}} = \hat{I}_N\sqrt{\frac{1}{2}-\frac{3\sqrt{3}}{4\pi}} \tag{29}$$

$$\Delta i_{Ly,pp,\max} = \frac{\sqrt{2}\sqrt{3}u_{a,\mathrm{rms}}}{4L_yf_P} \tag{30}$$

$$L_y \geq \frac{\sqrt{2}\sqrt{3}u_{a,\mathrm{rms}}}{4\Delta i_{Ly,pp,\max}f_P}. \tag{31}$$

When selecting the output capacitor *C*, the value of u_{pn} and an additional safety margin, i.e., 10% of u_{pn}, must be taken into consideration

$$u_C > 1.1u_{pn}. \tag{32}$$

The rms value of the capacitor current ripple $\Delta i_{C,\mathrm{rms}}$ and the peak-to-peak value of the voltage ripple $\Delta u_{C,pp}$ are given by

$$\Delta i_{C,\mathrm{rms}} = \sqrt{\frac{\Delta i_{L,pp,\max}^2}{12}} \quad \text{and}$$

$$\Delta u_{C,pp} = \frac{u_{pn}}{16f_P^2CL}(2-\sqrt{3}M) \tag{33}$$

$$C \geq \frac{u_{pn}}{16Lf_P^2\Delta u_{C,pp}}(2-\sqrt{3}M). \tag{34}$$

The capacitor C_f is selected to limit the rise of the voltage at the output of the diode bridge *u*. A safety margin to limit the maximum voltage ripple Δu around 2.5% of *u* must be taken into consideration

$$C_f \geq \frac{\hat{I}_N}{2\Delta u_C f_S}\left(1-M_{\min}\right). \tag{35}$$

C. Rectifier Analytical Model Accuracy

In order to verify the accuracy of the derived equations modeling the voltage and current stresses of the proposed rectifier, an appropriate switching frequency and the values of the passive components according to Table II have been selected. A switching frequency of $f_P = 36$ kHz is designated as it constitutes a good compromise between high efficiency, high power density, and high control bandwidth. Advantageously, the fourth switching frequency harmonic is found near, but below the beginning of the considered electromagnetic compatibility measurement range (150 kHz). With $f_P = 36$ kHz, the values for the $L_y = 2$ mH and output filter $L = 610$ μH, $C = 470$ μF, and $C_f = 4$ μF

TABLE II
RECTIFIER SPECIFICATIONS

Input phase voltage $u_{a,b,c}$	230 V *rms* ±10%
Mains frequency f_N	50 Hz
Switching frequency f_P	36 *k*Hz
Rated output power P	5 *k*W
Output capacitor C	470 μF
Input capacitor $C_{F,i}$	4.4 μF
Input capacitor $C_{F,i}$	4 μF
DC inductor L	610 μH
Current injection inductor L_y	2 *m*H

TABLE III
COMPARISON OF ACTIVE AND PASSIVE COMPONENT STRESSES DETERMINED BY ANALYTICAL CALCULATIONS AND DIGITAL SIMULATIONS

	Analytical Calculations	Simulation	Deviation [%]
$I_{Sy,avg}/I_{Dy,avg}$	0.44	0.44	+0.00
$I_{Sy,rms}/I_{Dy,rms}$	1.23	1.28	-3.90
$I_{DN,avg}$	2.83	2.82	+0.35
$I_{DN,rms}$	4.98	5.07	-1.77
$I_{T,avg}$	0.24	0.25	-4.0
$I_{T,rms}$	0.8	0.84	-4.7
$I_{DT,avg}$	1.05	1.07	-1.87
$I_{DT,rms}$	1.98	2.03	-2.46
$I_{SF,avg}$	9.32	9.27	+0.54
$I_{SF,rms}$	10.79	10.83	+0.37
$I_{DF,avg}$	3.18	3.20	-0.62
$I_{DF,rms}$	6.31	6.32	-0.16
$\Delta i_{L,pp,max}$	5.27	5.28	-0.19
$\Delta i_{Ly,pp,max}$	1.99	1.93	+3.1

are selected. The component values of the input filter stage are $L_{F,i} = 220$ μH and $C_{F,i} = 4.4$ μF.

In Table III, the values of the average and rms component stresses calculated with the respective equations for Table II specified converter are compared to the results obtained with a digital simulation and show a good accuracy.

V. EXPERIMENTAL EVALUATION

A laboratory prototype of the hybrid active third-harmonic injection rectifier according to the specifications given in Table II has been built. The implemented prototype is shown in Fig. 6. With respect to the operating principle of the converter, the injection switches S_y, i are implemented with the latest generation Trench and Fieldstop (T&FS) IGBTs (1200 V/25 A, IKW25N120, Infineon) with an antiparallel freewheeling diode and are optimized for low conduction losses as they are switched with only twice the mains frequency. For the transistors T_+, T_-, and S_F, high-speed T&FS IGBTs (1200 V/40 A, IGW40N120H3, Infineon) are used in combination with SiC MPS diodes (1200 V/20 A, C2D20120A, CREE) for D_T+, D_T-, and D_F to enable low switching losses at the selected switching frequency of $f_P = 36$ kHz. The prototype was strategically designed to enable operation also as the SR, where due to the lower stress across the fast switches, a higher power capability can be achieved (7.5 kW).

Fig. 7(a) shows the experimental results of the H3R converter without applying the harmonic current injection method. The dc–dc buck converter (back-end) is controlled to provide constant power load at the rated output voltage and 4 kW output power. As can be seen, the input current i_a exhibits a quasi-

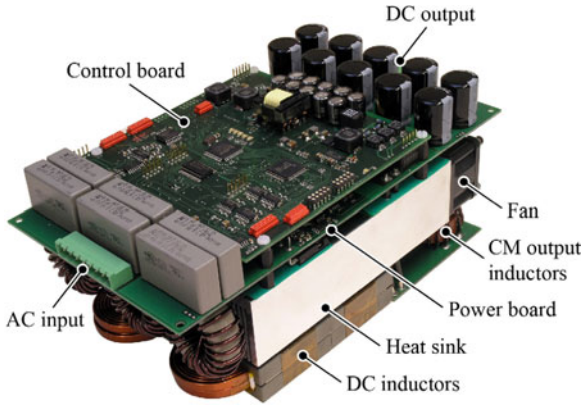

Fig. 6. Implemented H3R and SR third-harmonic current injection rectifiers.

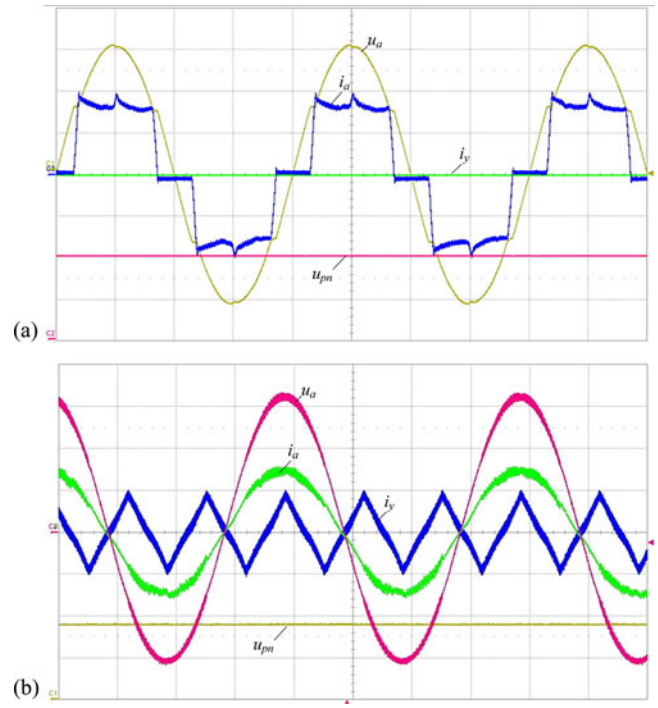

Fig. 7. H3R experimental results: operation (a) without and (b) with current injection circuit enabled. Input current i_a (5 A/div), injection current i_y (5 A/div), input voltage u_a (100 V/div), and output voltage u_{pn} (200 V/div).

square wave shape with amplitude varying in opposite phase to the six-pulse rectifier voltage (constant power load). Fig. 7(b) presents the experimental results for operation with enabled harmonic current injection circuit. The injected current is referenced and controlled as presented in Fig. 5, thus generating a sinusoidal current on the input side, without affecting the operation of the back-end converter. In this case, an input current THD of 3.7% and a power factor of $\lambda = 0.99$ have been measured using a Yokogawa WT3000 precision power analyzer.

The main waveforms for the SR operation are given in Fig. 8 for an output power of 7.5 kW, where an input current THD of 4% and a power factor of $\lambda = 0.99$ have been measured.

In Fig. 9, the efficiency measured with the H3R and SR systems is plotted for different output power operation. According

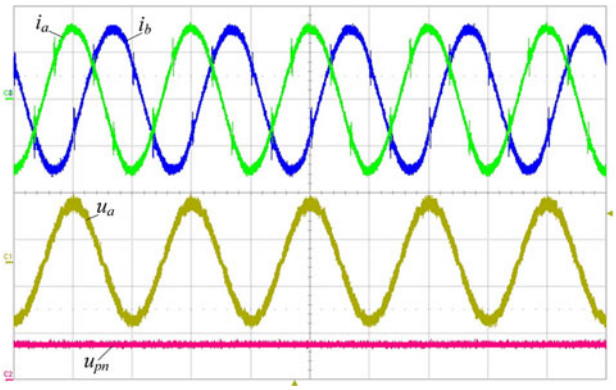

Fig. 8. SR experimental waveforms for 7.5-kW operation (i_a and i_b: 10 A/div; u_a: 250 V/div; and u_{pn}: 500 V/div).

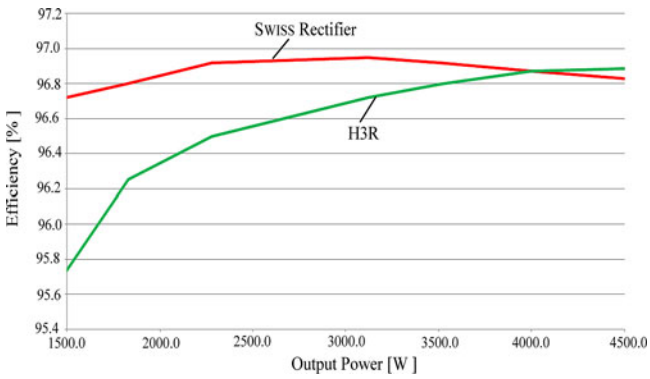

Fig. 9. Measured efficiency with the implemented prototype.

to the results, the systems can achieve very similar line power quality performance, thus validating the implementation of the systems for buck-type mains interfaces. However, the H3R display better efficiency for high power operation, while the SR has better performance for partial load operation. This efficiency result could change for different operating conditions, i.e., different switching frequencies, because intrinsically when implementing the same device technology, the SR displays a better switching loss performance, while the H3R has superior conduction loss features.

VI. Conclusion

This paper deals with the design and implementation of a three-phase buck-type PFC rectifier employing an active third-harmonic current injection rectifier. The principle of operation, the main designing expressions, suitable modulation scheme, and PWM control have been described. Additionally, a 5-kW hardware prototype has been implemented and tested in the laboratory in order to attest the feasibility of this rectifier concept. Finally, the implemented system has been compared to another remarkable buck-type rectifier, the SR.

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