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Analysis of the Design Space of Single-Stage and Two-Stage LC Output Filters of Switched-Mode AC Power Sources

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***Abstract*—This paper proposes a systematic approach to design the output filter of a 10 kW, low-voltage 400 $V_{ll,rms}$, four-output phase, hard-switched AC source based on the Three-Level Neutral Point Clamped Voltage Source Converter topology. Given specifications of the AC source, such as the voltage quality, the control performance or the conducted EMI at the output of the source, are translated into corresponding families of curves in the parameter space of the output filter. The area/volume enclosed by these curves represents the design space of the output filter in which all tuples (L_f, C_f), e.g. for a single-stage LC-filter, fulfill every single AC source specification. From all possible filter parameters in the design space, the set of parameters resulting in the smallest filter volume, the lowest filter weight, the highest filter efficiency and/or the lowest filter costs can be selected.**

I. Introduction

For developing and testing power electronic equipment and associated control strategies, controllable power sources, which have the ability to emulate certain electrical characteristics, may help to accelerate the development and test procedures and thus are able to save costs as well as efforts. Examples of such controllable power sources are:

- Motor emulators for testing inverters [1]–[3], also in combination with power hardware-in-the-loop simulations [4];
- Grid emulators for testing utility connected distributed generators [5]–[7] such as fuel cell based systems [8]. This can include the testing of safety and protection functions [9] as well as testing of the implemented control strategy, which again can be done with hardware-in-the-loop simulations [10];
- Grid emulators for optimizing the control scheme for traction vehicles [11].

Such controllable AC power sources can basically be implemented with a linear or a switched power amplifier. To reduce the weight as well as the volume, a switched system is preferred.
However, to achieve a certain quality in the output voltage with a switched system, an output filter is essential and thus the proper dimensioning of the output filter is critical in respect of the system performance. This paper proposes a systemic procedure to design such an output filter.

This paper is organized as follows: **Section II** describes the AC source output stage. The performance requirements of the AC source are summarized in **Section III** and **Section IV** explains the proposed design approach. The paper is concluded with **Section V**.

II. Realisation of the AC Source Output Stage

The output stage of the AC source considered in this paper is depicted in Fig. 1, and its specifications are summarized in Table I. The system is bidirectional and the output topology is a hard-switched three-level Neutral Point Clamped (NPC) Voltage Source Converter (VSC). For the four bridge-legs, a custom made power module (based on the 600 V APTGT50TL60T3G module - trench + field stop IGBT technology - from Microsemi) is employed, where the four highlighted Si diodes in Fig. 2 are replaced by SiC diodes in order to reduce the turn-on losses of the switches and the diode turn-off losses. The other two diodes are not involved in normal operation 3-level current commutations. The average junction temperature over the rms output current $i_{out,rms}$ for different switching frequencies f_s is depicted in Fig. 2 for supplying an ohmic load. A water cooling system with a constant heat-sink temperature of 80°C is assumed.
In order to ensure a maximum average junction temperature of $T_{j,avg,max} = 125°C$, a maximal switching frequency of $f_s = 48\,\text{kHz}$ is admissible at twice the nominal current (Fig. 2). Assuming a median temperature ripple of 20% of 125°C (peak) and leaving a certain margin to the maximal allowable semiconductor junction temperature of 175°C, the indicated value of $T_{j,avg,max} = 125°C$ is an appropriate choice. The selected switching frequency $f_s = 48\,\text{kHz}$ justifies the employment of a 3-level NPC VSC. The curves

TABLE I Electrical specifications of the AC source.

Nominal output power $P_{out,n}$	10 kW
Nominal output voltage $u_{out,n}$ (rms, line to neutral)	230 V
Maximum output voltage $u_{out,max}$ (peak, line to neutral)	350 V
Nominal DC-link voltage $U_{DC,n}$	700 V
Maximum DC-link voltage $U_{DC,max}$	800 V
Nominal output current $i_{out,n}$ (rms)	15 A
Maximum output current $i_{out,max}$ (rms)	30 A
Output frequency f_{out}	50 Hz
Output stage switching frequency f_s	48 kHz
Small-signal bandwidth bw_{ss}	1 kHz
Nominal efficiency η_n	$\geq$ 95%

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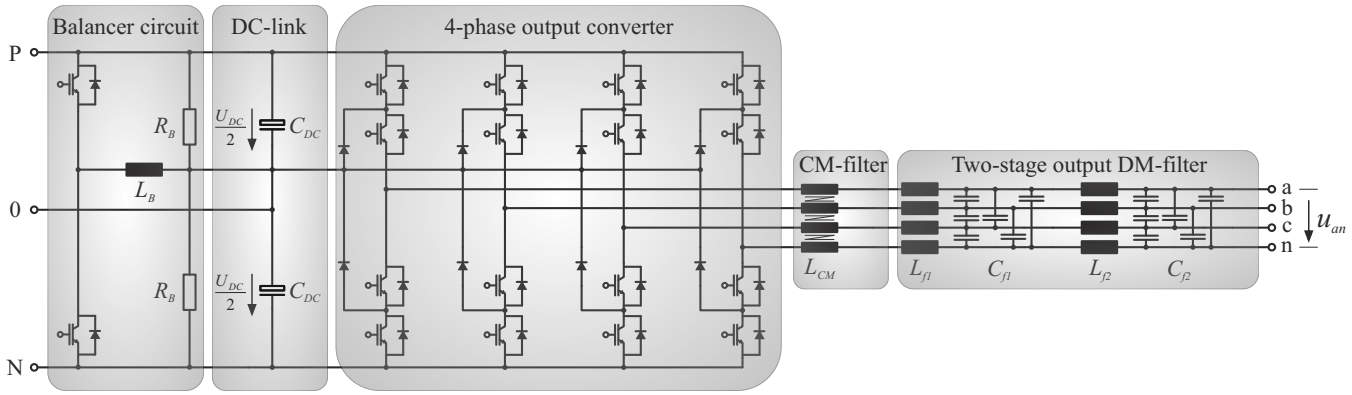

Fig. 1 Schematic of the 4-phase AC source output stage including the output filter and a balancer circuit in the DC-link.

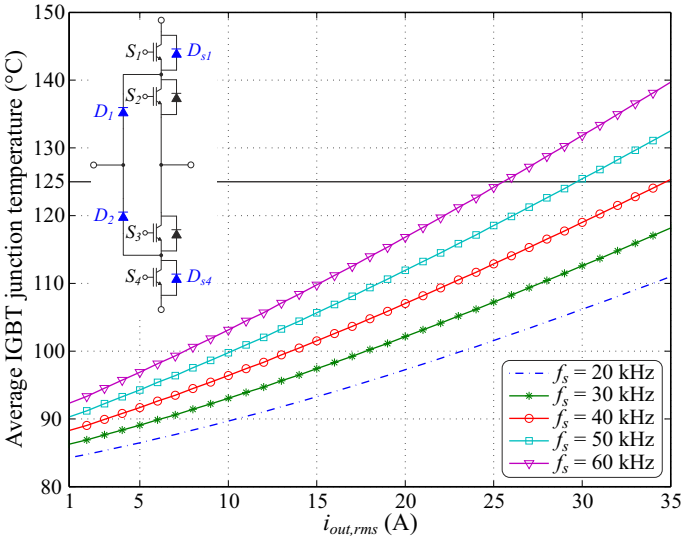

Fig. 2 Computed average IGBT junction temperature (of switches S_1 and S_4) over the rms output current $i_{out,rms}$ for the custom made power module based on the APTGT50TL60T3G module from Microsemi, for which the four labelled diodes are SiC Schottky diodes. The output current and voltage were assumed to be in phase and sinusoidal with a frequency of 50 Hz. The computation of the curves is based on measured switching losses of the module.

given in Fig. 2 are based on the measured switching losses of the module [12].

As a rule of thumb, the permanent blocking voltage of the IGBTs should not exceed $2/3$ of its rated voltage of 600 V [13] (100-fit voltage [14]). Thus, the DC-link voltage U_{DC} is set to 700 V to comply with the 100-fit specification of the IGBT module and to leave a certain margin. However, in order to also allow the temporary generation of an AC source output phase voltage of $u_{an} = 350$ V, the maximal DC-link voltage is defined to be $U_{DC,max} = 800$ V.

The AC source needs to cope with single-phase as well as three-phase loads and needs to be able to generate asymmetric grid conditions. Therefore, each phase is controlled independently, receiving the references from a master control unit. In accordance, the single-phase equivalent circuits shown in Fig. 3 are considered for the subsequent analysis. A CM filter takes theoretically little influence on the elaborated results, and hence, in a first step, only the DM filter is considered.

III. Output Filter Performance Requirements

The output filter of the AC source needs to be designed in such a way that the given specifications regarding output voltage waveform quality, dynamics and conducted EMI can be met. For the considered system, the requirements are shortly described in the following, referring to the circuits depicted in Fig. 3.

- *Peak-to-peak voltage ripple Δu_{out} of the output voltage u_{out} below 7.6% of the peak nominal output voltage $u_{out,n,peak}$ [cf. Fig. 4(a)]*: According to IEEE 1547.1, the THD of the output voltage should be less than 2.5%. This can be fulfilled if the maximal Δu_{out} is below 7.6% of $u_{out,n,peak}$ (for $U_{DC} = 700$ V). The THD is computed over the full frequency spectrum of the output voltage.
- *Peak-to-peak current ripple Δi_L of the filter inductor current i_L below 30% of the peak nominal output current $i_{out,n,peak}$ [cf. Fig. 4(b)]*: This value was selected as a compromise between inductor size, inductor losses, ease of controllability of i_L and the stress on the power semiconductors. The higher the current ripple, the lower the value of L_f becomes and in accordance, the smaller the inductor volume. However, a high current ripple increases the inductor high frequency losses. On the other hand, the larger the current ripple, the greater is its $\partial \Delta i_L(t)/\partial t$, and hence the current sampling delays become more important. This has an impact on the current controller design. Finally, if the current ripple Δi_L is significant, one semiconductor in a commutation sequence is stressed more than the others, since this semiconductor always switches off at the maximum of the current ripple (the IGBT turn-off losses are higher than the turn-on losses). Because of the mentioned reasons, a standard choice for

the ripple amplitude is $20 - 40\%$ of $i_{out,n,peak}$. In this paper, 30% was selected (for $U_{DC} = 700$ V).

- *Minimum slew rate SR of the output voltage of* $204\ \mathrm{V/ms}$ *[cf. Fig. 4(c)]*: This criterion represents the set-point tracking performance of the output stage. For testing the immunity of electronic equipment connected to the output stage, the peak voltage of a signal superimposed on u_{out}, which should be generated at the AC source output, is defined in IEC/EN 61000-4-13. Accordingly, the maximal value of the imposed signal is 10% of $u_{out,n,peak}$ at a frequency of 500 Hz. For the considered AC source, the 10% limit was intentionally extended up to a frequency of 1 kHz. A sinusoidal voltage with a peak value of $0.1 \cdot u_{out,n,peak}$ and a frequency of 1 kHz has a maximum slope of $204\ \mathrm{V/ms}$. The *SR* indicates the average increase in u_{out} if the voltage U_{DC}/2 is continuously applied at the output of the converter.
- *Maximum "small-signal" output impedance* z_{out} *of* $3.2\ \Omega$ *[cf. Fig. 4(d)]:* This requirement is related to the ability of the output stage to reject disturbances at its output. In accordance to IEC/EN 61000-3-12, where for low frequencies (< 100 Hz), the output impedance should not be higher than 6% of the nominal output impedance, the desired maximal z_{out} is $0.06 \cdot z_{out,n} = 0.06 \cdot 230\ \mathrm{V}/15\ \mathrm{A} = 0.92\ \Omega$ for all frequencies. Since this is rather hard to satisfy and since the output impedance is not a mandatory criterion, a 3.5 times higher maximum output impedance of $z_{out} = 3.24\ \Omega = 0.21 \cdot z_{out,n}$ is assumed. A current step of 10 A then leads to a maximum voltage drop/rise of 32.4 V ($z_{out} = 3.24\ \Omega$).
- *Meet the standard for conducted emission levels according to IEC/EN 55011 Class A*: In the frequency range from 150 kHz to 500 kHz, the conducted emissions need to be below 79 dBV (QP detector) and for the frequency range between 500 kHz and 30 MHz below 73 dBV.

In addition, the output filter should have a minimal volume, minimal weight, minimal losses and/or minimal costs. In the following, a systematic output filter design approach is proposed, which finds the filter with the smallest volume and the highest efficiency for given constraints and components/materials. The other mentioned criteria can be implemented in the same way.

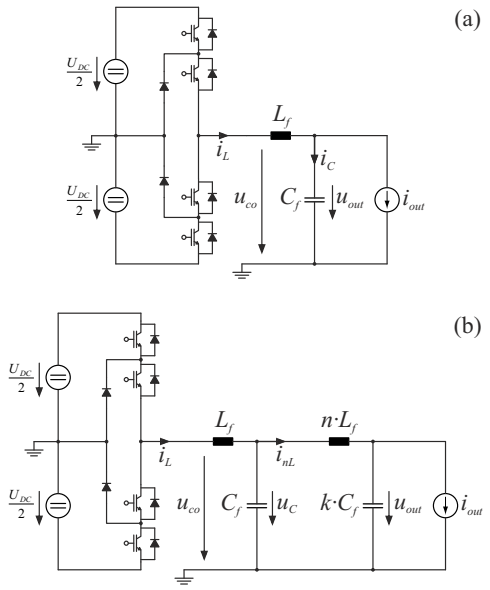

Fig. 3 Simplified equivalent circuit of the three-level NPC output stage for (a) a single-stage and (b) a two-stage output filter. The load is represented as a current source, since a typical loading is inductive.

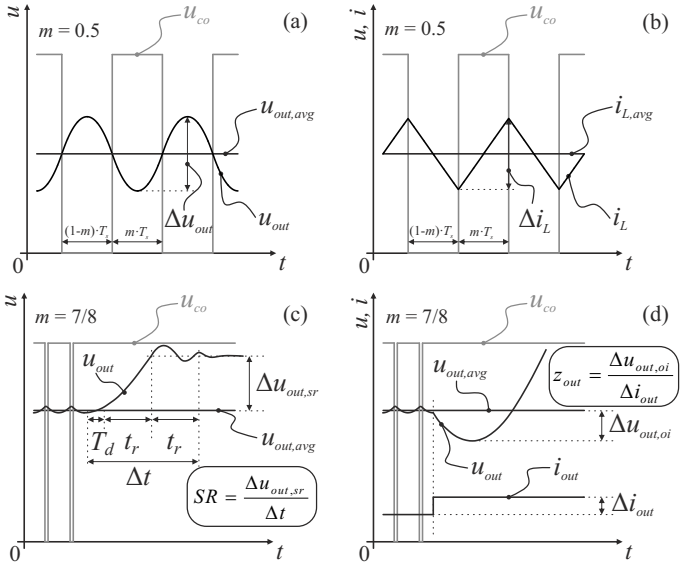

Fig. 4 Visualization of the design criteria for the (a) voltage ripple, (b) current ripple, (c) slew rate and (d) output impedance for a three-level NPC VSC.

IV. Output Filter Design Approach

The idea of the output filter design approach is to translate the requirements listed above into boundaries of the design space, i.e. in the L_f-C_f plane, shown in Fig. 5. Furthermore, other limits such as a maximum reactive filter capacitor current can be included in the L_f-C_f plane. The design procedure does not only enable to determine optimal filter parameters but also to assess the potential advantages of different filter topologies, e.g. single-stage or multi-stage filters, or an output stage with interleaving. The idealized circuit, depicted in Fig. 3(a), is considered for the curves in Fig. 5. For a single-stage output filter and a three-level output stage, the design requirements listed above can be approximated by the equations below. From these equations, the basic dependency of the voltage ripple, current ripple, etc. from the DC-link voltage U_{DC}, the switching frequency f_s, and the filter parameters L_f and C_f can be extracted.

The equations do not consider the controller dynamics and the PWM. The approach to compute the subsequent equations is equal for all cases and exemplary shown for the slew rate *SR*. To simplify the analysis, it is assumed that the output voltage

u_{out} remains constant to magnetize the inductance L_f. Thus, the additional current

$$\Delta i_C(t) = \frac{1}{L_f} \cdot \left(\frac{U_{DC}}{2} - u_{out} \right) \cdot t = \frac{1}{L_f} \cdot \frac{U_{DC}}{2} \cdot (1-m) \cdot t \tag{1}$$

is charging the capacitance C_f since $i_{out} = const.$ m denotes the modulation index defined as $m := \frac{2 \cdot u_{out}}{U_{DC}}$. Therefore, the extra charge results in

$$\Delta Q_C = \int_0^{\Delta t} \Delta i_C(t) \cdot dt = \frac{1}{2 \cdot L_f} \cdot \frac{U_{DC}}{2} \cdot (1-m) \cdot \Delta t^2. \tag{2}$$

With $C_f = \frac{\Delta Q_C}{\Delta u_{out}}$, it follows

$$SR = \frac{\Delta u_{out}}{\Delta t} = \frac{1}{4 \cdot L_f \cdot C_f} \cdot U_{DC} \cdot (1-m) \cdot \Delta t. \tag{3}$$

Since for a sinusoidal output voltage u_{out} Δt is inversely related to the angular frequency ω_{ss}, the slew rate can be approximated by

$$SR \cong \frac{1}{4 \cdot L_f \cdot C_f} \cdot \frac{U_{DC} \cdot (1-m)}{\omega_{ss}}. \tag{4}$$

Proceeding in the same manner as for the slew rate, the following equations are obtained:

- *Max. output voltage ripple*:

$$\begin{aligned} \Delta u_{out} =& \frac{m \cdot (1-m) \cdot U_{DC}}{16 \cdot L_f \cdot C_f \cdot f_s^2} \\ \underset{m=0.5}{\leq}& \frac{U_{DC}}{64 \cdot L_f \cdot C_f \cdot f_s^2} \leq 24.7 \text{ V}, \end{aligned} \tag{5}$$

  where f_s denotes the switching frequency. The voltage ripple Δu_{out} is proportional to the DC-link voltage U_{DC} and inversely proportional to the switching frequency squared.
- *Max. inductor current ripple*:

$$\begin{aligned} \Delta i_L =& \frac{m \cdot (1-m) \cdot U_{DC}}{2 \cdot L_f \cdot f_s} \\ \underset{m=0.5}{\leq}& \frac{U_{DC}}{8 \cdot L_f \cdot f_s} \leq 6.4 \text{ A}, \end{aligned} \tag{6}$$

  which, due to simplifying assumptions, is not dependent on the value of the filter capacitance C_f. The current ripple Δi_L is proportional to the DC-link voltage U_{DC} and inversely proportional to the switching frequency f_s.
- *Min. slew rate*:

$$\begin{aligned} SR =& \frac{(1-m) \cdot U_{DC}}{4 \cdot L_f \cdot C_f \cdot \omega_{ss}} \\ \underset{m=350/400}{\geq}& \frac{U_{DC}}{32 \cdot L_f \cdot C_f \cdot \omega_{ss}} \geq 204 \text{ V/ms}, \end{aligned} \tag{7}$$

  for $U_{DC} = 800$ V and where ω_{ss} is the angular frequency of the on the output voltage superimposed signal and is given by $\omega_{ss} = 2 \cdot \pi \cdot 1$ kHz. The *SR* is directly proportional to the DC-link voltage U_{DC} and decreases with increasing angular frequency ω_{ss}. This leads to the approximated curves in Fig. 5. The voltage over the inductance L_f decreases as the output voltage increases, leading to a slower increase of the output voltage than assumed in the approximated Eq. (7). Thus, the calculated curve lies below the approximated one.
  For the presented computation and to approximate the controller dynamics, a maximum delay T_d, resulting from the Pulse Width Modulation (PWM), of half of the switching period T_s is assumed ("double update mode"). Furthermore, it is assumed that the output dynamics of the controlled converter are dominated by the complex conjugated pole pair which lies closest to the imaginary axis in the complex plane. These two poles have the slowest dynamics and hence the dynamics can be modelled by a second order system. Modifying slightly the equations given in [15], the ratio between settling time t_s (considering a tolerance band of $\pm 5\%$) and rise time t_r (from 0% to 100%) is given by

$$\frac{t_s}{t_r} \approx \frac{3}{2.5 \cdot \zeta} \underset{\zeta=0.6}{=} 2. \tag{8}$$

  In the above equation, ζ is the damping constant of the poles. It is assumed that the maximal overshoot of a step response is limited to 10%, which leads to $\zeta = 0.6$ [15]. In conclusion, the time which is required by the output voltage to reach its new value is multiplied by a factor of 2.
- *Max. output impedance*:

$$\begin{aligned} z_{out} =& \frac{L_f}{2 \cdot (1-m) \cdot C_f \cdot Z_{in}} \\ \underset{m=350/400}{\leq}& \frac{4 \cdot L_f}{C_f \cdot Z_{in}} \leq 3.24 \ \Omega, \end{aligned} \tag{9}$$

  where Z_{in} is defined as $Z_{in} := \frac{U_{DC}}{2 \cdot \Delta i_{out}}$ with $\Delta i_{out} = 7.5$ A. The output impedance z_{out} is linear proportional to the ratio between filter inductance and filter capacitance $\frac{L_f}{C_f}$. For this approximation, the PWM delay $T_d = T_s/2$ is not considered. However, for the final computation the delay is taken into account.
- *Conducted emission (at nominal operation)*: To assess the worst case, the magnitudes of each harmonic in the lower and upper 4.5 kHz sidebands of the multiples of the switching frequency are summed up to $\hat{u}_{sum}$ (cf. IEC/CISPR 16-2-1, 9 kHz bandpass filter). The voltage $\hat{u}_{sum}$ can be considered as a single spectral component at the corresponding multiple of the switching frequency and needs to be below the limit given by the IEC/EN 55011 class A standard. Thus, the Line Impedance Stabilization Network (LISN) must not be modelled.
- *Maximum reactive filter capacitor current*: The peak reactive current is given by $i_{C,max} = \omega_{out} \cdot C_f \cdot \sqrt{2} \cdot u_{out,n} \leq 2.1$ A and should not be greater than 10% of $i_{out,n,peak}$. ω_{out} denotes the angular output frequency, thus $\omega_{out} = 2 \cdot \pi \cdot 50$ Hz.

The plotted curves without the controller dynamics and the PWM in Fig. 5 describe the physical limits for given

combinations of filter values L_f and C_f. The curves resulting from the given equations are labelled as "approximated". The ones computed by solving the differential equations of the output filter are named as "calculated". The difference between the approximated and the calculated curves is the assumption that the increase in the output voltage is negligible compared to its initial value. Each curve separates the L_f-C_f plane (the filter parameter space) in two regions: one where the requirement is satisfied and one where it is violated, indicated by arrows in Fig. 5. The arrow points into the region where the criterion is satisfied. The area, which is enclosed by all curves, represents the design space (= feasible parameter space) of the output filter. If the curves do not surround a common area, no design fulfilling all requirements exists. In this case, the requirements need to be reconsidered and/or relaxed, and the filter or the output stage converter topology have to be modified (e.g. interleaved converter stages must be employed). As can be seen in Fig. 5, no design space exists for a single-stage output filter and the considered three-level converter. The EMI criterion cannot be met at the same time as the other requirements.

It is remarked that a two-level topology would also result in an empty design space, because it generates a higher voltage ripple as well as current ripple (minimal inductance of $L_f = 573$ µH for the same current ripple).

To ensure an output filter design with a single-stage filter, the slew rate and EMI limit curves in Fig. 5 should orbit an area in which both requirements are satisfied. This means that the high frequency components (> 150 kHz) in the output voltage need to be attenuated more or the converter should allow faster output voltage dynamics. Thus, there is a clear trade-off between the output voltage dynamics and the high frequency output voltage attenuation. In case the requirements cannot be relaxed, there are three main options to find a common design space:

1) Multiple bridge-legs per phase could be connected in parallel to a single-stage filter and operated interleaved (since the switching frequency cannot be increased for one bridge-leg due to the resulting converter losses). In this way, the apparent switching frequency seen in the output ripple is increased.
   For the same max. peak-to-peak voltage ripple, compared to a not interleaved solution with a harmonic amplitude A_h at a harmonic frequency f_h, m-interleaved output stages result approximately in the same harmonic amplitude A_h at m-times the harmonic frequency f_h. However, for reaching the same ripple Δi_L in each inductor, the voltage ripple is reduced by m^2.
   The amplitude of the harmonics in the frequency spectrum decay approximately with $f_h^{2.7}$. Thus, for a switching frequency of $f_s = 48$ kHz (no interleaving), the fourth voltage ripple harmonic is the critical harmonic in the EMI spectrum, and hence the reduction factor between $A_{48\,\mathrm{kHz}}$ and $A_{192\,\mathrm{kHz}}$ is slightly higher than 42. In conclusion, only $m = 3$ and $m \geq 7$ result in a benefit regarding the conducted EMI requirement.
   On the other hand, m-interleaved output stage results in m-times the dynamics of a single converter solution (for the same current ripple Δi_L) and the current stress of the bridge-legs is divided by m. This may also allows to increase the switching frequency and hence to reduce the output voltage ripple.
2) The number of voltage levels could be increased in order to reduce the high frequency voltage ripple at the output. This would be beneficial for the EMI criterion, but it would not affect the *SR* requirement.
3) Multiple bridge-legs per phase could be connected in parallel to a single stage filter and operated hard in parallel (same gate drives for the different bridge-legs can be used). In this way, the current stress of the bridge-legs is reduced and the output dynamics are improved [as for point 1)].
4) The number of output filter stages could be increased to obtain higher attenuation for higher frequency components (> 150 kHz) in the output voltage. The *SR* criterion is not relaxed by this solution.

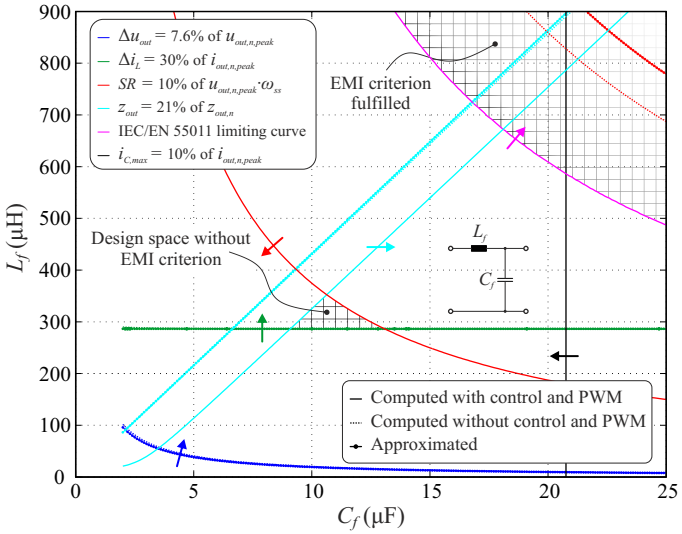

Fig. 5 Into the L_f-C_f plane translated requirements (listed above) for the circuit of Fig. 3(a): approximated (solid-dotted lines) and calculated (solid and dashed lines). The arrowheads indicate the area where the requirements can be met.

The first three options are rather expensive to implement and increase the volume, the weight and the complexity of the circuit and its control significantly. Thus, the fourth option is selected, and hence a second stage is added to the output filter [Fig. 3(b), first stage (L_f, C_f) and second stage ($n \cdot L_f$, $k \cdot C_f$)].

The scaling weights n and k of the second filter stage can be selected in such a way that the smallest total filter volume results. This is shown in Fig. 6, where the total filter volume is plotted over n and k. To compute the inductor volumes, two "basic" inductor volumes were calculated based on the

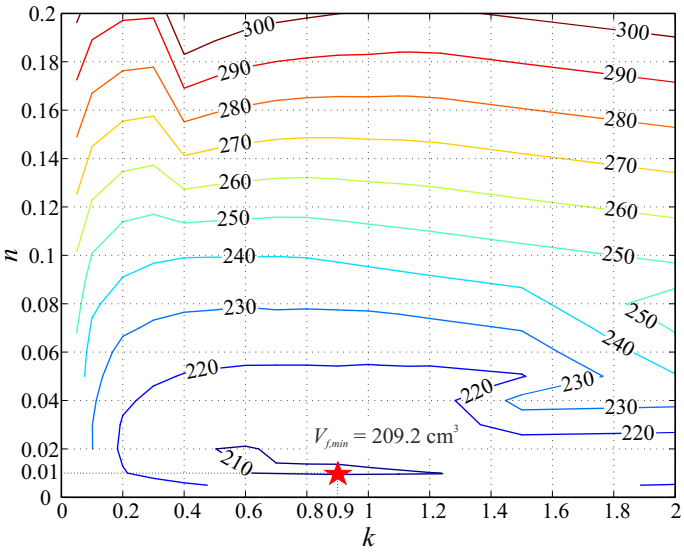

Fig. 6 Lines of constant filter volume (in cm^3) in the n-k plane showing that the smallest volume is obtained for $n = 0.01$ and $k = 0.9$.

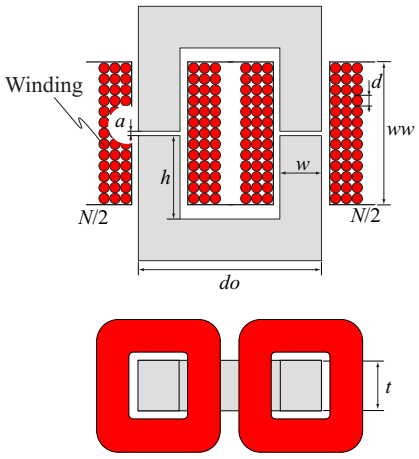

Fig. 7 Geometry of the designed inductors for the computation of the basic inductances, volumes and losses.

approach presented in [16], [17]. The design of the inductors was optimized to obtain the smallest volume. By applying a scaling law, the inductor volume was derived as a function of the inductance value.

The shape of the two designed inductors is depicted in Fig. 7. Two ferrite C-cores (N87 from Epcos) are used, due to the high switching frequency of $f_s = 48\,\mathrm{kHz}$, and the winding was equally split to the two core legs. The winding is implemented with a litz wire. The basic inductor volume for the first and second filter stage is $V_{B,1} = 172.6\,\mathrm{cm}^3$ ($L_{B,1} = 290\,\mu\mathrm{H}$) and $V_{B,2} = 22.1\,\mathrm{cm}^3$ ($L_{B,2} = 12\,\mu\mathrm{H}$), respectively. The inductors are designed for the specifications given in Table II.

The two basic equations governing the design of an inductor are

$$\begin{aligned} A_{Fe} \cdot \hat{B}_s \cdot N &= L \cdot \hat{i}, \\ A_w &= \tfrac{N}{k_w} \cdot \tfrac{I_{rms}}{S_{rms}}. \end{aligned} \tag{10}$$

In the above equations $A_{Fe} = w \cdot t$, $A_w = (2 \cdot h + a) \cdot (do - 2 \cdot w)$, $\hat{B}_s$ is the maximal allowable flux density in the core, k_w denotes the winding filling factor and S_{rms} is the maximal current density in the litz wire. If an inductor design at the thermal limit is assumed, the total losses P_{losses} (core and winding losses) can only be extracted from the component over its surface A, which scales quadratic to a basic length l_B (in m), thus $P_{losses} \sim {l_B}^2$ (under ideal thermal distribution). For a constant frequency, assuming that the core losses are given by the Steinmetz equation, the core losses are proportional to $P_{core} \sim \hat{B}_s^{\beta} \cdot {l_B}^3$. Accordingly, in a thermal restricted design, the peak flux density in the core scales with $\hat{B}_s \sim {l_B}^{-1/\beta}$. On the other hand, the winding losses are proportional to $P_{winding} \sim {S_{rms}}^2 \cdot {l_B}^3$, which leads to $S_{rms} \sim {l_B}^{-1/2}$ [18]. Putting all the relations together, the following equation

TABLE II Parameters for the two designed "basic" inductors.

Parameter	$L_{B,1}$	$L_{B,2}$
Inductance value	290 µH	12 µH
Boxed inductor volume	172.6 cm^3	22.1 cm^3
Inductor losses (for nominal operation)	30 W	13 W
Fundamental frequency	50 Hz	50 Hz
Ripple frequency	48 kHz	48 kHz
Fundamental nominal rms current	15 A	15 A
Max. peak to peak current ripple	7.2 A	1 A
Max. flux density	0.3 T	0.3 T
Max. winding temperature	125°C	125°C
a	1.5 mm	7.4 mm
w	14.7 mm	6.2 mm
Number of turns N	23	22
do	40.5 mm	20.7 mm
h	6.9 mm	17.2 mm
t	71.0 mm	6.4 mm
ww	13.7 mm	34.3 mm
d	1.2 mm	1.0 mm

results:

$${l_B}^4 \sim A_{Fe} \cdot A_w = \frac{1}{k_w} \cdot \frac{L \cdot \hat{i} \cdot I_{rms}}{\hat{B}_s \cdot S_{rms}} \sim {l_B}^{1/2+1/\beta} \cdot L \cdot \hat{i} \cdot I_{rms}. \tag{11}$$

Assuming $\beta = 2$, this means that the inductance value L scales linearly with its volume V_L in a thermal constrained design (for a certain peak and rms current), hence

$$L \sim V_L \rightarrow V_L(L) = \frac{L}{L_B} \cdot V_B, \tag{12}$$

as long as the inductance value does not change in order of magnitude. This is the reason why two basic inductors were designed.

For the assessment of the capacitor volume, the volume of the commercially available $400\,\mathrm{V_{rms}}$ MKP (AC application, wound) capacitors from Epcos was fitted into a linear function

$$V_C(C) = 4.15\,\mathrm{cm}^3 \cdot C[\mu\mathrm{F}] - 0.15\,\mathrm{cm}^3. \tag{13}$$

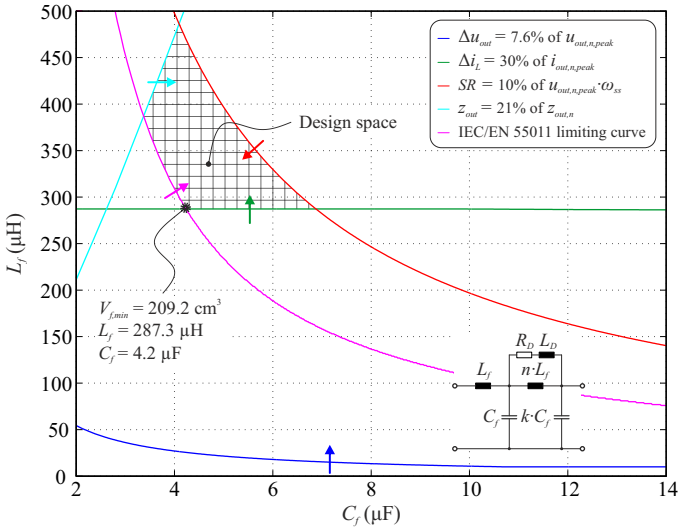

Fig. 8 Design space for a two-stage filter [Fig. 3(b)] with $n = 0.01$ and $k = 0.9$ to obtain the smallest filter volume. The arrowheads indicate the area where the requirements can be met.

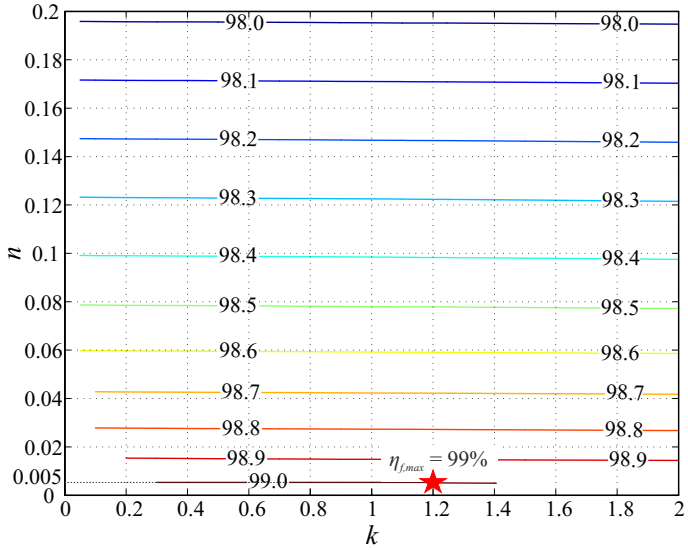

Fig. 9 Lines of constant filter efficiency (in %) in the n-k plane, showing that the highest efficiency is obtained for $n = 0.005$ and $k = 1.2$.

400 V_{rms} capacitors were selected since the maximum DC output voltage is 350 V.
Comparing the volumes of the inductors to the ones of the capacitors, it follows that $V_C(12\ \mu\text{F})/V_L(12\ \mu\text{H}) = 49.7\ \text{cm}^3/22.1\ \text{cm}^3 = 2.25$.
Since for the computation of the design spaces for different n and k (weighting factors of the second filter stage) resonances of the second filter stage can be excited, a parallel R_D-L_D damping (Fig. 8) is added to the second filter stage. The values of $R_D = 5\ \Omega$ and $L_D = n \cdot L_f/2$ were selected in such a way that the influence of the different curves in the L_f-C_f plane is minimal (basically, there is a trade-off between high frequency attenuation degradation and output impedance).

As it can be deduced from Fig. 6, the smallest filter volume is $V_{f,min} = 209.2\ \text{cm}^3$ and is obtained for $n = 0.01$ and $k = 0.9$ (for one phase). The resulting design space is depicted in Fig. 8, which demonstrates that a common design space exists for a two-stage output filter. For one phase, the volume partitioning for $n = 0.01$ and $k = 0.9$ between the different components is

$$\begin{aligned} V_{L_f} &= 171.0\ \text{cm}^3 \quad V_{n\cdot L_f} = 5.3\ \text{cm}^3, \\ V_{C_f} &= 28.5\ \text{cm}^3 \quad V_{k\cdot C_f} = 25.6\ \text{cm}^3. \end{aligned} \tag{14}$$

For the assessment of the nominal output filter efficiency, the procedure is similar to the one for the filter volume. The computed losses for the two inductor designs and a scaling law are employed to assess the inductor losses; these are $P_{losses,B,1} = 30$ W and $P_{losses,B,2} = 13$ W (core losses are almost negligible). Considering again a thermal constrained

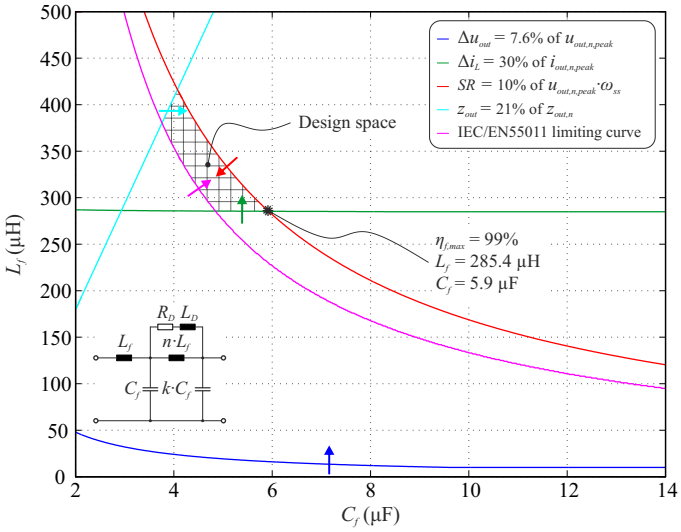

Fig. 10 Design space for a two-stage filter [Fig. 3(b)] with $n = 0.005$ and $k = 1.2$ to get the filter with the highest efficiency. The arrowheads indicate the area where the requirements can be met.

inductor design, it follows

$$\begin{aligned} P_{losses} &\sim {l_B}^2 \underset{L\sim {l_B}^3}{\sim} L^{2/3} \\ &\rightarrow P_{losses}(L) = P_{losses,B} \cdot \left(\frac{L}{L_B}\right)^{2/3}. \end{aligned} \tag{15}$$

The capacitor losses are assessed with (neglecting the losses due to the fundamental output frequency of 50 Hz)

$$ESR = \frac{\tan\delta}{\omega \cdot C} \rightarrow P_{losses}(C) = ESR \cdot i_{C,rms}^2, \tag{16}$$

where $\tan(\delta) = 2 \cdot 10^{-3}$ (at 1 kHz). To simplify the computations, the capacitor rms currents are assumed to be con-

stant and given by $i_{C_f,rms} = \frac{8.2\,\mathrm{A}}{\sqrt{2}}$ and $i_{k\cdot C_f,rms} = \frac{1\,\mathrm{A}}{\sqrt{2}}$, respectively.

The filter efficiency over the weighting factors n and k of the second filter stage is plotted in Fig. 9. It can be seen that the losses of the capacitors are negligible compared to the ones in the inductors. The highest filter efficiency is reached for $n = 0.005$ and $k = 1.2$, and is $\eta_{f,max} = 99\%$ (total losses of $P_{f,min} = 32.9\,\mathrm{W}$ for one phase). The resulting design space is illustrated in Fig. 10. The loss-partitioning for nominal operation is

$$\begin{aligned} P_{losses,L_f} &= 29.7\,\mathrm{W} \quad P_{losses,n\cdot L_f} = 3.2\,\mathrm{W}, \\ P_{losses,C_f} &= 35\,\mathrm{mW} \quad P_{losses,k\cdot C_f} = 1\,\mathrm{mW}. \end{aligned} \tag{17}$$

Comparing the filter design for the maximum efficiency and the one for the smallest volume, it can be concluded that both designs do not differ too much. This means that the optimum in volume and efficiency can almost be met simultaneously for the related boundary conditions. In addition, the design spaces also show that the voltage ripple requirement (THD criterion) does not affect the designs and is thus a weak criterion compared to the other requirements. Alternatively, the weighting factors n and k of the second filter stage can also be determined in such a way that the minimum filter weight or the minimum filter costs are obtained.

For higher output power levels (higher output currents) interleaving of bridge-legs may be unavoidable to achieve the required output performance of the AC source. Moreover, if the current ripple in i_L is kept fixed to 30% of $i_{out,n,max}$, the inductance L_f can be reduced for higher output currents. This allows the AC source to achieve higher output voltage dynamics.

V. Conclusions

A systematic multi-objective output filter design approach for an output stage of a high performance $10\,\mathrm{kW}, 400\,\mathrm{V_{ll,rms}}$ 4-phase AC source is demonstrated, which enables to determine the smallest filter volume or the highest filter efficiency while fulfilling all given AC source specifications. The suggested approach translates the specifications regarding output waveform quality, output dynamics (control performance) and EMI into boundaries in the L_f-C_f filter parameter plane. The common area in the L_f-C_f filter parameter plane defines the design space of the output filter. Finally, the optimal design among the filter component values L_f and C_f in the resulting design space can be identified.

Is is shown that, for the case at hand, no design space exists for the given specifications for a single-stage output filter (L_f, C_f) and a 3-level NPC voltage source converter. There is a trade-off between the output voltage dynamics (namely the ability to dynamically increase/decrease the output voltage - the slew rate) and the attenuation of high frequency output voltage harmonics (required for the conducted EMI requirement). To solve the problem, a second filter stage ($n\cdot L_f$, $k\cdot C_f$) is added to increase the attenuation at high frequencies. With a two-stage output filter, a common design space exists. The weighting parameters of the second filter stage n and k can be selected in order to achieve the smallest total boxed volume of the filter inductors and capacitors ($209.2\,\mathrm{cm}^3$ per phase) or the highest filter efficiency (99% for nominal operation).

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