Power Electronic Systems
Laboratory

IEEE Transactions on Power Electronics, Vol. 28, No. 8, pp. 4074-4082, August 2013

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***Abstract*—Switching devices based on SiC offer outstanding performance with respect to operating frequency, junction temperature, and conduction losses enabling significant improvement of the performance of converter systems. There, the cascode consisting of a MOSFET and a JFET has additionally the advantage of being a normally off device and offering a simple control via the gate of the MOSFET. Without dv/dt-control, however, the transients for hard commutation reach values of up to 45kV/μs, which could lead to electromagnetic interference problems. Especially in drive systems, problems could occur, which are related to earth currents (bearing currents) due to parasitic capacitances. Therefore, new dv/dt-control methods for the SiC JFET/Si MOSFET cascode as well as measurement results are presented in this paper. Based on this new concepts, the outstanding performance of the SiC devices can be fully utilized without impairing electromagnetic compatibility.**

***Index Terms*—dv/dt-control methods, SiC JFET, SiC-Si cascode.**

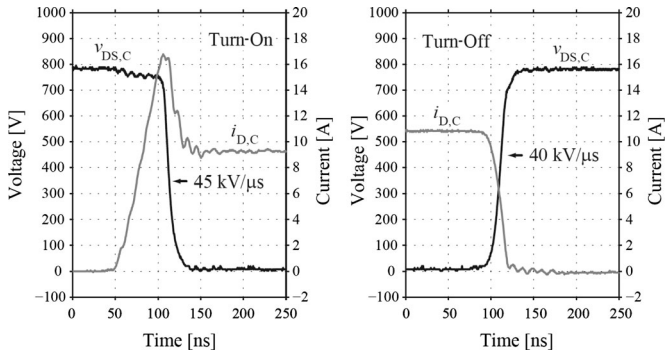

Fig. 1. Switching behavior of the SiC-Si MOSFET (IRLR024N)/JFET cascode at $V_{\rm dc} = 800$ V/ $i_{D,C} = 9$A/11A. Proper hard switching behavior at turn ON and turn OFF event.

I. Introduction

THE trend for the design of power electronic systems applied for example in telecom applications is toward higher power density and higher efficiency values. In order to reduce the system volume and achieve a higher power density, first the appropriate topology for the intended application must be chosen. Second, the design parameters must be selected so that minimal volume and/or higher efficiency result. Due to the large number of design parameters and coupling among them, it is advantageous to use an optimization procedure as presented in [1]. There, a high switching frequency is usually required for minimizing the volume of the passive components. Furthermore, switching losses of the semiconductors must be low for achieving a high efficiency.

Manuscript received May 28, 2012; revised September 25, 2012; accepted November 13, 2012. Date of current version January 18, 2013. Recommended for publication by Associate Editor H.-P. (Guest EIC-Wide Bandgap) Nee.

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Digital Object Identifier 10.1109/TPEL.2012.2230536

For voltages up to 600V, high performance MOSFET switches (e.g., COOLMOS) capable of working at high switching frequency with low switching losses are used in power factor correction converter systems (e.g., *VIENNA* rectifier [2], [3]). However, these devices offer a poor performance with respect to conduction losses in the 1200 V range, so that usually insulated-gate bipolar transistors (IGBTs) are used, which have significantly higher switching losses. This limits the required operating frequency in this voltage range and therewith also the achievable power density. In order to overcome this limitation, maturing devices based on wide bandgap semiconductor materials such as SiC could be used.

The SiC JFET [4] from SiCED/Infineon offers very fast switching with transients up to $45\ \mathrm{kV}/\mu\mathrm{s}$ (see Fig. 1) with a blocking voltage of 1200 V due to its optimized vertical JFET structure with lateral channel [5]. However, the normally ON behavior of the SiC JFET prevents that the switch is fully accepted for industry applications, in particular for voltage source converters (in current source pulse width modulation converter normally ON devices are preferable), although improved gate drive circuits have been developed [6]–[10].

A normally OFF behavior could be achieved by using a cascode configuration with a low-voltage Si MOSFET in series with the 1200V SiC JFET as shown in Fig. 2, without losing the excellent characteristics of the SiC device. In this configuration, only the low-voltage MOSFET is actively controlled whereas the SiC JFET is inherently controlled by the drain–source voltage of the MOSFET. The gate drive circuit for the SiC-Si cascode is a standard IGBT/MOSFET driver and therefore the currently used Si switches could directly be replaced by the SiC JFET/Si MOSFET cascode.

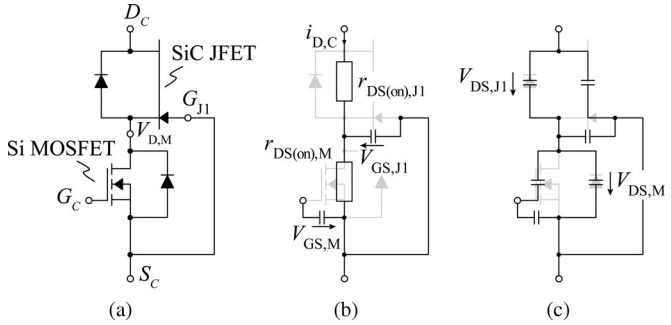

Fig. 2. Cascode configuration and the two typical states of the SiC-Si cascode: (a) cascode switch topology, (b) the conduction mode ($V_{GS,M} > V_{\mathrm{th},M}$, where $V_{GS,M}$ is the MOSFET gate–source voltage and $V_{\mathrm{th},M}$ denotes the threshold voltage), and (c) the blocking mode ($V_{GS,M} < V_{\mathrm{th},M}$).

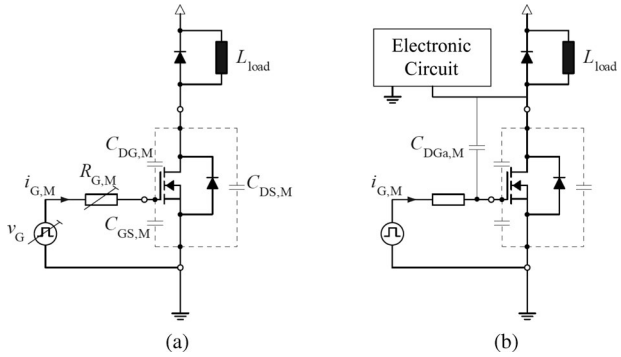

Fig. 3. Often used dv/dt limitation methods for MOSFET and IGBT switches. (a) Varying gate resistors and two- or three-step controlled gate voltage. (b) Additional drain–source capacitor $C_{DGa,M}$ causes an increased negative miller feedback.

As a result of high di/dt-values of 450 A/μs, which are achieved with the SiC-Si cascode in hard commutated switching actions as shown in Fig. 1, the effort for the design of a low inductive layout avoiding switching related overvoltages is mandatory. In [11], it was pointed out that overvoltages are occurring due to parasitic and not avoidable module and layout inductances. Furthermore, the desire for a controllable dv/dt of the cascode switching transients is also high to minimize electromagnetic interference (EMI) filtering effort [12], [13] and to reduce conduction and emission aspects in certain applications [14] and [15]. In [16], techniques are published for actively control the dv/dt behavior of MOSFET devices to reduce voltage overshoots without requiring bulky and lossy snubber circuits.

In this paper, novel methods to control and adjust the dv/dt-behavior of the SiC JFET/Si MOSFET cascode are presented. First, standard and well-known control techniques for MOSFET and IGBT semiconductors are shortly discussed in Section II. Second, the application of the conventional techniques controlling dv/dt is evaluated related to the cascode configuration. Moreover, the novel dv/dt-controlling methods are described in detail in Section III. Section IV presents experimental results of fast and controlled transients voltage edges of the cascode. Finally, the switching energy losses of the SiC-Si cascode are analyzed and conclusions are drawn.

II. Conventional Dv/Dt-Limitation Techniques

For state-of-the-art semiconductors as Si MOSFET and IGBT devices, several techniques [14] to reduce and control the dv/dt at fast switching edges are well known as shown in Fig. 3. The most simple and most frequently applied one is the control of the dv/dt with an external gate resistor $R_{G,M}$, where the optimal gate resistance is selected based on the corresponding switching device. In [15], the evaluation between varying gate resistors and an active gate voltage control (two- or three-step gate voltage) is presented. There are different and more complex active gate control methods as published, e.g., in [16] where an additional external ("artifical") Miller capacitance is electronically adjusted in order to implement a proper effective gate–drain capacitance. A further advanced method is introduced in [13] where the current of the external Miller capacitance is electronically controlled and at the same time the optimal point for minimal switching losses is calculated.

Most of these dv/dt limitation methods are based on the Miller Effect, $1 + G_M$ [cf. (2)], which describes a capacitive feedback between the output and the input, e.g., of a MOSFET *M* device

$$G_M = -\frac{d(v_{DS,M})}{d(v_{GS,M})}. \tag{1}$$

Therefore, the total equivalent input capacitance $C_{iss(eq)}$ seen from the gate–source junction during the ON/OFF transition results in [17]

$$\begin{aligned} i_{G,M} &= (C_{GS,M} + (1 + G_M) \cdot C_{DG,M}) \cdot \frac{dv_{GS,M}}{dt} \\ &= C_{iss(eq)} \cdot \frac{dv_{GS,M}}{dt}. \end{aligned} \tag{2}$$

Applying the conventional dv/dt-control techniques to the SiC-Si cascode does not result in the desired control behavior of reducing the fast switching voltages edges. The reason is the series connection of the low-voltage MOSFET and the SiC JFET. The conventional methods only influence the behavior of the active controlled low-voltage MOSFET which is analyzed and explained in the following.

A. SiC-Si Cascode

To investigate the influence of the conventional dv/dt-control methods on the SiC-Si cascode configuration, a simulation setup (cf. schematic of experimental setup in Fig. 8) with $LTSPICE$ is elaborated. Here, standard SPICE models as supplied by the manufacturers are used for the low-voltage MOSFETs [18] and the freewheeling SiC diode [19]. The applied SiC JFET model is proposed in [20] where also the Spice parameters of a SiC JFET from SiCED/Infineon have been extracted from experimental measurements.

The LTSpice simulation is implemented with the standard dv/dt-control method using gate resistors to control the dv/dt. For the simulation, $R_{G,M} = 15\,\Omega$ and $R_{G,M} = 3\,\Omega$ were utilized. It should be noted that the same or similar simulation results could also be achieved with a two- or three-step voltage applied to the gate–source junction or with an additional

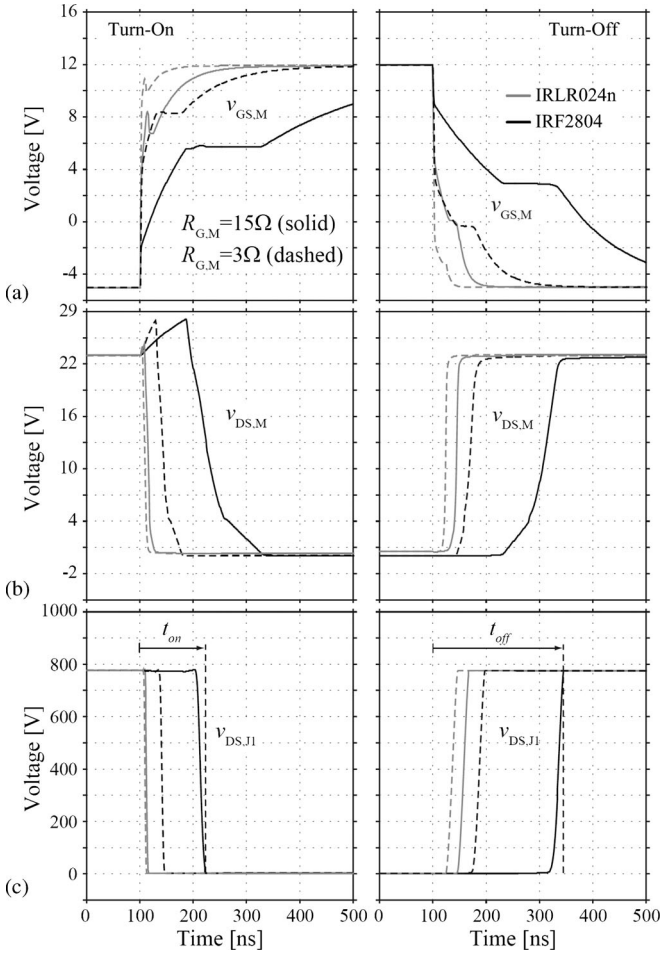

Fig. 4. SiC-Si cascode simulation results using conventional dv/dt-limitation techniques with different gate resistors (3 Ω dashed line, 15 Ω solid line) and diverse MOSFET switches. (a) MOSFET gate–source voltage $v_{GS,M}$. (b) MOSFET drain–source voltage $v_{DS,M}$. (c) SiC JFET drain–source voltage $v_{DS,J1}$.

TABLE I
MAIN CHARACTERISTICS OF THE SELECTED LOW-VOLTAGE SI MOSFETS FROM INTERNATIONAL RECTIFIER [18]

	IRLR024n	**IRF2804**
V_{DSS}	55 V	40 V
I_D@T_c = 25 C	17 A	75 A
$R_{DS(on)}$@V_{GS} = 10 V	65 mΩ@I_D = 10 A	2 mΩ@I_D = 75 A
$C_{iss,M,V_{ds}=0}$	680 pF	7800 pF
$C_{oss,M,V_{ds}=0}$	480 pF	5000 pF
$C_{rss,M,V_{ds}=0}$	230 pF	2100 pF

drain–gate capacitor $C_{DGa,M}$ (artificial increasing of the Miller capacitance) in the low-voltage Si MOSFET.

The conventional techniques influence only the turn ON and turn OFF behavior of the low-voltage Si MOSFET as demonstrated in Fig. 4 with the simulation results. Illustrated are the turn ON and turn OFF switching behavior at load currents of 4 A (hard turn ON switching) and 7.5 A (turnOFF transient) for two different low-voltage MOSFETs which are specified in Table I. The MOSFET type $IRLR024n$ is characterized by low parasitic capacitance values in the range of some pF and the MOSFET $IRF2804$ exhibits an extremely low on resistance of 2 mΩ. Depending on the MOSFET capacitance values

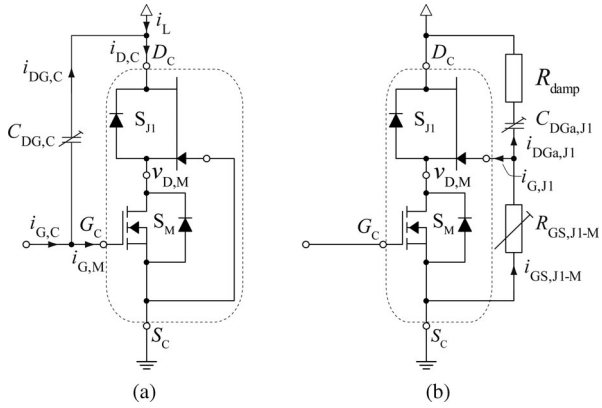

Fig. 5. Novel dv/dt controlling concepts for the SiC-Si MOSFET/JFET cascode. (a) Additional drain–gate capacitance resulting in an increased negative feedback to the MOSFET gate. (b) RC circuit between drain–gate of the SiC JFET and the external JFET gate resistor.

($C_{iss,M}$, $C_{oss,M}$, and $C_{rss,M}$) and the gate resistor $R_{G,M}$, the charge and discharge behavior of the gate–source capacitance $C_{GS,M} = C_{iss,M} - C_{rss,M}$ are drastically influenced as can be observed by the gate–source voltage $v_{GS,M}$. Also, the MOSFET drain–source voltage is strongly influenced as expected and well known in power electronics circuits. However, there is only a marginal observable change in the dv/dt-behavior of the SiC-Si cascode.

The conventional methods to control the dv/dt-value of the SiC-Si cascode influences the drain–source voltage edge of the JFET insignificantly as illustrated in the simulation result in Fig. 4. The impact of different gate resistors is reflected in the starting time of the rise and fall events of the drain–source voltage $v_{DS,J1}$. In this case, the delay times ($t_{\rm on}$, $t_{\rm off}$) can be controlled but the dv/dt of the drain–source voltage keeps the same, independent of the MOSFET type.

III. NOVEL dv/dt-LIMITATION METHODS—SIC JFET/SI MOSFET CASCODE

This section investigates novel methods to control the dv/dt in the SiC-Si cascode topology. Resulting are two concepts to slow down the very fast voltages edges at turn ON as well as at turn OFF. Fig. 5 shows two novel topologies for the cascode configuration to control the dv/dt-behavior. One of the novel topologies is based on the conventional technique for MOSFETs/IGBTs to reduce the dv/dt values with an additional capacitor $C_{DG,C}$ from the JFET drain to the MOSFET gate and therefore increasing the input capacitance [cf. Fig. 5(a)]. The other method consists of an RC-circuit ($R_{\rm damp}$, $C_{DGa,J1}$) which is used to increase the input capacitance of the SiC JFET and the additional gate resistance ($R_{GS,J1-M}$) which slows down the turn ON behavior of the JFET [cf. Fig. 5(b)]. Both dv/dt-control methods are analyzed in detail and verified with experimental results as presented in the following.

A. Drain–Gate Capacitor $C_{DG,C}$ (Concept A)

The first concept consists of an additional capacitor $C_{DG,C}$ which is connected between the MOSFET gate and the JFET

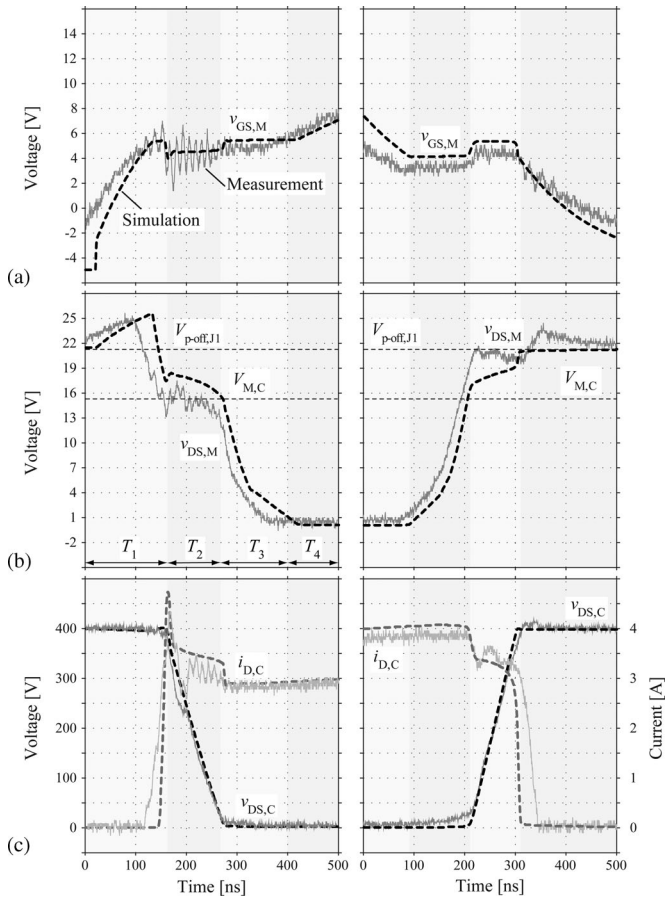

Fig. 6. Measurement (solid) and simulation (dashed) results of the SiC-Si cascode illustrating the influence of the additional capacitor $C_{DGa,C}$ at $400\ \mathrm{V}/3\mathrm{A}$ (turn ON) and at $400\ \mathrm{V}/4\ \mathrm{A}$ (turn OFF). (a) MOSFET gate–source voltage $v_{GS,M}$, (b) MOSFET drain–source voltage $v_{DS,M}$, (c) cascode drain–source voltage $v_{DS,C}$ and cascode current $i_{D,C}$. Measurement and simulation parameters: MOSFET type *IRF2804*, $C_{DG,C} = 100\ \mathrm{pF}$, $R_{G,C} = 20\ \Omega$.

drain or the SiC-Si cascode drain, respectively [cf. Fig. 5(a)]. The effect of this capacitor is the same as for a single discrete switch where the negative feedback of the Miller capacitance is increased and therefore it takes longer to complete the dynamic switching behavior due to a too small current provided by the gate driver. Therefore, the dv/dt controlling concept with the additional drain–gate capacitor $C_{DG,C}$ is based on the conventional method used in MOSFET.

The cascode gate current $i_{G,C}$ of the circuit shown in Fig. 5(a) is calculated to

$$\begin{aligned} i_{G,C} &= i_{G,M} + i_{DG,C} \\ &= i_{G,M} + C_{DG,C} \cdot -\frac{d(v_{GS,M} - v_{DS,C})}{dt}. \end{aligned} \tag{3}$$

It has to be noticed that the MOSFET gate current $i_{G,M}$ in the cascode topology is different from the gate current in a single MOSFET device. The detailed operating principle to control the dv/dt of the cascode drain–source voltage $v_{DS,C}$ is explained with experimental switching waveforms in four time intervals T_1–T_4 according to Fig. 6. The dashed lines show the simulated voltage and current waveforms which match very well with the experimental results (solid lines).

Interval T_1: During T_1, a positive voltage is applied to the MOSFET gate–source terminals and the corresponding capacitance $C_{GS,M}$ is charged. This results in a marginal increment of the MOSFET drain–source voltage. As long as $v_{GS,M} < V_{\mathrm{th},M} \approx 4\mathrm{V(max)}$, $i_{D,C}$ remains zero. Once $v_{GS,M}$ reaches $V_{\mathrm{th},M}$ the MOSFET starts conducting. While the drain current $i_{D,C}$ is increasing, the drain–source voltage starts to decrease slightly and stops abruptly when the MOSFET gate–source voltage reaches the Miller plateau. The cascode switch, mainly represented by the high voltage blocking device of the SiC JFET, is still OFF and the behavior is comparable to a single MOSFET device.

Interval T_2: At the beginning of T_2, the gate–source voltage reaches the Miller plateau where the drain current is equal to the load current and the current stops to conduct through the freewheeling SiC diode. The MOSFET drain–source voltage $v_{DS,M}$ remains at a voltage level which herein is called cascode Miller level $V_{M,C}$. This cascode Miller level is kept almost constant until the SiC JFET drain–source voltage $v_{DS,J1}$ decreases to the ON-state voltage. The cascode Miller level of $V_{M,C} \approx 16\ \mathrm{V}$ depends on the cascode drain current $i_{D,C}$. Assuming, that $v_{GS,M}$ and $v_{DS,M}$ keep a constant level [cf. Fig. 6(a) and (b)], the voltage variation in time results in

$$\frac{d(v_{GS,M})}{dt} = \frac{d(v_{DG,M})}{dt} = 0. \tag{4}$$

Therefore, during time period T_2, the MOSFET gate current $i_{G,M}$ is zero and the cascode drain current can be approximatively calculated to

$$\begin{aligned} i_{D,C} &= i_{G,C} + i_L \\ &= i_{DG,C} + i_L. \end{aligned} \tag{5}$$

The drain–gate capacitive current $i_{DG,C}$ is defined by the applied voltage across the gate resistor $R_{G,C}$ to

$$i_{DG,C} = \frac{v_G - v_{GS,M}}{R_{G,C}} = C_{DG,C} \cdot \frac{d(v_{DS,J1})}{dt}. \tag{6}$$

The SiC JFET drain–source voltage $v_{DS,J1}$ decreases linearly and the fall time t_f can be calculated with the gate current $i_{G,C}$ which is limited by the gate resistor as

$$t_f = \frac{C_{DG,C} \cdot \Delta v_{DS,J1} \cdot R_{G,C}}{V_G - v_{GS,M}}. \tag{7}$$

With a gate drive voltage of $V_G = 12\ \mathrm{V}$, a fall time of 114 ns is expected. The same fall time can be verified experimentally as demonstrated in Fig. 6(c). The cascode Miller level $V_{M,C}$ depends on the load current i_L and the capacitive drain–gate current $i_{DG,C}$. Thus, $V_{M,C}$ is decreasing with a larger drain current $i_{D,C}$ and vice versa increasing with a lower drain current. Responsible for the drain current-dependent cascode Miller level is the JFET characteristics, which has to open the channel to conduct the drain current and consequently the gate–source voltage of the JFET ($v_{DS,M} = v_{GS,J1}$) is forced to decrease. During this time interval, current oscillation can be observed which could be caused by parasitics [21]. The current ringing

effect is not yet analyzed in detail and is under investigation. At the end of interval T_2, the fast drop of $i_{D,C}$ [cf. Fig. 6(c)] indicates the complete discharge of capacitor $C_{DG,M}$ ($i_{DG,C} = 0$).

Interval T_3: During T_3, across the SiC JFET, there occurs just the voltage drop caused by the on resistances of the JFET and MOSFET channel. The gate–source voltage keeps still at the Miller plateau. In this case, it is the well-known Miller level of a single MOSFET while the MOSFET drain–source voltage decrease toward zero volts.

Interval T_4: During this stage, the cascode switch is completely in conduction mode and therefore the gate–source voltage is increasing to the nominal gate drive voltage v_G. Furthermore, the inductive load current increases depending of the load voltage and the inductance value. Therefore, the end of interval T_4 indicates also that the turn ON transient is finished.

The main influence to limit the dv/dt is taken in time interval T_2. There, only the gate drive limited current $i_{DG,C}$ is flowing through the capacitor $C_{DG,C}$ and therefore the duration of T_2 is controllable. It is important to note that the conventional dv/dt-techniques are applicable in combination with the proposed method adding a drain–gate capacitor.

At turn OFF, the dv/dt-control behavior is almost equal and analog as described in detail for the turn ON transient. First, $v_{GS,M}$ decreases and therefore $v_{DS,M}$ is driven into blocking state. The cascode drain current is still flowing through the MOSFET and JFET channels until the MOSFET drain–source voltage is between the cascode Miller level $V_{M,C}$ and the SiC JFET pinch-off voltage $V_{p\text{-off},J1}$. In fact, the SiC JFET gate–source voltage $v_{GS,J1}$ touches shortly the pinch-off voltage and immediately after, the cascode drain current drops down and the voltage $v_{DS,J1}$ increases. The JFET channel is not pinched-off completely and so still current is flowing trough both channels. The voltage variation with respect to time of $v_{DS,J1}$ is mainly controlled by the drain–gate current $i_{DG,C}$ of the additional capacitor $C_{DG,C}$. Assuming that $i_{G,M}$ is zero and the voltages applied to the MOSFET ($v_{GS,M}$ and $v_{DS,M}$) are nearly constant, the voltage variation in time can be calculated as follows:

$$\frac{d(v_{DS,J1})}{dt} = -i_{DG,C} \cdot \frac{1}{C_{DG,C}} = \frac{v_G - v_{GS,M}}{R_{G,C}} \cdot \frac{1}{C_{DG,C}}. \quad (8)$$

Due to the nearly constant current $i_{DG,C}$, the slope of the voltage change is linear and thus well controllable with the proposed configuration. Finally, the total dc-link voltage is applied across the SiC JFET and the cascode drain current decreases fast to zero. Both devices, low-voltage MOSFET and high-voltage SiC JFET, are in blocking mode.

B. RC-Circuit and JFET Gate Resistor (Concept B)

An alternative concept to control the dv/dt-behavior of the SiC-Si cascode consists of adding a RC-circuit and an additional resistor $R_{GS,J1-M}$. The idea of this configuration is to affect the drain–gate capacitance of the high voltage device, which mainly determines the dv/dt-characteristic of the SiC-Si cascode. The detailed evaluation of the dynamic behavior is described based on the experimental measurement presented in Fig. 7. The turn ON and turn OFF transitions are partitioned in five time intervals from T_1 to T_5.

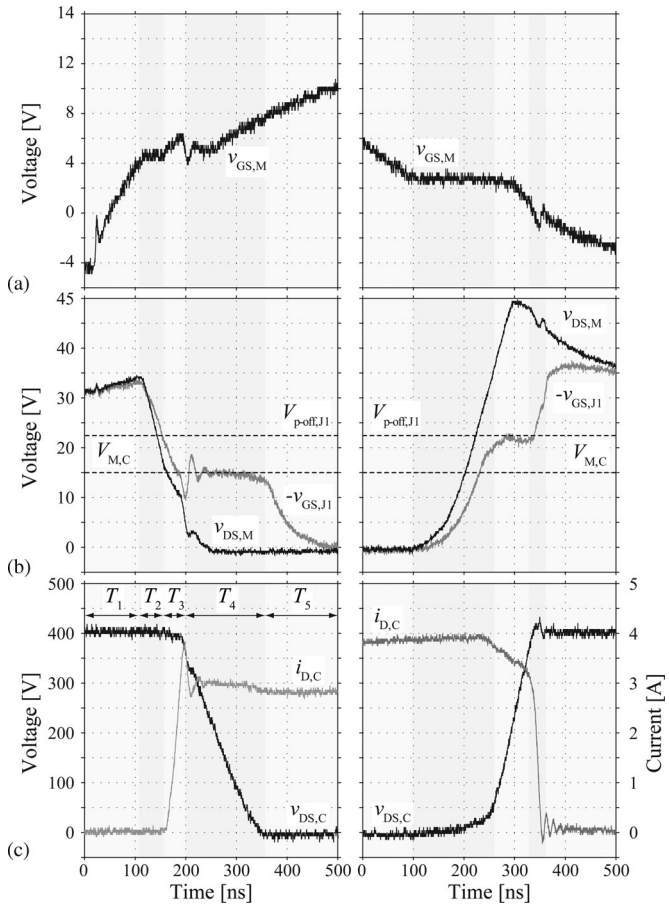

Fig. 7. Measurement results of the SiC-Si cascode illustrating the influence of the RC-circuit and the JFET gate resistor $R_{GS,J1-M}$ at 400 V/3 A (turn ON) and at 400 V/4 A (turn OFF). (a) MOSFET gate–source voltage $v_{GS,M}$, (b) MOSFET drain–source voltage $v_{DS,M}$ and the JFET gate–source voltage, (c) cascode drain–source voltage $v_{DS,C}$ and cascode current $i_{D,C}$. Measurement parameters: MOSFET type *IRF2804*, $R_{\mathrm{damp}} = 100\ \Omega$, $C_{DGa,J1} = 100$ pF, $R_{GS,J1-M} = 47\ \Omega$, and $R_{G,C} = 20\ \Omega$.

Interval T_1: Interval T_1 is equal to the proposed first control method where an additional drain–gate capacitor $C_{DG,C}$ is added. The gate–source voltage is applied and the MOSFET gate–source capacitor is charged until the Miller level is achieved. Remarkable at this time interval is that the level of the MOSFET drain–source voltage is above the pinch-off voltage of the JFET $V_{p\text{-off},J1}$. The discussion of this characteristic SiC-Si cascode overvoltage effect is shifted to the analysis of the turn OFF behavior.

Interval T_2: The gate–source voltage of the MOSFET is equal to the Miller level while the drain–source voltage of the MOSFET and the gate–source voltage of the SiC JFET decreases rapidly at the same time, hence

$$-\frac{d(v_{DS,M})}{dt} = -\frac{d(-v_{GS,J1})}{dt}. \quad (9)$$

The drain–source voltage of the JFET keeps still at the same voltage level because the corresponding gate–source junction

$v_{GS,J1}$ is still pinched off as shown in the measurement [cf. Fig. 7(b)].

Interval T_3: At the beginning of T_3, $v_{GS,J1}$ reaches the JFET pinch-off voltage and continuous decreasing. Therefore, the SiC JFET channel is not any more completely pinched off and the cascode current rises very fast with a capacitive peak current. Once, the cascode drain current $i_{D,C}$ achieves the load current, the freewheeling diode stops to conduct and the load current is commutated to the SiC-Si cascode. The MOSFET drain–source voltage is also decreasing and the gate–source voltage is still equal to the Miller plateau voltage.

Interval T_4: At the beginning of this period, the low-voltage MOSFET is completely turned ON and $v_{GS,M}$ increases to the nominal gate voltage V_G. The JFET gate–source voltage $v_{GS,J1}$ reaches the cascode Miller voltage $V_{M,C}$ and keeps the voltage level over the whole time period, thus resulting as

$$\frac{d(v_{GS,J1})}{dt} = 0. \tag{10}$$

The constant voltage $v_{GS,J1}$ is also applied across the JFET gate resistor $R_{GS,J1-M}$ and therefore the current which is responsible for discharging the JFET drain–gate capacitors ($C_{DG,J1}$ and $C_{DGa,J1}$) can be calculated to be

$$i_{GS,J1-M} = \frac{v_{GS,J1}}{R_{GS,J1-M}}. \tag{11}$$

The current $i_{GS,J1-M}$ could be separated into two parts depending on the impedance of the capacitor $C_{DG,J1}$ and the series connection of the capacitor $C_{DGa,J1}$ and resistor R_{damp}. The valid analytical expression during this time period is

$$\begin{aligned} i_{GS,J1-M} &= i_{G,J1} + i_{DG,J1-C} \\ &= C_{DG,J1}(v_{DS,J1}) \cdot \frac{d(v_{DS,J1})}{dt} \\ &\quad + C_{DGa,J1} \cdot \frac{d(v_{DGa,J1})}{dt}. \end{aligned} \tag{12}$$

Due to the nonlinear characteristics of the SiC JFET parasitic drain–gate capacitor $C_{DG,J1}(v_{DG,J1})$ which strongly depends on the corresponding drain–gate voltage $v_{DG,J1}$, the dv/dt is mainly controlled by the additional drain–gate capacitor $C_{DGa,J1}$. Out of the measurement, the resulting calculated drain–gate capacitor at 400 V is

$$C_{DG,J1}(400\ \mathrm{V}) \approx 25\ \mathrm{pF} < C_{DGa,J1} \tag{13}$$

which is smaller than the additional capacitor [22]. With a total drain–gate capacitance of 125 pF, the calculated fall time is approximately 150 ns.

While the current $i_{GS,J1-M}$ discharges the drain–gate capacitors of the SiC JFET, the $v_{DS,J1}$ decreases linearly. The cascode drain current contains the sum of the load current and the discharge currents which are equal to

$$i_{D,C} = i_{G,J1} + i_{DGa,J1} + i_L. \tag{14}$$

In Fig. 7(c), a small increment in the cascode current is visible as expressed in (14) during the whole time period.

Interval T_5: In the last part of the turn ON transition, $v_{GS,J1}$ decreases to the on voltage of the conduction mode. The final discharging process becomes truly an RC-circuit mechanism conformed by the JFET gate–source capacitor $C_{GS,J1}$ and the JFET gate resistor $R_{GS,J1-M}$.

The dv/dt-limitation in this concept for the cascode topology takes place in the fourth interval T_4 where the discharge of the capacitor occurs. The resistor R_{damp} is required to damp the appearing MOSFET gate drive oscillation. The dv/dt limitation is mainly controlled by two parameters, the $C_{DGa,J1}$ and the $R_{GS,J1-M}$.

The turn OFF event is analog to the turn ON transition and therefore only specific issues are discussed. The MOSFET drain–source voltage $v_{DS,M}$ is increasing until the SiC JFET pinch-off voltage is reached. At this point, the JFET drain–source voltage $v_{DS,J1}$ starts to increase while the MOSFET drain–source voltage is further increasing as far as the whole voltage is blocked by the cascode. In addition, the voltage variation in time of $v_{DS,J1}$ is zero. The SiC JFET gate–source voltage is constant and close to the pinch-off voltage level. The JFET channel, however, is still not completely diminished (pinched off) and so a drain current is flowing. After the actual turn off transition at $t \approx 340$ns, the JFET gate–source voltage rises very fast caused by the capacitor $C_{GS,J1}$ charging current

$$\begin{aligned} -i_{GS,J1-M} &= \frac{v_{DS,M} - v_{GS,J1}}{R_{GS,J1-M}} \\ &= C_{GS,J1} \cdot -\frac{d(-v_{GS,J1})}{dt}. \end{aligned} \tag{15}$$

The JFET gate–source diode is driven into avalanche until the dynamic balancing process is completed. Also, the low-voltage MOSFET is closely driven to its avalanche voltage and under different conditions, the maximal MOSFET blocking voltage can be possibly reached. In case of continuous operation at high frequency, the gate–source diode will not be able to recover properly and will operate continuously in avalanche mode. This effect can be observed by the turn ON transition in Fig. 7(b) where the JFET gate–source voltage is above the pinch-off voltage.

In order to provide simulation results demonstrating the before discussed dv/dt-behavior, the accurate avalanche behavior of the SiC JFET gate–source diode has to be implemented. The SPICE model used in this paper presents an ideal behavior and no avalanche mode can be observed. Therefore, no simulation results regarding this technique for dv/dt-control are presented and just experimental results are shown to see the effectiveness of the method.

As seen in Figs. 6 and 7, both concepts can reduce the dv/dt-rating of the SiC-Si cascode. The main advantage of the first concept is the proper operation in the nominal and specified ranges of the devices. In the second concept, there are more parameters to control the dv/dt but also the avalanche mode operation of the JFET gate–source diode plays an important role. Furthermore, both concepts have additional losses due to the additional capacitors and the decreased dv/dt of the cascode voltage edges. In the following, a set of experimental results demonstrates the controllability of the proposed SiC-Si cascode configurations.

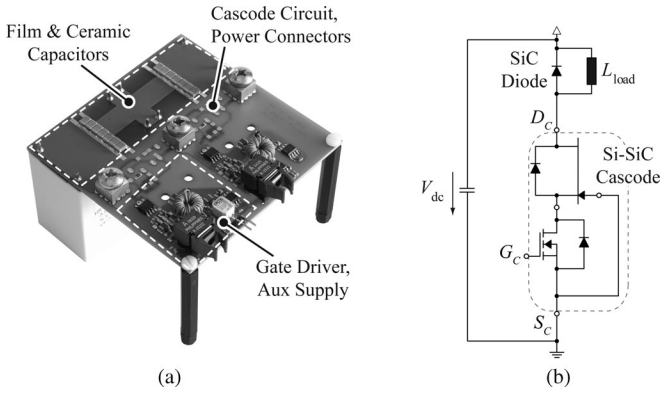

Fig. 8. (a) Experimental setup to verify the concepts of the dv/dt-control by the proposed methods for the SiC JFET/Si MOSFET cascode. (b) Schematic of the experimental topology (two-pulse test setup).

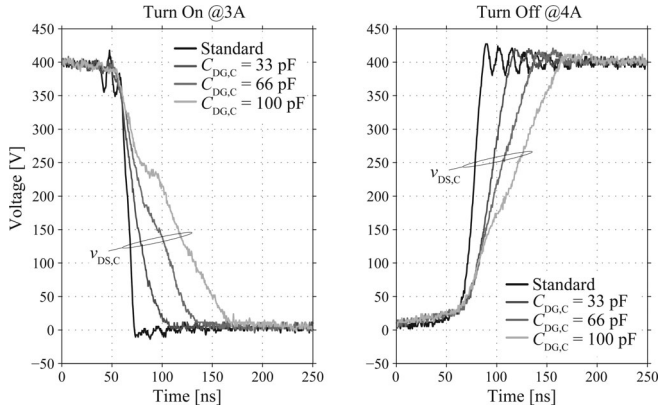

Fig. 9. Measurement results of the dv/dt-control concept A at $V_{\rm dc}$ =400 V and different values of the drain–gate capacitance $C_{DG,C}$.

IV. Experimental Results

In the following, measurement results using a test prototype (cf. Fig. 8) are presented to verify both aforementioned concepts (A and B) with different values of the parameters ($C_{DG,M}$, $C_{DGa,J1}$, and $R_{GS,J1-M}$). The measurement labeled as standard, means the cascode topology with a low-voltage MOSFET and the SiC JFET without any additional components. The gate resistance $R_{G,C}$ for this configuration is selected to be 4.7 Ω. For all the other measurement to verify both concepts, a gate resistance of $R_{G,C} = 20\,\Omega$ is used. The experimental setup is a buck topology whereas the cascode circuit and the SiC diodes are mounted on the bottom side of the PCB between the power connectors. Furthermore, the passive dv/dt network is placed on the top side of the PCB between the power connectors as close as possible to the cascode circuit. The voltages have been measured with a standard LeCroy voltage probe and the current measurement has been performed with a current transformer which has been compensated in terms of delay according to the voltage measurement. Due to the timely adjustment, the switching energies are directly calculated out of the measurements.

Fig. 9 presents the measurement results of concept A with the additional drain–gate capacitor. The tests are performed with three parameters of $C_{DG,C} = \{33,\ 66,\ \text{and}\ 100\ \text{pF}\}$. The larger values of the additional drain–gate capacitor will result in lower experimental dv/dt values. The fall time approximately calculated with (7) scales directly with the drain–gate capacitance assuming the same gate resistor and gate drive voltage.

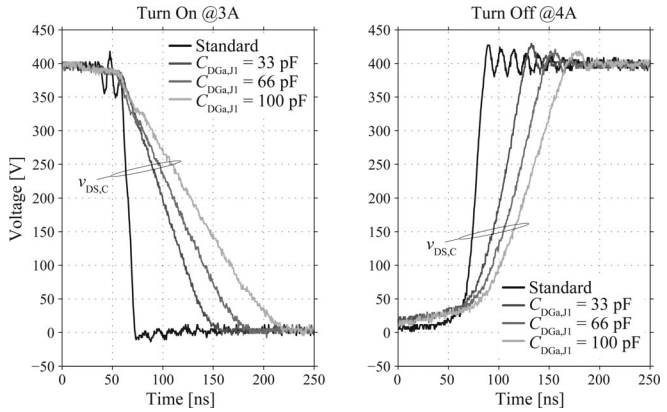

Fig. 10. Measurement results of the dv/dt-control concept B at $V_{\rm dc} = 400$ V and different values of the capacitance $C_{DGa,J1}$, with a damping resistor $R_{\rm damp} = 100\,\Omega$ and JFET gate resistance $R_{GS,J1-M} = 47\,\Omega$.

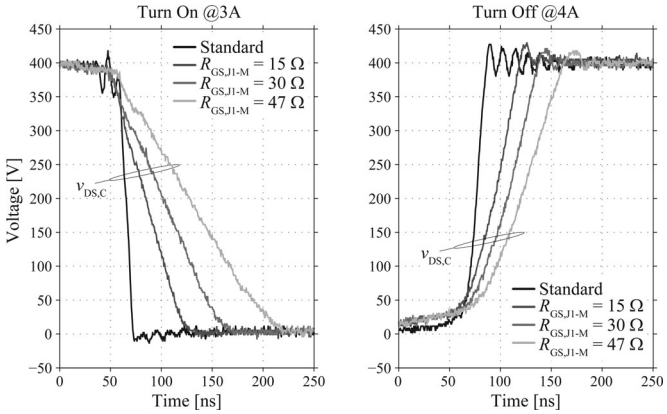

Fig. 11. Measurement results of the dv/dt-control concept B at $V_{\rm dc} = 400$ V and different values of the JFET gate resistance $R_{GS,J1-M}$, with a drain–gate capacitance $C_{DGa,J1} = 100$ pF and damping resistor $R_{\rm damp} = 100\,\Omega$.

The experimental voltage waveforms of concept B with the RC-element and the JFET gate resistor $R_{GS,J1-M}$ are demonstrated in Figs. 10 and 11. On the one hand, Fig. 10 shows that the dv/dt is controlled by different values of drain–gate capacitance $C_{DGa,J1} = \{33,\ 66,\ \text{and}\ 100\ \text{pF}\}$. On the other hand, the voltage variation in time is regulated by different SiC JFET gate resistances $R_{GS,J1-M} = \{15,\ 30,\ \text{and}\ 47\,\Omega\}$. In addition, all measurements show that the ringing at turn OFF is damped with controlled and lower dv/dt-values.

Based on the experimental ON/OFF switching transitions performed with the test setup shown in Fig. 8, the energy losses of the SiC-Si cascode are evaluated. The turn ON/OFF energy losses are calculated from the measured switching voltage $v_{DS,C}$ and switching current $i_{D,C}$.

In Fig. 12(a), the energy losses of concepts A and B are shown versus the voltage variation in time (dv/dt). With lower and controlled dv/dt-values, the energy losses are increasing. Due to the fact that the fall and rise times of the SiC-Si

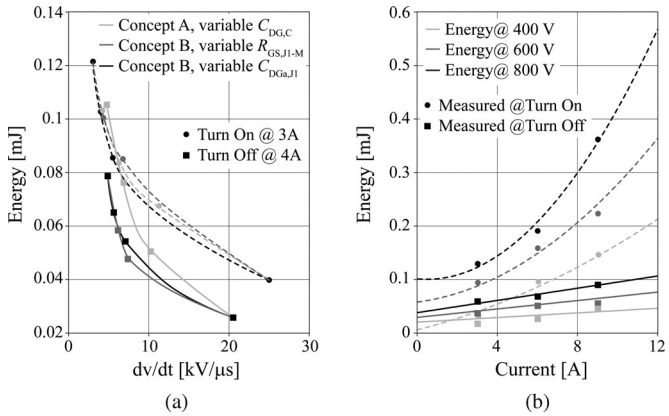

Fig. 12. Switching energy losses measured in a buck converter configuration with a SiC Diode (*C2D10120*) and the SiC-Si cascode (SiC JFET V_p-off = 22.3 V, $R_{DS(\mathrm{on}),J1} = 0.33\,\Omega$, MOSFET (*IRF2804*)): (a) Turn ON/OFF energy losses of the dv/dt-control concepts A and B at 400 V. (b) Evaluated energy losses of the standard SiC-Si cascode at dc-link voltage levels of $V_{\mathrm{dc}\text{-link}} = \{400, 600, 800\,\mathrm{V}\}$. Note: The measurements are performed at room temperature.

cascode are increased, the product of voltage and current is larger over time which results in increased energy losses. Moreover, the required passive elements for controlling the dv/dt-behavior generate additional energy losses. Out of it, a tradeoff between switching losses and EMI filtering is resulting. It is part of future investigation to define a methodology how to select the parameters for dv/dt control to optimize the switching behavior of the SiC-Si cascode leading to acceptable EMI and less switching losses.

In case of concept A, the additional drain–gate capacitor $C_{DG,C}$ of 100 pF stores an energy of 8 μJ at 400 V. The capacitor energy is completely dissipated per switching cycle in the SiC-Si cascode. The measured energy losses at turn ON and turn OFF for concept A with $C_{DG,C}$= 100 pF result in $\approx$ 120 μJ (ON) and $\approx$ 105 μJ (OFF). Comparing these values with the measured energy losses of the standard SiC-Si cascode (measurement with highest dv/dt-values: lower right corner) of $\approx$ 40 μJ (ON) and $\approx$28 μJ (OFF) makes clear that the larger energy losses by lower dv/dt-values are mainly caused by the voltage variation over time. The influence of the additional capacitor energy losses is comparably small. The concepts A and B have almost the same turn ON energy losses. However, the turn OFF switching transitions concept A shows more energy losses than the concept B especially at lower dv/dt values or larger capacitor of $C_{DG,C}$, respectively. This additional amount of energy losses can be partially explained by the cascode drain–source voltage shown in Fig. 9. At turn OFF, the drain–source voltage $v_{DS,C}$ increases faster to 150V. At this point, the measured waveform shows almost an s-shaped characteristic most probably caused by the SiC JFET channel diminishing almost completely (for a very short time) (cf. Fig. 6(b) at $t = 250$ ns). This effect could also be related to stray inductance in the circuit. Therefore, a short delay time in voltage variation occurs while almost the whole drain current is flowing through the device.

In case of concept B, it should be considered that the stored energy in capacitor $C_{DGa,J1}$ is not completely dissipated in the SiC-Si cascode due to the series resistors of R_{damp} and $R_{GS,J1-M}$. Furthermore, the energy losses caused by the avalanche mode of JFET gate–source diode [cf. Fig. 7(b)] are not considered in both, the analysis and in Fig. 12(a).

In Fig. 12(b), the energy losses of the standard SiC-Si cascode are presented for different voltage and current levels measured at room temperature. The turn ON energy losses increase with a polynomial second order whereas the turn OFF energy losses increase linearly with current. At hard switching and with a nominal current of 5A, the SiC JFET does not exceed the value of 200μJ. Therefore, the SiC-Si cascode shows an attractive alternative to nowadays standard Si semiconductor technology aiming for high-frequency operation or high power density.

V. Conclusion

As shown in this paper, SiC devices in a cascode structure with a low-voltage Si MOSFET are characterized by very fast switching behavior. Depending on the application area, it is sometimes desired to reduce the voltage edges in order to limit EMI effects. Therefore, novel concepts to control and adjust the dv/dt of the SiC JFET/Si MOSFET cascode has been presented. It has been shown with experimental measurements that the voltage edges of the cascode switch could be controlled extending the gate drive with passive components utilizing the Miller effect. Therefore, problems like layout caused overvoltages, earth leakage currents, or EMI problems in general could be handled and facilitates the utilization of the SiC cascode switch in a wide range of application. However, the results illustrated that there is the tradeoff between switching losses and dv/dt-rate which must be considered in the course of the converter design.

References

[1] J. Biela, U. Badstuebner, and J. W. Kolar, "Design of a 5-kW, 1-U, 10-kW/dm^3 resonant DC–DC converter for telecom applications," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1701–1710, Jul. 2009.

[2] J. W. Kolar and H. Ertl, "Status of the techniques of three-phase rectifier systems with low effects on the mains," presented at the 21st Int. Telecommun. Energy Conf., Copenhagen, Denmark, Jun. 1999.

[3] S. D. Round, P. Karutz, M. L. Heldwein, and J. W. Kolar, "Towards a 30 kW/liter, three-phase unity power factor rectifier," in *Proc. Power Convers. Conf.*, Apr. 2007, pp. 1251–1259.

[4] P. Friedrichs, "Silicon carbide power devices—Status and upcoming challenges," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2007, pp. 1–11.

[5] M. Shur, S. Rumyantsev, and M. Levinshtein, *SiC Materials and Devices—Volume 2 (Selected Topics in Electronics and Systems)*. Singapore: World Scientific, 2007, vol. 43.

[6] M. L. Heldwein and J. W. Kolar, "A novel SiC J-FET gate drive circuit for sparse matrix converter applications," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2004, vol. 1, pp. 116–121.

[7] A. Orellana and B. Piepenbreier, "Fast gate drive for SiC-JFET using a conventional driver for MOSFETs and additional protections," in *Proc. 30th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2004, vol. 1, pp. 938–943.

[8] R. Kelley and M. S. Mazzola, "SiC JFET gate driver design for use in DC/DC converters," presented at the 21st Annu. IEEE Applied Power Electronics Conf. Expoosition, Dallas, TX, Mar. 2006.

[9] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in *Proc. 14th IAS Annu. Meet. Ind. Appl. Conf.*, Oct. 2005, vol. 1, pp. 410–416.

[10] R. Kelley, F. Rees, and D. Schwob, "Optimized gate driver for enhancement-mode SiC JFET," in *Proc. Int. Conf. Power Electron. Intell. Motion Power Quality*, 2009.

[11] L. Yang and W. G. H. Odendaal, "Measurement-based method to characterize parasitic parameters of the integrated power electronics modules," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 54–62, Jan. 2007.
[12] M. Moreau, N. Idir, P. Le Moigne, and J. J. Franchaud, "Utilization of a behavioural model of motor drive systems to predict the conducted emissions," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 4387–4391.
[13] J. D. Kagerbauer and T. M. Jahns, "Development of an active dv/dt control algorithm for reducing inverter conducted EMI with minimal impact on switching losses," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 894–900.
[14] P. Lefranc and D. Bergogne, "State of the art of dv/dt and di/dt control of insulated gate power switches," in *Proc. Conf. Power Supply Energy Manage. Def. Appl.*, Jan. 2007.
[15] N. Idir, R. Bausiere, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 849–855, Jul. 2006.
[16] S. Park and T. M. Jahns, "Flexible dv/dt and di/dt control method for insulated gate power switches," *IEEE ASSP Mag. Trans. Ind. Appl.*, vol. 39, no. 3, pp. 657–664, May/Jun. 2003.
[17] M. Rashid, *Power Electronics Handbook*. New York: Academic, 2001.
[18] *International Rectifier* [Online]. Available:http://www.irf.com
[19] CREE [Online]. Available:http://www.cree.com
[20] Y. Wang, C. J. Cass, T. P. Chow, F. Wang, and D. Boroyevich, "SPICE model of SiC JFETs for circuit simulations," in *Proc. IEEE Workshop Comput. Power Electron.*, Jul. 2006, pp. 212–215.
[21] I. Josifovic, J. Popovic-Gerber, and J. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3843–3854, Aug. 2012.
[22] T. Funaki, T. Kimoto, and T. Hikihara, "Evaluation of capacitance-voltage characteristics for high voltage SiC-JFET," *IEICE Electron. Expr.*, vol. 4, no. 16, pp. 517–523, Aug. 2007.

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