Power Electronic Systems
Laboratory

Proceedings of the 8th International Conference on Power Electronics (ECCE Asia 2011), The Shilla Jeju, Korea,
May 30-June 3, 2011.

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Comparison of 2- and 3-level Active Filters with Enhanced Bridge-Leg Loss Distribution

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***Abstract*-- In this paper an efficiency comparison between 3-phase shunt active filters derived from the 2-level VSC, the 3-level NPC, Active NPC (A-NPC) and the T-type VSC is presented. In order to address the loss distribution issue of the 3-level topologies, while keeping the efficiency of the system high, a space vector modulation scheme incorporating a special clamping of the phase is proposed. It is shown that 3-level active filters can have their losses well distributed over the chip dies, leading to only a small difference in their operating temperatures. Additionally, a semiconductor area based comparison is used to further evaluate the studied active filter systems. Finally, experimental results obtained with a 12kVAr/48kHz 3-level NPC based shunt active filter employing custom SiC power modules are presented in order to demonstrate the performance and feasibility of this solution.**

***Index Terms*—Active filter, space vector modulation.**

I. Introduction

In industrial applications such as photovoltaic grid inverters, rectifiers, motor drives and active filters intended for low DC-link voltage level, the 3-phase 3-level Voltage Source Converters (VSC) are not wide spread because of the intrinsically large number of parts and consequent high costs [1]. Another disadvantage of the 3-level topologies is the essential active control of their neutral-point potential [2]. On the other hand, 3-level VSC systems built with 600V semiconductors can achieve lower losses than conventional 2-level converters built with 1200V devices if the considered switching frequency is high enough [3] and [4].

Shunt active power filters are frequently used to minimize the harmonic disturbances created by non-linear loads, as they improve the filtering efficiency, and also solve many issues arising with classical passive filters [5]. During the design of such a system, special attention has to be paid to the load currents, which are intended to be compensated. Together with the modulation strategy employed, the load currents determine the circulating current in the power devices of the selected VSC topology. Especially in 3-level active filters, the commonly irregular load can lead to an uneven loss distribution in the semiconductors of a bridge leg. Consequently, in active filters employing standard commercial bridge-leg modules, the thermal mismatch of the components can lead to induced thermal stresses on the materials within the module. Thus, thermo-mechanical damage can arise, reducing the system reliability [6] and [7].

In this paper, 3-phase shunt active filters derived from the 3-level NPC, A-NPC and the T-type VSC are proposed as alternatives to the standard 2-level VSC for a medium switching frequency range and a low DC-link voltage level. In order to address the loss distribution problem of the typical 3-level structures, a space vector modulation scheme incorporating a special clamping of the phase is proposed. This strategy can be used to maximize the efficiency of the system and/or to distribute the component losses, such that the thermal mismatch of the individual elements in a bridge leg is minimized. Consequently, for many typical industrial loads, the use of a more complex and expensive active filter topology, such as the active NPC, becomes difficult to justify.

This article is organized as follows. In Section II, suitable shunt active filters derived from the 3-level NPC, active NPC and the T-type VSC are presented. An efficiency comparison between these topologies is shown

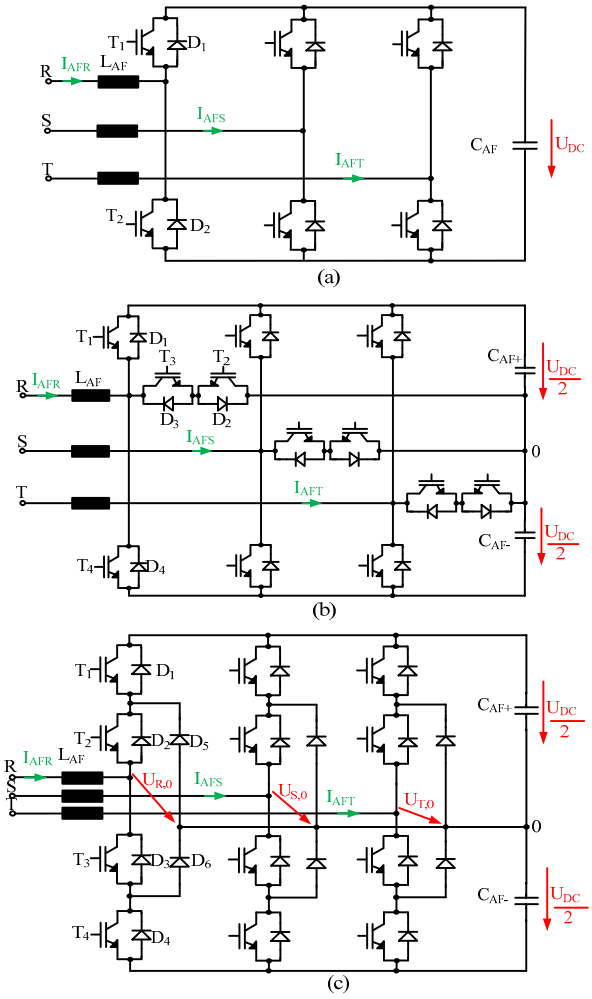

Fig. 1- Active Filter based on: (a) 2-level VSC; (b) 3-level T-type VSC and (c) 3-level NPC.

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in Section III. The analyses are performed for converter operation in the switching frequency range of 5 kHz to 48 kHz and with low DC-link voltage level. Three typical industrial loads are considered in the loss analysis with switching loss measurements of commercial semiconductors obtained in a test setup. In Section IV the loss calculation is extended to a variable chip area to allow a fair comparison between the studied systems. This approach not only provides a distinct figure-of-merit for comparison, but also can be used to determine the semiconductor costs of the different topologies. Finally, in Section V experimental results obtained with a 12kVAr 3-level NPC active filter are presented to demonstrate the performance and feasibility of this solution.

II. 3-LEVEL SHUNT ACTIVE FILTERS

Shunt active filters derived from the 2-level VSC, the 3-level T-type VSC and the 3-level NPC are shown in Fig. 1(a), 1(b), and 1(c), respectively.

The 3-level T-type VSC constitutes a standard 2-level VSC with an active bidirectional switch connecting the AC terminal with the DC-link mid-point "0". For low DC-link voltage level (U_{DC}) in the range of 700V to 1000V, as for the 2-level VSC, the studied T-type VSC would require 1200V IGBTs and diodes for the top and bottom switches. Since the bidirectional mid-point switches have to block only half of the DC-link voltage, 600V IGBTs and anti-parallel diodes can be used.

The switch states of a single phase leg of the 3-level T-type VSC are given in Table I. Assuming the operating conditions where the AC terminal has impressed positive or negative current, I_{AFR}, and positive input voltage, U_N, the commutation to or from the terminals "P" and "0" (P↔0) are depicted in Fig. 2(a). As can be seen, all commutations take place between one active switch and one diode. Accordingly, only one active switch and one diode experience essential switching losses.

The 3-level NPC shown in Fig. 1(c) requires 6 diodes and 4 IGBTs per phase-leg. The number of IGBTs and isolated gate drivers is twice that of the 2-level VSC. Compared to the T-type VSC, the NPC needs 2 more diodes per phase-leg. The switching states described in Table I are also suitable for the 3-level NPC, where the switch transitions to or from the terminal "P" and "0" (P↔0) are depicted in Fig. 2(b).

As can be observed in Fig. 2, the direction of the phase current establishes the utilization of the upper, bottom and inner switches of the 3-level NPC and T-type VSCs. Evidently, a high utilization of the power semiconductors is desired to reach the lowest converter cost per kVA processed. However, this becomes very difficult to achieve with active filters based on these 3-level structures. Due to the fact that, shunt active filters are usually used to compensate very irregular currents, conditions of unsymmetrical loss distribution across the phase-leg semiconductors are common. As in every converter, the losses in the most stressed device limit the switching frequency and the power capability, a de-rating of the converter current can become mandatory to ensure long term stability [2].

Table. I- Switch States of the 3-level NPC and T-type VSC.

	T_1	T_2	T_3	T_4
State P	1	1	0	0
State 0	0	1	1	0
State N	0	0	1	1

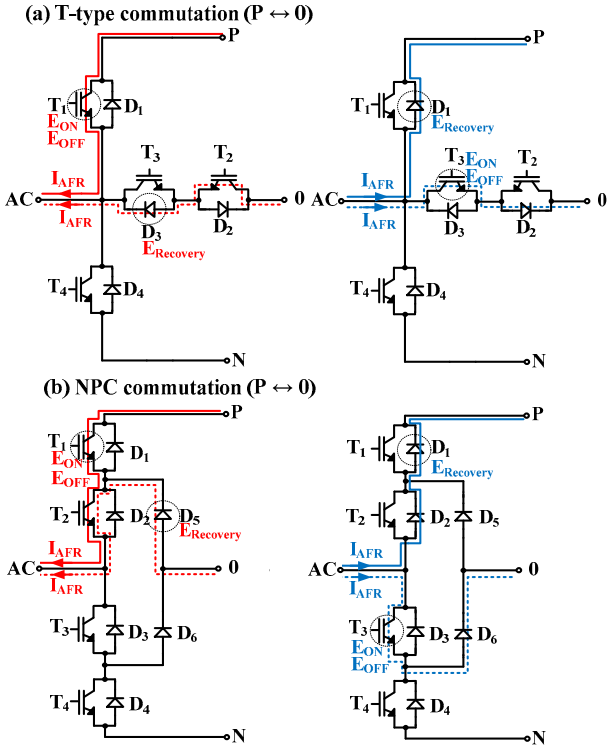


Fig. 2. Commutations (P↔0) in the 3-level: (a) T-type VSC; and (b) NPC. Note that the switches suffering essential switching losses are encircled. E_{ON}, E_{OFF} and $E_{Recovery}$ represent the turn-on, turn-off and recovery losses, respectively.

A 3-level Active NPC (A-NPC), which features loss balancing capability, is shown in Fig. 3. The two extra active switches per phase-leg added to the 3-level NPC, T_{Ax1} and T_{Ax2}, allow a substantial improvement in semiconductor loss distribution (cf. [2]). The main factors preventing the 3-level A-NPC from being successful in the active filter market are the substantial increase of costs and complexity. When compared to the 2-level VSC, the A-NPC requires 12 extra active switches, diodes and isolated gate drivers.

The switch states of a single phase of the 3-level A-NPC are given in Table II. Fig. 4 shows the commutations to or from "P" and "0" with the redundant zero states "0U1", "0U2", "0L1" and "0L2". By distributing conduction and switching losses more evenly across the phase-leg's devices, the A-NPC can achieve high utilization of the upper, lower and mid-point switches [8]. Unfortunately, the 3-level A-NPC cannot operate at higher efficiency than a 3-level NPC. In fact, these systems have similar power losses, as during each commutation, one diode and one active switch always experience essential switching and conduction losses.

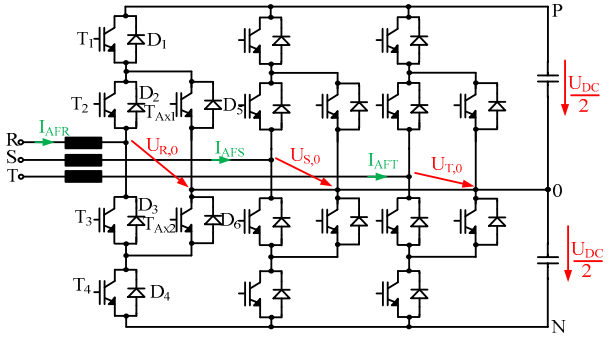


Fig. 3- Active Filter based on 3-level active NPC.

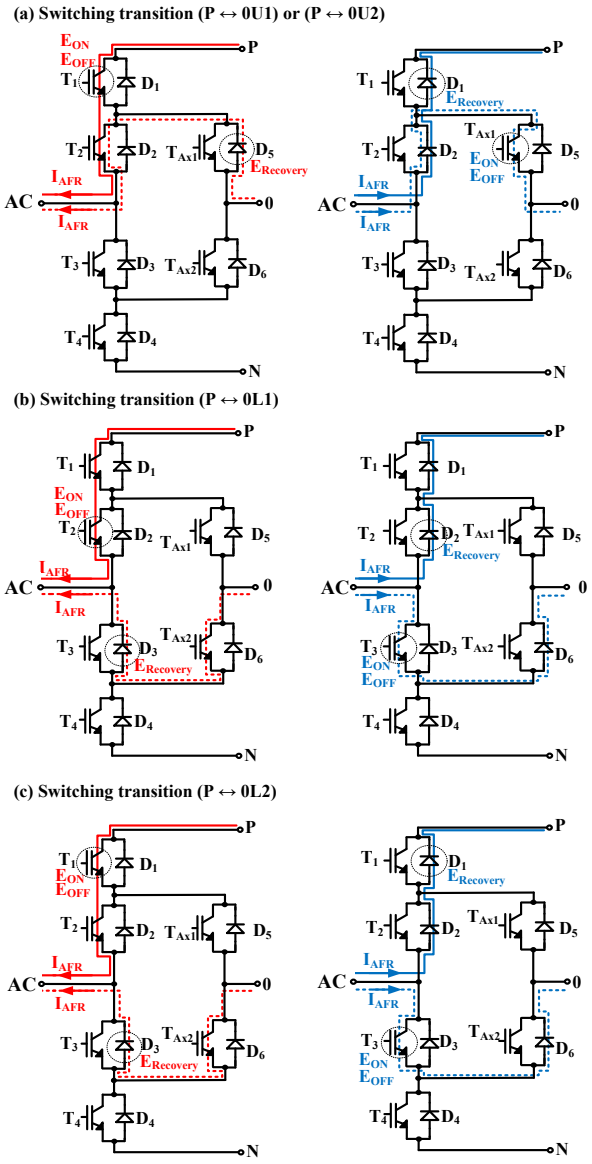


Fig. 4. Commutations in the 3-level A-NPC: (a) (P↔0U1) or (P↔0U2); (b) (P↔0L1); and (c) (P↔0L2). Note that the switches suffering essential switching losses are encircled. E_{ON}, E_{OFF} and $E_{Recovery}$ represent the turn-on, turn-off and recovery losses, respectively.

In the following, a DQ-frame based control concept suitable for the active filters studied here will be presented and its characteristics described. A control strategy suitable for the balancing of the DC-link capacitor voltages, which incorporates a non-linear control, will be introduced.

Table. II- Switch States of the 3-level A-NPC.

Device	T_1	T_2	T_3	T_4	T_{Aux1}	T_{Aux2}
State P	1	1	0	0	0	1
State 0U1	0	1	0	1	1	0
State 0U2	0	1	0	0	1	0
State 0L1	1	0	1	0	0	1
State 0L2	0	0	1	0	0	1
State N	0	0	1	1	1	0

A. Combined Loss Minimized and DC-link balancing Space Vector Modulation

Several modulation and control strategies exist for the 3-level NPC, which could be used in the A-NPC and T-type VSCs. For the systems presented in this paper, a space vector modulation (SVM) scheme, based on [9], is considered for analysis. It is possible to stop the switching operation of each phase leg of a 3-phase VSC for 120 degrees in one fundamental grid period, generating almost the same distorted output current as typical sinusoidal PWM methods [9]. When aiming for high efficiency, especially during high switching frequency operation, the "no switching interval" can be set to match the phase leg with the highest current values. On the other hand, to keep the symmetry of losses in the three phase-legs, the no switching duration must be 60 degrees for positive and negative voltage.

In this work, depending on the current shape of the load compensated by the active filter, the top and bottom DC-link capacitors are alternately loaded according to a carrier signal with 3 or 9 times the fundamental frequency of the grid. Fig. 5(a) and 5(b) show both modulation strategies adjusted for a 3-phase 12-pulse diode rectifier with constant output current as load. Therein, a considerable reduction of losses would be achieved by clamping the bridge leg that handles the highest current values (cf. Fig. 5(a)). By increasing the frequency of the clamping process and preventing the switching intervals from matching the instant of high current values, a better controllability of the loss distribution among the bridge leg components can be obtained (cf. Fig. 5(b)).

Together, the proposed current clamping scheme and the generally high values for the capacitors of the active filter are commonly sufficient to balance the DC-link voltages over one fundamental cycle. On the other hand, asymmetries in the circuit and load variations can cause a steady drift of the neutral-point potential. In order to ensure the balancing of the DC-link capacitor voltages, while keeping the symmetry of loss between the phase legs, a proper selection of the redundant zero vectors is required. The charging cycle of the DC-link capacitors become equal when the duty cycle (D) of the carrier signal is set to 50%. Any other duty cycle value produces an asymmetric modulation and it can be used for the balancing control of the DC-link capacitor voltages as shown in Fig. 5(c).

The DQ-frame based control suitable for the 3-level active filters is shown in Fig. 6. It consists of a fast current control loop and a slow voltage control loop. Additionally, there is a partial DC-link voltage control

which balances the capacitor voltages. Note that other strategies such as PQ theory, Fryze currents, generalized integrators, frequency domain strategies (DFT and RDFT), etc. (cf. [5]), could also be employed.

In order to obtain a good controllability of the active filter currents, the current controller (*G(s)*) bandwidth is selected to be fifty times higher than the main DC-link voltage controller (*H(s)*). In order to some extent, to maintain the optimal clamping of the currents during imbalances of the DC-link voltages, the bandwidth of the partial DC-link voltage controller (*R(s)*) is selected as one fifth (1/5) of the main voltage loop bandwidth. A non-linear control combining hysteresis and linear concepts is employed as shown in Fig. 7. For low voltage imbalances, the output signal of the *R(s)* controller is compared to a PWM modulator with 3 or 9 times the mains frequency. This determines the carrier duty cycle that selects one of the redundant zero vectors on the inner hexagon of the space vector modulation scheme. For high voltage imbalances, the modulator saturates and a hysteresis-like control takes over.

Note that the synchronization of the carrier modulator with the grid voltages or load currents is essential to perform the clamping during the desired non-switching intervals. The current clamping can be defined in advance by an accurate analysis of the necessarily known load currents. In cases where the displacement of the load current varies considerably with the handled power, a look-up table can be built to tune the carrier accordingly.

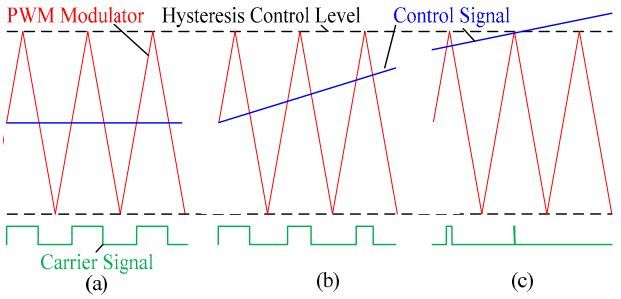


Fig. 7- Partial DC-link voltage control scheme: (a) balanced condition; (b) light imbalanced DC-link voltages, partially preserving clamping; and (c) high voltage imbalances requiring hysteresis control.

III. Comparison of 2- and 3-Level Active Filters

In this section an efficiency comparison between 12kVAr rated 3-phase shunt active filters derived from the 2-level VSC, the 3-level NPC, A-NPC and T-type VSCs is presented. For the A-NPC modulation the loss

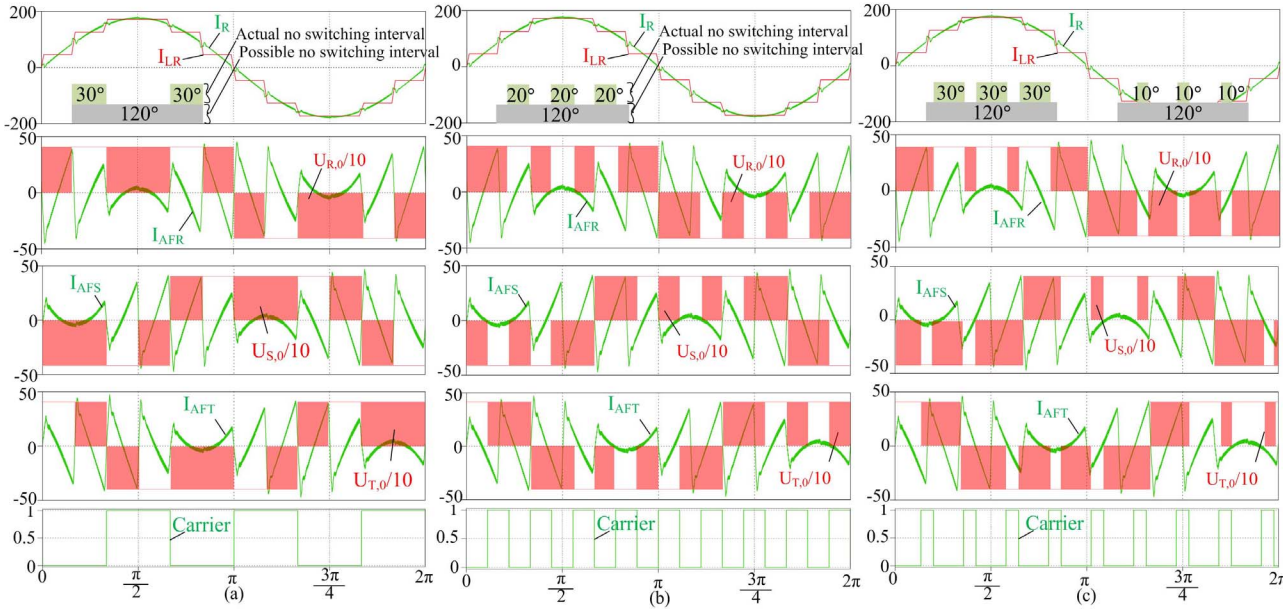


Fig. 5- 3-level active filter modulation schemes: (a) clamping strategy with 3rd harmonic frequency carrier; (b) clamping strategy with 9th harmonic frequency carrier; and (c) clamping strategy during imbalanced DC-link capacitor voltages with 9th harmonic frequency carrier.

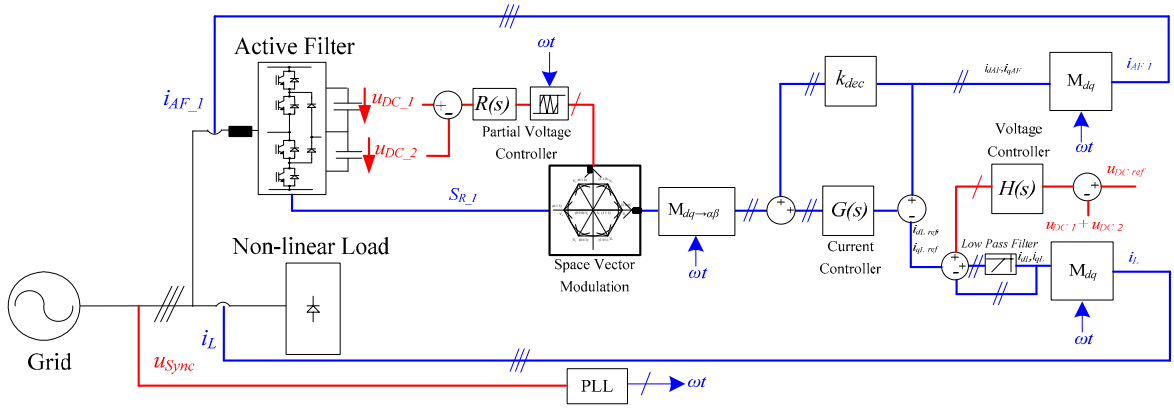


Fig. 6- Active filter control strategy based on DQ-frame theory.

balancing scheme proposed by [2] is used. Three typical industrial loads comprising 3-phase 6- and 12-pulse diode rectifiers are considered in the analysis. The Infineon IGBTs 600V IKW30N60T and 1200V IKW25T120 are selected for the assessment.

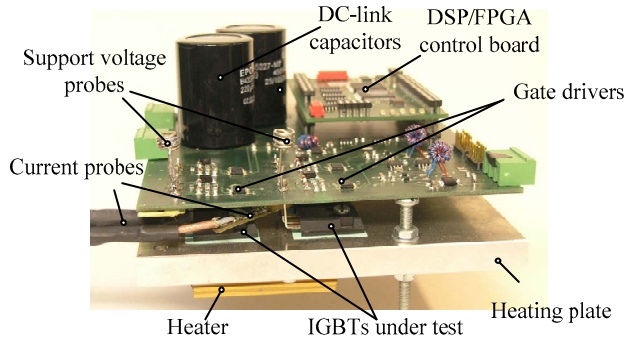


Fig. 8- Switching losses test set-up of a single bridge leg.

For an accurate analysis of the switching losses, using only the information from the datasheets would not be enough to enable a fair comparison among the studied systems. Due to the mismatch of voltage rated devices in the T-type topology, the turn-on energy of the 1200V IGBTs will be lower if the commutating diode is only 600V rated because of the considerably lower reverse recovery charge. In the same matter, the 600V active switch turn-on energy or the diode recovery loss will be higher if the commutating device is 1200V rated. Therefore, the test set-up shown in Fig. 8 was built in order to determine the loss characteristics of the selected IGBTs.

Fig. 9 presents the studied non-linear loads and the active filter currents including the selected clamping pattern for high efficiency operation. With the semiconductor loss data and the defined phase clamping, the losses of each device within a phase-leg are directly obtained in a circuit simulator. In Fig. 10 for each non-linear load the pure semiconductor efficiencies of the 12 kVAr active filters are presented for operation in the switching frequency range of 5 kHz to 48 kHz. In this analysis, each system operates with a 230Vrms/50Hz grid voltage and 800V DC-link.

As can be observed in Fig. 10, the A-NPC and the conventional NPC display very similar power losses. This happen, because in both systems during each commutation one diode and one active switch always experience essential switching and conduction losses.

Due to the fact that the 1200V devices in the T-type active filter are mostly commuted at half DC-link voltage instead of the 800V of the 2-level VSC, the switching losses are considerably reduced. Therefore, for low switching frequency values, the 3-level T-type active filter already shows superior performance than the conventional 2-level version.

Compared to the 3-level NPC and A-NPC topologies, the T-type system has lower conduction losses, but higher switching losses. In general, the efficiency of the T-type converter is outstanding for up to 20~25 kHz switching frequency. On the other hand, for higher switching frequencies, the 3-level NPC and A-NPC are superior.

The resulting averaged power loss distributions of the individual elements in a bridge leg for all 3-level active filters operating at switching frequency of 48 kHz are shown in Fig. 11. Fig. 12 presents the operating junction temperature (T_J) of the phase leg components of the 3-level active filters for nominal operation with a 3-phase 12-pulse diode rectifier with constant output current as load. An optimized heat sink with thermal resistance of *Rth*=0.1K/W has been designed and considered in the thermal analysis. The thermal models of the IGBTs are obtained directly from the datasheet, including the

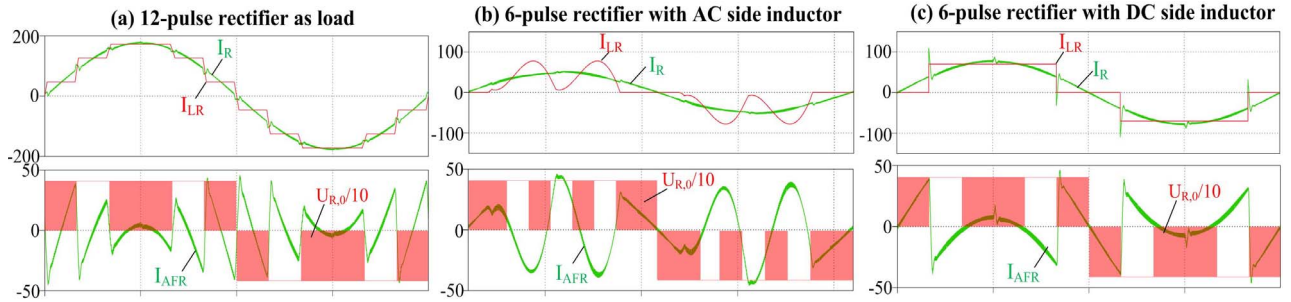


Fig. 9. Active filter non-linear loads and selected clamping pattern for high efficiency operation: (a) 12-pulse rectifier with constant output current; (b) 6-pulse rectifier with AC side inductor; and (c) 6-pulse rectifier with constant output current.

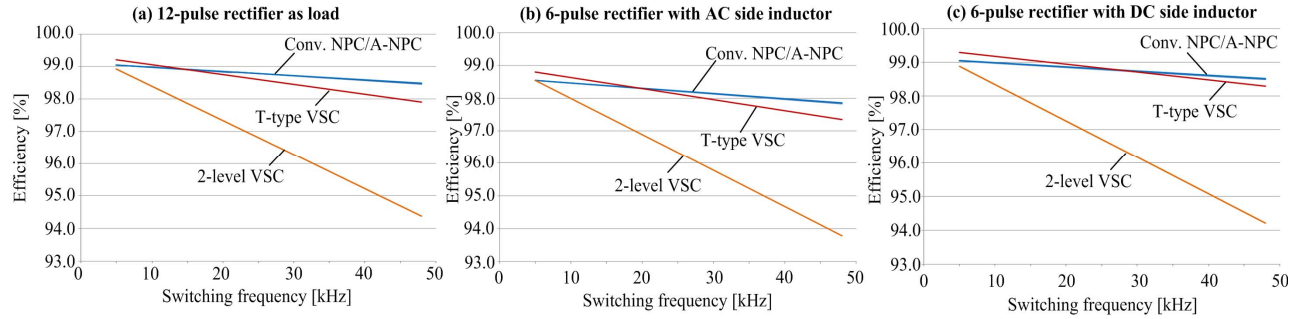


Fig. 10. Efficiency comparison between the different topologies of 12kVAr active filters employing commercial semiconductors: (a) 12-pulse rectifier with constant output current; (b) 6-pulse rectifier with AC side inductor; and (c) 6-pulse rectifier with constant output current.

thermally conductive insulating material Hi-flow from Bergquist (Rth≈0.4K/W).

It can be seen that during high switching frequency operation the loss distribution across the switches of the T-type active filter are very different. Additionally, this system exhibits the lowest efficiency among the 3-level systems. The 3-level A-NPC active filter achieves an outstanding loss distribution performance, enabling all semiconductor chips for IGBTs or diodes to operate with similar junction temperatures. As for the 3-level NPC active filter, the A-NPC system achieves excellent efficiency. Finally, with the selected clamping pattern the conventional NPC structure achieves very good loss distribution across the components of a phase-leg. In fact, for the 6-pulse rectifier load shown in Fig. 9(c), a much better loss distribution would be achieved if the clamping scheme was inverted, as the IGBTs T_1 and T_4 would suffer higher losses (cf. Fig 2(b)). Unfortunately, for this clamping condition, the NPC and T-type active filters would present much lower efficiency.

IV. Chip Area Based Comparison

As could be observed in Fig. 11, for a specific load and operating point, the 3-level topologies have very different power loss features. As the mismatch of this characteristic across the devices within the phase-leg is directly related to the reliability of the system, a pure efficiency comparison between them would not be absolutely reasonable.

For a fair comparison between the 2-level and 3-level active filters, the chip sizes of each system could be adapted for a given operating point such that the maximum or average IGBT and diode junction temperatures, $T_{J,T/D}$, are equal or less than a predefined maximum value, *e.g.* $T_{J,max}=125^oC$. This strategy not only guarantees optimal chip area partitioning and semiconductor material usage, but also provides a common basis for converter topology comparisons [10].

Due to their good documentation and data availability, the Infineon Trench and Field Stop 1200V IGBT4 and 600V IGBT3 series have been chosen as the data basis. With a statistical analysis of many commercial devices, datasheets and manufacturer data, the power losses and thermal characteristics of these semiconductor series can be modelled with a chip die size, $A_{S,T/D}$. A thorough description of the employed chip area optimization, including the resulting expressions for the IGBTs and diodes power loss and thermal characteristics modelled with a nominal chip area, are given in [4] and [10].

In this work, using the derived chip area mathematical expressions, the optimization algorithm calculates the losses of each topology and chip sizes until the average junction temperature of each semiconductor chip reaches $T_J=125^oC$, assuming a heat sink temperature of $T_{Sink}=80^oC$. By summing up all optimized chip sizes, the total chip area, the semiconductor costs and the total efficiency for a topology and corresponding operation point can be found. Therein, the chip area of each element is limited to a minimum of $A_{Smin}=2mm^2$. This is due to unconsidered side effects becoming dominant for small chip sizes and due to the limits in the bonding technology.

Fig. 13 shows the optimization results for all studied 12kVAr active filters operating with the loads depicted in Fig. 9. Therein, the total chip area is calculated depending on the switching frequency.

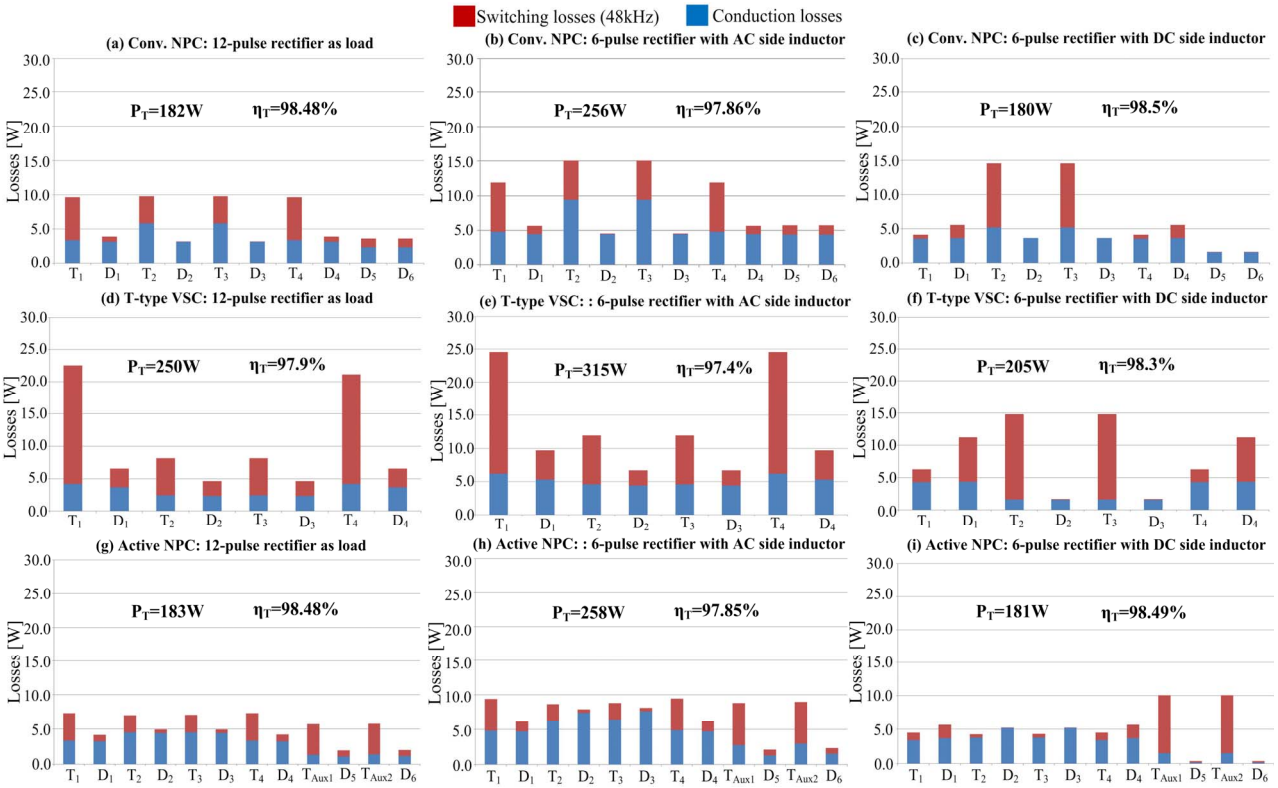


Fig. 11. Bridge leg components loss distribution for active filters operating at 48 kHz based on: (a)-(c) 3-level NPC, (d)-(f) 3-level T-type VSC; and (g)-(i) 3-level A-NPC active filter.

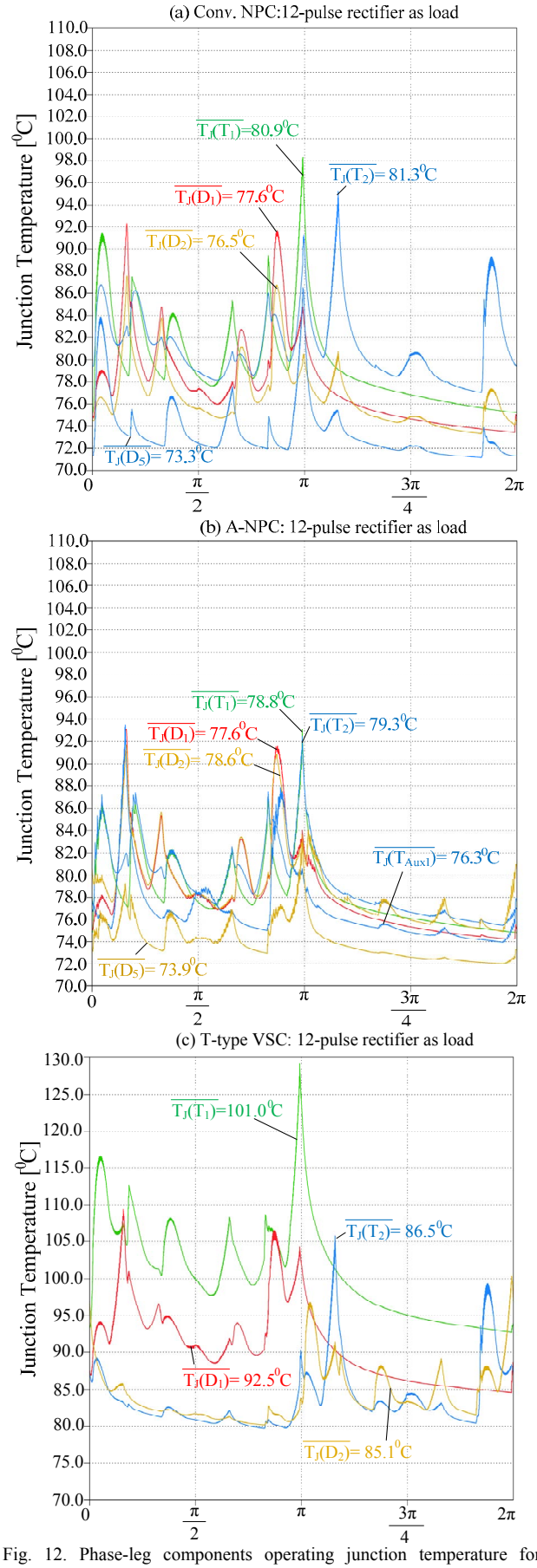


Fig. 12. Phase-leg components operating junction temperature for 12kVAr/48kHz active filters based on VSC:(a) NPC; (b) A-NPC; and (c) T-type.

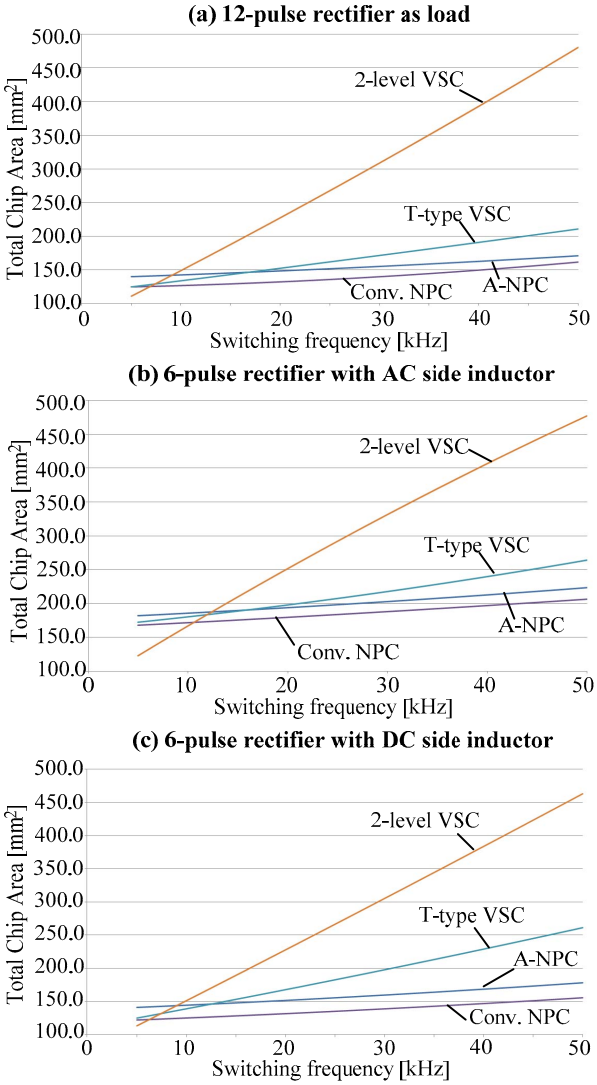


Fig. 13. Comparison of the total semiconductor area of 12kVAr active filters: (a) 12-pulse rectifier with constant output current; (b) 6-pulse rectifier with AC side inductor; and (c) 6-pulse rectifier with constant output current.

In general the total chip area of all 3-level topologies is already lower than for the 2-level VSC for switching frequencies above 12 kHz. At 50 kHz, depending on the active filter load, the necessary chip area of the 2-level version can be about 3 times larger than the area of the 3-level NPC and more than twice the area of the T-type converter. The 3-level NPC active filter requires less chip area than the T-type version for frequencies above 5 kHz.

The area increase with the switching frequency is the lowest for the 3-level NPC and A-NPC, because of the intrinsically small increase in switching losses. Due to the fact that the A-NPC operates to distribute the switching losses across the outer and the inner devices, the increment of chip area in relation to the switching frequency can be slightly smaller than for the NPC. Consequently, the A-NPC can exhibit better results than the NPC, if the considered switching frequency is high enough. Interestingly, the loss distribution features of the A-NPC permit that, for a large range of switching frequencies, the required chip areas of the individual devices are very similar. This characteristic definitely has

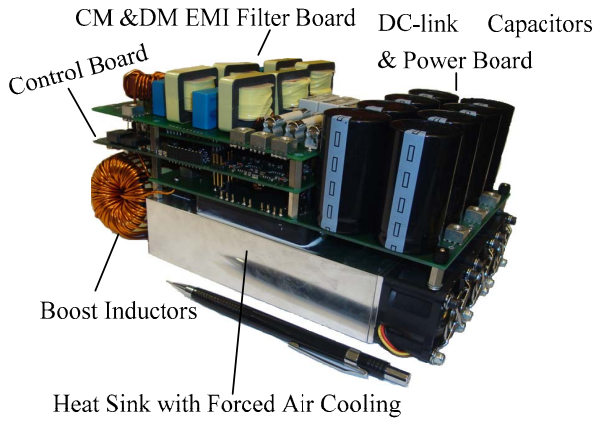
a positive impact on the costs of an optimized 3-level A-NPC module.

Finally, this study shows that for the evaluated active filter loads and low voltage level operation, the 3-level active filters would need less silicon area than a corresponding 2-level topology for low switching frequencies. The part count and the count for external circuitry such as isolated gate drivers is increased, but the total cost of the semiconductors can be expressively lower, especially for high switching frequencies.

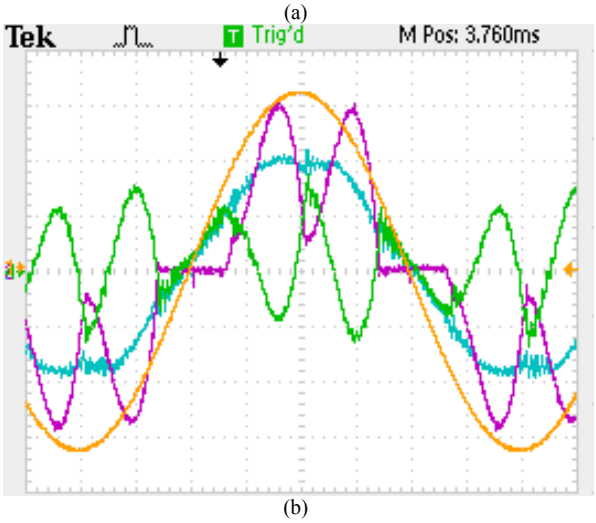
In the following, due to the outstanding performance, a 12kVAr/48kHz 3-level NPC based shunt active filter is designed and the experimental results obtained are presented to demonstrate the feasibility of this solution.

V. Experimental Evaluation

Fig. 14(a) shows a designed 12kVAr/48kHz 3-phase 3-level NPC active filter. It uses custom 3-level bridge-leg modules employing silicon carbide (SiC) Schottky diodes to enable highly efficient operation (diodes D_1, D_4, D_5 and D_6 in Fig. 1(c)). A digital signal processing board with a TI DSP and a Lattice FPGA is used to implement the control strategy shown in Fig. 6. Three inductors with inductance values of 300µH are employed. In total, eight 470µF/450V electrolytic capacitors are arranged to obtain an equivalent DC link capacitance of 940µF. The power density of this active filter is 3.65kW/dm^3.



(a)



(b)

Fig. 14. Experimental evaluation: (a) 3-level NPC active filter prototype; and (b) main waveforms for operation with 6-pulse rectifier with AC side inductor. Ch1: Mains voltage, Ch2: Line current, Ch3: Load current, and Ch4: Active filter current.

The performance of the designed active filter operating with a 3-phase 6-pulse diode rectifier is shown in Fig. 14(b). As can be noted, the system can efficiently compensate the current harmonics of the load as the line currents have close to sinusoidal shape. The results attest the feasibility of this solution.

VI. Conclusions

In this paper an efficiency comparison between 3-phase shunt active filters derived from the 2-level VSC, the 3-level NPC, A-NPC and the T-type converter was presented for operation in the switching frequency range of 5kHz to 50kHz and low DC-link voltage level. In order to address the loss distribution issue of the 3-level VSC topologies, while keeping the efficiency of the system high, a space vector modulation scheme, incorporating an optimal clamping of the phase, was proposed. Additionally, a semiconductor area based comparison is used to further evaluate the studied active filter systems. Surprisingly, at low DC-link voltage level the total silicon chip area of the 3-level topologies is already considerably smaller than for the 2-level topology for a switching frequency above 12 kHz. Finally, experimental results obtained with a 3-level NPC based shunt active filter employing custom SiC power modules are presented to demonstrate the feasibility of this solution.

References

[1] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparison and implementation of a 3-level npc voltage link back-to-back converter with sic and si diodes," in Proc. Twenty-Fifth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), pp. 1527-1533, 2010.

[2] T. Brückner, S. Bernet, and H. Güldner, "The active npc converter and its loss-balancing control," IEEE Trans. Ind. Electron., vol. 52, no. 5, pp. 855-868, June 2005.

[3] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low voltage drives, traction, and utility applications," IEEE Trans. Ind. Appl., vol. 41, pp. 855-865, May-June 2005.

[4] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, "Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies," in Proc. 36th Annual Conf. of IEEE Industrial Electronics (IECON), 2010.

[5] L. Asiminoaei, F. Blaabjerg and S. Hansen, "Evaluation of Harmonic Detection Methods for Active Power Filter Applications" Applied Power Elec. Conf. and Expo. (APEC), Vol. 1, pp.635-641, 2005.

[6] A. Stupar, D. Bortis, U. Drofenik, and J. W. Kolar, "Advanced setup for thermal cycling of power modules following definable junction temperature profiles," IPEC, Sapporo, Japan, 2010.

[7] C. Bailey, T. Tilford, and H. Lu, "Reliability analysis for power electronics modules," Electronics Technology, 30th International Spring Seminar on, vol., no., pp.12-17, 9-13 May 2007.

[8] L. Ma, T. Kerekes, R. Teodorescu, X. Jin, D. Floricau, and M. Liserre, "The high efficiency transformer-less pv inverter topologies derived from npc topology," in Proc. 13th European Conf. Power Electronics and Applications EPE, pp. 1–10, 2009.

[9] B. Kaku, I. Miyashita, and S. Sone, "Switching loss minimized space vector pwm method for igbt three-level inverter," IEE Proceedings. Electric Power Applications, Vol. 144, pp. 182-190, May 1997.

[10] T. Friedli and J. W. Kolar, "A Semiconductor area based assessment of ac motor drive converter topologies", in Proc. Twenty-Forth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), pp. 336 - 342, Feb. 2009.