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Abstract—**In this paper a generalized description and an overview of degrees of freedom and selected measures for efficiency improvement of power electronics converters is given. The background of all considerations is formed by single-phase PFC rectifier systems, but the concepts shown are fundamental and fully applicable for other converter systems. First, the influence of the main components of the losses of a converter on the efficiency characteristic over the output power is discussed. Subsequently, a detailed analysis of the possibilities, of minimizing the semiconductor losses, the losses of the passive components including the EMI filter, and the power requirements of auxiliary systems in the course of the design process are given. In this context also the technological boundaries that limit the maximum efficiency of a converter are clarified and the compromise that always has to be made between efficiency and power density is highlighted. Furthermore, a control procedure is discussed to maximize the efficiency in the partial load range and a resonant transition mode ZVS converter system is presented that allows to attain efficiencies significantly over 99% without the use of SiC semiconductors. In addition the accuracy of the input and output power measurements required for measuring highest efficiencies is clarified, whereby the advantage of a direct loss measurement by means of a calorimeter becomes immediately clear. Finally, results of measurements on a demonstrator of a CCM single-phase PFC rectifier system with 99.1% max. efficiency and $\eta > 99\%$ above half rated power, and on a resonant transition mode PFC rectifier system with $\eta_{max} = 99.3\%$ and $\eta > 99\%$ above 15% rated power are presented.**

Index Terms—**Efficiency Optimization, Light-Load Efficiency, Efficiency Measurement Accuracy, Calorimeter, Technological Limits, Figure-of-Merit, Single-Phase PFC Rectifiers**

I. INTRODUCTION

Driven by the continuous increase of the integration density of microelectronic circuits, the further development of power supplies in computer centres and data processing and telecom installations over the last few decades has been characterized by a constant demand for increase in power density (and decrease in relative costs) [1]. The decrease in volume while maintaining thermal limits could be attained only by simultaneous reduction in the maximum losses, i.e. by increase of the efficiency at full load, i.e. at rated power. However, because of the relatively low efficiency of the overall power supply chain in IT-systems and the widespread increase in environmental consciousness, as well as rising energy costs, raising the efficiency has become a primary development goal (cf. Fig. 1). This is exemplified by the 80Plus Programm originating from EPRI, the Climate Saver Computing Initiative of power supply manufacturers and the Energy Star Programm of the US Environmental Protection Agency [1]. Here, for certification, strict requirements are placed on the efficiency not only at full load but also primarily at partial load, i.e. at 10%, 20% and 50% of rated power (redundant parallel operation of two systems); moreover, in some cases, associated minimum values are required for the power factor. The special challenge in the development of new systems thus consists today in maintaining and / or improving a previously attained power density and simultaneously assuring a very high efficiency no longer only at rated power but over the entire range of output power.

In the literature numerous concepts are described for increasing the (light-load) efficiency of converter systems, whereby apart from
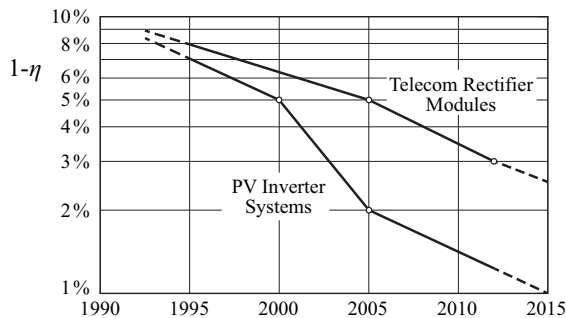

Fig. 1. Development of the (rated power) efficiency of telecom power supply modules and PV inverters since 1995 [2]–[4].

inverters for variable speed drives, often single-phase PFC rectifiers and DC/DC converters are or primary interest, i.e. the main elements of power supplies for IT-systems. The proposed concepts there are generally related to special circuits and are shown for a limited power range.

In the present work, in contrast, a generalized description and an overview of degrees of freedom and selected measures for efficiency improvement for converters will be given. Furthermore, the technological boundaries are shown that limit the maximum efficiency of a converter and the compromise is discussed that always has to be made between efficiency and power density in the course of a design. The background of these considerations is formed by single-phase PFC rectifier systems, but the concepts shown are fundamental and also applicable for other converter systems.

As an introduction, in section II, the influence of the main components of the losses of a converter on the efficiency characteristic are discussed. In section III follows a detailed analysis of the possibilities, within the scope of the design, of minimizing the semiconductor losses, the losses of the passive components and the power requirement of auxiliary systems. Furthermore, a control procedure is discussed to maximize the efficiency in the partial load range and finally a resonant transition mode ZVS converter system is presented that enables to attain efficiencies significantly over 99% without the use of SiC semiconductors. Section IV is concerned with the accuracy of the input and output power measurements required for measuring highest efficiencies, whereby the advantage of a direct loss measurement by means of a calorimeter becomes immediately clear. In section V, results of measurements on demonstrators of PFC rectifier systems, i.e. of a system working in CCM with 99.1% max. efficiency and $\eta > 99\%$ above half rated power, and of a resonant transition mode converter system with $\eta_{max} = 99.3\%$ and $\eta > 99\%$ above 15% rated power are presented. In conclusion, the conceptional fundamentals following from the considerations for the

future development of high-efficiency power supplies are summarized in section VI.

For the remainder of the paper it should be noted that the requirement for increasing the efficiency is of equal significance to that for reducing the losses. In the general use of language and for the sake of simpler understanding of the usability of a power flow on the input side, however, in communication preference is often given to the efficiency. However, with high-efficiency systems it is more sensible from a technical standpoint to speak of the quantitatively much more comprehensible relative losses. In the following, both terms are used in parallel.

II. CONVERTER LOSS COMPONENTS AND EFFICIENCY CHARACTERISTICS

As mentioned in section I, for modern power supplies, a very high efficiency is required even for low output power, i.e. the flattest possible efficiency characteristic $\eta = \eta(P_2)$ is aimed for. The dependence of the efficiency on P_2 is defined according to

$$\eta = \frac{P_2}{P_1} = \frac{1}{1 + \frac{P_V}{P_2}} \approx 1 - \frac{P_V}{P_2}, \quad (1)$$

with

$$P_1 = P_2 + P_V \quad (2)$$

as input power, by the relative losses, i.e. the relative losses referred to the output power define (for η near 1 or $P_V \ll P_2$) the deviation of the efficiency characteristic from the ideal value $\eta = 1.0$. As exemplified by the approximate analysis of the losses P_V of a DC/DC boost converter (cf. Fig. 2) operating in continuous conduction mode (CCM),

$$P_V = (P_{aux} + \tfrac{1}{2}C_{E,eq}U_2^2 f_P) + (U_F + k_P f_P)I_2 + \\ (1 - D)^{-2}(R_L + DR_{DS(on)} + D(1 - D)R_{ESR})I_2^2, \quad (3)$$

typically three loss components with characteristic dependence on the output power P_2 are occurring for a power electronic system,

$$P_V = P_{V,0} + P_{V,I} + P_{V,II} = k_0 + k_I P_2 + k_{II} P_2^2. \quad (4)$$

The loss fraction $P_{V,0}$, independent of the output power, is e.g. caused by the power consumption P_{aux} of auxiliary systems (measuring and control electronics, drive circuits for the power transistors, blowers for forced cooling, etc.). Furthermore, there are contributions from the capacitive switching losses of the power semiconductors ($C_{E,eq}$ designates the energy equivalent output capacitance of the transistor T associated with U_2), as well as the core losses of the input inductor (neglected in (3)), which are in a first approximation not dependent on P_2 but only on duty cycle D, the output voltage U_2 and the switching frequency f_P. In addition, the core losses of the transformer would have to be taken into account for galvanically isolated systems.

The loss fraction $P_{V,I}$, linearly dependent on P_2, is caused by power semiconductors with largely current independent forward voltage drop (diodes and IGBTs or generally speaking bipolar semiconductor elements), or also by often approximately linearly current dependent switching losses.

Finally, the loss fraction $P_{V,II}$ characterizes quadratically current dependent, i.e. ohmic loss components. Here, typical examples are the conduction losses of power MOSFETs, or the winding losses of inductive components, as well as the losses in (electrolytic) capacitors as a result of the equivalent series resistance R_{ESR}.

In order to obtain a clear picture of the influence of the individual power loss contributions on the efficiency characteristic and thus at
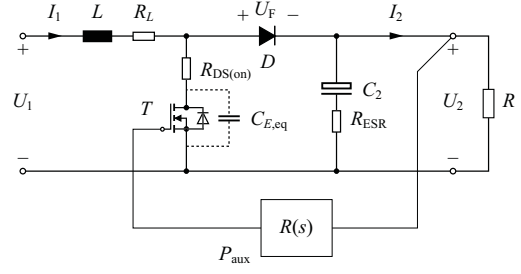

Fig. 2. Non-idealities of a DC/DC boost converter resulting in power conversion losses.

the end to be able to consider measures for a suitable shaping of the efficiency curve, in the following only one loss component at a time will be considered and the associated efficiency curve calculated (cf. Fig. 3).

If only constant losses $P_{V,0} = k_0$ are present,

$$\eta_0 = \frac{1}{1 + \frac{P_{V,0}}{P_2}} = \frac{1}{1 + \frac{k_0}{P_2}} \approx 1 - \frac{k_0}{P_2}, \quad (5)$$

the influence of the losses on the efficiency falls with increasing output power. The efficiency η_0 thus reaches values near to 1 for high output power. For low output power, however, an overproportional influence of $P_{V,0}$ exists and the efficiency curve is inevitably dragged to zero for $P_2 = 0$. Hence a higher partial load efficiency can in any case only be attained by minimizing the constant losses.

Output power proportional losses correspond to constant relative losses and thus lead to a constant lowering of the efficiency characteristic over P_2,

$$\eta_I = \frac{1}{1 + \frac{P_{V,I}}{P_2}} = \frac{1}{1 + k_I} \approx 1 - k_I = \text{const.} \quad (6)$$

Quadratically current dependent losses are reduced quadratically on lowering the output power; correspondingly the relative losses fall linearly and for $P_2 = 0$, $\eta = 1$ is reached. However, at high power an increasing influence exists on the efficiency curve or a proportionally increasing reduction of the efficiency occurs,

$$\eta_{II} = \frac{1}{1 + \frac{P_{V,II}}{P_2}} = \frac{1}{1 + k_{II} P_2} \approx 1 - k_{II} P_2. \quad (7)$$

Hence for a high efficiency at the rated operating point, one should in all cases aim for a minimization of the ohmic parts of the conduction losses and the ohmic resistances of passive components.

As is immediately clear from the above considerations, a maximum in the efficiency characteristic,

$$\eta = \frac{1}{1 + \frac{k_0}{P_2} + k_I + k_{II} P_2} \approx 1 - \left(\frac{k_0}{P_2} + k_I + k_{II} P_2\right), \quad (8)$$

occurs in the presence of a constant and an ohmic loss fraction $P_{V,0}$ and $P_{V,II}$ (cf. Fig. 4), which via

$$\frac{P_V}{P_2} = \frac{k_0}{P_2} + k_I + k_{II} P_2 \to \min \quad (9)$$

can be simply calculated to

$$P_{V,II,\eta_{max}} = P_{V,0}. \quad (10)$$

Maximum efficiency thus occurs when the constant and quadratic losses are equal. (This fact is e.g. frequently also considered in the dimensioning of transformers, where for maximum efficiency at a
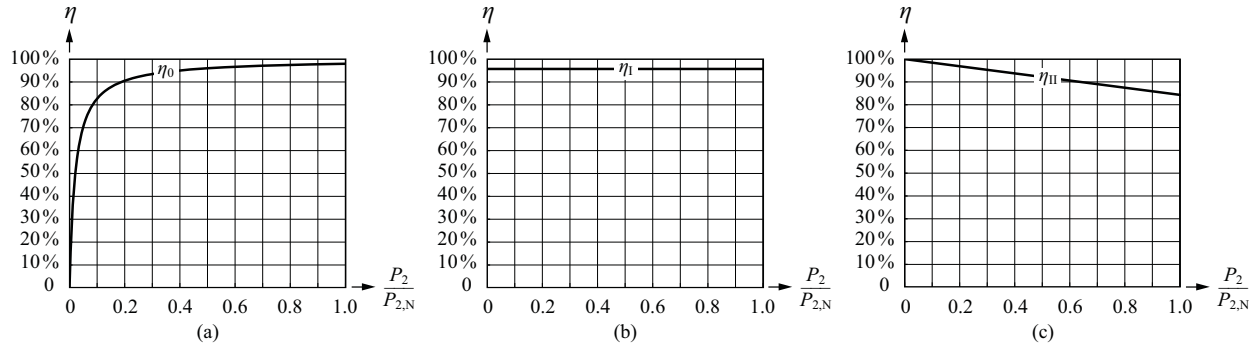
Fig. 3. Effect of the loss components of a power electronics converter on the efficiency characteristic; (a) only constant losses $P_{V,0}$; (b) only linear on the output power P_2 dependent losses $P_{V,I}$; (c) only quadratic on P_2 dependent (ohmic) losses $P_{V,II}$.
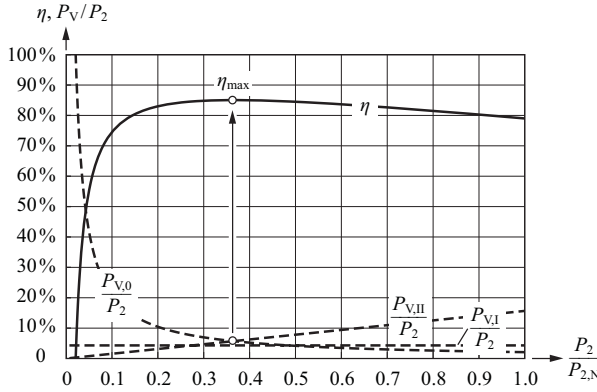

Fig. 4. Efficiency curve $\eta = \eta(P_2)$ of a power electronics converter and efficiency maximum η_{max}.

given operating point equal iron and copper losses are selected). The maximum value of the efficiency is

$$\eta_{max} = 1 - k_I - 2\sqrt{k_0 k_{II}}, \tag{11}$$

and occurs at

$$P_{2,\eta_{max}} = \sqrt{\frac{k_0}{k_{II}}}, \tag{12}$$

and is also dependent on the constant relative loss component k_I. The value P_2 at which the maximum occurs is not influenced by k_I, but the efficiency characteristic is lowered to a constant value by k_I, so that k_I also has an effect on η_{max}.

A. Mission Efficiency

When the efficiency is defined by (1), the losses of a converter are considered for single operating points. If a converter system is operated with a load profile $p_2(t)$, i.e. with a temporally varying operating point, the mean efficiency η_m over an entire cycle T_m of the Mission Profile,

$$\eta_m = \frac{E_2}{E_1} = \frac{1}{1 + \frac{E_V}{E_2}} = \frac{1}{1 + \frac{\int_{T_m} \left(\frac{1}{\eta\{p_2(t)\}} - 1\right) p_2(t)\, dt}{\int_{T_m} p_2(t)\, dt}}, \tag{13}$$

(E_1 designates the total energy supplied within T_m, E_2 that delivered to the load) is additionally of interest. With (13) as a quality criterion,

an optimum adaptation of the efficiency characteristic $\eta = \eta(p_2(t))$ to a load profile $p_2(t)$ can be performed. If e.g. in the simplest case two converters are connected in parallel (redundancy) and / or the rated power of a system is split into equal parts, the design should certainly provide for an efficiency maximum at half and not at full rated power and thus perhaps enable a reduction in the realization effort.

B. Efficiency vs. Power Factor

In connection with PFC rectifier systems one often discusses the compromise between a purely sinusoidal input current (and / or high power factor) and efficiency, as a lower quality input current could possibly be achieved with higher efficiency. For example, three-phase rectifiers with block-shaped input current typically exhibit a higher utilization of the power semiconductors and a higher efficiency than rectifiers with sinusoidal current consumption. For a quantitative assessment, the rectifier system shown in Fig. 5 will be considered, which is operated on a mains with internal resistance R_i. At a power consumption P_1 we have for the component η_i (caused by R_i) of the overall efficiency, the relation

$$\eta = \eta_i \cdot \eta_c, \tag{14}$$

$$\eta_i \approx 1 - \frac{P_{V,R_i}}{P_1} = 1 - \frac{I_1^2 R_i}{U_1 I_{1,(1)} \cos\phi}. \tag{15}$$

With the resistance referred to rated voltage $U_{1,N}$ and rated current $I_{1,(1),N}$

$$r_i = R_i \frac{I_{1,(1),N}}{U_{1,N}} \tag{16}$$

and considering the definition of the power factor,

$$\lambda = \frac{P_1}{S_1} = \frac{I_{1,(1)}}{I_1} \cos\phi = \frac{1}{\sqrt{1 + THD_i^2}} \cos\phi, \tag{17}$$

there then follows

$$\eta_i = 1 - r_i \frac{\cos\phi}{\lambda^2} \frac{\frac{I_{1,(1)}}{I_{1,(1),N}}}{\frac{U_1}{U_{1,N}}}. \tag{18}$$

If the system is operated at rated current and rated voltage,

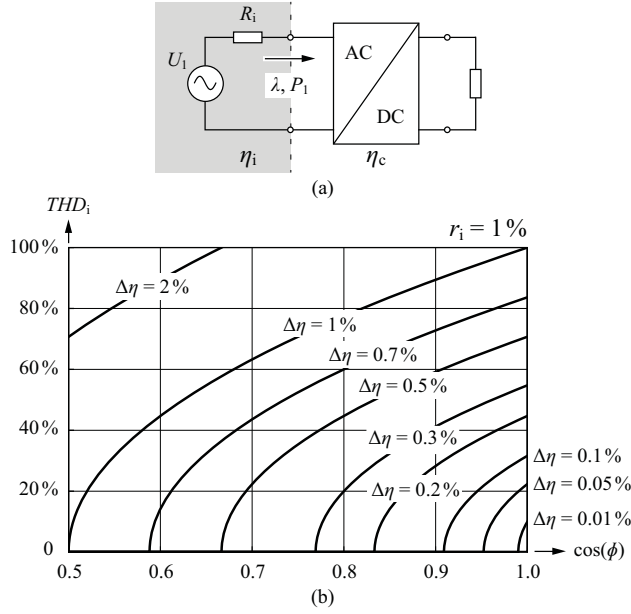$$\eta_i = 1 - r_i \frac{\cos\phi}{\lambda^2} \tag{19}$$

applies.

Fig. 5. (a) Operation of a power electronics converter with input power factor λ (or displacement factor $\cos\phi$ and THD_i of the input current) on a mains with internal resistance R_i; (b) resulting efficiency difference vs. operation with $\lambda = 1$ for $r_i = 1\%$ (cf. (20)).

Compared to a load with purely sinusoidal current consumption in phase with the mains voltage, i.e. $\lambda = 1$ ($\cos\phi = 1$, $THD_i = 0$), an efficiency reduction of

$$\Delta\eta = (1 - r_i) - \left(1 - r_i \frac{\cos\phi}{\lambda^2}\right) = r_i\left(\frac{1 + THD_i^2}{\cos\phi} - 1\right) \quad (20)$$

thus occurs (cf. Fig. 5 for $r_i = 1\%$). Hence, according to Fig. 5, a poorer current quality could be preferable for achieving a higher efficiency (in case the voltage distortions resulting from the current harmonics could be tolerated and high frequency effects neglected); e.g., there results for $r_i = 1\%$, $\cos\phi = 0.95$ and $THD_i = 30\%$ only a loss increase by 0.15% owing to the internal resistance of the mains. This value could perhaps be overcompensated for by a higher efficiency of a simpler converter circuit (fewer measuring and drive circuits, higher utilization of the installed silicon area, etc.).

III. GENERAL MEASURES FOR EFFICIENCY IMPROVEMENT

In this section, measures for minimizing the losses of a boost converter operating in continuous conduction mode (CCM) in the course of the design process will be discussed and technological limits will be identified. These losses are essentially arising from the following three groups: semiconductors, passive components (inductors/EMI filter and capacitors), and auxiliary systems. Furthermore, a control concept will be explained which allows the converter to be operated at its maximum efficiency point also in case of partial load. Subsequently, the advantages of a phase-shifted parallel operation of several systems will be shown. Moreover, a modification of the topology and the modulation method is described which allows to achieve a zero voltage switching (ZVS) operation of the semiconductors in the entire load and/or operating range. As shown by examples, this resonant transition mode can advantageously also be employed for buck-type and buck+boost type topologies. Finally, the efficiency increase by partial power conversion will be shown

as well as possibilities to maximize the efficiency of a converter operating in a wide input voltage range.

A. Design Measures

1) Switching and Conduction Losses of Power Semiconductors:
As shown in section II, power transistors with ohmic forward characteristic, such as MOSFETs, should be employed to achieve high efficiencies for partial load. For hard switching converters, however, the potential in loss reduction by increasing the chip area A_{Si} is limited. While the on resistance, $R_{DS(on)}$, is lowered by increasing chip area, the parasitic capacitances, which are determining the switching losses, are proportionally increased as will be shown in the following. Thus, an optimal chip area leading to minimal overall transistor losses can be derived for a certain switching frequency f_P.

The parasitic differential capacitances

$$\begin{aligned}
C_{GS} &= C_{iss} - C_{rss} \\
C_{GD} &= C_{rss} \\
C_{DS} &= C_{oss} - C_{rss}
\end{aligned} \quad (21)$$

(cf. Fig. 6) of a power MOSFET show a strong voltage dependency except for the gate-source capacitance C_{GS}. E.g., for C_{oss}

$$C_{oss}(U_{DS}) = C_{oss,ref}\sqrt{\frac{U_{DS,ref}}{U_{DS}}} \quad (22)$$

holds approximately (except for low voltages). The energy stored in C_{oss} is then given by

$$E_{C_{oss}}(U_{DS}) = \int_0^{t(U_{DS})} u_{DS}\, i\, \mathrm{d}t = \int_0^{U_{DS}} u_{DS} C_{oss}(u_{DS})\, \mathrm{d}u_{DS}$$
$$= \tfrac{2}{3} C_{oss,ref}\sqrt{U_{DS,ref}} U_{DS}^{3/2}. \quad (23)$$

Based on (23), with

$$E_{C_{oss}}(U_{DS}) = \tfrac{1}{2} C_{E,eq}(U_{DS}) U_{DS}^2 \quad (24)$$

an energy-equivalent, linear capacitance $C_{E,eq}$

$$C_{E,eq}(U_{DS}) = \tfrac{4}{3} C_{oss}(U_{DS}) \quad (25)$$

can be defined, which allows the calculation of the stored energy in the usual way. The stored electric charge in C_{oss} can be calculated by

$$Q_{C_{oss}}(U_{DS}) = \int_0^{U_{DS}} C_{oss}(u_{DS})\, \mathrm{d}u_{DS} = 2 C_{oss,ref}\sqrt{U_{DS,ref} U_{DS}}, \quad (26)$$

which leads to a charge-equivalent linear capacitance in dependency on the voltage U_{DS}

$$Q_{C_{oss}}(U_{DS}) = C_{Q,eq}(U_{DS}) U_{DS}. \quad (27)$$

This results in

$$C_{Q,eq} = 2 C_{oss}(U_{DS}), \quad (28)$$

i.e., approximately twice the value of the energy-equivalent capacitance $C_{E,eq}$ (cf. (25)). It has to be noted that for superjunction power transistors the voltage dependency according to (22) is not valid, since for small voltages high capacitance values occur. The charge-equivalent capacitance at typical operating voltages is therefore clearly beyond the approximation in (28) (cf. Fig. 6).

Based on these considerations the chip area $A_{Si,opt}$ resulting in minimum total transistor can be calculated. For the sake of simplicity it shall be assumed that only the capacitance of the transistor is causing switching losses, while the capacitance of the inductor, which impresses the current, is neglected as well as the capacitance (and reverse recovery current) of the free-wheeling diode, the capacitances
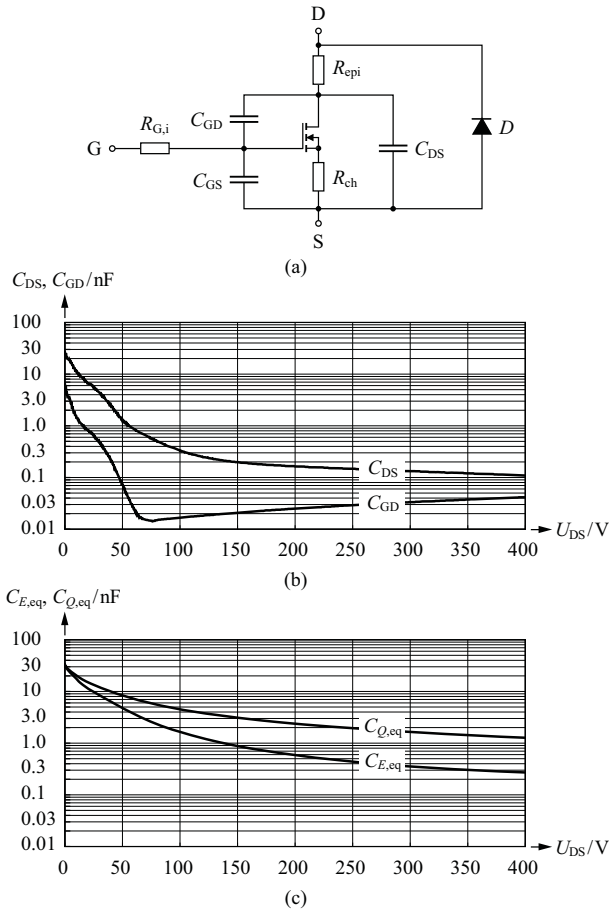
Fig. 6. (a) Parasitic capacitances and resistances of a power MOSFET; (b) voltage dependency of the capacitances C_{DS} and C_{GD} of a superjunction power MOSFET (Infineon IPW60R041C6) and the attributed energy-equivalent and charge-equivalent capacities $C_{E,eq}$ and $C_{Q,eq}$, respectively (cf. (c)).

against the heat sink and other loss portions. Additionally, the dependency of the $R_{DS(on)}$ on temperature and current will not be considered. The total losses are then given by

$$P_{V,T} = I_{DS,rms}^2 R_{DS(on)} + \tfrac{1}{2} C_{E,eq}(U_2) U_2^2 f_P. \quad (29)$$

If the on-resistance and the equivalent capacitance are set in relation to the chip area,

$$R_{DS(on)} = \frac{R_{DS(on)}^*}{A_{Si}}, \quad (30)$$
$$C_{E,eq} = C_{E,eq}^* A_{Si},$$

(29) can be rewritten as

$$P_{V,T} = \gamma_C \frac{1}{A_{Si}} + \gamma_P A_{Si} f_P \quad (31)$$

(cf. Fig. 7) resulting in an optimal silicon area of

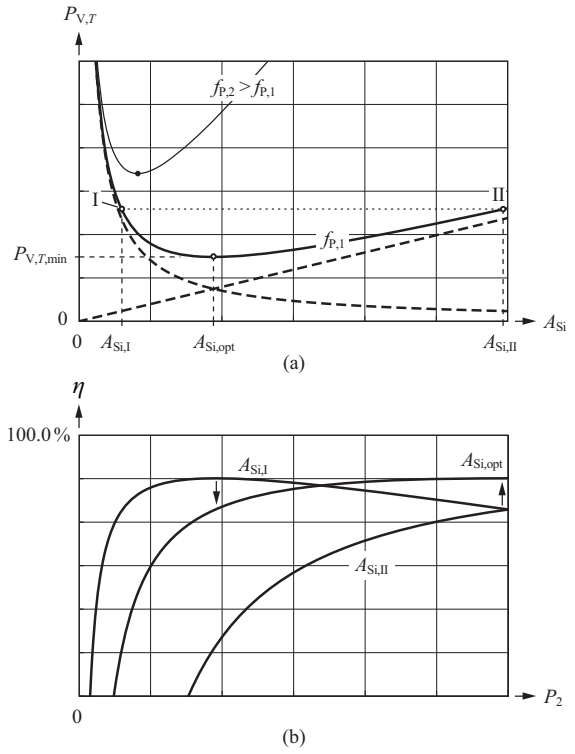$$A_{Si,opt} = \sqrt{\frac{1}{f_P} \frac{\gamma_C}{\gamma_P}} \quad (32)$$

Fig. 7. (a) Dependency of the conduction and switching losses of power MOSFETs on the chip area for a certain switching frequency $f_{P,1}$. For $f_{P,2} > f_{P,1}$ the chip area that yields to minimal total losses shows smaller values, resulting in higher losses $P_{V,T,min}$ [5]; (b) resulting dependency of the efficiency on the output power for optimal chip area $A_{Si,opt}$ as well as for $A_{Si,I} < A_{Si,opt}$ and $A_{Si,II} > A_{Si,opt}$ (only considering transistor losses). The selection of an excessive chip area leads to lower efficiency in the whole operating area, while for high efficiency at light loads advantageously $A_{Si,I}$ should be chosen.

for minimum losses [5], [6]. These are given by

$$P_{V,T,min} = 2\sqrt{\gamma_C \gamma_P} \sqrt{f_P} = \sqrt{2} I_{rms} U_2 \sqrt{f_P} \sqrt{R_{DS(on)}^* C_{E,eq}^*} \propto \frac{1}{FOM_\eta} \quad (33)$$

and are dependent on the switching frequency as shown in Fig. 7. For higher switching frequencies relatively higher switching losses occur leading to smaller optimal chip areas and larger minimal total losses. Higher efficiency can therefore be achieved by lower switching frequencies, what however also results in larger construction volume. It is important to note that (33) describes a technological limit for efficiency improvement, which can be characterized by a Figure-of-Merit [5]–[7],

$$FOM_\eta = \frac{1}{\sqrt{R_{DS(on)}^* C_{E,eq}^*}} = \sqrt{\frac{G_{DS(on)}^*}{C_{E,eq}^*}}. \quad (34)$$

For the above considerations only the parasitic capacitance of the power transistor has been taken into account. For the sake of completeness, now also the parasitic capacitance of the freewheeling diode shall be considered briefly. As shown in [8] (cf. p. 246), this describes already the general case, since all parasitic capacitances can be transformed into parallel capacitances C_I and C_{II} (plus a capacitance C_{III} in parallel to the dc link capacitor) by star-delta

transformation.

Looking at the turn-on behavior of a transistor the switching loss energy $E_{V,P}$ is directly resulting from the energy balance

$$E_{C_{I,1}} + E_{C_{II,1}} + E_d = E_{C_{I,2}} + E_{C_{II,2}} + E_{V,P}, \quad (35)$$

where $E_{C_{I,1}}$, $E_{C_{II,1}}$ and $E_{C_{I,2}}$, $E_{C_{II,2}}$ respectively, denote the energy values stored in C_I and C_{II} before (index 1) and after (index 2) the switching instant ($E_{C_{I,1}} = 0$, $E_{C_{I,2}} = 0$). E_d represents the energy taken from the DC output voltage.

With this, (35) can be rewritten as

$$\tfrac{1}{2}C_{I,E,eq}U_d^2 + C_{II,Q,eq}U_d^2 = \tfrac{1}{2}C_{II,E,eq}U_d^2 + E_{V,P} \quad (36)$$

resulting in switching losses

$$P_{V,P,T} = f_P E_{V,P} = \left(\tfrac{1}{2}C_{I,E,eq}U_d^2 + C_{II,Q,eq}U_d^2 - \tfrac{1}{2}C_{II,E,eq}U_d^2\right)f_P. \quad (37)$$

If $C_{I,E,eq} = C_{II,E,eq}$ is assumed (this simplification relates to employing a power transistor instead of a freewheeling diode and / or to synchronous rectification), the total losses are

$$P_{V,P} = C_{II,Q,eq}(U_d)U_d^2 f_P. \quad (38)$$

From this it becomes apparent that not the energy-equivalent, but the charge-equivalent capacitance (which is especially for superjunction transistors significantly larger) is determining the switching losses.

2) Gate Drive Losses: If a unipolar gate drive circuit is assumed for sake of simplicity, the gate drive losses are given by

$$P_{V,G} = U_{GG}Q_G(U_{GG})f_P = U_{GG}Q_G^*(U_{GG})A_{Si}f_P, \quad (39)$$

where Q_G denotes the gate charge, Q_G^* the gate charge per chip area, $Q_G^* = Q_G/A_{Si}$, and U_{GG} is the gate voltage occurring after turn-on. Q_G depends on the switching type (hard-switching or ZVS) and on the switched voltage. The losses $P_{V,G}$ are proportional to the chip area and the frequency like the capacitive switching losses of the transistor. If capacitive switching losses can be entirely eliminated, such as for ZVS, only $P_{V,G}$ remains and a new optimal chip area can be derived. However, in any case a low switching frequency is advantageous. A further reduction of $P_{V,G}$ can be achieved by a decrease of U_{GG}, whereby here the dependence of the on-resistance on U_{GG} has to be taken into account.

3) Losses in Foil and Electrolytic Capacitors: The losses of filter and DC output capacitors are generally given by

$$P_{V,C} = I_{C,rms}^2 R_{ESR}. \quad (40)$$

The equivalent series resistance, R_{ESR} is dependent on the frequency (plus temperature, etc.) and can be calculated with the dissipation factor $\tan\delta$ given in the datasheets according to

$$R_{ESR}(f) = \frac{\tan\delta(f)}{2\pi f C}. \quad (41)$$

For foil capacitors the dissipation factor typically shows a falling frequency characteristic at low frequencies (dielectric losses decreasing with $1/f$) and a characteristic increasing with $\sqrt{f}$ for high frequencies (skin effect). The situation is similar for electrolytic capacitors, where the R_{ESR} is typ. also decreasing with the frequency (in dependence on the operating temperature) in the frequency range of $10\,\text{Hz}$ to $10\,\text{kHz}$.

As for the design, a reduction of the capacitor losses is only possible through paralleling of multiple components (increase of total volume), i.e. by reduction of the effective R_{ESR}.
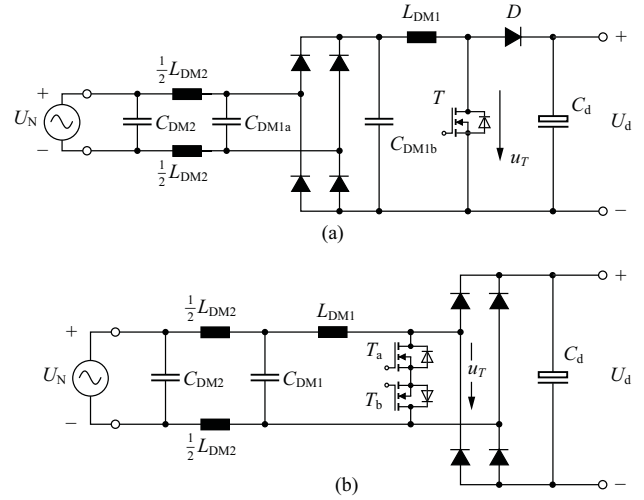

Fig. 8.   Single-phase PFC rectifier systems with input diode bridge (a) and AC-side switch (b); only the components required for the DM EMI filtering are shown (related to industrial practice where typically a two-stage DM filter is employed).

4) Losses in Inductive Components: The following considerations will be done for a boost-type single-phase PFC rectifier system for the sake of clarity, but are generally valid for topologies with an input diode bridge as well as for systems with an AC-side switch [9] (cf. Fig. 8). It has to be noted that the boost inductor can be viewed as part of the first stage of a DM (differential mode) EMI input filter, which should suppress the switching frequency harmonics of the PWM voltage generated by the power switch in order to fulfill the EMI standards (CISPR 11). Thus, in the following in a first step the required filter attenuation should be calculated. Subsequently, the appropriate switching frequency for minimum attenuation requirement and the optimal filter structure is discussed. With this, relatively small filter components can be chosen, or, if a certain construction space is given, a filter with higher efficiency can be realized. For the sake of brevity, only the differential mode filtering will be considered.

As shown in the following, the required filter attenuation can be derived easily with an approximation. The pulse-width-modulated voltage at the input of the rectifier system comprises a mains frequency component and switching frequency components. The latter (including sidebands) occur at multiples of the switching frequency and show linearly decreasing amplitudes with increasing harmonic order. Due to this decrease, higher harmonics contribute to a very low extent to the total harmonic power; e.g. the second harmonic $\hat{U}_{2n} = 0.5\hat{U}_n$ contributes only 1/4 of the power compared to the first harmonic $\hat{U}_n$ occurring at the switching frequency f_P. Thus, the whole harmonic power contained in u_T can be calculated analytically in the time domain easily and assigned only to the first harmonic of the switching frequency in a first approximation (this harmonic is denominated as equivalent switching frequency harmonic $\hat{U}_{f_P,eq}$ in the following). A spectral analysis of the voltage u_T is not necessary. For the design of the EMI input filter the amplitude of the first harmonic of the switching frequency, which falls into the measurement band given in the standards, is relevant. The amplitude of this n-th harmonic ($f = nf_P$ of the switching frequency can be derived easily from the equivalent switching frequency harmonic

$\hat{U}_{f_P,eq}$ by division by the frequency ratio $n = f/f_P$.

With the modulation index of the rectifier system

$$M = \frac{\hat{U}_N}{U_d} \qquad (42)$$

the rms value of the PWM voltage u_T is given by

$$U_{T,\text{rms}} = \sqrt{\frac{1}{\pi} \int_\pi u_T^2 \, d\varphi_N} \approx \sqrt{\frac{1}{\pi} \int_\pi U_d^2 (1-d) \, d\varphi_N} = \sqrt{\frac{2}{\pi} M} U_d, \qquad (43)$$

where d denominates the local duty cycle of the power transistor,

$$d = 1 - M \sin \varphi_N. \qquad (44)$$

With (42), the rms value of the fundamental harmonic of u_T is given by

$$U_{N,\text{rms}} = M \frac{U_d}{\sqrt{2}}; \qquad (45)$$

accordingly the rms value of the equivalent switching frequency harmonic

$$U_{f_P,eq,\text{rms}}^2 = U_{T,\text{rms}}^2 - U_{N,\text{rms}}^2 \qquad (46)$$

results in

$$U_{f_P,eq,\text{rms}} = \sqrt{M \left(\frac{2}{\pi} - \frac{M}{2} \right)} U_d. \qquad (47)$$

The dependence of $U_{f_P,eq,\text{rms}}$ on M is shown in Fig. 9. In Fig. 10 the calculation of the amplitude of the switching frequency harmonic relevant for the EMI filter design is illustrated along with the conducted emissions limit defined by CISPR 11 Class B. For simplifying the calculations,

$$U_{f_P,eq,\text{rms}} \approx 0.5 \cdot U_d \qquad (48)$$

can be considered as a worst case approximation. This rough approximation is valid since even a deviance by a factor of 2 would only mean a higher attenuation requirement Att_{req} of the EMI filter by $6 \, \text{dB}$. For typical required attenuation values in the range of $80 \ldots 90 \, \text{dB}$ this is tolerable.

Also for phase-shifted parallel operation of e.g. 2 systems the equivalent harmonic voltage $U_{2f_P,eq,\text{rms}}$ can be calculated easily analogous to (46) (cf. Fig. 9)

$$U_{2f_P,eq,\text{rms}} = \begin{cases} \sqrt{M \left(\frac{1}{\pi} - \frac{M}{2} \right)} U_d & \forall \quad 0 \le M \le 0.5 \\ \sqrt{M \left(\frac{1}{\pi} - \frac{M}{2} \right) + \frac{\sqrt{4M^2-1} - \arccos\left(\frac{1}{2M}\right)}{\pi}} U_d & \forall \quad 0.5 < M \le 1 \end{cases} \qquad (49)$$

however has to be assigned to twice the switching frequency. For a worst case approximation here

$$U_{2f_P,eq,\text{rms}} \approx 0.25 \cdot U_d \qquad (50)$$

can be used. This illustrates that for switching frequencies below $150 \, \text{kHz}$ (which is the lower limit of the frequency band defined by CISPR11) and for only 2 parallel systems no volume reduction of the EMI filter results, but only a reduction of the switching frequency ripple at the first filter capacitor.

For the selection of the switching frequency f_P the dependence of the filter attenuation on f_P has to be looked at. For the sake of clarity, the cut-off frequency of a 1-, 2- or 3-stage filter, which fulfills the attenuation requirements, will be calculated instead of the filter attenuation itself. A high cut-off frequency then goes along with low realization effort. These considerations are illustrated in Fig. 11.
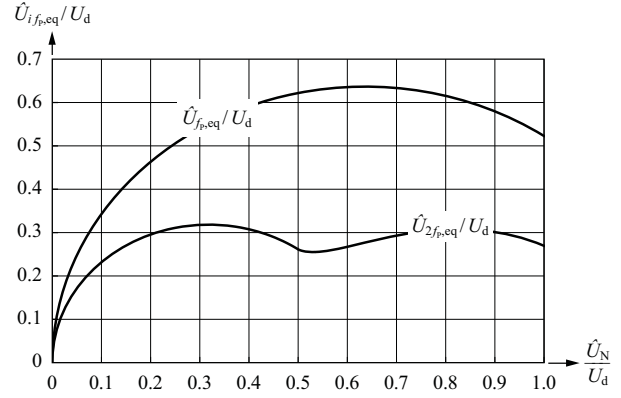

Fig. 9. Dependency of the amplitude $\hat{U}_{f_P,eq}/U_d$ of the equivalent switching frequency harmonic voltage of a single-phase boost-type PFC rectifier system on the modulation index M; in addition: amplitude $\hat{U}_{2f_P,eq}/U_d$ of the equivalent switching frequency harmonic voltage (with frequency $2f_P$) for the case of a 180° phase-shifted parallel operation of 2 systems (cf. section III-C).
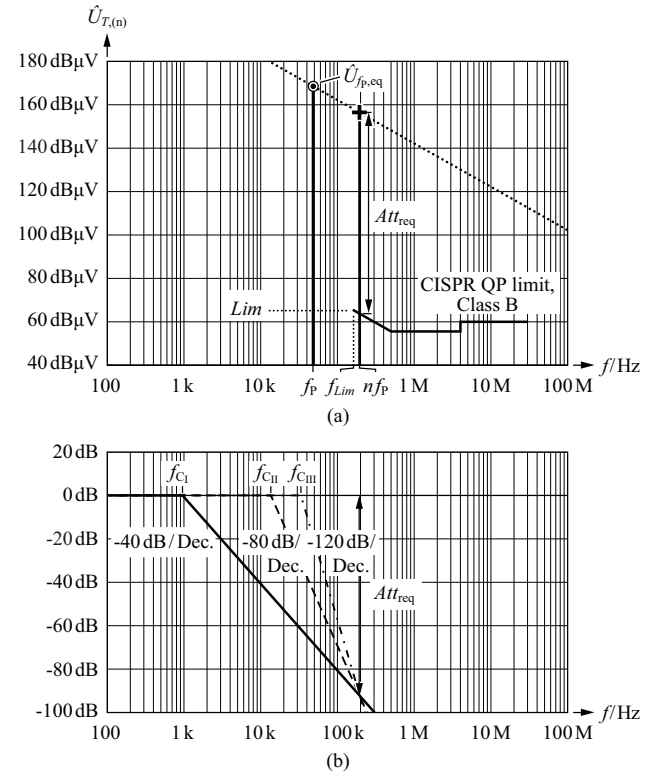

Fig. 11. (a) EMI limit according to CISPR 11 Class B QP and equivalent harmonic voltage $\hat{U}_{f_P,eq}$ (for $f_P = 48 \, \text{kHz}$) and approximation of the disturbance level for higher harmonics (decrease of the amplitude by $-20 \, \text{dB/decade}$). The required filter attenuation ($Att_{\text{req}} = 92 \, \text{dB}$) is determined by the first harmonic being located within the frequency band defined in the standard (for the case at hand $f = 4f_P = 192 \, \text{kHz}$); (b) attenuation characteristics of 1-, 2-, and 3-stage LC filter structures, which feature the required attenuation Att_{req}. For higher filter orders a higher cut-off frequency can be chosen and the total realization effort can be reduced, respectively. Parameters: mains voltage $U_{N,\text{rms}} = 230 \, \text{V}$, output voltage $U_d = 400 \, \text{V}$.
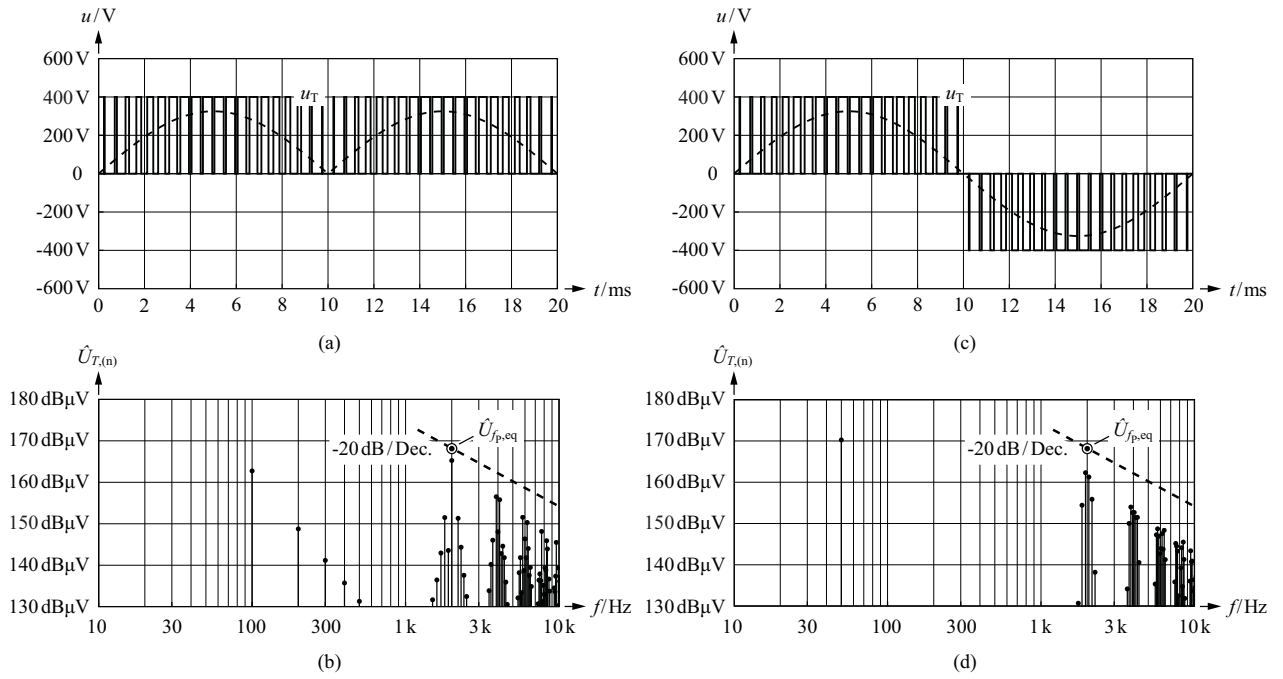
Fig. 10.   (a) and (b): Switching frequency voltage and related spectrum for the single-phase PFC rectifier topology with input diode bridge (cf. Fig. 8 (a)); (c) and (d): as (a) and (b) but for the AC-switch topology (cf. Fig. 8 (b)). The spectral characteristic can be approximated well by the equivalent harmonic voltage $\hat{U}_{f_P,eq}$ in both cases (also the sidebands have to be taken into account to evaluate the approximation).

If the harmonic at the n-th switching frequency is located within the frequency band defined in the standards, $f \geq f_{Lim}(150\,\text{kHz})$,

$$\frac{1}{n}\hat{U}_{f_P,eq}\frac{1}{\left(\frac{n f_P}{f_C}\right)^2} \leq \frac{Lim}{\left(\frac{n f_P}{f_{Lim}}\right)} \tag{51}$$

must hold true for the fulfillment of the standard. Hereby, a frequency proportional decrease of the EMI limit (CISPR 11, Class B, QP) is assumed (valid until $f = 500\,\text{kHz}$) and a single-stage filter is considered. The relation (51) is only valid for switching frequencies in the range of

$$f_P \in \left(\frac{1}{n}f_{Lim}, \frac{1}{n-1}f_{Lim}\right), \tag{52}$$

since for $f_P = f_{Lim}/(n-1)$ the harmonic at the $(n-1)$-th order of the switching frequency, which shows a higher amplitude, lies beyond f_{Lim} and therefore determines the required attenuation. Now, with (51) a required cut-off frequency can be assigned to a switching frequency according to

$$f_C = n\sqrt{\frac{Lim}{U_{f_P,eq}}}\sqrt{f_P f_{Lim}} \propto \sqrt{f_P}. \tag{53}$$

Due to the increase of the filter attenuation with $40\,\text{dB/decade}$ and the characteristics of the EMI limit, which decreases only with $20\,\text{dB/decade}$, a higher cut-off frequency can be chosen for higher switching frequencies within the frequency band defined by (52). However, if the neighbouring, lower harmonic falls into the CISPR 11 frequency band, a higher attenuation, i.e. a lower cut-off frequency has to be considered. Since this harmonic shows a higher amplitude, the attenuation requirement increases in total with f_P. However, for higher filter orders (typically a two-stage filter is employed) this increase is not very distinct anymore (cf. Fig. 12).
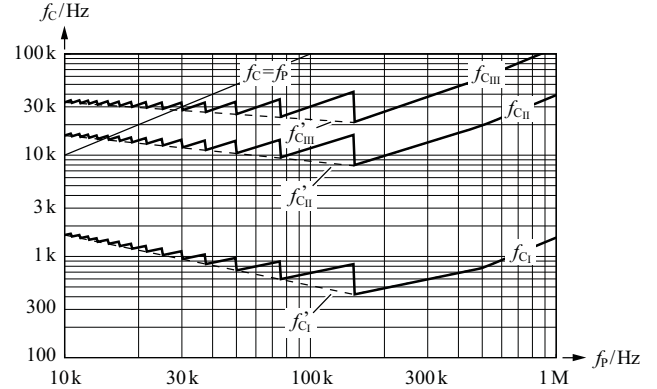

Fig. 12.   Required cut-off frequencies f_{C_I}, $f_{C_{II}}$ and $f_{C_{III}}$ of a 1-, 2- and 3-stage LC filter for the fulfillment of the EMI standards according to CISPR 11 Class B QP in dependence on the switching frequency [10]; in addition: approximation (55) depicted by dashed lines. Parameters: mains voltage $U_{N,rms} = 230\,\text{V}$, output voltage $U_d = 400\,\text{V}$.

A worst case approximation of (51) can be found such that the occurrence of harmonics at discrete frequencies $n f_P$ is neglected and only the attenuation required at f_{Lim} is calculated. This results in

$$\frac{\hat{U}_{f_P,eq}}{\frac{f_{Lim}}{f_P}}\frac{1}{\left(\frac{f_{Lim}}{f'_{C_I}}\right)^2} \leq Lim \tag{54}$$

($f_P < f_{Lim}$). The approximation for the cut-off frequency which is

continuously valid within $f_P \in (0, f_{Lim})$ is then

$$f'_{C_I} = \sqrt{\frac{Lim}{U_{f_{P,eq}}}} f_{Lim} \sqrt{\frac{f_{Lim}}{f_P}}. \tag{55}$$

With this, the increasing attenuation requirement (reduction of f'_{C_I}) with higher switching frequencies becomes immediately evident (cf. Fig. 12). In summary, also the analysis of the EMI filter leads to an advantage of lower switching frequencies (though this advantage is relatively small for a higher number of filter stages).

a) Frequency Modulation: For constant switching frequency the harmonics are concentrated around multiples of the switching frequency. In order to minimize the disturbance level at a certain frequency and/or the required attenuation of the EMI filter, it is sensible to distribute the harmonic power as equally as possible over the frequency range. This is possible with a modulation of the switching frequency, e.g. by a sinusoidal or triangular modulation with twice the mains frequency

$$f_{P\varphi} = f_{P,avg} + f_{P,\sim}, \tag{56}$$

where a triangular modulation leads to a broader distribution of the harmonics [11]. The modulation amplitude is set such that only a portion of the power (compared to concentrated harmonics) is detected by the bandpass of the EMI test receiver (bandwidth 9 kHz). With this, a reduction of the disturbance level of about $6 \dots 10$ dB results [11] (cf. Fig. 13) which consequently leads to a lower EMI filter volume.

b) Optimization of the EMI-Filter: If the required attenuation of the EMI filter is known, in a next step the filter structure and the filter component values have to be defined. Typically, a two-stage filter is selected, whereby the boost inductance has to be regarded as part of the first filter stage, as mentioned before. The task is now to determine the component values for a given available volume such that minimal total losses result. Alternatively, the filter could also be optimized regarding minimal volume or minimal costs for given certain thermal boundary conditions.

The efficiency optimization can only be done based on a detailed modeling of the low and high frequency components of the iron and copper losses of the magnetic components [12]. The filter capacitors show comparatively low losses, which can be considered easily through the $\tan\delta$ (cf. (41)) Thermal limits are typically of minor importance in the course of an efficiency optimization, as for an ultra-high efficiency systems sufficient space must be provided to ensure very low losses (resulting only in a small increase of the temperature).

The efficiency increase for larger volume can be verified easily through a simplified consideration regarding the scaling of the iron and copper losses with the linear dimensions [5]. For an intended inductance value L, a given switching frequency f_P and a given current ripple Δi_L the flux density ripple

$$\Delta B = \frac{L\Delta i_L}{N A_E} \propto \frac{U_d}{f_P A_E} \propto \frac{1}{A_E} \propto \frac{1}{l^2} \tag{57}$$

results. With this, and the Steinmetz law the iron losses are scaling with

$$P_{V,E} \propto f_P^\alpha \Delta B^\beta V_E \propto \approx \frac{1}{l^4} l^3 \propto \frac{1}{l} \tag{58}$$

($\beta \approx 2$). The scaling of the copper losses can be calculated according to

$$P_{V,W} = I_{rms}^2 R_W \propto \frac{l}{\kappa A_W} \propto \frac{l}{l^2} = \frac{1}{l}. \tag{59}$$

Hence, both iron and copper losses are decreasing with increasing linear dimension l.
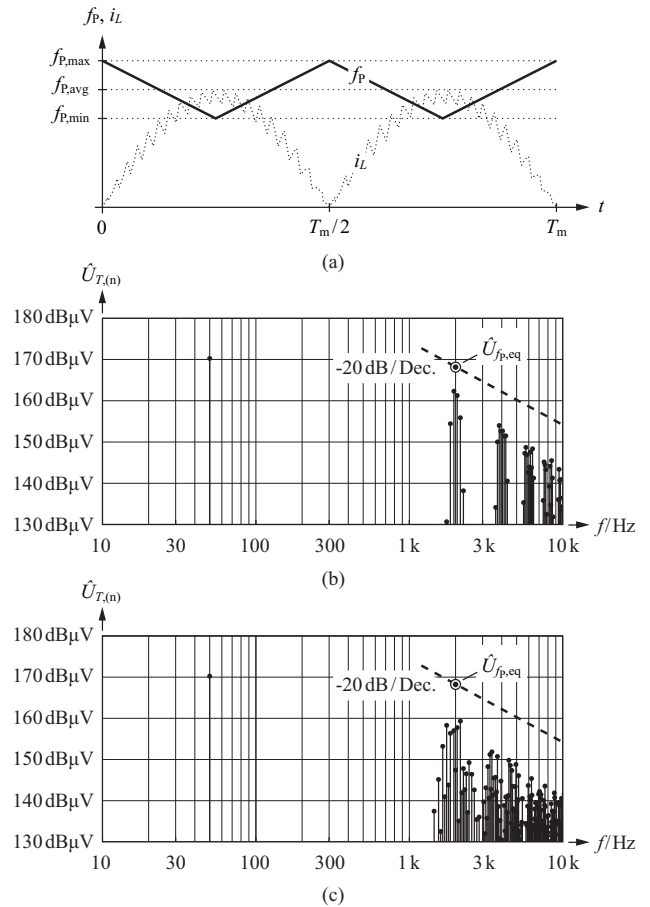

Fig. 13. (a) Modulation of the switching frequency and resulting broader spectral distribution of the harmonic power and/or reduction of the amplitudes of individual harmonics; (b) constant switching frequency $f_P = f_{P,avg}$; (c) modulated switching frequency according to (a). For the sake of clarity, the situation is shown for a very low switching frequency.

It is of special interest to include the selection of the switching frequency into the optimization. As additional parameter the ratio of the maximum amplitude of the current ripple to the fundamental current amplitude at nominal load, $k_i = \Delta\hat{i}_{max}/I_{N,(1),N}$, could be selected. The optimization leads then (for a given k_i) to a compromise between a decreasing inductance value L (and therefore lower filter attenuation) for increasing f_P and an increasing attenuation requirement (cf. (55)) and/or increasing losses or an increasing volume of the other filter components. For industrial systems k_i is typically selected in the range of $k_i = 0.1 \dots 0.2$ to limit the time delay errors of the current sampling.

However, in any case it makes sense to analyze an additional range of k_i, since it can be seen then directly if e.g. for a certain system an operation in discontinuous conduction mode (DCM) would be preferable. Generally, the optimization regarding the switching frequency must be performed for the overall system, i.e. also the semiconductor losses have to be considered for a certain current shape k_i or a given switching frequency. Here, the above considerations regarding the optimal selection of the chip area can be taken into account advantageously.

In the following, on the example of the single-phase PFC rectifier illustrated in Fig. 8 (a) (nominal power $P_N = 1.5\,\text{kW}$, mains frequency $f_N = 50\,\text{Hz}$, $U_d = 400\,\text{V}$, $U_{N,\text{rms}} = 230\,\text{V}$), it is shown how the switching frequency and the ripple ratio k_i affect the filter volume and losses. EMC filters are designed for different combinations of switching frequencies and ripple ratios f_P/k_i. Each filter design is performed to aim for low volume or low losses, while guaranteeing the attenuation to meet the CISPR 11 class A standard. A thermal model assuming natural convection is used, as the maximum temperature ($125\,^\circ\text{C}$) allowed is the limiting factor when reducing volume. The capacitance density to calculate the capacitors volume are approximated with $0.18\,\mu\text{F/cm}^3$ (the filter capacitors are selected from the EPCOS X2 MKP film capacitors series). The inductors are designed as toroids of iron powder from Micrometals. Litz wires of copper are taken for the conductors.

The results for volumetric optimized designs are given in Fig. 14 (a) and (b). When the frequency f_P is kept constant, and the ripple ratio k_i is varied, the filter volume share between the boost inductor L_{DM1} and the rest of the filter, i.e. the filter part consisting of L_{DM2}, $C_{DM1} = C_{DM1a} + C_{DM1b}$, and C_{DM2}, changes. For low values of k_i, the boost inductor L_{DM1} occupies the major part of the filter volume; for high values of k_i the $C_{DM2}/L_{DM2}/C_{DM1}$-part occupies the major part. There is, for each frequency, an optimal k_i at which the filter volume is reduced. The same can be concluded when k_i is kept constant and the frequency f_P is varied. There is, for each k_i, an optimal frequency f_P. An overall optimal f_P/k_i combination can be found; in Fig. 14 (c) this operating point is detailed. In Fig. 14 (b) the losses to the designs are given. It can be seen that more voluminous designs have generally higher losses. This is obvious, since all designs are at the thermal limit, higher losses are tolerable with a higher volume, as the surface for the heat dissipation increases with increasing volume. In the results to the optimization at hand, the comparable high capacitance value leads to a relative high reactive power consumption. This reactive power consumption can be reduced by selecting lower capacitances; the optimization procedure could limit the maximum capacitance values as another optimization constraint and, therewith, the reactive power consumption would be limited.

In the example of Fig. 14, the filter volume was minimized under thermal constraints. Another objective could be to select the filter components such that, for a given filter volume V_{max}, the losses in the filter are minimized. In Fig. 15 results of loss-optimized designs are given. The volume was limited to $0.4\,\text{dm}^3$. It can be seen that the optimal combination of f_P/k_i is close to the one of the volumetric optimal design. A hypothesis that explains this behavior is, that the volume difference between volumetric optimized designs and the limit V_{max} is maximal for the point of volumetric optimal design; thus, the losses can be reduced most at this point.

It is important to note that due to the limitation of k_i for CCM operation typically very different inductance values of the two EMI filter stages result. This partitioning of the total inductance is clearly not optimal regarding attenuation. For maximal filter attenuation the total inductance would have to be partitioned equally to the two filter stages. This becomes apparent through a simple calculation. If for both filter stages the same capacitance C is selected and the total inductance L is distributed such that the filter inductances kL and $(1-k)L$ are chosen for the first and the second stage the filter transfer function at high frequencies is given by

$$G_F \approx \frac{1}{\omega^4 k(1-k)L^2 C^2}. \tag{60}$$

(a)

(b)

Operating Point
f_P 48 kHz
k_i 0.075

Attenuation 85 dB

Filter Values
$L_{DM1} = 1.5$ mH
$L_{DM2} = 204$ µH
$C_{DM1} = C_{DM2} = 6.4$ µF

Volume Partitioning

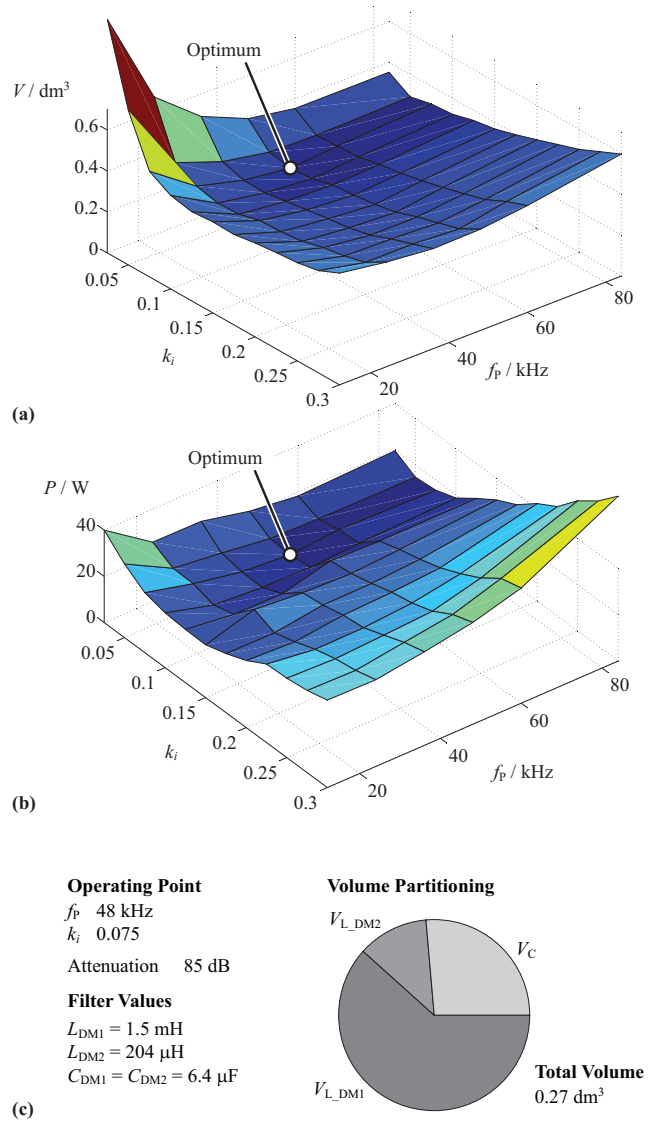**Total Volume**
0.27 dm³

(c)

Fig. 14. (a) Impact of switching frequency and ripple ratio k_i on filter volume (results to volumetric-optimized designs). (b) Power losses to the designs of (a). (c) Details to overall optimal design.
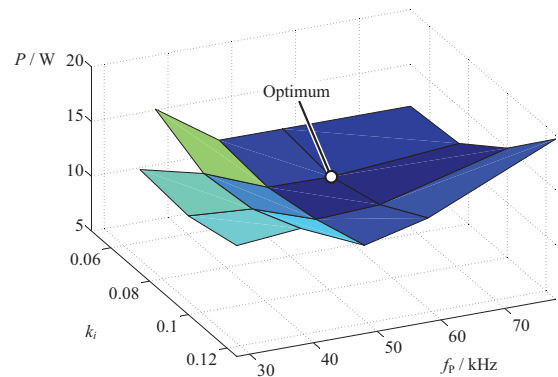

Fig. 15. Results to the loss-optimized / volumetric-limited optimization ($V_{max} = 0.4\,\text{dm}^3$). Optimum at $k_i = 0.075$ and $f_P = 58$ kHz.

This directly results in an attenuation maximum at

$$k_{\text{opt}} = 0.5, \qquad (61)$$

i.e. an equal distribution of L to both stages. A similar consideration can be done for the filter capacitors [13], [14].

c) Filter with Optimal Volume Utilization: Along with the selection of the filter elements it shall be now shown briefly, in which way the volumes of the filter inductors and capacitors would have have to be selected to achieve a maximal filter attenuation (and not minimal losses) [15].

In a first step a single-stage LC filter is considered, where the volumes of the filter components are proportional to their energies

$$V_C = \rho_C \tfrac{1}{2} C U^2 = k_C C, \\ V_L = \rho_L \tfrac{1}{2} L I^2 = k_L L \qquad (62)$$

(ρ_C and ρ_L denominate the energy densities). A given total volume V is partitioned into two parts with rV for the capacitor and $(1-r)V$ for the inductor volume,

$$V_C = rV, \\ V_L = (1-r)V. \qquad (63)$$

Maximal attenuation means minimal cut-off frequency

$$\omega_C = \frac{1}{\sqrt{LC}} \to \min, \qquad (64)$$

which can be rewritten with (62) and (63) as

$$LC = \frac{1-r}{k_L} \frac{r}{k_C} V^2 \to \max, \qquad (65)$$

resulting in an optimal volume partitioning of

$$r_{\text{opt}} = 0.5. \qquad (66)$$

Accordingly, the available volume should be advantageously partitioned equally to the inductor and the capacitor. However, due to the relatively higher inductor losses this volume partitioning is obviously not optimal in terms of losses. Furthermore, high capacitance values would result, which could not be employed in single-phase PFC rectifiers due to the high reactive power consumption from the mains.

d) Filter with Minimal Costs: Finally it should be noted that also costs could be used as a quality criterion for the filter optimization. However, for the sake of brevity, we here would like to refer to [16].

5) Losses of Auxiliary Systems: The power consumption of auxiliary devices, such as current / voltage sensors, digital control electronics, fans for forced air-cooling, are independent of the output power level and have to be minimized by proper control measures to achieve high efficiency especially for partial load (cf. (5) and Fig. 3 (a)). This can be achieved by e.g. reduction of the clock frequency of the digital control electronics or by a temporary deactivation of the fans at partial load. For systems with ultra-high efficiency, fans can be omitted completely (cf. section V).

B. Control Measures

As has been shown in section II there is a significant efficiency reduction at low output power due to constant losses. However, high efficiency could be maintained if at partial load P_2 is not delivered continuously, but a higher power P_2' is delivered to the output intermittently [17]. The delivered average power value is then set by the duty cycle $T_{\text{on}}/T_{\text{rep}}$ (T_{rep} denominates the cycle time). P_2' can be chosen advantageously equal to the power level $P_{2,\eta_{\max}}$ showing the maximum efficiency $\eta_{\max}$. Thus the system always
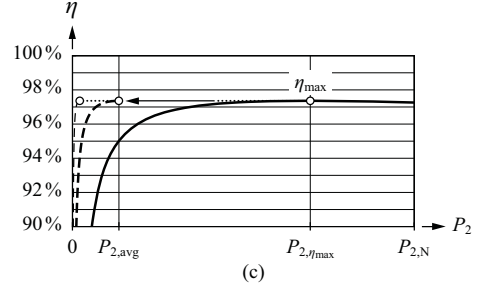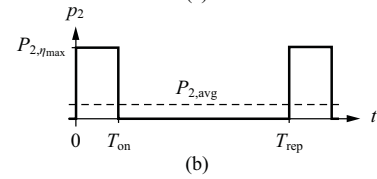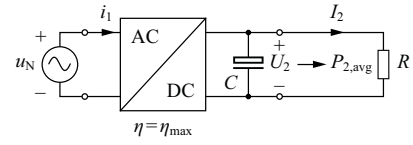

Fig. 16. (a) Converter topology, (b) output power and (c) efficiency characteristic for intermittent operation of a converter yielding for maximal efficiency.

works at its maximum efficiency level given that no stand-by losses occur in the power off state (cf. Fig. 16). However, in order to achieve an averaging of the discontinuous power delivery and have a continuous power flow $P_2 = P_{2,\text{avg}}$ at the output, a sufficiently large energy storage and eventually a charging and discharging circuit (with efficiency values η_c and η_d) must be provided.

Given the energy balance

$$(P_{2,\eta_{\max}} - P_{2,\text{avg}})\eta_c T_{\text{on}} = \frac{P_{2,\text{avg}}}{\eta_d}(T_{\text{rep}} - T_{\text{on}}), \qquad (67)$$

the required relative duty cycle is determined by

$$D = \frac{T_{\text{on}}}{T_{\text{rep}}} = \frac{1}{1 + \left(\frac{P_{2,\eta_{\max}}}{P_{2,\text{avg}}} - 1\right)\eta_c \eta_d}. \qquad (68)$$

The efficiency is then given by

$$\eta = \frac{P_{2,\text{avg}} T_{\text{rep}}}{P_{1,\eta_{\max}} T_{\text{on}}} = \frac{P_{2,\text{avg}} T_{\text{rep}}}{\frac{P_{2,\eta_{\max}}}{\eta_{\max}} T_{\text{on}}} = \eta_{\max} \frac{\eta_c \eta_d}{1 - D(1 - \eta_c \eta_d)}. \qquad (69)$$

In case no explicit charging and discharging circuit is required, e.g. if a PFC rectifier features a sufficiently large output capacitor (voltage sag immunity), $\eta_c = \eta_d = 1$ is valid. This simplifies (69) to

$$\eta = \eta_{\max} \qquad (70)$$

and the relative duty cycle results in

$$\frac{T_{\text{on}}}{T_{\text{rep}}} = \frac{P_{2,\text{avg}}}{P_{2,\eta_{\max}}}. \qquad (71)$$

For PFC rectifiers the efficiency varies during the mains period [18] and shows around the zero-crossings very low values due to the low delivered power and reaches its maximum at the maximum of the mains voltage. Thus, the partial load efficiency can be improved by operating the system only around the voltage maxima [17]. This results, however, in a higher input current distortion.
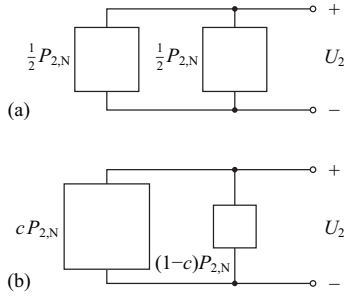
Fig. 17. Partitioning of a converter into multiple phase-shifted subsystems; (a) symmetrical distribution; (b) asymmetrical distribution for an optimal matching with a mission profile with only very low and very high output power demand.

C. Topology and Control Measures

The previous considerations were limited to hard switching converter systems operating in CCM operation. The optimal chip area of the power transistors yielding maximal efficiency at the nominal operating point has been calculated in (32). However, this calculation leads to relatively low efficiencies at partial load due to load-independent capacitive switching losses. As shown in Fig. 7, the efficiency could be improved at partial load by reduction of the chip area. Thus, it is reasonable to split the system up into multiple parallel systems and operate just as many systems as required at partial load to achieve a maximum efficiency of the power conversion. With the selection of the number of active systems the effective chip area can therefore be adapted according to the power to be delivered. As will be shown in the following, parallel operation furthermore offers advantages regarding the total input and output current and can be used for the reduction of conducted electromagnetic emissions. However, these benefits are only present in case all subsystems feature the same rated power $P_{2,n} = P_{2,N}/n$. Accordingly, an asymmetric distribution of the power (cf. Fig. 17 (b)) e.g. to cover a mission profile with only very low and very high output power demand with high efficiency [19], is typically not employed.

1) Phase Shifted Operation of Parallel Systems: For the subsequent analysis the parallel operation of $n = 2$ boost converters will be considered. As known from literature, [20], the subsystems should be preferably operated with 180° (in general $\Delta\varphi = 360°/n$ [21]) phase shift. Only the input current ripple will be calculated. Analogously, also the switching frequency components of the output current and / or the output capacitor losses are reduced.

a) Reduction of the Ripple of the Total Input Current: If the input voltage u_1 is assumed to be variable and the output voltage U_d is constant, as it is the case for single-phase PFC rectifiers, and the voltage transfer ratio is defined as

$$m = \frac{u_1}{U_d}, \tag{72}$$

the amplitude of the current ripple of a simple system (cf. Fig. 18 (a)) is given by

$$\Delta\hat{i} = \frac{U_d}{2f_P L}m(1-m), \tag{73}$$

where L ist the boost inductance. The maximum amplitude of the ripple appears for $m = 0.5$ (cf. Fig. 19) and is given by

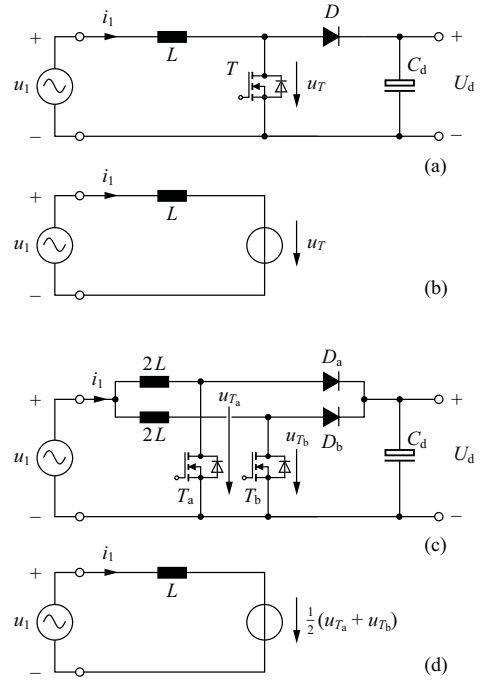$$\Delta\hat{i}_{\text{max},n=1} = \frac{U_d}{8f_P L}. \tag{74}$$

Fig. 18. Partitioning of a single-phase boost-type PFC rectifier (cf. (a)) into two phase shifted partial systems (cf.(c)); (b) and (d): equivalent circuits for same relative ripple of all inductor currents relevant for the calculation of the ripple of the total input current of the systems depicted in (a) and (c), respectively. For the system depicted in (c) the ripple is determined by the inductance resulting from the parallel connection of the two inductors $2L$ of the partial systems, i.e. again by L as for the single system (a).

If now two converter systems are operated with 180° phase shift (cf. Fig. 18 (c)), the current harmonic components at odd multiples of the switching frequency cancel each other out as can be immediately understood from the equivalent circuit in Fig. 18 (d). The maximum ripple amplitude is then lowered to

$$\Delta\hat{i}_{\text{max},n=2} = \frac{U_d}{32f_P L} \tag{75}$$

and appears then at $m = 0.25$ and $m = 0.75$, respectively (cf. Fig. 19). Equation (75) is valid in case a boost inductance $2L$ is provided for each subsystem, i.e. the input currents of the subsystems have the same relative ripple as the input current of the single system. The ripple reduction by a factor of 4 can be explained by two facts; on the one hand the frequency of the voltage $(u_{T_a} + u_{T_b})/2$ which causes the ripple is doubled due to the cancelation of the harmonics at the switching frequency (relates to a doubling of the impedance of the inductance); and on the other hand the amplitude of the voltage causing the ripple is halved (linear decrease of the amplitudes of the voltage harmonics with increasing ordinal number). Here it is important to note, that the effective increase of the frequency which defines the ripple is achieved without increase of the switching losses, since both subsystems operate at the same frequency as the single system and at half current.

Due to the reduction of the total current ripple the capacitance of the input capacitor could be reduced by a factor of 8 compared to a single system for a certain voltage ripple amplitude. Alternatively, an inductance of only $1/4L$ could be provided for each subsystem
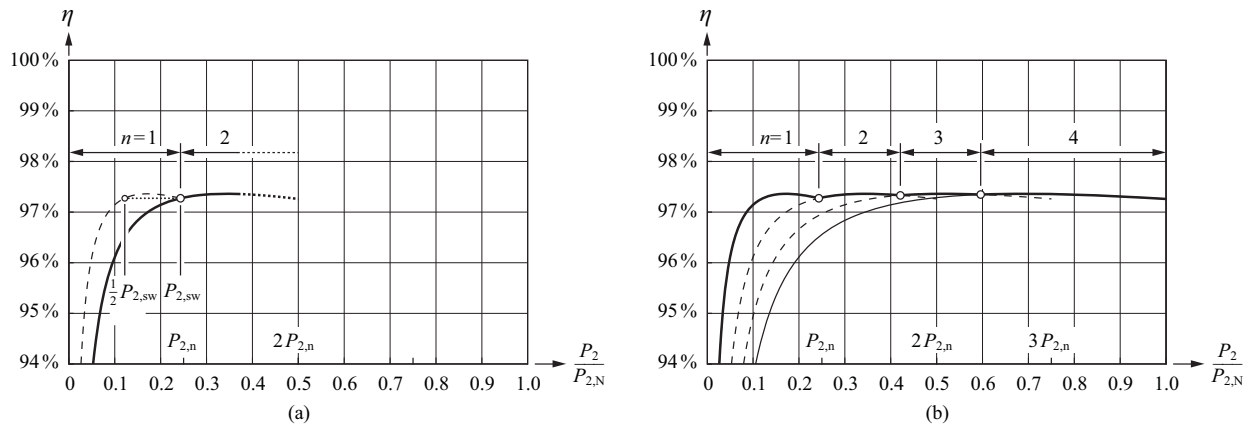
Fig. 20. Parallel operation of $n = 4$ subsystems for achieving maximum power conversion efficiency. (a) Switchover from $n = 1$ to $n = 2$ at the power level $P_{2,\text{sw}}$ which is characterized by maintaining the efficiency value $\eta(P_{2,\text{sw}})$ given in advance to the switching action, i.e. by $\eta(P_{2,\text{sw}}) = \eta(1/2 P_{2,\text{sw}})$; a switchover has to be performed in any case if the output power P_2 would exceed the rated power $P_{2,n}$ of a single system; (b) efficiency characteristic resulting for efficiency optimal activation of 4 partial systems.
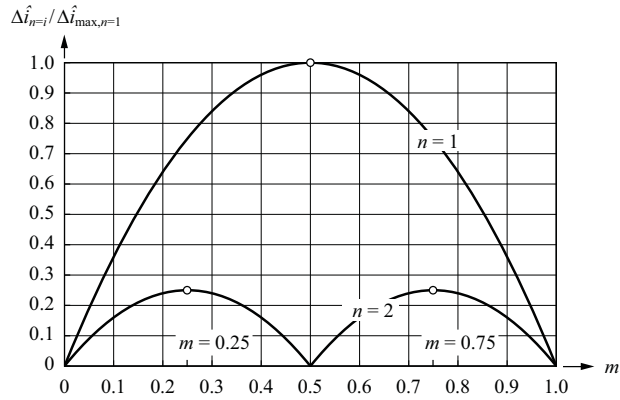

Fig. 19. Amplitude of the input current ripple of a boost converter in dependence of the voltage transfer ratio m for a single system ($n = 1$) and for two $180°$ phase shifted partial systems ($n = 2$); structure of the power circuit of the systems as shown in Figs. 18 (a) and (c).

in case the capacitance stays unchanged. In both cases, however, the remaining components of the EMI filter would have to be increased in order to still fulfill the EMI standards.

b) Efficiency-Optimal Partitioning of the Total Power between the Subsystems: Now it shall be analyzed in which way n subsystems can be utilized to achieve maximum efficiency for a given output power range. For low power levels it makes sense to only activate one subsystem, since this system then operates at a relatively high power level and therefore at a higher efficiency than multiple parallel systems equally sharing the power. The question arises at which power level $P_{2,\text{sw}}$ an additional system has to be activated and which power distribution between the two subsystems should be set. To answer this question, the efficiency characteristics of a subsystem is approximated (valid for power levels P_2 sufficiently larger than 0) by

$$\eta = 1 - \frac{P_\text{V}}{P_2} = 1 - \left(\frac{k_0}{P_2} + k_\text{I} + k_\text{II} P_2 \right). \tag{76}$$

If 2 subsystems (system a and system b) are operated in parallel and if the total power P_2 is partitioned according to

$$P_{2,\text{a}} = a P_2,$$
$$P_{2,\text{b}} = (1 - a) P_2, \tag{77}$$

the efficiency of the total system is given by

$$\eta = \frac{P_2}{P_2 + (P_{\text{V},1} + P_{\text{V},2})} = \frac{1}{1 + 2\frac{k_0}{P_2} + k_\text{I} + k_\text{II}(1 - 2a + 2a^2) P_2}. \tag{78}$$

The maximum efficiency then is determined by

$$\frac{\mathrm{d}\eta}{\mathrm{d}a} = k_\text{II} P_2 (4a - 2) = 0 \tag{79}$$

and / or is resulting for

$$a = 0.5. \tag{80}$$

Thus, the output power has to be partitioned equally between the two subsystems. This can be explained by the minimum sum of the ohmic losses of the two subsystems achieved in this case. A reduction of the power of one system leads to a reduction of the relative ohmic losses of this system, but also to an increase of the losses of the second system. The maximum reduction of the total losses is then given for $a = 0.5$. Here, constant losses and losses which depend linearly on the output current (power) do not affect this optimum distribution. The reason lies in the fact that constant losses occur in any case, i.e. independent of the power level, and the linear power-proportional losses cause the same efficiency decrease in the whole power range (cf. section II).

Now it has to be clarified, at which point the number n of parallel systems has to be increased in order to achieve maximum efficiency. It is sensible to perform the switchover at the intersection of the efficiency curves of n systems and $n + 1$ systems, i.e. at

$$\eta \left\{ \frac{1}{n} P_{2,\text{sw}} \right\} = \eta \left\{ \frac{1}{n+1} P_{2,\text{sw}} \right\} \tag{81}$$

where $P_{2,\text{sw}}$ is the total output power at the intersection. With (76) $P_{2,\text{sw}}$ is given by

$$P_{2,\text{sw}} = \sqrt{\frac{k_0}{k_\text{II}}} \sqrt{n(n+1)} = P_{2,\eta_\text{max}} \sqrt{n(n+1)} \tag{82}$$

where $P_{2,\eta_{\max}}$ is the power level of a subsystem related to the efficiency maximum. According to (82) the switchover from $n = 1$ to $n = 2$ has to be performed at $P_{2,\text{sw}} = \sqrt{2}P_{2,\eta_{\max}}$, i.e. after the maximum. For larger values of n the switchover from $n \to n+1$ has to be performed approximately at $P_{2,\text{sw}} = nP_{2,\eta_{\max}}$ (cf. Fig. 20).

For the case that (82) gives a value $P_{2,\text{sw}}$ which lies beyond $P_{2,n}$, the switchover has to be done at

$$P_{2,\text{sw}} = n \cdot P_{2,n}. \tag{83}$$

This is the case, if the maximum of the efficiency characteristic lies very close to the nominal power or if the efficiency characteristic shows a purely monotonic behavior (without maximum).

c) EMI Filter for Phase-Shifted Operation: The reduction of the total current ripple as described in section III-C1a) can be explained by the cancelation of the harmonics at odd multiples of the switching frequency (cf. Fig. 21 (a)). The voltage and current harmonics of the two subsystems (voltages u_{T_a} and u_{T_b}, and currents i_{L_a} and i_{L_b}) show the same amplitudes and opposite phase. The harmonics at even multiples of the switching frequency, however, stay unchanged, i.e. the spectrum of the voltage u_T and of the voltage $1/2(u_{T_a} + u_{T_b})$ exhibit harmonics with the same amplitudes at these frequencies. Consequently, regarding EMI filtering there results no advantage of the phase-shifted parallel operation. Only some harmonics are removed from the spectrum, while others remain and have to be attenuated as before. An advantage can only be seen compared to a simple system operated at double switching frequency (which is the effective frequency of the parallel system), which exhibits a higher noise level by a factor of 2 at $2f_P$ and would consequently require a higher filter attenuation (cf. Fig. 21 (a)).

An interesting case is a switching frequency f_P lying slightly below the frequency band defined in the EMI standards. With $\Delta\varphi = 180°$ the switching frequency harmonic is canceled. With this, an advantage is given for the dimensioning of the input capacitor (cf. section III-C1a)) for a specified voltage ripple, while for the design of the EMI filter no benefit results, since f_P does not fall into the frequency band of the standard. The required filter attenuation is defined by the amplitude of the harmonic at $2f_P$, which occurs in the same manner as for synchronous operation of the subsystems. This raises the question which phase-shift is optimal from the viewpoint of the EMI filter design. As described in [22] and depicted in Fig. 21 (b) an optimal value is given for $\Delta\varphi = 90°$ (asymmetric interleaving) in case of two subsystems.

It has to be noted that at light loads only one subsystem is active and also in this case the EMI standards have to be complied with. This is alleviated by the fact that then the full input inductance $2L$ of the subsystem is present and not the parallel connection of 2 inductances. In any case, the worst-case condition has to be checked, where it could become apparent that the advantage of asymmetrical interleaving cannot be utilized.

In summary it can be stated that for the case of a switching frequency lying outside the frequency band of the EMI standard a compromise concerning the selection of $\Delta\varphi$ has to be made. Either a reduction of the ripple current for the input and output capacitor or a reduction of the input inductance could be achieved, or the conducted emission could be reduced and shifted to higher frequencies and / or the dimensioning of the total EMI filter could be less demanding.

2) Transition from CCM to Resonant Transition Mode (ZVS): In section III-C1) the limit (33) given by the semiconductor technology was broken by partitioning of the system into multiple subsystems. Alternatively, the technological limits can be disabled by avoiding the capacitive switching losses, i.e. by transition to zero voltage
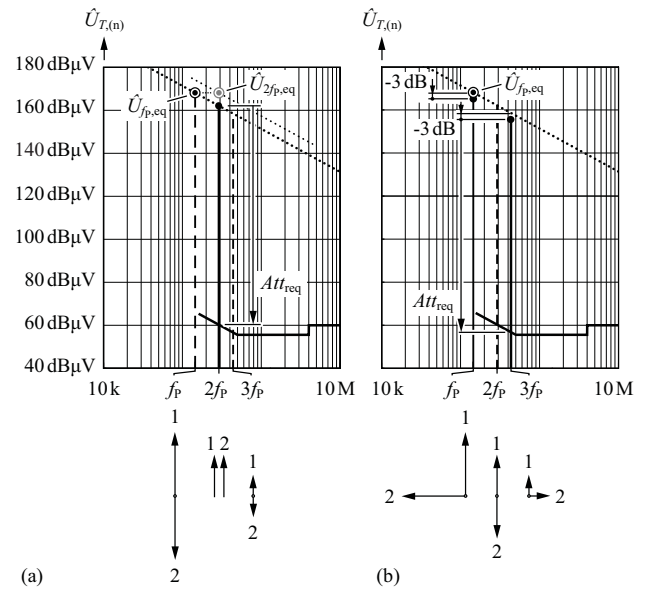

Fig. 21. Design of the EMI filter in dependency of the phase shift $\Delta\varphi$ of two parallel subsystems (assumption: switching frequency slightly lower then the frequency range covered by CISPR 11; the phase relation of the harmonics of the subsystems is illustrated by phasors). (a) $\Delta\varphi = 180°$, the voltage harmonic at $2f_P$ is determining the filter design; in addition: equivalent harmonic voltage of a system operated with $2f_P$. (b) asymmetric interleaving, $\Delta\varphi = 90°$, for minimizing the required filter attenuation. The filter has to be designed in consideration of the voltage harmonic at $3f_P$ which is lower in amplitude by a factor of $\sqrt{2}$ (3 dB) compared to a frequency proportional decrease of the equivalent noise voltage $\hat{U}_{f_P,\text{eq}}$. In contrast to (a) the voltage harmonic at f_P now is not cancelled but only reduced in amplitude by 3 dB.

switching (ZVS) based on a concept proposed in [23], [24] which can be applied in modified form to PFC rectifier topologies as shown in Fig. 22. There, instead of freewheeling diodes power MOSFETs are employed, which are turned on during the freewheeling period (synchronous rectification) and are kept in the on-state until a sufficiently high negative current value is reached. After turn-off this negative current, which is impressed by the inductor, provides a fully resonant transition of the voltage, i.e. ZVS conditions for the opposite transistor in the bridge leg. This allows to (ideally) completely avoid switching losses. Furthermore, contrary to the CCM operation, the conduction losses can be reduced by paralleling a high number of power transistors. It is important to note that a constant efficiency reduction resulting from the on-state voltage of freewheeling diodes is avoided in this case (synchronous rectification) and / or a high efficiency can be achieved for partial load.

With reference to the resonant transition of the transistor voltage at turn-on and turn-off (where a certain minimal current has to be guaranteed by the control) and the triangular shape of the inductor current, respectively, this operation mode is denominated as resonant transition mode or Triangular Current Mode (TCM), respectively (cf. Fig. 23). In order to minimize the current stress on the input and output capacitors, multiple converter stages should be operated in parallel. This also gives the possibility to turn off subsystems in order to achieve maximum efficiency for partial load as described in section III-C1b). Furthermore, extreme switching frequencies at low output power levels can then be avoided.

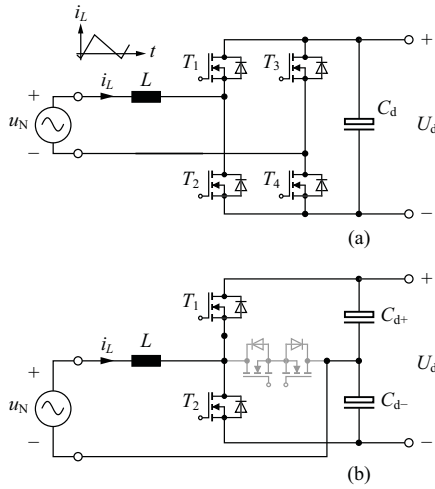The concept of the resonant transition mode operation is not limited

Fig. 22. Circuit topologies of (bidirectional) single-phase boost-type resonant transition mode PFC rectifier systems. (a) full-bridge circuit; the bridge leg T_3, T_4 is switched with mains frequency and performs the rectifier function; (b) the switches T_3 and T_4 could be omitted for direct connection of a mains terminal with the DC voltage center point (voltage doubler circuit); furthermore, the systems could be extended into a three-level topology by employing a four-quadrant switch (light-colored).
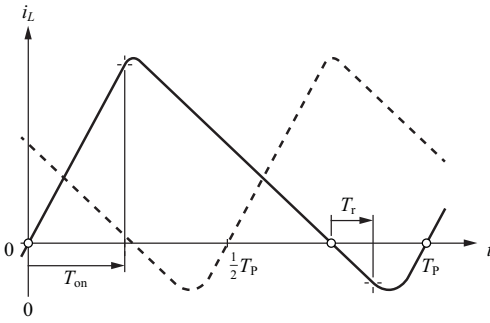

Fig. 23. Time behavior of the inductor current i_L of a resonant transition mode ZVS boost converter. According to the shape of the current waveform the systems is also denominated as triangular current mode (TCM) converter. Furthermore shown: input current of a system operated in parallel with a phase shift of $180°$.
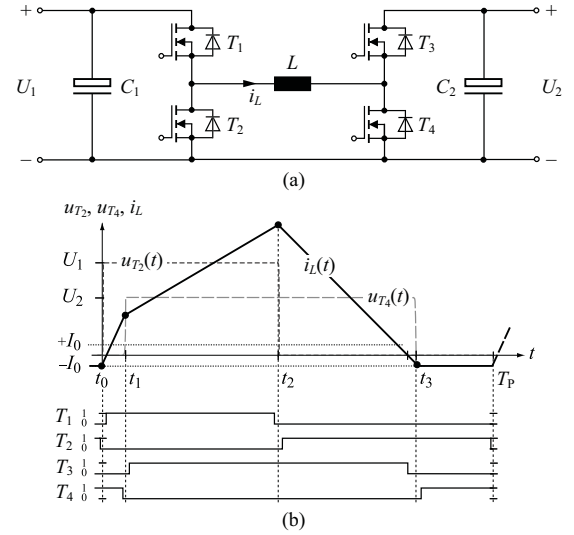

Fig. 24. Resonant transition mode buck+boost DC/DC converter according to [25]. (a) structure of the power circuit and (b) time behaviour of the inductor current i_L; by proper control a current I_0 is provided which ensures a complete discharge of the parasitic capacitance of a power transistors (or a completed charging of the capacitance of the opposite transistor in the bridge leg) and/or ZVS. (c) $12\,\mathrm{kW}$ demonstrator of the system specified for $U_1 = 150\ldots400\,\mathrm{V}$ and $U_2 = 150\ldots400\,\mathrm{V}$; maximum efficiency: $\eta = 99.3\,\%$ (for $U_1 = 450\,\mathrm{V}$, $U_2 = 450\,\mathrm{V}$); power density: $30\,\mathrm{kW/dm^3}$.

to boost converters but can advantageously also be used e.g. for buck+boost converters, i.e. converters with overlapping input and output voltage ranges. The inductor current then shows a trapezoidal shape instead of a triangular shape. An example of a converter for automotive applications is shown in Fig. 24.

3) Further Converter Concepts for Efficiency Increase: In the precedent sections possibilities for efficiency improvements of power electronic converters have been discussed. Hereby, the focus has been on the appropriate design and the advantageous selection of the operation mode. To conclude, further conceptual methods for an efficiency increase shall be demonstrated by two examples. First, the concept of a limitation of the power conversion to a portion of the output power (partial power conversion), and secondly, the reconfiguration of converter subsystems from series to parallel connection in order to cover a wide input or output voltage range with limited duty cycle variation.

a) Partial Power Conversion: In order to visualize the advantages of the partial power concept [26], [27], a DC/DC buck converter is considered, which converts an input voltage U_1 to an output voltage $U_2 \le U_1$. In contrast to a conventional converter structure not the whole output power is converted, but only an adjustable series voltage U_c is generated, which is subtracted from U_1 in such a way, that the desired output voltage

$$U_2 = U_1 - U_c \tag{84}$$

results. In analogy to an auto-transformer for AC voltages the power to be converted is then limited to a much lower level (Partial Power Conversion)

$$p_c = \frac{P_{c,1}}{P_1} = \frac{\frac{U_c}{U_2}}{1 + \frac{U_c}{U_2}}, \tag{85}$$

i.e. the converter can be designed for a much lower power level. Another advantage arises from the fact that for $U_c \ll U_2$ the major part of the output power is delivered directly from the input, i.e. does not need to be converted. Thus, the influence of the efficiency of the converter on the total power conversion efficiency is extenuated
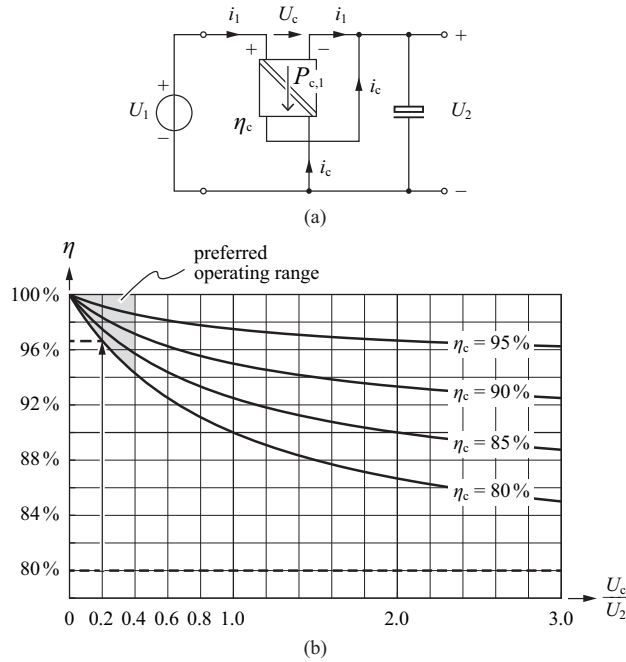
Fig. 25. (a) Structure of the power circuit of a Partial Power DC/DC buck converter and (b) dependency of the overall efficiency on the relative output voltage U_c/U_2 and of the efficiency η_c of the partial power processing converter.

according to

$$\eta = \frac{P_2}{P_1} = \frac{1 + \frac{U_c}{U_2}\eta_c}{1 + \frac{U_c}{U_2}} \tag{86}$$

(cf. Fig. 25, [28]), since losses only occur for the portion of the power which passes through the converter. E.g., for $U_c/U_2 = 0.2$ and a converter efficiency of $\eta_c = 0.8$ a total efficiency of over $\eta = 0.96$ can be realized. The converter efficiency is determining the total efficiency only for $U_c/U_2 \to \infty$ entirely, i.e. $\eta = \eta_c$ is given in this case. This concept can also be employed for boost operation and buck-boost operation [27].

b) Limitation / Adaption of the Operation Voltage Range: If a wide input voltage range is desired for the operation of a power converter, it can be advantageous to pre-condition the voltage by an additional converter stage [29]. With this measure, the values of the design parameters in the course of the optimization of the efficiency of the main converter can be chosen in a wider range, and / or the losses of the additional converter stage could potentially be overcompensated. Furthermore, typically a lower realization effort is given in this case.

As shown in Fig. 26 (a), the additional converter stage can be activated only in case the input voltage is out of its nominal range. This situation e.g. appears for single-phase PFCs at mains voltage failures. An additional DC/DC boost stage is activated then, which brings the sagging DC link voltage back to its nominal value [30].

As an alternative to the continuous voltage adaption also an adjustment of the voltage by series-parallel reconfiguration of the input or output stage of the converter is a possibility. This concept is known from series-parallel-connection of the windings of AC machines with a wide rotational speed range [31]. Fig. 26 (b) shows exemplarily a system which allows the series-parallel reconfiguration
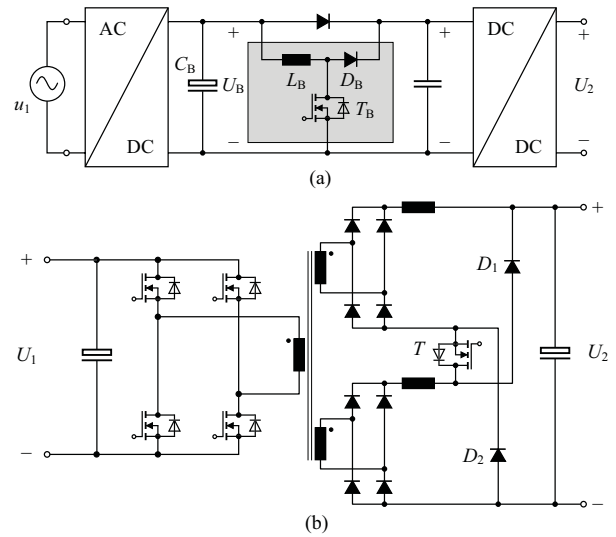

Fig. 26. (a) DC/DC boost converter for increasing the voltage of the output capacitor of a single-phase PFC rectifier in case of mains outages in order to provide a largely constant supply voltage for the DC/DC converter connected in series; (b) DC/DC converter with two secondary circuits which could be arranged in series or parallel in order to provide a wide output voltage range with limited duty cycle variation.

of the output stages of an isolated DC/DC converter [32] in order to cover a wide output voltage range. For low output voltages the transistor T stays blocked and both systems deliver the output current in parallel. For high output voltages the transistor T is activated and a series connection of the 2 systems results (which relates to an increase of the transformer turns ratio by a factor 2). A transient change of the output voltage U_2 at the switchover is avoided by proper adjustment of the duty cycle on the primary side.

IV. HIGHLY ACCURATE EFFICIENCY MEASUREMENT

The measurement of high efficiencies according to

$$\eta = \frac{P_2}{P_1} \tag{87}$$

results high demands on the accuracy of the measurement of the input and output power. In the following, the resulting error in the efficiency measurement will be calculated for a given error in the power measurement and thus the accuracy requirements specified. Hereby it must be taken into account that on the one hand, the measurement serves to determine the degree of utilization of an incoming power P_1 in the form of (87), and on the other hand, especially with highly efficient systems, the (relative) losses are actually of interest. A comparison of efficiency values near 1, e.g. of $\eta = 0.991$ and 0.992, hence gives little information on the losses. Thus in the final analysis, the required accuracy of the power measurement must be defined in dependence on the desired accuracy of the power loss determination.

Starting from (87) and considering

$$\mathrm{d}\eta = \frac{\partial \eta}{\partial P_2}\mathrm{d}P_2 + \frac{\partial \eta}{\partial P_1}\mathrm{d}P_1, \tag{88}$$

there follows for the maximum error in the efficiency at absolute errors ΔP_1 and ΔP_2 of the power measurements

$$\Delta\eta = \eta\left(\frac{\Delta P_2}{P_2} + \frac{\Delta P_1}{P_1}\right), \tag{89}$$
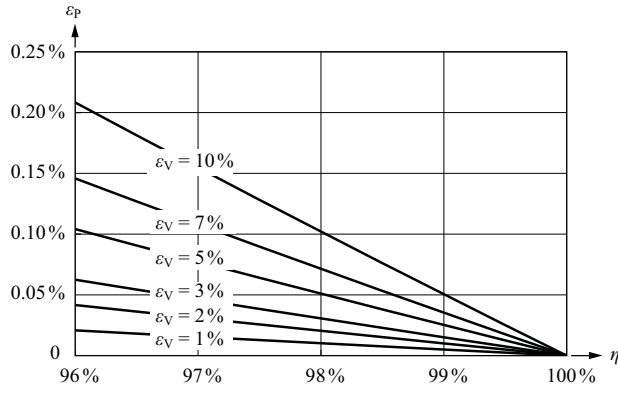
Fig. 27. Maximum permissible relative error in the power measurement ε_P for the determination of the losses with a max. relative error of ε_V in dependence on the efficiency.

Fig. 28. Two-chamber calorimeter for high-precision measurement of the losses of power electronics converters ($\varepsilon_V < 3.5\,\%@10\,\mathrm{W}$, $< 1.0\,\%@100\,\mathrm{W}$, $< 0.5\,\%@200\,\mathrm{W}$) developed at ETH Zurich [33], [34]; the temperature inside the inner chamber, i.e. the ambient temperature of the device under test can be set in the range $T_\mathrm{c} = T_\mathrm{a} + 10\,^\circ\mathrm{C}$ to $85\,^\circ\mathrm{C}$ (T_a is the temperature at the surface of the outer chamber).

and hence for the maximum relative error of the efficiency

$$\varepsilon_\eta = 2\varepsilon_P, \qquad (90)$$

whereby ε_P designates the relative error in the power measurement. Equation (87) according to

$$\eta = 1 - \frac{P_V}{P_1} \qquad (91)$$

also characterizes the relative losses, so that the relation

$$\Delta\eta = \frac{\mathrm{d}\eta}{\mathrm{d}P_V}\Delta P_V \qquad (92)$$

exists between the absolute error in the losses and the absolute error in the efficiency, and

$$\varepsilon_\eta = \varepsilon_V \frac{1-\eta}{\eta} \qquad (93)$$

follows for the relative error.

By equating (90) and (93) the accuracy of power measurement can thus be related to the accuracy of the loss determination. There follows

$$\varepsilon_V = \frac{2\eta}{1-\eta}\varepsilon_P \qquad (94)$$

(cf. Fig. 27). Equation (94) makes clear that a high accuracy in the power loss determination at efficiencies near 1 (or $(1-\eta)$ near zero) requires extreme accuracy in the power measurement and/or efficiency determination (cf. (90)). If e.g. the losses of a system with $\eta = 99\,\%$ are to be determined with max. $10\,\%$ relative error, i.e. with $\varepsilon_V \le 0.1$, a maximum error in the power measurement of only $\varepsilon_P = 0.05\,\%$ is permissible. This value is attained only by best-in-class power measurement instruments such as the Yokogawa WT3000 ($\varepsilon_P^* = 0.02$, cf. (95)).

Here it must be considered that the error of a power measurement instrument is typically stated with reference to the end value P^* of the measurement range. Hence for the possible relative error for the power P to be measured,

$$\varepsilon_P \le \frac{\Delta P}{P^*}\frac{P^*}{P} = \frac{1}{c_\mathrm{r}}\varepsilon_P^* \qquad (95)$$

applies, where $c_\mathrm{r} \le 1$ characterizes the utilization of the measurement range.

In the measurement of the input and output power discussed above, the losses are determined indirectly, i.e. from the difference between P_2 and P_1, so that for very high efficiency, extreme accuracy demands on the power measurement result. Hence, for highly efficient systems, the alternative of a direct measurement of the losses by means of a calorimeter should be considered. Typical accuracies there lie in the range of $\varepsilon_V = 1\ldots2\,\%$ (cf. Fig. 28, [33], [34]). With reference to

$$\eta = 1 - \frac{P_V}{P_1} = \frac{1}{1 + \frac{P_V}{P_2}}, \qquad (96)$$

the efficiency can also be calculated with high accuracy,

$$\varepsilon_\eta = \frac{1-\eta}{\eta}(\varepsilon_V + \varepsilon_P), \qquad (97)$$

whereby it is advantageous for AC/DC converters in (96) to use the relation with the output power. The power measurement on the DC side can be performed much more simply with high accuracy than on the AC side, because no power-forming harmonics up to high ordinal numbers with low phase difference must be included.

V. EXTREME EFFICIENCY PFC RECTIFIER SYSTEMS

Based on the consideration described above, within the framework of a research project of the European Center for Power Electronics (ECPE, www.ecpe.org) at the ETH Zurich (www.pes.ee.ethz.ch), concepts of single-phase rectifier circuits with sinusoidal current consumption were analyzed with regard to maximum attainable efficiency. In the following, core results of the project are briefly summarized which make clear on the one hand, today's de facto limit to the loss reduction and on the other hand the still to be achieved power density thereby. The rated power of the system was defined as $P = 3.3\,\mathrm{kW}$ with regard to applications in the field of IT power supply and the increasingly important charging of E-vehicle batteries. The power density in all cases should be $\rho > 1\,\mathrm{kW/dm^3}$.

Where extreme efficiency is demanded, it is obvious to use a rectifier structure without input diode bridge, i.e. the concept known as bridgeless or double-boost PFC rectifier [9], [35]–[37]. In this specific case, in a first step to assure high partial load efficiency, two phase-shifted sub-ystems with Si-superjunction MOSFETs (CoolMOS C6) and SiC freewheeling diodes and operating in CCM were employed (cf. Fig. 29 (a), (b)). The CM component of the output voltage
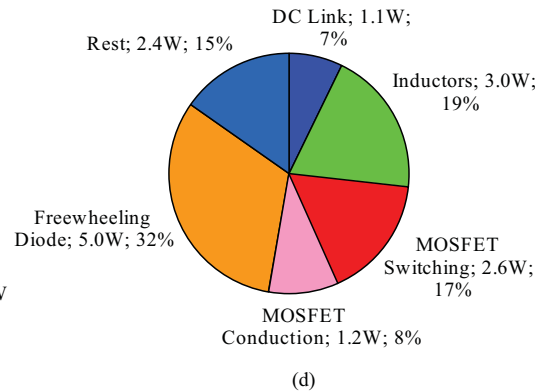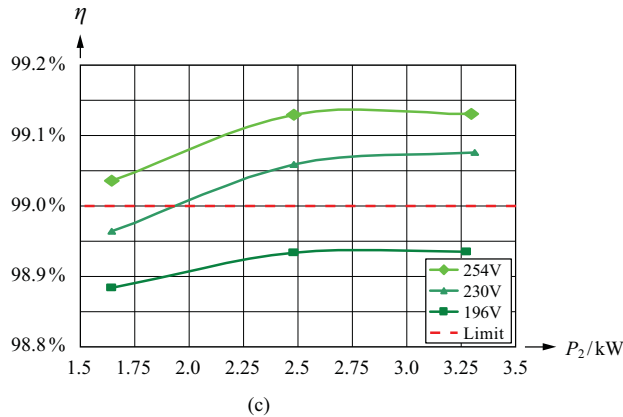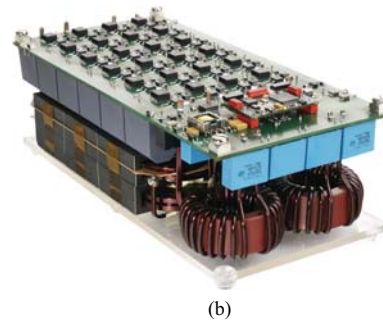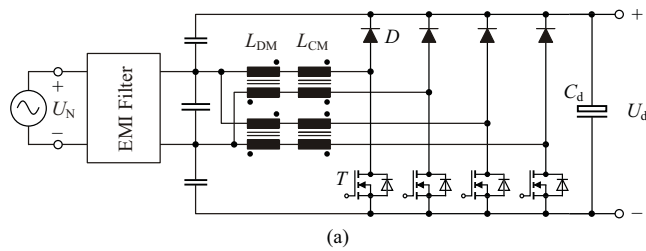
Fig. 29. 3.3 kW continuous conduction mode (CCM) bridgeless boost-type PFC rectifier system: (a) power circuit structure, (b) demonstrator of the system, (c) efficiency characteristic, (d) loss distribution.

of the bridgeless concept was essentially suppressed by an internal capacitive connection of the output terminals to the AC side and by insertion of a common-mode inductor into this inner loop [5]. Out of the consideration for the efficiency, moreover, a relatively low switching frequency of $f = 33$ kHz was selected, and to broaden and lower the EMI interference spectrum, a double mains frequency switching frequency modulation with 6 kHz swing was implemented. The rated-load efficiency thus attained at rated voltage is 99.1 % incl. all auxiliary supplies (cf. Fig. 29 (c)). By increasing the number of parallel MOSFETs and diodes, a reduction in the conduction losses would result, but at the same time the capacitive switching losses would increase (the stated efficiency value applies for the optimum number of components). If the capacitive switching losses should remain unchanged despite a large number of components, the switching frequency would have to be lowered. However, this would lead to a higher volume of the boost inductors and hence to a further reduction of the already low power density of 1.1 kW/dm^3.

Loss reduction at the same power density is thus only possible by changing the circuit concept. In order to reduce the conduction loss fraction of the diodes, which is specially prominent in the loss balance (cf. Fig. 29 (d)), as described in III-C, MOSFETs are used instead of the diodes (synchronous rectification) and the operating mode of the system is changed to a resonant transition mode. In this way a zero-voltage turn-on and turn-off of the transistors is assured, or switching losses (ideally) completely avoided. Thus in contrast to CCM operation, the possibility of lowering the conduction losses by increasing the number of semiconductor elements operated in parallel is open. In order to attain already without EMI filtering a relatively smooth input and output current curve and/or a relatively low current

loading of the input and outputs capacitors, it is of advantage to operate a higher number n of switching stages then for the CCM system in parallel. The circuit executed in the present case is shown in Fig. 30 (a), (b). Rectification of the mains voltage is achieved by a second bridge leg that is switched only at mains frequency. The choice of $n = 6$ is justified by the resulting favourable current loading of the MOSFETs (single switches) and by the availability of magnetic core shapes enabling an overall compact converter construction; a further important aspect is that a high partial load efficiency can thus be easily realized.

Due to the imprecisely defined reaction time of a DSP to an external hardware interrupt signal, the system is controlled by means of a CPLD. The lengths of the individual periods of the triangular current shape (cf. Fig. 31 (a)) are calculated here by the DSP in dependence on the mains and output voltages and the average current value to be set (defined by the superposed output voltage controller) and passed on via the SPI interface to the CPLD. The control sequence of the switches is triggered by the the digital output signal of a current zero-crossing detector (ZCD), a saturable toroidal magnetic core (R6.3) that leaves saturation only in the proximity of the current zero-crossings, and accordingly induces a positive or negative voltage in the secondary winding and thus switches over a comparator (cf. Fig. 31 (a)). Through the CPLD a reaction within 40 ns is possible; the sequence of the individual periods including the interlocking delay time of the switches of a bridge leg is defined by a state machine that also monitors maximum times. Because of the triangular current shape, the switching frequency varies over the mains period, so that an advantageously broad distribution of the switching frequency harmonic power results and hence a locally low
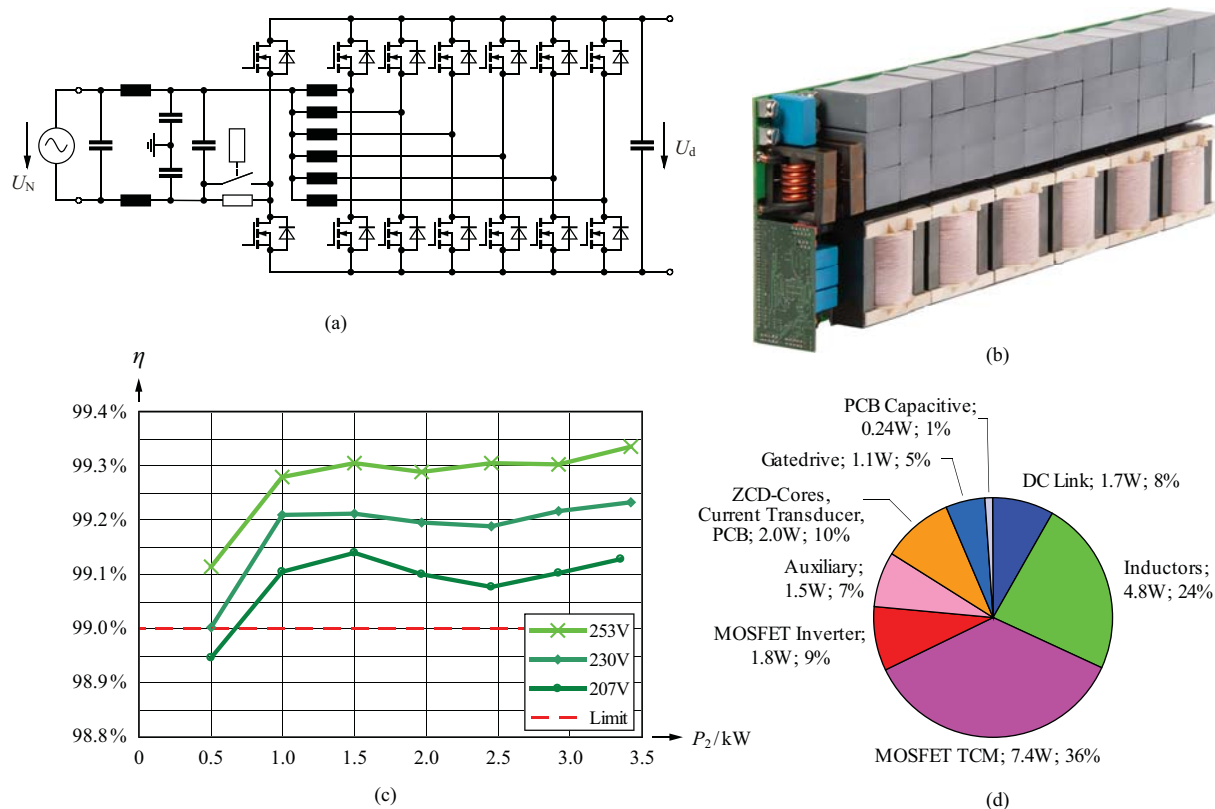
Fig. 30. 3.3 kW Resonant transition mode and / or triangular current mode (TCM) boost-type PFC rectifier system: (a) power circuit structure, (b) demonstrator of the system, (c) efficiency characteristic, (d) loss distribution.

level of the conducted interference. In consideration of the core and winding losses, a relatively low average switching frequency is selected and the maximum switching frequency is limited to 100 kHz, which leads to zero-current intervals and / or a minor current distortion in the proximity of the voltage zero-crossings.

The optimum phase shift of the subsystems in operation (turn-off of branches at partial load) is set by a control; the CPLD measures here the duration of a switching period of the triangular current of a master phase and the edges of the current zero-crossing signals in the other phases referred to reference times defined by the active phase number. The time differences to the reference points then form control deviations for synchronization control circuits, which change the turn-on times of the branches in such a way that the time differences are regulated to zero.

As shown by a loss analysis and an efficiency measurement by means of a power analyzer (Yokogawa WT3000, accuracy of the efficiency measurement 0.04 %) (cf. Fig. 30 (c)), the system (power density 1.1 kW/dm³) exhibits at rated voltage a rated-load efficiency of 99.23 % and at the upper input voltage tolerance limit (+10 %) an efficiency of 99.34 %. Correspondingly, the efficiency increase over CCM operation (see above) is achieved while maintaining the power density. There occur overall losses of only ca. 20 W at an output power of 3.3 kW! To the authors' knowledge, this represents the highest efficiency measured to date for single-phase PFC rectifier circuits, taking into account all auxiliary supplies and loss components.

Because of the low losses, forced cooling is unnecessary; after an hour of operation, the maximum temperature rise above ambient is only 23 °C. The losses are caused to nearly 50 % by the power MOSFETs and to about 25 % by the boost inductors (cf. Fig. 30 (d)) which are specially made in a core material that has its loss minimum at relatively low temperature (Ferroxcube 3C95). The losses of the output capacitors, which in the interest of loss minimization are realized as foil capacitors instead of electrolytic capacitors (leakage currents, equivalent series resistance) in order to minimize any loss components, amount to approximately 1.7 W (8 %). Further losses are from the gate drives at 1.1 W (5 %, gate control voltage 10 V), the DSP and CPLD 1.5 W (7 %) and from current zero-crossing detection (ZCD) and current measurement at roughly 2 W (10 %). By reduction of the number of active branches, the efficiency can be kept at values > 99 % down to 500 W output power.

Measurements of the conducted electromagnetic emission show (cf. Fig. 31 (b)), despite only a single-stage EMI filter is employed, an interference level at 150 kHz that lies 6 dB below the limit of CISPR 22/Class B/QP because of the relatively low medium switching frequency that varies strongly over the mains period; furthermore, as steep switching voltage changes are lacking, the interference emission exhibits a characteristic that falls monotonically towards high frequencies (cf. Fig. 31 (b)).

As can be readily seen from the basic converter circuit structure, the PFC rectifier system also allows energy to be returned to the mains (e.g. for vehicle-to-grid applications). Here, however, without
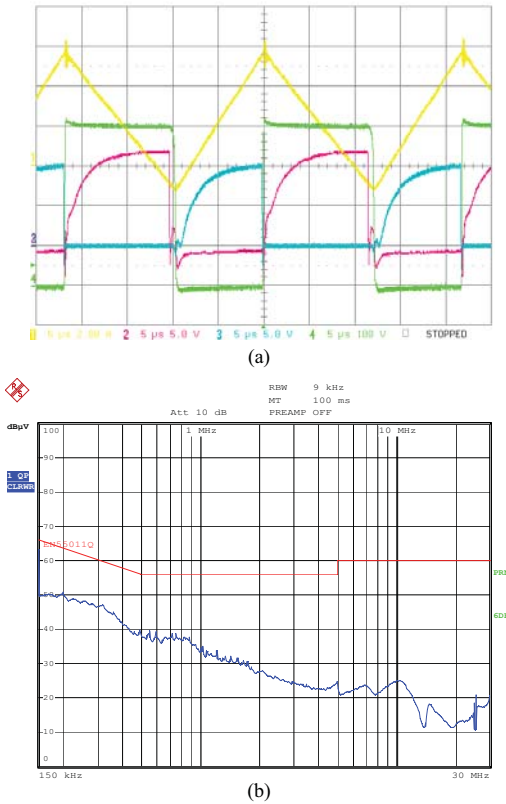
(a)

(b)

Fig. 31. (a) Measured input current waveform of a subsystem of the circuit shown in Fig. 30; also illustrated: drain-source voltage and gate-source voltage of the associated MOSFETs and output signal of the current zero-crossing detector; (b) conducted EMI emissions.

galvanic isolation of the load, the mains frequency square-wave CM voltage caused by the polarity switching bridge leg must be taken into account.

In the field of telecom power supplies one expects today for the conversion of the single-phase mains voltage into an isolated DC voltage (feeding the $-48\,\mathrm{V}$ bus) at $50\,\%$ rated power, typically an efficiency of $97\,\%$ (for $230\,\mathrm{V_{rms}}$ mains voltage) at a power density of $2.5\ldots3\,\mathrm{kW/dm^3}$. Accordingly, assuming the same power density and efficiency of the rectifier and DC/DC converter stage, an efficiency of $98.5\,\%$ per subsystem at a power density of $5\,\mathrm{kW/dm^3}$ must be realized. Furthermore, a very flat efficiency curve must be assured over the output power range, in particular a high partial-load efficiency. As shown by a closer theoretical analysis, this requirement can be fulfilled by the resonant transition mode rectifier concept described above. For practical verification of these considerations, the $3.33\,\mathrm{kW}$ telecom power supply module shown in Fig. 32 with three interleaved subsystems of the input stage and a phase-shift full-bridge isolated DC/DC converter as output stage was realized. By splitting the output stage into two subsystems, the power density could be increased to over $3\,\mathrm{kW/dm^3}$ and the efficiency at $50\,\%$ rated power to $> 97\,\%$.

VI. Conclusions

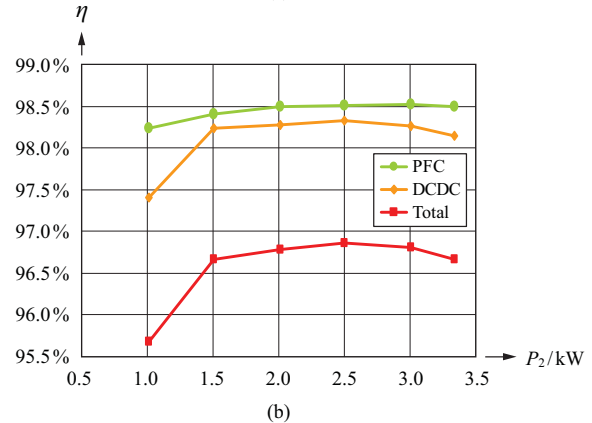The present work shows with the example of a single-phase PFC rectifier system that converters with an efficiency well over $99\,\%$ may

(a)

(b)

Fig. 32. $3.33\,\mathrm{kW}$ telecom power supply module (input stage: resonant transition mode boost-type PFC rectifier system with 3 phase-shifted branches, output stage: phase-shift full-bridge isolated DC/DC converter): (a) demonstrator of the system, power density: $2.5\,\mathrm{kW/dm^3}$, (b) efficiency curve.

be realized over a wide load range if a suitable converter concept and operating mode are chosen, and digital signal electronics and modern Si semiconductor technology are employed.

The converter concept proposed here, on the one hand, is based on the very low turn-on resistance of modern superjunction-MOSFETs, which exhibit only low conduction losses even for a high ripple of the input currents of the subsystems; on the other hand, it is enabled by the high functionality and flexibility of integrated digital circuits in the form of DSPs and FPGAs. Only in this way an exactly phase-shifted synchronization and precise control of the individual subsystems can be assured. The turn-off currents of the power transistors here are always set such that the parasitic output capacitance of a power transistor is always completely discharged via a resonant transition and no capacitive switching losses occur. Since the parasitic capacitance in addition acts as a turn-off snubber, switching losses are thus ideally avoided, or in contrast to hard switching, the chip area of the power transistors can be increased without having to accept rising capacitive losses. This degree of freedom represents one of the main advantages of this converter concept, apart from the possibility of using Si superjunction-MOSFETs as synchronous rectifiers instead of SiC freewheeling diodes. Moreover it should be emphasized that the resonant commutation is obtained without auxiliary networks, i.e. with a minimum of realization effort.

Because of the triangular current shape, moreover, only a relatively small input inductance must be provided for each subsystem, but despite this, owing to the phase-shifted operation of several subsystems, a largely smooth overall current waveform is attained. Hence for compliance with regulations concerning conducted electromagnetic

interference, only an EMI filter of relatively low volume must be provided. This is also supported by the natural variation of the switching frequency over the mains period, which leads to an uniform spectral distribution of the harmonic power and / or avoids the occurrence of harmonics of high amplitude at multiples of a defined switching frequency. Furthermore, a simple detection of the zero-crossings of the currents can be employed instead of explicit current measurements for each subsystem.

Finally, because of the splitting of the overall system into several subsystems, a turn-off of some systems at partial load is possible, again utilizing the high functionality of digital control. This reduces the drive and magnetic core losses or a very high efficiency can be assured even at light loads. Moreover, this also suppresses the occurrence of very high switching frequencies even at low output power.

In summary, it is important to point out that the proposed concept is heavily based on modern technologies with high future development potential [38] and the use of passive components with low development dynamic (inductors, capacitors) is minimized. Further technological improvements thus lead directly, i.e. without further development effort, to an improvement in performance.

Because of the above mentioned advantages, more widespread use of multiple parallel, interleaved resonant transition mode converter systems is to be expected in future, e.g. for DC/DC converters in the automotive area or for charging the batteries in E-vehicles. As shown in section III, despite the discontinuous current, a very high efficiency η and power density ρ may be realized even at high power. Here it should be noted that higher efficiencies for a converter are fundamentally always possible by increasing the volume of the unit. Hence, when judging the efficiency, both figures (and also the realization effort) must always be considered. This can be visualized very clearly in the form of the Pareto-front in the $\eta - \rho$-plane [39] (cf. Fig. 33).

In conclusion it must be stated that in future, apart from the optimization of individual converters, above all the optimum (e.g. minimum loss) conception of an overall power supply system will gain in importance. Only in this way the operation ranges of the individual converter stages can be mutually attuned in an optimal manner, e.g. with regard to the tolerance range of the input and output voltages, or an optimal splitting of the overall function into partial functions could be defined. For example, a constant output voltage could be required for an isolated DC/DC converter for a wide input voltage range. Or the voltage could be already conditioned by an upstream stage and only the isolation executed with constant voltage transfer ratio, for which purpose systems with extremely high efficiencies could be realized. For the support of such a comprehensive treatment, universities should develop suitable optimization procedures and simulation tools that also allow to take economic aspects into account.
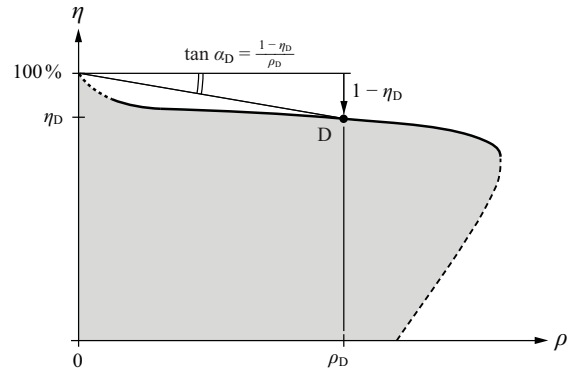
Acknowledgment

Fig. 33.   Pareto-front of a converter system (best possible compromise attainable via optimization between efficiency and power density) in the $\eta - \rho$-plane. For the characterization of performance, e.g. the ratio $\tan \alpha$ of the relative losses and power density of a design can be employed (cf. [39]); an analogous, but purely mathematical characterization is described in [6].

References

[1] M. M. Jovanović, "Power supply technology - past, present and future," in *Proc. of the Power Conversion and Intelligent Motion Conf. (PCIM China)*, Shanghai, China, Mar. 2007, pp. 3–15.

[2] B. Sahan, S. V. Araújo, C. Nöding, and P. Zacharias, "Comparative evaluation of three-phase current source inverters for grid interfacing of distributed and renewable energy systems," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2304–2318, Aug. 2011.

[3] A. Falk, M. Meinhardt, and V. Wachenfeld, "Efficiency and grid compatibility of photovoltaic inverters - state-of-the-art and future trends," in *Proc. of the Power Conversion and Intelligent Motion Conf. (PCIM Europe)*, Nuremberg, Germany, May 2009, pp. 14–20.

[4] R. Mallwitz and B. Engel, "Solar power inverters," in *Proc. of the 6th Int. Conf. on Integrated Power Electronic Systems (CIPS)*, Nuremberg, Germany, Mar. 2010, pp. 237–244.

[5] J. W. Kolar, J. Biela, and J. Miniböck, "Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency vs. 7kW/dm³ power density," in *Proc. of the 6th IEEE Int. Power Electronics and Motion Control Conf. (IPEMC)*, Wuhan, China, May 2009, pp. 1–21.

[6] M. März, "Parasitics in power electronics," in *Proc. of the ECPE Workshop "Future Trends for Power Semiconductors"*, Zurich, Switzerland, Jan. 2012.

[7] I.-J. Kim, S. Matsumoto, T. Sakai, and T. Yachi, "New power device figure of merit for high-frequency applications," in *Proc. of the 7th Int. Symp. on Power Semiconductor Devices and ICs (ISPSD)*, Yokohama, Japan, May 1995, pp. 309–314.

[8] F. Krismer, "Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies," Ph.D. dissertation, Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, 2010.

[9] L. Huber, Y. Jang, and M. M. Jovanović, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.

[10] C. Wang, M. Xu, F. C. Lee, and Z. Luo, "Light load efficiency improvement for multi-channel PFC," in *Proc. of the IEEE Power Electronics Specialists Conf. (PESC)*, Rhodes, Greece, Jun. 2008, pp. 4080–4085.

[11] M. Albach, "An AC-DC converter with low mains current distortion and minimized conducted emissions," in *Proc. of the 3rd European Conf. on Power Electronics and Applications (EPE)*, Aachen, Germany, Oct. 1989, pp. 457–460.

[12] ——, "Induktive Komponenten in der Leistungselektronik (in German)," in *6. ETG-Fachtagung - Bauelemente der Leistungselektronik und ihre Anwendungen*, Bad Nauheim, Germany, Apr. 1989.

[13] H. van der Broeck, K. Löhn, F. Chevalier, H. Dethienne, and W. Lemmens, "A compact high performance 300 W/5 V switched mode power supply," in *Proc. of the 3rd European Conf. on Power Electronics and Applications (EPE)*, Aachen, Germany, Oct. 1989, pp. 1455–1459.

[14] M. L. Heldwein, "EMC filtering of three-phase PWM converters," Ph.D. dissertation, Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, 2008.

[15] M. März, A. Schletz, B. Eckardt, S. Egelkraut, and H. Rauh, "Power

electronics system integration for electric and hybrid vehicles," in *Proc. of the 6th Int. Conf. on Integrated Power Electronic Systems (CIPS)*, Nuremberg, Germany, Mar. 2010, pp. 227–236.

[16] A. Nagel, "Leitungsgebundene Störungen in der Leistungselektronik: Entstehung, Ausbreitung und Filterung. (in German)," Ph.D. dissertation, RWTH Aachen University, Germany, 1988.

[17] Y. Jang and M. M. Jovanović, "Light-load efficiency optimization method," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 67–74, Jan. 2010.

[18] J. Biela, D. Hassler, J. Miniböck, and J. W. Kolar, "Optimal design of a 5 kW/dm^3 / 98.3% efficient TCM resonant transition single-phase PFC rectifier," in *Proc. of the IEEE Int. Power Electronics Conf. (IPEC-ECCE Asia)*, Sapporo, Japan, Jun. 2010, pp. 1709–1716.

[19] M. Vasic, S. D. Round, J. Biela, and J. W. Kolar, "Mission profile based optimization of a synchronous-buck DC-DC converter for a wearable power system," in *Proc. of the 6th IEEE Int. Power Electronics and Motion Control Conf. (IPEMC)*, Wuhan, China, May 2009, pp. 1384–1389.

[20] B. A. Miwa, D. M. Otten, and M. E. Schlecht, "High efficiency power factor correction using interleaving techniques," in *Proc. of the 7th Annual IEEE Applied Power Electronics Conf. and Exposition (APEC)*, Boston, MA, USA, Feb. 1992, pp. 557–568.

[21] O. Garcia, P. Alou, J. A. Oliver, P. Zumel, and J. A. Cobos, "A high number of phases enables high frequency techniques and a better thermal management in medium power converters," in *Proc. of the 5th Int. Conf. on Integrated Power Electronic Systems (CIPS)*, Nuremberg, Germany, Mar. 2008, pp. 281–284.

[22] Q. Li, F. C. Lee, M. Xu, and C. Wang, "Light load efficiency improvement for PFC," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, San Jose, CA, USA, Sep. 2009, pp. 3755–3760.

[23] D. Maksimović and S. Ćuk, "Constant-frequency control of quasi-resonant converters," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 141–150, Jan. 1991.

[24] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. John Wiley & Sons, Inc., 2003.

[25] S. Waffler, "Hochkompakter bidirektionaler DC-DC-Wandler für Hybridfahrzeuge (in German)," Ph.D. dissertation, Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, 2011.

[26] E. Bataller-Planes, N. Lapea-Rey, J. Mosquera, F. Orti, J. A. Oliver, O. Garcia, F. Moreno, J. Portilla, Y. Torroja, M. Vasic, S. C. Huerta, M. Trocki, P. Zumel, and J. A. Cobos, "Power balance of a hybrid power source in a power plant for a small propulsion aircraft," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2856–2866, Dec. 2009.

[27] R. M. Button, "An advanced photovoltaic array regulator module," in *Proc. of the 31st Intersociety Energy Conversion Engineering Conf. (IECEC)*, vol. 1, Washington, D.C., USA, Aug. 1996, pp. 519–524.

[28] J. H. R. Enslin and D. B. Snyman, "Combined low-cost, high-efficient inverter, peak power tracker and regulator for PV applications," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 73–82, Jan. 1991.

[29] Y. Ren, M. Xu, G. Yao, Y. Meng, and F. C. Lee, "A novel simple and high efficiency "DC/DC transformer"," in *Proc. of the CPES Seminar*, Blacksburg, VA, USA, Apr. 2002, pp. 173–177.

[30] Y. Jang, M. M. Jovanović, and D. L. Dillman, "Hold-up time extension circuit with integrated magnetics," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 394–400, Mar. 2006.

[31] J. W. Kolar, R. S. Wieser, and H. Ertl, "Analysis of a wide speed range starter/alternator system based on a novel converter topology for series/parallel stator winding configuration," in *Proc. of the 34th IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 4, Phoenix, AZ, USA, Oct. 1999, pp. 2631–2641.

[32] P. Sun, L. Zhou, and K. M. Smedley, "A reconfigurable structure DC–DC converter with wide output range and constant peak power," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2925–2935, Oct. 2011.

[33] D. Christen, U. Badstübner, J. Biela, and J. W. Kolar, "Calorimetric power loss measurement for highly efficient converters," in *Proc. of the IEEE Int. Power Electronics Conf. (IPEC-ECCE Asia)*, Sapporo, Japan, Jun. 2010, pp. 1438–1445.

[34] Enertronics GmbH. [Online]. Available: www.enertronics.ch.

[35] Y. Jang and M. M. Jovanović, "A bridgeless PFC boost rectifier with optimized magnetic utilization," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 85–93, Jan. 2009.

[36] F. Musavi, W. Eberle, and W. G. Dunford, "A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1833–1843, Jul./Aug. 2011.

[37] F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies," *IEEE Trans. Smart Grid*, vol. 3, no. 1, pp. 413–421, Mar. 2012.

[38] G. Deboy and D. Chiola, "Trends und Herausforderungen bei IGBTs und Superjunction-Bauelementen (in German)," in *6. ETG-Fachtagung - Bauelemente der Leistungselektronik und ihre Anwendungen*, Bad Nauheim, Germany, Apr. 2011.

[39] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstübner, "Performance trends and limitations of power electronic systems," in *Proc. of the 6th Int. Conf. on Integrated Power Electronic Systems (CIPS)*, Nuremberg, Germany, Mar. 2010, pp. 17–36.