# High-Efficiency Transcutaneous Energy Transfer for Implantable Mechanical Heart Support Systems

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*Abstract*—Inductive power transfer technology is a promising solution for powering implantable mechanical circulatory support systems, due to the elimination of the percutaneous driveline, which is still the major cause of severe infections. However, at the present time, no transcutaneous energy transfer (TET) system is commercially available and ready for long-term use. Specifically, the heating of the tissue due to power losses in the TET coils and the implanted electronic components are a major problem. The focus of this paper is, therefore, on the design and realization of a highly efficient TET system and the minimization of the power losses in the implanted circuits in particular. Parameter sweeps are performed in order to find the optimal energy transmission coil parameters. In addition, simple and meaningful design equations for optimal load matching are presented together with a detailed mathematical model of the power electronic stages. To achieve highest efficiencies, a high-frequency self-driven synchronous rectifier circuit with minimized volume is developed. Extensive measurements are carried out to validate the mathematical models and to characterize the performance of the prototype system. The optimized system is capable of transmitting 30 W of power with an efficiency greater than 95 %, even at a coil separation distance of 20 mm (0.79 in) and 70 mm (2.76 in) coil diameter.

*Index Terms*—Gallium–Nitride field effect transistor (FET), inductive power transfer (IPT), power loss modeling, resonant converter, synchronous rectifier, transcutaneous energy transfer (TET).

## I. INTRODUCTION

IN the industrial nations, an ever-growing number of people suffer from severe heart failure. At the end stage, a heart transplantation is the only curative treatment. However, the availability of suitable donor hearts is very limited. This trend promotes the development of mechanical circulatory support systems (MCSS), such as left ventricular assist devices (LVADs). Recent progress in the development of continuous flow LVADs, which are smaller in volume and of lower mechanical complexity than early developments, make a fully implantable solution the next logical step in the optimization of MCSS [1]. The idea of powering an artificial heart via an inductively coupled resonator originated in 1960 [2]. Nevertheless, in today's MCSS, the power supply is still connected to the blood pump via a percutaneous driveline, which is responsible for the majority of device-related infections [3]. There are
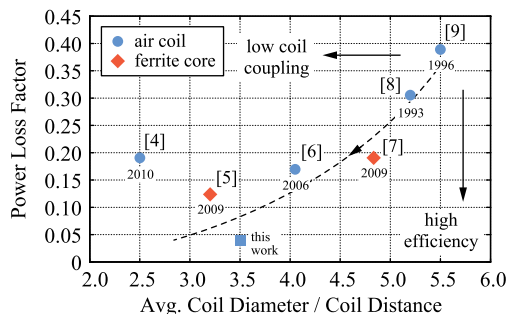
Fig. 1. Comparison of the power loss factor ($\lambda = P_{\text{loss}}/P_{\text{out}}$) and the average coil diameter divided by the coil distance of several TET systems found in the literature at the highest reported coil separation distance in each case. The rectangular marker highlights the system performance reported in this paper.

several developments of transcutaneous energy transfer (TET) systems reported in the literature. However, a direct comparison of the TET systems is difficult because the operating conditions, the used components and materials, as well as coil sizes vary greatly. Nevertheless, the power loss factor defined by $\lambda = P_{\text{loss}}/P_{\text{out}}$ and the average coil diameter divided by the coil distance are good measures to estimate the TET system performance. Fig. 1 shows the performance measures of the TET systems described in [4]–[9] evaluated at the largest reported coil separation distance in each case. Even though the systems differ in many aspects, there is a trend visible toward higher system efficiency at low couplings, which is mainly due to the design of high-quality inductive power transfer (IPT) coils and improved power electronic circuits. But even though TET systems have been successfully tested in a small number of patients [10], there are several unresolved problems and further technological improvements are needed to enhance the reliability and safety of this technology. In response to the limitations of existing technology, the Zurich Heart Project was founded in 2013 as a collaboration of the ETH Zurich, the University of Zurich, and the University Hospital of Zurich, supported by Hochschulmedizin Zürich. The aim of the project is to develop new circulatory support devices and to optimize existing technology, including the development of a TET system and to make improvements in particular with respect to reliability and robustness, as well as thermal management. Hence, this paper describes the efficiency optimization/loss minimization of the wireless energy transmission system and the development of a prototype TET system. In Section II, the concept of a fully implantable MCSS is introduced and the main challenges associated with the TET system are outlined. The design and the optimization of the energy transmission coils require good knowledge of the resonant converter they are operated in. Therefore, in Section III,
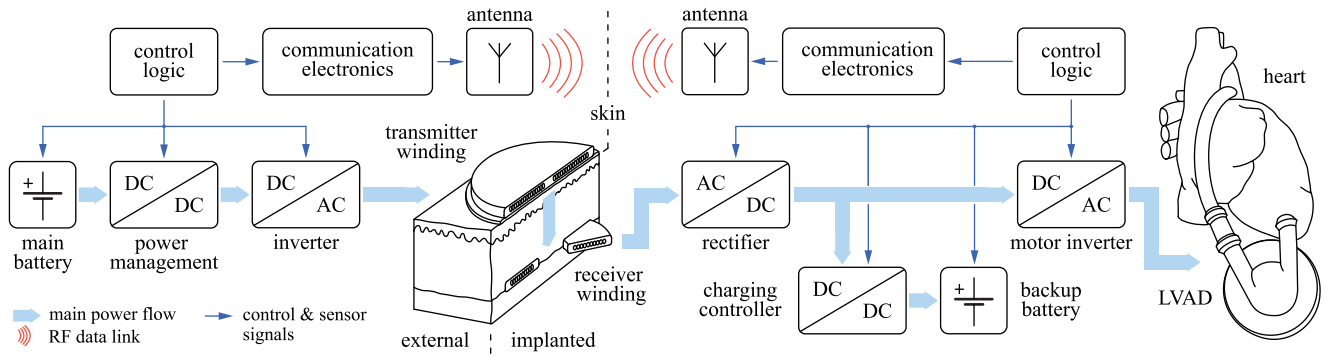
Fig. 2.    Schematic concept of a fully implantable MCSS.

the electrical characteristics of the proposed converter topology are presented in detail, where a simplified equivalent circuit model is used to derive analytical design equations. In addition, the coil design and optimization process are outlined. In Section IV, a more detailed model of the system is developed including an accurate power loss model of the power electronic circuits, which is the basis for further system optimization. To validate the theoretical considerations, a hardware prototype of the TET system is realized and is shown in Section V. In order to improve the TET system performance even further, a self-driven synchronous rectifier is developed and presented in Section VI. Finally, a discussion of the obtained results is given in Section VII.

## II. SYSTEM OVERVIEW AND DESIGN CHALLENGES

A fully implantable MCSS employs four key parts, which are the TET system, the control and communication electronics, the internal battery backup, and the blood pump itself. A detailed illustration of the system concept is given in Fig. 2. An external battery pack provides the main power supply to operate the LVAD. An inverter circuit as part of the TET system supplies the transmitter coil winding, which is placed in close proximity to the surface of the skin. The energy is transferred by electromagnetic induction to the receiver winding, which is implanted underneath the skin. On the secondary side, the induced ac voltage is rectified to a dc voltage and is applied to the motor inverter driving the LVAD.

An internal battery backup permits a fully untethered operation of the LVAD and facilitates activities that demand increased mobility of the patient. Today's implantable lithium–ion batteries provide energy densities of up to 255 W/l [11]. Accordingly, with a battery volume of about 8 cl and an average power consumption of approximately 7 W, the blood pump could be operated independently for 1−2 h, depending on the allowed depth of discharge. A charging controller supplies the internal lithium–ion battery and provides fast control of the battery voltage.

Furthermore, a wireless communication channel is used to enable feedback control of the power transferred through the skin and to transmit monitoring data. There are several options reported in literature on how to implement the wireless data

transmission, such as radio frequency communication [12] or simultaneous energy and data transmission with the IPT coils [13]. Another possibility to control the transferred energy is to estimate the coil coupling and the system output voltage from the measurement of the primary side operating conditions as it is reported in [14] or by the direct control of the received amount of power on the secondary side [15]. In both cases, an additional data channel would be needed for the transmission of the monitoring data. However, the decoupled control of the energy transmission system would relax the requirements on the wireless communication significantly.

There are two main challenges associated with the operation of a TET system. First, the coupling of the two energy transmission coils is low and can vary greatly during operation, since the position of the coils can vary with movements of the patient. Additionally, the data transfer rate of the wireless communication is limited and there is the possibility of a failure within the communication channel itself. Nevertheless, a tight control of the TET system's output voltage is mandatory for a reliable operation of the implanted system. It is, therefore, proposed to include an additional dc–dc converter as interface to the implanted battery to relax the constraints on the control of the TET system and to protect the battery from unpredictable changes in the operating conditions.

Second, the power loss in the transmission system must be sufficiently low to keep the heat dissipation inside the body within safe limits. The nominal power requirements for the TET system powering a LVAD is in the range of 8–12 W [1]. However, for the additional charging of the implanted battery and some added margin, a total power delivery of 25–30 W is required. Specifically in a full load condition, excessive heat generation can lead to permanent tissue damage. The minimization of the secondary side power loss is, therefore, one of the main objectives in the optimization process of the TET system, which is the focus of the subsequent sections.

## III. IPT SYSTEM DESIGN

The selection of the converter topology of the IPT system has a major influence on the design of the energy transfer coils and it also determines the distribution of the power losses within the TET system. The main challenge in the design of IPT systems
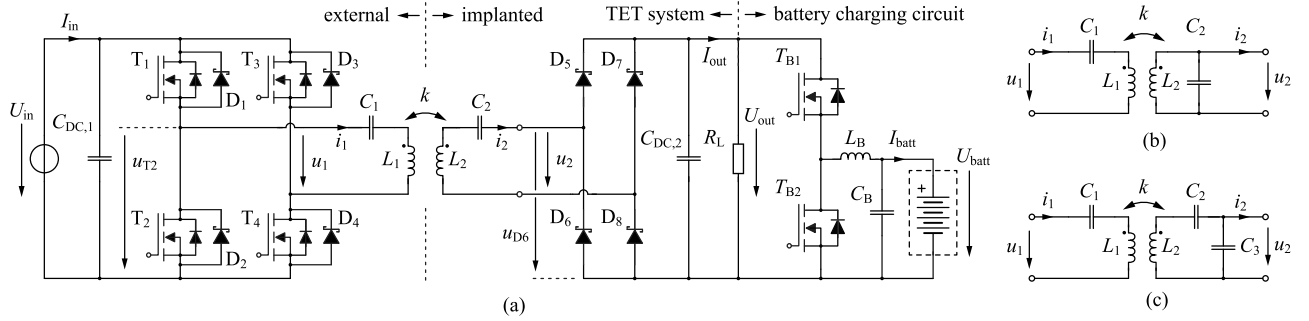
Fig. 3.  (a) Proposed series–series resonant converter topology of the TET system and the charging controller of the implanted battery. The motor inverter and the blood pump are modeled as a single load resistor $R_L$. (b)–(c) They  show two other secondary side compensation methods for the resonant circuit.

is the low magnetic coupling of the energy transmission coils. In order to increase the efficiency, the IPT coils are operated in a resonant converter topology, including capacitors on the primary and secondary side for the compensation of the large stray inductance.

In a preliminary step, four promising topologies, known from previous literature [5], [16]–[21], the series-series (SS), series–parallel (SP) and the series-series-parallel (SSP) compensation as well as the SS compensated topology operated at conditions for load independent unity voltage gain (SSU) were studied and compared regarding their transfer characteristics and specifically regarding the secondary side power losses. The resonant converter topologies are shown in Fig. 3(a)–(c). The main disadvantage of the parallel compensated topologies is the constant power loss due the reactive power circulating within the resonant circuit even at light load conditions. This is specifically undesired on the secondary side of the TET system due to the heating of the skin and since the TET system will be mainly operated in a partial load condition, where only the power for the blood pump has to be transferred. The SS compensated systems in contrast, operated at constant output voltage, exhibit a behavior, where the secondary side resonant peak current is decreasing at the rate of the output power. It is, therefore, proposed to use a SS compensated topology for the TET system, even though the required receiver coil inductance is typically of larger value compared to a SP compensated topology with the same voltage transfer ratio and matching of the secondary side inductor to the maximum load [22]. However, a reduction of the receiver coil size is only of partial advantage. A larger coil geometry allows for higher inductances and higher quality factors [cf., [23], Fig. 4(a)]. As a result, the losses within the coils are reduced and spread over a larger surface, which simplifies the cooling. Additionally, higher coupling factors between primary and secondary side coil can be achieved with an increased tolerance to misalignment. According to cardiology specialists of the University Hospital of Zurich, the maximum feasible coil diameter is about 70 mm (2.76 in), which is used as a geometric limitation in the coil optimization.

In the subsequent sections, the design of the TET system is described. First, in order to find the optimal coil parameters and the compensation capacitors, design equations are derived using a simplified equivalent model of the system. Second, the coil

optimization process, which is described in detail in [23], will be explained briefly.

### A.  IPT System Characteristics

The basic topology of the prototype TET system considered in this paper is shown in Fig. 3(a). The series resonant primary side is supplied by a full-bridge inverter. On the secondary side, as a first step, a full-wave rectifier is used to convert the ac voltage into a dc output voltage. The blood pump and the motor inverter are modeled as resistive load $R_L$, which is connected in parallel to the output of the TET system and the charging controller of the backup battery. The charging controller consists of a buck-type converter with synchronous rectification in order to allow for bidirectional power flow, and is used to step down the TET system output voltage to a nominal battery voltage of $U_{batt} = 14.4\,V$.

The voltage transfer characteristics and the phase angle of the input impedance of the SS compensated system described in this paper are shown in Fig. 4(a)–(b) with respect to frequency and for variable load conditions and coupling factors. The peak gain resonance frequency of the system is at $f_r = f_0\sqrt{1 - k_0}$ and is below the operating frequency $f_0$, which is known as operating point with load independent voltage gain and is explained in detail in [5], [17], and [20]. In order to operate the system at this specific operating point, the compensation capacitors have to be chosen as

$$C_1 = \frac{1}{\omega_0^2 L_1 (1 - k_0)} \quad \text{and} \quad C_2 = \frac{1}{\omega_0^2 L_2 (1 - k_0)} \qquad (1)$$

where $\omega_0$ is the angular operating frequency and $L_1$ and $L_2$ are the primary and secondary coil self-inductances, respectively. The design variable $k_0$ is the coupling at which the system will exhibit a load independent voltage gain at the operating frequency $f_0$, and will be determined during the further design process. The actual coupling factor $k$ can potentially have any value in the range of 0 to 1, and could substantially differ from the value of $k_0$.

Neglecting the parasitic resistances in the resonant system, the absolute value of the voltage transfer ratio at the operating
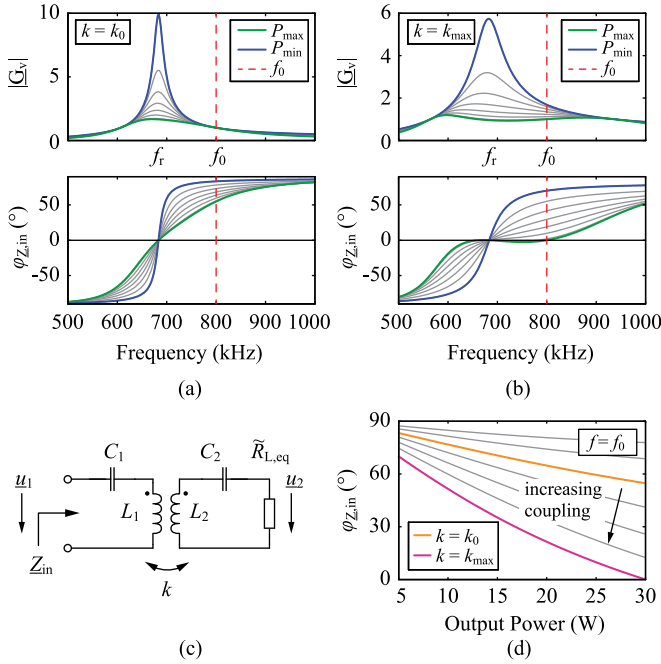
Fig. 4. (a)–(b) Calculated voltage transfer characteristics and phase angle of the input impedance of the prototype SS resonant energy transmission system described in Section V, using the simplified equivalent circuit of the resonant system shown in (c). (d) Phase angle of the input impedance at variable output power and coil coupling factor.

frequency $f_0$ and at a coupling $k_0$ can be calculated as

$$|\underline{G}_v| = \left| \frac{\underline{u}_2}{\underline{u}_1} \right| = \sqrt{\frac{L_2}{L_1}} \tag{2}$$

which is unity if the primary and secondary side coils are of equal inductance value, and is referred to as SSU operation. Note that with a fixed operating frequency $f_0$, the load independent voltage gain can only be achieved at the design coupling $k_0$. As the coupling $k$ increases, the point of load independent voltage gain will move toward higher frequencies.

It was shown in [21], [22] and [24] that the energy transmission efficiency of an IPT system is a maximum, if the load is matched to the secondary side inductance. Using a similar analysis, the transmission efficiency of the considered system at the operating frequency $\omega_0$ can be calculated as

$$\eta_0 = \frac{\gamma_0 k^2 Q_1 Q_2^2}{1 + Q_2 \left( 2\gamma_0 + k^2 Q_1 + (\gamma_0^2 + k_0^2 + \gamma_0 k^2 Q_1) Q_2 \right)} \tag{3}$$

where $\gamma_0 = \frac{\tilde{R}_{L,eq}}{\omega_0 L_2}$ denotes the load factor and $Q_1$ and $Q_2$ are the quality factors of the primary and secondary side coils respectively. According to [25], the simplified equivalent load $\tilde{R}_{L,eq}$ is used to model the actual load together with the full-wave rectifier

$$\tilde{R}_{L,eq} = \frac{8}{\pi^2} \frac{U_{out}^2}{P_{out}}. \tag{4}$$

Later, in Section IV, an extended load model is presented which also accounts for parasitics in the rectifier circuit and will be used for the derivation of the power loss model. However, the simplified load model is a good approximation of the circuit and

provides meaningful and simple design equations which will be given in the following.

Using (3), the maximum efficiency of the resonant system can be found by matching the load to the secondary side coil and can be described by the optimal load factor $\gamma_{opt}$

$$\gamma_{opt} = \frac{\tilde{R}_{L,eq}}{\omega_0 L_{2,opt}} = \frac{1}{Q_2} \sqrt{1 + k^2 Q_1 Q_2 + (k_0 Q_2)^2}. \tag{5}$$

If both, $Q_1$ and $Q_2$ are large (e.g., $Q > 200$), the optimal load factor can be approximated by

$$\gamma_{opt} \approx \sqrt{k^2 + k_0^2}. \tag{6}$$

Using (4)–(6), at full load operation and at the coupling $k = k_0$, the optimal secondary side inductance can be found as

$$L_{2,opt} = \frac{8}{\pi^2} \cdot \frac{U_{out}^2}{\sqrt{2}\omega_0 k_0 P_{out,max}} \tag{7}$$

which is referred to as load matching condition.

Since the resonant circuit is supplied by a full-bridge inverter using field effect transistors (FETs), which exhibit a finite output capacitance, the input impedance and/or the current phase angle of the resonant network seen by the inverter has a significant influence on the losses generated within the inverter itself. In order to achieve soft-switching, i.e., zero voltage switching (ZVS) of the inverter switches, the input impedance of the resonant circuit must exhibit an inductive behavior. Using the simplified equivalent circuit shown in Fig. 4(c), the phase angle of the input impedance at the coupling $k_0$ and operating frequency $f_0$ can be calculated as

$$\varphi_{\underline{Z},in} = \arccos \left( \frac{k_0 \omega_0 L_2}{\sqrt{\tilde{R}_{L,eq}^2 + k_0^2 L_2^2 \omega_0^2}} \right). \tag{8}$$

Note that, under these operating conditions, the phase angle is independent of the primary side coil inductance $L_1$. If the maximum load is matched to the secondary side coil at the coupling $k = k_0$, the phase angle becomes

$$\varphi_{\underline{Z},in} = \arccos \left( \frac{1}{\sqrt{3}} \right) = 54.7°. \tag{9}$$

If the resonant system is designed for load matching at $k_0$, but during operation $k \neq k_0$, then the phase angle of the input impedance is equal to

$$\varphi_{\underline{Z},in} = \arccos \left( \sqrt{\frac{2}{3}} \frac{k^2}{\sqrt{k^4 - 2k^2 k_0^2 + 3k_0^4}} \right). \tag{10}$$

The characteristic of the phase angle of the input impedance at the operating frequency $f_0$ is shown in Fig. 4(d). The phase angle of the input impedance decreases with increasing coupling coefficient and increasing output power. In order to ensure that the phase angle is still positive at maximum load, the system has to be designed for a coupling $k_0$ chosen as

$$k_0 \leq \frac{k_{max}}{\sqrt{3}} \tag{11}$$

where $k_{max}$ is the maximum achievable coupling with the system at hand. Given the coil geometry and the minimum coil

distance, $k_{\max}$ can be determined by experiment or simulation. The secondary side inductance $L_2$ is determined for load matching at $k_0$ using (7) and (11), given the operating conditions. Finally, the required compensation capacitances and the primary side inductance can be determined with (1) and (2).

In order to validate the theoretical results shown in this section, the prototype system presented in Section V was designed such that the phase angle of the input impedance is zero at maximum coupling and maximum output power. However, this means that under this operating condition, soft-switching is lost. Therefore, in a practical design, depending on the switches used in the inverter circuit, the coupling $k_0$ must be chosen with some margin, such that the phase angle of the input impedance is high enough and the primary side resonant current $i_1$ provides sufficient charge to ensure soft-switching.

### B. Coil Design and Optimization

It was shown in previous publications that the theoretical maximum achievable efficiency of an IPT system is determined by the coupling factor and the quality factors of the inductors $\eta \approx 1 - 2/(k\sqrt{Q_1 Q_2})$ [24]. Therefore, the product $kQ$, i.e., $Q = \sqrt{Q_1 Q_2}$, is the figure-of-merit (FOM) for the efficiency, which must be maximized to achieve a high energy transmission efficiency.

For the coil geometry, it was shown in [22] that a circular coil geometry leads to the highest coupling factor compared to other coil geometries like rectangular or square shaped coils with the same enclosed area. Therefore, flat circular coils with only one layer of litz wire winding are used to achieve also a low profile and a high mechanical flexibility, which is in particular needed for the implanted receiver coil. Even though additional magnetic material could be used in the coil design to improve the coupling factor, it would also limit the mechanical flexibility of the coils and increase the coil volume. It was, therefore, decided to omit any additional magnetic material in the coil design.

The coil optimization process is based on the estimation of the coil losses and the coupling factor and was performed based on parameter sweeps using both FE simulation and analytical models. It was shown in in the previous section that the primary and secondary side coils must have the same inductance value to achieve unity voltage gain at the matched loading. Therefore, the primary and secondary side coils are designed with equal winding configuration and geometry. The litz-wire was chosen from commercially available wires with strand diameters $d_i$ ranging from 32 to 71 μm (AWG 48 to 41) and a number of strands ranging from 200 to 420. The outside coil radius $R_a$ was chosen between 25 and 35 mm (0.98 and 1.38 in) and for the coil separation distance $d_c$, a range of 10 to 25 mm (0.39 to 0.98 in) was specified in discussion with medical experts.

In order to compute the coil quality factor, the ac losses of the coils must be determined. The loss components can be divided into dc, skin-, and proximity-effect losses. With the considered strand diameters, the skin-effect losses can be eliminated within the considered frequency range of 100 kHz–1.5 MHz. Hence, only the proximity-effect losses contribute to the frequency-dependent part of the total losses. In order to calculate the
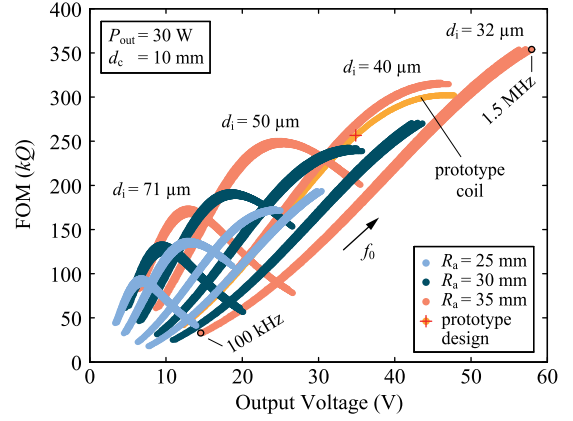


Fig. 5. Coil designs with the largest figuer-of-merit (FOM = $kQ$) at minimum coil separation distance with respect to the TET output voltage for load matching at maximum output power. Additionally, the FOM of the prototype coil and the operating point according to the specifications given in Section V, Table I(c) are indicated.

ac resistance of each coil design, the coils are simulated at a fixed frequency and the peak magnetic field is extracted in each conductor to calculate the proximity-effect losses. Given the field distribution and the peak current in each coil, the ac resistance can be extrapolated with good accuracy for the considered frequency range, using the analytical loss model for litz-wire windings described in [26]. In parallel, the magnetic coupling between two equal coils was computed for all combinations of coil geometries and coil separation distances. The influence of the living tissue on the coil coupling factor can be neglected since the magnetic field distribution is barely disturbed by the tissue due to its low conductivity [27] and the relative permeability close to 1.

Given the quality factor and the achievable coupling factors of each design, the optimal output voltage of the IPT system can be computed from (5). For a load matching at maximum power output and coupling $k_0$, the optimal output voltage is

$$U_{\text{out,opt}} = \frac{\left(2k_0^2 Q'^2 + 1\right)^{1/4} \cdot \pi \sqrt{2P_{\text{out,max}}\omega_0 L'}}{4\sqrt{Q'}} \quad (12)$$

where $L' = L_1 = L_2$ and $Q' = Q_1 = Q_2$ are used. With the approximation (6), this simplifies to

$$U_{\text{out,opt}} = \frac{2^{3/4}}{4}\pi\sqrt{k_0\omega_0 L_2 P_{\text{out,max}}} \,. \quad (13)$$

Fig. 5 shows the FOM of the coil designs that provide the highest quality factor at a certain operating frequency, with respect to the optimal output voltage, calculated with (12), and designed for a coupling $k_0$, according to (11). The individual designs are colored according to the outside coil radius. As expected, the designs using the smallest strand diameter and the largest outside coil diameter have the highest FOM.

In order to find the optimal coil design and electrical operating conditions, the total secondary side losses are calculated for each coil design with maximum FOM. In addition, as described in [23], a thermal simulation model of the coils and the human skin was used to identify the feasible designs. The
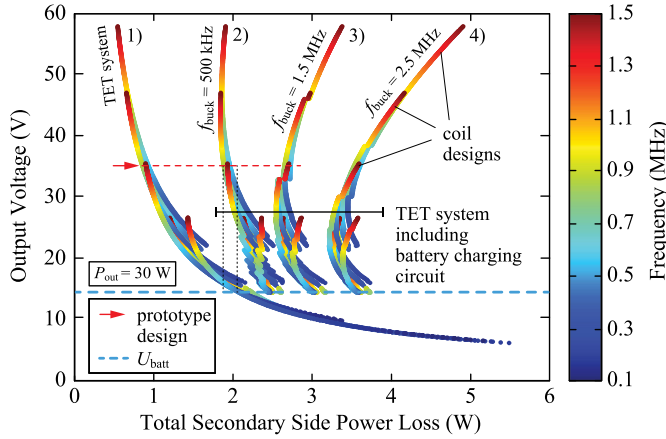
Fig. 6.   Optimal TET output voltage for the coil designs with highest FOM with respect to the total secondary side power losses, excluding designs that violate the thermal limit on the receiver coil temperature found in [23]. The trajectories in 1) do not include the battery charging controller and describe only the secondary side power losses of the TET system. 2)–4) show the losses including the battery charging controller, operated at a switching frequency of 500 kHz, 1.5 MHz and 2.5 MHz. The indicated coil designs are colored according to the switching frequency of the primary side inverter circuit.

calculations include the losses in the receiver coil, the diode rectifier, and the losses generated within the battery charging controller. For this purpose, a detailed mathematical power loss model of the synchronous buck converter was created, including the switching losses of the gallium nitride FETs (EPC2016), which are used in the inverter circuit of the prototype system as well.

In Fig. 6, the coil designs are shown for the optimal TET system output voltage as a function of the total secondary side power losses, colored according to the inverter's operating frequency. 1) shows the total secondary side losses excluding the battery charging controller, while 2)–4) show the total secondary side losses including the buck-type charging controller operated at a switching frequency of 500 kHz, 1.5 MHz, and 2.5 MHz, respectively. The volume occupation and the heating of the tissue due to the rectifier and charging controller are not considered in this analysis and will be the topic of future work. With the designs shown in 1), where the backup battery would be connected directly to the TET system's output, a total secondary side power loss of approximately 2 W will be generated for 14.4 V battery voltage. An even lower secondary side power loss could be achieved, if the TET system is operated at 800 kHz and an output voltage of 35 V, including the battery charging controller operated at a switching frequency of 500 kHz.

As the quality factor of the considered coil designs increases with higher operating frequency and larger coil size, it can be seen that by including the buck converter, and hence allowing for a higher TET output voltage, it is possible to use coil designs with a much higher FOM, than it would be the case at a TET system output voltage of 14.4 V, which results in lower losses within the TET system. The corresponding coil design, indicated in Figs. 5 and 6, was built and is described in detail in Section V.

## IV. POWER LOSS MODELING

In addition to the design of the IPT system, the development of a highly efficient TET system requires a good knowledge of the impacts of the power electronic components and the distribution of the power loss components within the system. While the simplified equivalent IPT circuit model is particularly useful for the design of the resonant tank, a more detailed model has to be developed to accurately estimate the power losses within the realized prototype TET system, where component parasitics cannot be neglected.

### A. Extended Load Model

It was shown in [23] that the parasitic capacitances of the diode rectifier must be considered in order to allow for an accurate calculation of the primary and secondary side currents $i_1$ and $i_2$. The commutation of the current within the rectifier is delayed at the zero crossing of the secondary side current because the parasitic capacitance of the diodes must be either charged or discharged in order to commutate the current to the active branch of the rectifier circuit. During this time interval, there is no net energy supplied to the output of the rectifier that leads to a phase shift between the secondary side current $i_2$ and the fundamental of the rectifier input voltage $u_{2,(1)}$. This is particularly the case if the system is operated at high switching frequencies as it is the case with the prototype TET system. Therefore, the simplified load model given in (16) is extended to account for the rectifier's parasitic capacitances.

According to [28], the load can be modeled as a capacitor in parallel with a resistor as it is shown in Fig. 7(a). In order to obtain the equivalent load capacitance $C_{\text{L,eq}}$, it is necessary to calculate the first harmonic of the rectifier input voltage $u_{2,(1)}$, which requires the knowledge of the duration of the charging interval of the parasitic capacitances of the rectifier diodes, denoted by the angle $\theta_{\text{c,R}}$. The measured voltage and current waveforms of a switching transition of the synchronous rectifier, presented in Section VI, is shown in Fig. 8(a) (which are qualitatively equivalent to the waveforms of the diode rectifier at the secondary side current zero crossing). During the time interval $\theta_{\text{c,R}}$ the net power flow to the output of the rectifier is zero while the parasitic capacitances of the rectifier diodes are charged by the charge denoted as $\Delta Q_1$. As indicated in Fig. 8(b), the current $i_2$ is conducted through the upper and lower branch of the rectifier circuit simultaneously, connecting the parasitic capacitances $C_{\text{p,D5}}$ and $C_{\text{p,D6}}$ in parallel, which are additionally connected in series with the parallel connected capacitances $C_{\text{p,D7}}$ and $C_{\text{p,D8}}$. The nonlinear parasitic diode capacitance of the diodes used for the prototype TET system and the total parasitic capacitance $C_{\text{p,tot}}$ seen at the input of the rectifier circuit are shown in Fig. 8(c). The (linear) charge-equivalent capacitance $C_{\text{Q,eq}}$ [29] given by

$$C_{\text{Q,eq}}(V) = \frac{1}{V} \int_0^V C_{\text{p,tot}}(v_{ds})\,\mathrm{d}v_{ds} \qquad (14)$$
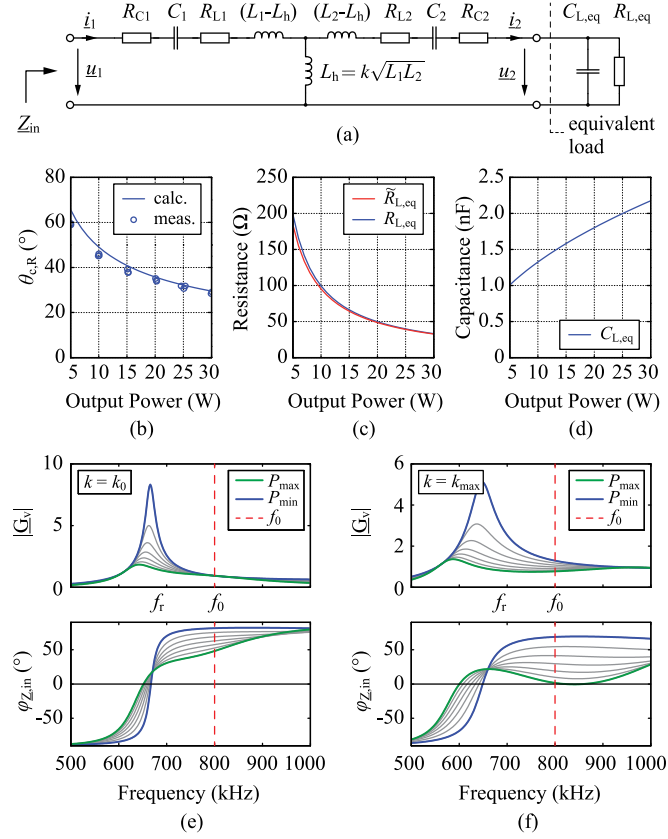
Fig. 7. (a) Detailed equivalent circuit of the resonant tank circuit and the extended load model. (b) Measured and calculated rectifier input voltage transition time interval, expressed as phase angle $\theta_{c,R}$ [cf., Fig. 8(a)]. (c)–(d) Calculated values of the equivalent load capacitance and resistance for the diode rectifier of the prototype TET system. (e)–(f) Voltage transfer characteristics and the phase of the input impedance of the prototype TET system using the extended load model.
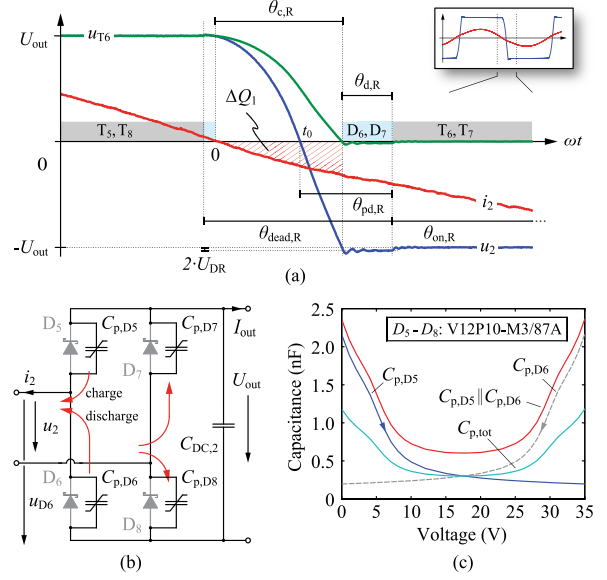


Fig. 8. (a) Measured switching waveforms of the synchronous rectifier input voltage and current including the labeling of the time intervals and terms used for the power loss modeling. (b) Illustration of the current flow during the time interval $\theta_{c,R}$. (c) Nonlinear parasitic capacitance of the rectifier diodes used for the prototype system and the total parasitic capacitance $C_{p,tot}$ seen at the input of the rectifier circuit during the time interval $\theta_{c,R}$.

is used to obtain the time interval $\theta_{c,R}$, which is given by

$$
\theta_{c,R} = \arccos\left(\frac{a_1 - b_1}{a_1 + b_1}\right)
$$

$$
a_1 = (P_{out} + P_{v,R})\,\pi
$$

$$
b_1 = 2U_{out}\omega_0 C_{D,Qeq} \cdot (U_{out} + U_{DR}) \tag{15}
$$

where $C_{D,Qeq}$ is the charge-equivalent capacitance of the total parasitic capacitance $C_{p,tot}$ evaluated at the voltage $V = (U_{out} + U_{DR,0})$, which is equal to the charge-equivalent capacitance of the single parasitic diode capacitance $C_{p,D}$ evaluated at the same voltage, since $C_{p,tot} = 2C_{p,D} \cdot \frac{1}{2}$. $U_{DR}$ is the rectifier diode forward voltage drop at the average output current $I_{out}$. The rectifier power losses $P_{v,R}$ can be calculated iteratively in order to achieve the highest accuracy. Fig. 7(b) shows the calculated and the measured charging time interval for the Schottky diode rectifier used in the prototype system under variable load conditions. Despite the nonlinearity of the diode junction capacitance and the assumption of purely sinusoidal currents in the resonant tank, the calculation fits the measurement with high accuracy.

Following the analysis reported in [28], the first harmonic of the rectifier input voltage $u_{2,(1)}$ can be calculated by means of calculating the first harmonic of the current delivering $\Delta Q_1$ to charge and discharge the parasitic diode capacitances at each zero crossing of the current $i_2$. The equivalent load resistance and the equivalent load capacitance are then found as

$$
R_{L,eq} = \frac{a_2^2 + b_2^2}{2\omega_0^2 C_{D,Qeq}^2 (P_{out} + P_{v,R})} \approx \tilde{R}_{L,eq} \tag{16}
$$

$$
C_{L,eq} = \frac{b_2}{a_2\omega_0 R_{L,eq}} \tag{17}
$$

using

$$
\hat{I}_2 = \frac{2\omega_0 C_{D,Qeq}(U_{out} + U_{DR})}{1 - \cos(\theta_{c,R})}
$$

$$
a_2 = \frac{\hat{I}_2}{\pi}\sin^2(\theta_{c,R})
$$

$$
b_2 = \frac{\hat{I}_2}{\pi}\left[\theta_{c,R} - \frac{1}{2}\sin(2\theta_{c,R})\right]. \tag{18}
$$

The calculated values of the extended load model are shown in Fig. 7(c)–(d) for the prototype system. It can be seen in Fig. 7(c) that the simple equivalent load resistor model given in (4) is still valid and a good approximation of the equivalent resistive load. Nevertheless, the equivalent load capacitance shown in Fig. 7(d) is highly dependent on the operating frequency and the output power, and is in the same order of magnitude as the primary and secondary side compensation capacitances. As

a result, the actual TET system's transfer characteristics illustrated in Fig. 7(e)–(f) show the behavior of a SSP compensated system. However, the load dependency of the phase angle of the input impedance does not change significantly at the operating frequency $f_0$, which justifies the use of the simple model to design the resonant tank.

The extended load model allows for an accurate calculation of the power loss components in the TET system as will be shown in the following.

### B. Diode Rectifier Losses

Using (15) and (18), the power loss of the full-wave diode rectifier can be calculated with

$$P_{v,R} = 2 \cdot \left( \frac{P_{out}}{U_{out}} U_{DR,0} + I_{2,RMS}^2 R_{DR,0} \right) \tag{19}$$

and

$$I_{2,RMS}^2 = \frac{\hat{I}_2^2}{2\pi} \cdot \left( \frac{1}{2} \sin(2\theta_{c,R}) - \theta_{c,R} + \pi \right) \tag{20}$$

where a simple rectifier diode model with the equivalent zero current diode forward voltage drop of $U_{DR,0}$ in series with the diode's differential resistance $R_{DR,0}$, both evaluated at the average output current $I_{out}$, is used.

### C. Resonant Tank Circuit Losses

The equivalent circuit of the resonant tank circuit is shown in Fig. 7(a) and is used to calculate the phase of the input impedance $\varphi_{Z,in}$ and the primary side current $i_1$. The parasitic resistances $R_{L1}$ and $R_{L2}$ of the energy transmission coils can be measured at the operating frequency or calculated using FE analysis and analytical models as it is explained in [26]. Assuming sinusoidal primary and secondary side currents $i_1$ and $i_2$, the total resonant tank circuit losses are given by

$$P_{v,Res} = \frac{\hat{I}_1^2}{2}(R_{L1} + R_{C1}) + \frac{\hat{I}_2^2}{2}(R_{L2} + R_{C2}). \tag{21}$$

The equivalent series resistances (ESR) $R_{C1}$ and $R_{C2}$ of the compensation capacitors are negligible in most of the cases, where multiple high-quality ceramic capacitors are used in parallel to build up the needed compensation capacitance.

### D. Inverter Losses

There are basically four loss mechanisms associated with the inverter circuit. These are the losses caused by the gate driver, the on-state and body diode conduction losses, as well as the switching losses. The occurrence of the last three loss mechanisms depends highly on the impedance $\underline{Z}_{in}$ seen by the inverter, and therefore, on the load conditions and the coil coupling coefficient.

Concerning the power losses, there exist two distinct operating modes of the inverter. During nominal operation, the inverter is operated with an inductive load such that the current $i_1$ is lagging the inverter's output voltage $u_1$. A measurement of the inverter switching waveforms for this particular operating mode is shown in Fig. 9(a). At the time instant, where the switches

$T_1$ and $T_4$ are turned off, the primary side current $i_1$ starts to discharge the parasitic output capacitance of the switches $T_2$ and $T_3$, while the capacitances of the switches $T_1$ and $T_4$ are charged. In this case, the charge $\Delta Q_2$ is large enough to discharge and charge the capacitances before the end of the deadtime interval denoted by $\theta_{dead,T}$. As soon as the voltage across the switch $T_2$ reaches zero, it is clamped by its body diode. Subsequently, the primary side current $i_1$ is conducted by the diodes $D_2$ and $D_3$ until the switches $T_2$ and $T_3$ are turned on at almost zero voltage. This operating mode is referred to as ZVS operation. The turn-off process of the switches $T_1$ and $T_4$ is lossless as long as the switches are turned off fast enough, such that the gate voltage is below the FET's threshold voltage before the voltage across the switch increases. Conduction losses are generated both during the body diode conduction interval $\theta_{d,T}$ and during the on-time interval of the switch due to the diode forward voltage drop and the on-state resistance of the switch, respectively.

The switching waveforms of the second operating mode are shown in Fig. 9(b). In this case, the charge $\Delta Q_2$ provided by inverter's output current $i_1$ is not large enough to completely discharge the parasitic output capacitances of the switches $T_2$ and $T_3$ before the end of the deadtime interval and the switches will turn on at a finite voltage $U_{s,0}$. In this case, the charge stored in the parasitic output capacitances is dissipated in the switches, which causes significant losses and is referred to as hard-switching operation. It was shown in Section III that this mode of operation can occur at high coupling factors and at high load conditions, where the phase angle of the input impedance is very small.

In order to calculate the total inverter power losses, it is necessary to determine the capacitive charging time interval $\theta_{c,T}$ and $\theta_I$ as well as the input voltage $U_{in}$. Similar to the considerations made in Section IV-A, it is assumed that the charging of the parasitic output capacitance of the switches is lossless and that no net charge is delivered from the power supply to the output of the inverter during this time interval. Furthermore, it is assumed that the primary side current $i_1$ is purely sinusoidal and that the phase angle of the input impedance $\varphi_{Z,in}$ is the same as the phase angle measured from the zero crossing of the primary side current $i_1$ to the zero crossing of the inverter output voltage $u_1$. These two assumptions simplify the calculations significantly, but impose limitations to the model, as the two assumptions show only limited validity at high coupling factors and high output power, where the inverter output current contains distinct higher order harmonic components and the zero crossing of the fundamental component of the voltage $u_1$ deviates from the zero crossing of the inverter output voltage $u_1$.

The input voltage $U_{in}$ can be found using the phase angle of the input impedance and the power delivered to the output of the inverter and is given by

$$U_{in} = \frac{\pi(P_{out} + P_{v,tot})}{2\left(\hat{I}_1 \cos(\varphi_{Z,in}) + \omega_0 C_{T,Qeq} U_{DT}\right)} \tag{22}$$

where $P_{v,tot}$ is the total TET system power loss and must be computed iteratively. The capacitance $C_{T,Qeq}$ is the charge
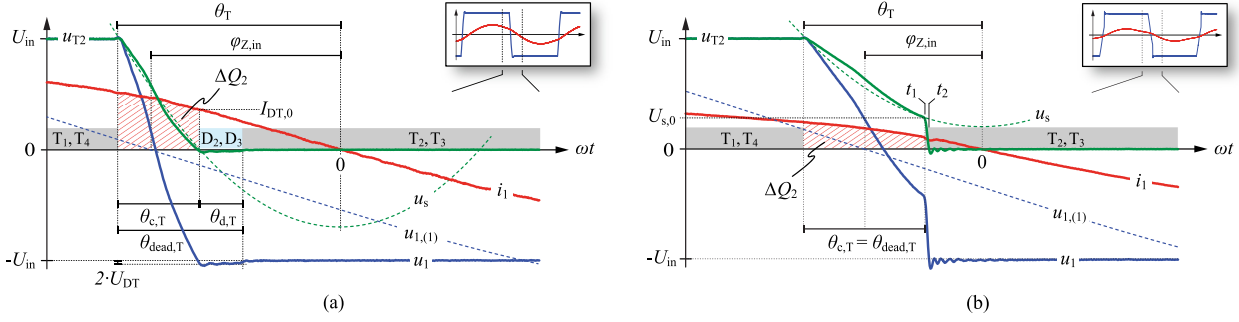
Fig. 9. Measured switching waveforms of the inverter's output voltage and current including the labeling of the time intervals and terms used for the power loss modeling. In (a), the switching waveforms are given for the case of soft-switching, where (b) shows the switching waveforms of the inverter experiencing hard-switching.

equivalent capacitance of the parasitic output capacitance of the inverter switches, evaluated at the voltage $(U_{\mathrm{in}} + U_{\mathrm{DT}})$, where $U_{\mathrm{in}}$ and the voltage drop of the FET's body diode $U_{\mathrm{DT}}$ can be calculated iteratively as well. However, in most of the cases, the value of the term $\omega_0 C_{\mathrm{T,Qeq}} U_{\mathrm{DT}}$ is very small and can be neglected.

The time intervals $\theta_{\mathrm{c,T}}$ and $\theta_{\mathrm{I}}$ can be derived, assuming that the charge $\Delta Q_2$ must fully charge and discharge the output capacitances of the corresponding switches within the time interval $\theta_{\mathrm{c,T}}$ and can be expressed with

$$\theta_{\mathrm{I}} = \arccos\left(\cos\left(\varphi_{\underline{Z},\mathrm{in}}\right) - \frac{U_{\mathrm{in}}\omega_0 C_{\mathrm{T,Qeq}}}{\hat{I}_1}\right) \quad (23)$$

$$\theta_{\mathrm{c,T}} = \theta_{\mathrm{I}} - \arccos\left(\frac{2\omega_0 C_{\mathrm{T,Qeq}}(U_{\mathrm{in}} + U_{\mathrm{DT}})}{\hat{I}_1} + \cos\left(\theta_{\mathrm{I}}\right)\right). \quad (24)$$

Using (23) and (24), the power losses during the body diode conduction interval $\theta_{\mathrm{d,T}}$ can be described with

$$P_{\mathrm{v,I,d1}} = \frac{2\hat{I}_1 U_{\mathrm{DT,0}}}{\pi}\left(\cos\left(\theta_{\mathrm{I}} - \theta_{\mathrm{dead,T}}\right) - \cos\left(\theta_{\mathrm{I}} - \theta_{\mathrm{c,T}}\right)\right)$$

$$P_{\mathrm{v,I,d2}} = \frac{\hat{I}_1^2 R_{\mathrm{DT,0}}}{\pi}\left(\frac{1}{2}\sin\left(2\left(\theta_{\mathrm{I}} - \theta_{\mathrm{dead,T}}\right)\right)\right.$$

$$\left. - \frac{1}{2}\sin\left(2\left(\theta_{\mathrm{I}} - \theta_{\mathrm{c,T}}\right)\right) - \theta_{\mathrm{c,T}} + \theta_{\mathrm{dead,T}}\right)$$

$$P_{\mathrm{v,I,d}} = P_{\mathrm{v,I,d1}} + P_{\mathrm{v,I,d2}} \quad (25)$$

with the equivalent zero current body diode forward voltage drop $U_{\mathrm{DT,0}}$ and the differential resistance $R_{\mathrm{DR,0}}$, evaluated at the current $I_{\mathrm{DT,0}}$.

The conduction losses due to the on-state resistance $R_{\mathrm{DS,on}}$ of the switches can be calculated using

$$P_{\mathrm{v,I,on}} = \frac{\hat{I}_1^2 R_{\mathrm{DS,on}}}{\pi}\left(\frac{1}{2}\sin\left(2\theta_{\mathrm{I}}\right)\right.$$

$$\left. - \frac{1}{2}\sin\left(2\left(\theta_{\mathrm{I}} - \theta_{\mathrm{dead,T}}\right)\right) - \theta_{\mathrm{dead,T}} + \pi\right) \quad (26)$$

The switching losses can be calculated by the evaluation of the energy balance of the energy stored in the inverter circuit at the time instant $t_1$ in Fig. 9(b) just before the turn-on of the switches $T_2$ and $T_3$ with respect to the energy stored after the switching operation at the time instant $t_2$. This analysis is described in detail in [29] and will be explained in the following. The energy loss due to the load current at the switching instant can be neglected since the current and the turn-on time interval are small.

In order to obtain the stored energies, the (linear) energy-equivalent capacitance [29] of the parasitic output capacitance $C_{\mathrm{oss}}$ of the switches, evaluated at the voltage $V$, is required and is described by

$$C_{\mathrm{E,eq}}(V) = \frac{2}{V^2}\int_0^V v_{ds} C_{\mathrm{oss}}(v_{ds})\mathrm{d}v_{ds}. \quad (27)$$

At the time instant $t_1$, the voltage across the switch $T_2$ is $U_{\mathrm{s,0}}$ and $(U_{\mathrm{in}} - U_{\mathrm{s,0}})$ across the switch $T_1$. The voltage $U_{\mathrm{s,0}}$ can be calculated approximatively with

$$U_{\mathrm{s,0}} \approx \frac{\hat{I}_1}{2\omega_0 C_{\mathrm{T,Qeq}}}\left(\cos\left(\theta_{\mathrm{I}}\right) - \cos\left(\theta_{\mathrm{dead,T}} - \theta_{\mathrm{I}}\right)\right) + U_{\mathrm{in}}. \quad (28)$$

The initially stored energy in the bridge leg of the switches $T_1$ and $T_2$ can be calculated using

$$E_{\mathrm{initial}} = \frac{1}{2}C_{\mathrm{E,eq}}(U_{\mathrm{s,0}}) \cdot U_{\mathrm{s,0}}^2$$

$$+ \frac{1}{2}C_{\mathrm{E,eq}}(U_{\mathrm{in}} - U_{\mathrm{s,0}}) \cdot (U_{\mathrm{in}} - U_{\mathrm{s,0}})^2. \quad (29)$$

At the turn-on of the switch $T_2$, the energy stored in its output capacitance will be dissipated into heat. Additionally, to charge the output capacitance of the switch $T_1$ to the input voltage, additional charge has to be delivered by the power supply, which is causing conduction losses in the switch $T_2$. By using the charge-equivalent capacitance, the delivered energy can be calculated with

$$E_{\mathrm{delivered}} = U_{\mathrm{in}}\left(C_{\mathrm{Q,eq}}(U_{\mathrm{in}})U_{\mathrm{in}}\right.$$

$$\left. - C_{\mathrm{Q,eq}}(U_{\mathrm{in}} - U_{\mathrm{s,0}}) \cdot (U_{\mathrm{in}} - U_{\mathrm{s,0}})\right). \quad (30)$$
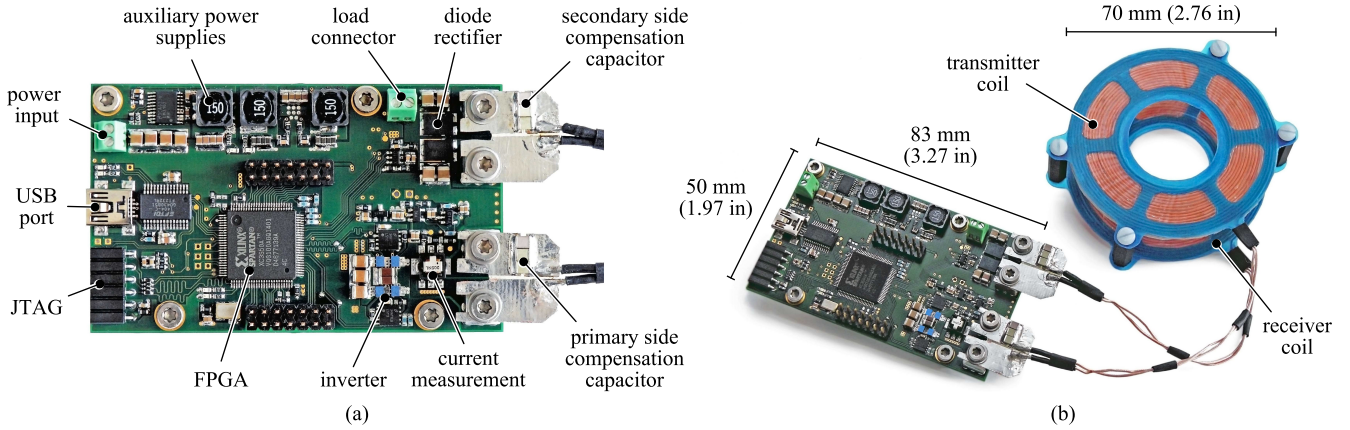
Fig. 10.    Photograph of the prototype converter board and the TET system assembly including the prototype energy transmission coils.

At the time instant $t_2$, the final stored energy, where the output capacitance of the switch $T_1$ is fully charged to the input voltage, is described by

$$E_{\text{final}} = \frac{1}{2}C_{\text{E,eq}}\left(U_{\text{in}}\right) \cdot U_{\text{in}}^2 . \qquad (31)$$

Both bridge legs experience the same amount of losses that occur twice in a switching period. Therefore, the total energy balance and the switching losses can written as

$$E_{\text{dissipated}} = 2 \cdot \left(E_{\text{initial}} + E_{\text{delivered}} - E_{\text{final}}\right)$$
$$P_{\text{v,I,sw}} = 2 \cdot f_0 \cdot E_{\text{dissipated}}. \qquad (32)$$

It is interesting to note that despite of the calculation of energies, the charge-equivalent capacitance has to be used in (30) to account for the total energy dissipation.

Additional losses are caused by the gate driver that can be calculated approximately by $P_{\text{v,I,gd}} = 4 \cdot Q_{\text{g,tot}} U_{\text{gd}} f_0$, where $Q_{\text{g,tot}}$ is the total gate charge of the FET and $U_{\text{gd}}$ is the gate driver power supply voltage. Depending on the type of the used gate driver, additional loss components are apparent, i.e., such as conduction and reverse recovery losses caused by the diode in a bootstrap circuit. The total inverter power loss is described by the sum of all the individual loss components and is given by

$$P_{\text{v,I}} = P_{\text{v,I,d}} + P_{\text{v,I,on}} + P_{\text{v,I,sw}} + P_{\text{v,I,gd}} . \qquad (33)$$

The derived power loss model enables the estimation of the individual power loss components with high accuracy. Note that the model is not limited to SSU systems only, but can be used also for SP and SSP compensated IPT systems as long as the input impedance $\underline{Z}_{\text{in}}$ exhibits an inductive behavior and the primary and secondary side resonant tank currents can be assumed to be sinusoidal.

## V. EXPERIMENTAL VERIFICATION

In order to validate the theoretical considerations of the SSU system operation along with the coil design and the power loss model, a prototype TET system was realized in hardware including the power transmission coils obtained from the coil optimization process. In the following, the specifications and the structure of the prototype TET system are given.

TABLE I
COMPONENT VALUES AND OPERATING CONDITIONS

| (a) Test Board Components | Value |
|---|---|
| Power FET $T_1$-$T_4$ | EPC2016 |
| Schottky diodes $D_1$-$D_4$ | MSS1P5-M3/89A |
| Rectifier diodes $D_5$-$D_8$ | V12P10-M3/87A |
| Capacitors $C_1$, $C_2$ | 2.97 nF / 1 kV |
| **(b) Energy Transmission Coils** | |
| Inductance $L_1$, $L_2$ | 18.8 $\mu$H, 18.4 $\mu$H |
| AC resistance $R_{L1}$, $R_{L2}$ | 210 m$\Omega$, 204 m$\Omega$ |
| Litz wire | 300×0.04 mm |
| Number of turns | 16 |
| Outside coil radius $R_a$ | 35 mm (1.38 in) |
| Inside coil radius $R_i$ | 17 mm (0.67 in) |
| **(c) Operating Conditions** | |
| Switching frequency $f_0$ | 800 kHz |
| Output voltage $U_{\text{out}}$ | 35 V |
| Output power $P_{\text{out}}$ | 5W–30 W |
| Design coupling $k_0$ | 0.268 |

### A. Prototype TET System

Fig. 10 shows a photograph of the converter board and the TET system assembly including the energy transmission coils. The specifications of the prototype coils and the driving circuit are given in Table I(a) and (b). The prototype coils have an outside diameter of 70 mm (2.76 in) and are wound with 16 turns of litz-wire on a single layer. The litz wire consists of 300 strands with a diameter of 0.04 mm (AWG 46). For simplicity, the primary and secondary side circuit of the TET system are placed on the same printed circuit board (PCB), excluding the battery charging controller. The full-bridge inverter is based on the EPC2016 enhancement mode gallium nitride (eGaN) FET. The switches offer a very low on-state resistance of 12 m$\Omega$ and a low-output capacitance of maximally 650 pF. Additionally, the eGaN FETs feature a low total gate charge of 5 nC and can be driven with 5 V logic levels. This allows for a high-switching frequency and lowers the gate driver losses considerably. Furthermore, the FET's outline dimensions are as small as 2.1×1.63 mm (0.083×0.064 in), which allows for a board layout with ultralow inductance in the commutation path of each half-bridge, which increases the switching performance. The eGaN FETs exhibit a source-to-drain forward voltage drop of
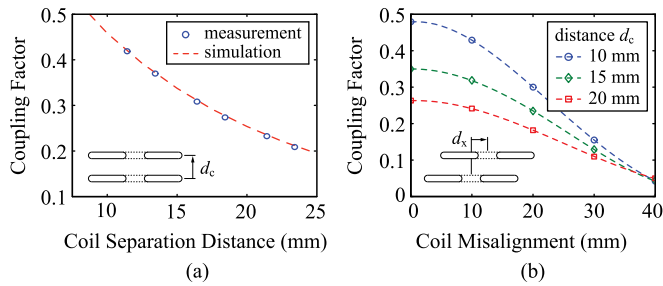
Fig. 11. (a) Measured and simulated values of the coil coupling factor at variable coil separation distance and perfect axial alignment. (b) Measurement of the coupling factor with variable axial coil misalignment at different coil separation distances.

approximately 1.5 V at 1 A, which causes significant losses during the body diode conduction interval. As proposed in [30], the FETs are equipped with additional antiparallel Schottky diodes $D_1$-$D_4$ [cf., Fig. 3(a)], which reduce the inverter power losses significantly. The small package of the FETs allows for the low-commutation inductance needed for a fast commutation of the current from the FET to the antiparallel Schottky diode. Furthermore, the high body diode voltage drop helps to reduce the commutation time additionally. Note that the additional Schottky diodes increase the total parasitic output capacitance of each FET, which must be considered in the power loss model.

The secondary side full-wave rectifier is composed of four Schottky barrier diodes with a low forward voltage drop of 0.38 V at a current of 1 A. The compensation capacitors of the resonant tank circuit are mounted on separate PCBs, which can be connected to the test board using screw terminals, in order to simplify the testing of different coils at different operating frequencies. However, the bulky connectors and the PCBs for the compensation capacitors are not suited for a high-frequency operation and exhibit a significant series resistance of about 32 mΩ at a frequency of 800 kHz.

The gate signals for the inverter switches are generated with the aid of a field programmable gate array (FPGA), which is also intended to be used in future applications, including closed-loop control of the TET system output voltage.

### B. Measurement Results

In order to evaluate the prototype's performance and to validate the mathematical power loss models, extensive measurements were carried out and are discussed in the following.

To characterize the energy transfer coils, the ac resistances were measured at the operating frequency and are given Table I(b). The resulting quality factor value is about 450 for each coil. The coupling factor was measured first for a variable coil separation distance and perfect axial alignment as it is shown in Fig. 11(a). In a second measurement, the reduction of the coupling factor with increased axial coil misalignment at a fixed coil separation distance was determined, as shown in Fig. 11(b). It can be seen that the coupling factor decreases rapidly with increasing coil separation distance at perfect axial alignment. Additionally, due to the movements of the patient, the coupling factor can be reduced significantly due to axial misalignment.
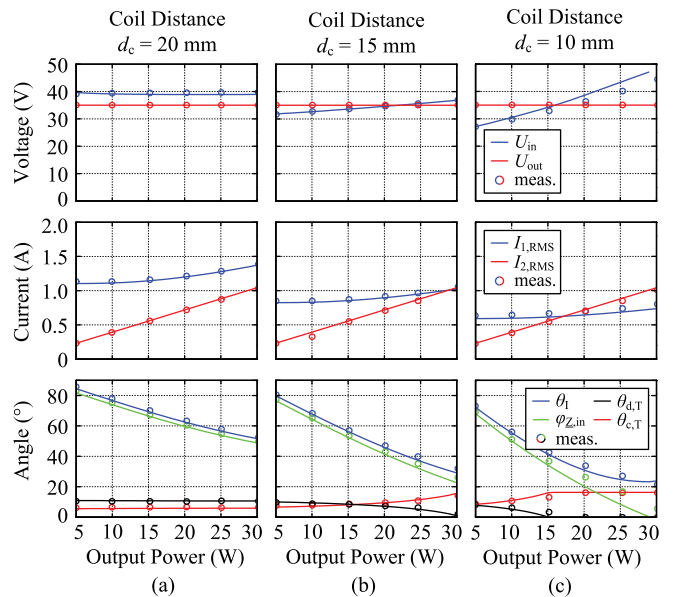


Fig. 12. Comparison of the measured system parameters and the calculated values using the mathematical model [cf., Section IV] at different coil separation distances and variable load conditions.

For the system at hand, it was found that a minimum coil coupling of 0.15 and, therefore, a fairly large coil misalignment of up to 30 mm can be tolerated in order to ensure that the inverter switches are not operated beyond their specified maximum ratings.

In order to measure the total power losses and the system parameter, the prototype TET system is operated with the specifications given in Table I(c). The output voltage of the TET system was set manually to a constant value of 35 V by adjusting the input voltage of the inverter. The measurements are performed at coil separation distances of 20 mm, 15 mm and 10 mm, which correspond to a coil coupling factor of $k = 0.263$, 0.353, and 0.489, respectively. The comparison of the measured system parameter and the values obtained with the mathematical models given in Section IV is shown in Fig. 12(a)–(c). It can be seen that the calculated values of all the relevant parameters fit the measurement with high accuracy. This is specifically true for large coil separation distances, where the coupling coefficient is small. The limitation of the mathematical model becomes clear at small coil separation distances, where the assumption of purely sinusoidal primary and secondary side resonant tank currents loses its validity. As a result, the starting point of the inverter hard-switching operation is predicted to be at a lower output power than it is observed in the measurements.

The calculated power loss distribution of the prototype TET system is shown in Fig. 13 together with the measured power losses. Note that the power loss measurements do not include the constant power losses of 258 mW caused by the FPGA and the auxiliary power supply circuits. Additionally, the power losses caused by the mentioned resonant circuit connectors are excluded from the power loss measurement since these losses are not covered by the model.
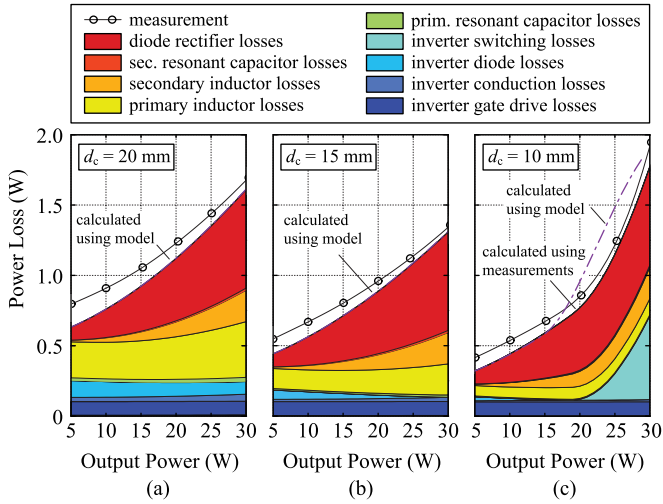
Fig. 13. Calculated power loss distribution and measurement of the total power losses for the prototype TET system at different coil separation distances and variable output power. In (c), the dashed line indicates the total power loss fully calculated with the mathematical loss model, whereas the power loss distribution is computed using the mathematical model together with measurements of the angles $\varphi_{\underline{Z},\mathrm{in}}$, $\theta_{\mathrm{I}}$, $\theta_{\mathrm{c},\mathrm{T}}$ and the voltage $U_{\mathrm{s},0}$.

In order to overcome the limitations of the power loss model at small coil separation distances, shown in Fig. 13(c), measurements of the angles $\varphi_{\underline{Z},\mathrm{in}}$, $\theta_{\mathrm{I}}$, $\theta_{\mathrm{c},\mathrm{T}}$ and the measured voltage $U_{\mathrm{s},0}$ are used to calculate the power loss component distribution. In this case, the switching losses make up almost 70 % of the total primary side losses. This shows clearly that a purely resistive operation of the IPT system is not practical and a minimum positive phase angle of the input impedance of the resonant circuit is needed at the highest coupling and maximum output power, in order to ensure that the inverter's output current is large enough to allow for ZVS.

On the secondary side, the diode rectifier makes the largest contribution to the total power losses within the TET system, which is almost 75 % of the total secondary side losses. This is specifically undesired since these losses would be generated within the patient's body. Therefore, a synchronous rectifier was developed to further reduce the secondary side power losses and is described in detail in the following section.

## VI. SYNCHRONOUS RECTIFICATION

With the improved power loss model, the power losses of the diode rectifier are determined to be approximately 700 mW at 30 W of output power. In addition, the small volume of the rectifier circuit leads to a very high power loss density and would make it impossible to keep the heating of the tissue within safe limits.

As a solution, a synchronous rectifier can be used to reduce these losses by replacing the rectifier diodes by active switches with low on-state resistance and control them actively in order to turn on the switch during the conduction time interval of the rectifier diode.

There are few reported implementations of synchronous rectifier circuits intended for the use in TET system applications.
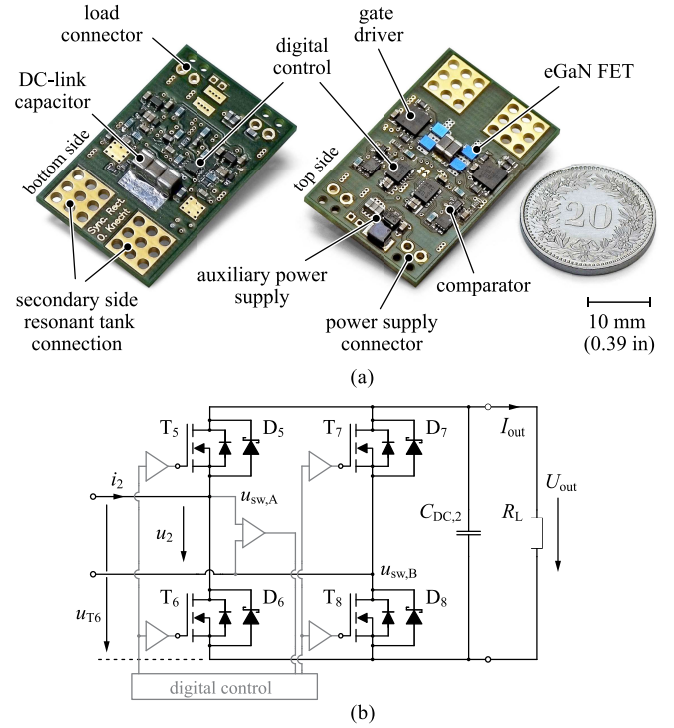


Fig. 14. (a) Photograph of the top and bottom side of the synchronous rectifier, implemented on a four-layer PCB. (b) Simplified schematic of the synchronous rectifier circuit with connected load.

The system with the highest reported efficiency is described in [6] with 93.4 % at a coil separation distance of 5 mm and an output power of 46 W. The push-pull type synchronous rectifier circuit was operated at 160 kHz and is using the synchronous gate drive control circuit STSR30, which allows for operating frequencies of up to 500 kHz. Another synchronous rectifier circuit described in [31] is running at 178 kHz and uses a push-pull type rectifier circuit as well.

The high operating frequency of the prototype TET system of 800 kHz imposes particular design challenges with respect to propagation delays in the digital control path, the gate drivers and the switches itself. In order to achieve a highly efficient self-driven synchronous rectifier, the developed rectifier circuit was optimized for lowest power consumption and small volume, while maintaining a reliable and safe operation of the circuit.

### A. Prototype Synchronous Rectifier

Fig. 14(a) shows a photograph of the top and bottom side of the implemented prototype synchronous rectifier. The actual rectifier circuit, excluding the connectors, occupies an area of only 22×18 mm (0.9×0.7 in) and is implemented on a four-layer PCB substrate. The same eGaN FETs are used for the rectifier as for the inverter circuit. The high switching speeds, the low on-state resistance and specifically the low total gate charge make the eGaN FETs the optimal choice for low power synchronous rectifier applications. A simplified schematic of the synchronous rectifier is shown in Fig. 14(b) and
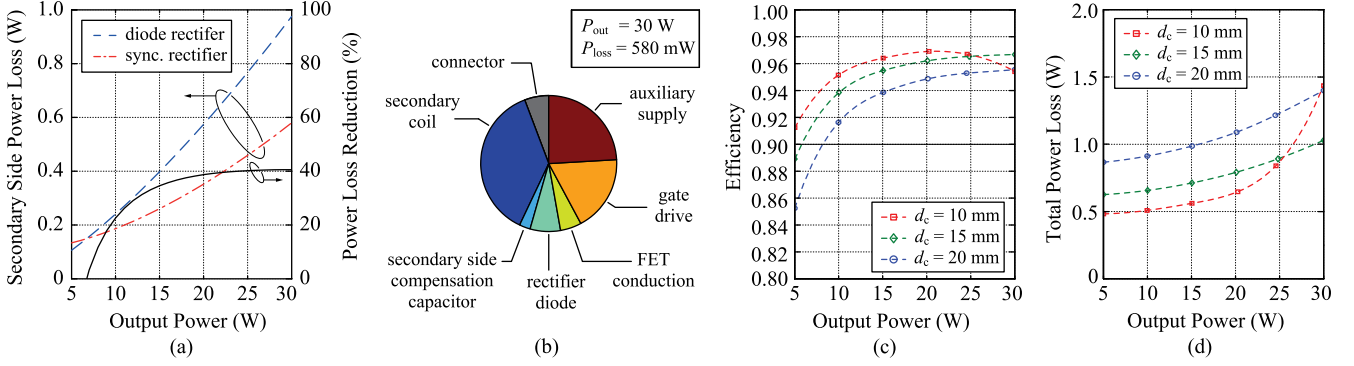
Fig. 15.  (a) Calculated secondary side power loss of the prototype TET system using the diode rectification in comparison to the system operated with the synchronous rectifier. (b) Calculated distribution of the secondary side power losses using the synchronous rectification. (c)–(d) Measured overall dc-to-dc conversion efficiency and the total power losses of the prototype TET system using the synchronous rectification. The power losses caused by the FPGA, which would reduce the efficiency by 0.8 % at full output power, are not included.

the measured switching waveforms of the rectifier are shown in Fig. 8(a).

High-speed comparators are used to detect the zero-crossing of the rectifier input voltage $u_2$ in order to synchronize the digital control circuit to the operating frequency of the TET system. As shown in Fig. 8(a), the switches $T_6$ and $T_7$ are turned on with a delay of $\theta_{\rm pd,R}$ after the voltage $u_2$ zero crossing. During the time interval $\theta_{\rm d,R}$, the body diodes of the FETs conduct the current $i_2$ which, as mentioned before, would cause high conduction losses without additional antiparallel Schottky diodes.

A one-shot circuit using the retriggerable monostable multivibrator 74AHC123 is implemented with adjustable on-time to generate the gate signals. This allows to adjust the on-state time interval such that the FETs are turned off just before the next current zero crossing, preventing a power flow in the reverse direction due to a delayed turn-off. Using this concept, the implemented circuit can be operated at a fixed switching frequency of up to 2 MHz. In addition, to prevent a shoot-through condition or other erratic operation, a digitally controlled interlock mechanism using high-speed D-type flip-flops and digital gates was implemented, which enables the corresponding comparator only for the voltage transition time interval $\theta_{\rm c,R}$. In order to predict the performance and the power loss distribution within the synchronous rectifier circuit, the power loss model of the previous section is extended.

### B. Synchronous Rectifier Power Losses

The charging time interval of the parasitic capacitances of the FETs at the secondary side current zero crossing can be computed with (15). In this case, the charge-equivalent capacitance $C_{\rm D,Qeq}$ includes the parasitic output capacitance of the FET and the junction capacitance of the additional antiparallel Schottky diode. The losses due to the diode conduction time interval $\theta_{\rm d,R}$ can be calculated with

$$P_{\rm v,SR,d} = \frac{\hat{I}_2^2 R_{\rm DR,0}}{\pi}\left(\frac{1}{2}\sin\left(2\omega_1\right) - \omega_1 - \frac{1}{2}\sin\left(2\omega_2\right) + \omega_2\right)$$
$$+ \frac{2\hat{I}_2 U_{\rm DR,0}}{\pi}\left(\cos\left(\omega_1\right) - \cos\left(\omega_2\right)\right) \quad (34)$$

using $\omega_1 = \theta_{\rm c,R}$ and $\omega_2 = (\theta_{\rm c,R} + \theta_{\rm d,R})$. The conduction losses caused by the on-state resistance of the FETs during the fixed on-time interval $\theta_{\rm on,R}$ can be written as

$$P_{\rm v,SR,on} = \frac{\hat{I}_2^2 R_{\rm DS,on}}{\pi}\left(\frac{1}{2}\sin\left(2\omega_2\right) - \omega_2 \right.$$
$$\left. - \frac{1}{2}\sin\left(2\omega_3\right) + \omega_3\right) \quad (35)$$

with $\omega_3 = (\theta_{\rm c,R} + \theta_{\rm d,R} + \theta_{\rm on,R})$. In addition, the gate drive losses $P_{\rm v,SR,gd}$ and the auxiliary power supply losses $P_{\rm v,SR,aux}$ caused by the control circuit must be taken into account. Therefore, the total synchronous rectifier power loss is given by

$$P_{\rm v,SR} = P_{\rm v,SR,d} + P_{\rm v,SR,on} + P_{\rm v,SR,gd} + P_{\rm v,SR,aux}. \quad (36)$$

In order to show the performance of the realized rectifier, power loss measurements are carried out and compared to the measurements made with the TET system using the diode rectifier.

### C. Measurement Results

The secondary side power losses are difficult to measure directly, but the losses can be estimated with high accuracy using the power loss models presented in the previous sections and the difference of the measured total power loss of the prototype TET system using the diode rectifier and the synchronous rectifier, respectively. The calculated secondary side power losses are shown in Fig. 15(a). It can be seen that the secondary side power losses are reduced by approximately 40 % at full load operation using the synchronous rectifier. Hence, the secondary side efficiency is increased from approximately 96.9 % to 98.1 % at an output power of 30 W and is greater than 97 % for the entire load range. The diode rectifier shows an equal or slightly better performance at light load conditions compared to the synchronous rectifier. This is due to the relatively high constant power consumption of the synchronous rectifier caused by the gate drives and the digital control circuit.

Fig. 15(b) illustrates the calculated distribution of the secondary side power losses of the TET system including the
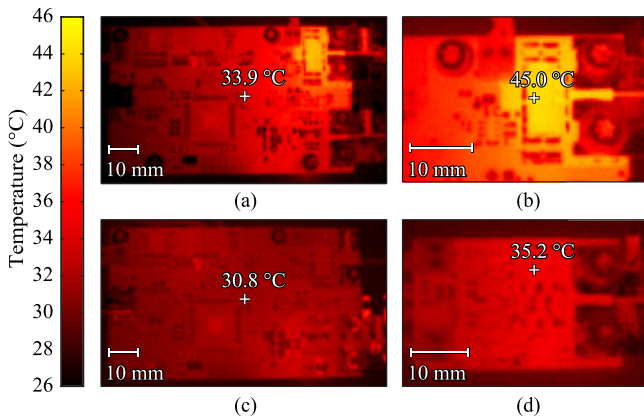
Fig. 16.　Thermographic images of the prototype inverter board operated at full load and a coil separation distance of 15 mm using either (a) the diode rectifier or the synchronous rectifier circuit (c). (b) shows a close-up of the top side of the diode rectifier and (d) shows the top side of the synchronous rectifier board operated at the same operating conditions.

synchronous rectifier for an output power of 30 W. The major contributors to the rectifier power losses are the gate drive losses and the auxiliary power supply losses and are, therefore, the main factors that determine the rectifier's performance. These losses could be further reduced by the use of GaN FETs with even lower total gate charge and by the use of a lower driving voltage of the digital circuit.

The reduction of power losses can also be investigated with the thermal images of the prototype system shown in Fig. 16, taken with a Fluke Ti9 thermographic camera. Fig. 16(a)–(b) shows the inverter PCB and a close-up of the diode rectifier operated at full load conditions and a coil separation distance of 15 mm. The ambient temperature was 26 °C and the PCB experienced passive air cooling only. Fig. 16(c)–(d) shows the thermal image of the system operated with the same operating conditions, but using the synchronous rectifier. As a result of the reduced secondary side power loss, the temperature of the synchronous rectifier is approximately 10 °C lower compared to the Schottky diode rectifier.

The secondary side coil power losses of the prototype system are calculated to be 206 mW at maximum output power and make up about 35.5 % of the total secondary side power losses as shown in Fig. 15(b). These losses are well below the limit of 500 mW, which were found in [23] to be the maximum allowable secondary coil power loss in order to keep the maximum tissue temperature at the surface of the secondary side coil below a safe limit of 39 °C.

The measurements of the dc-to-dc power conversion efficiency and the total power losses of the final prototype TET system including the synchronous rectification are shown in Fig. 15(c)–(d). The measurements include all losses except of the constant power losses of 258 mW caused by the FPGA and the auxiliary power supplies on the inverter PCB, which would reduce the efficiency by 0.8 % at full output power. However, the FPGA and the auxiliary circuits on the inverter PCB are not optimized for low power consumption. The peak effi-

ciency was measured to be 96.91 % at a coil separation distance of 10 mm (0.39 in) and is greater than 95 % for the considered coil diameter and separation distances and full load operation. With respect to the system using the diode rectifier, the efficiency was increased by approximately 1 % at full load conditions.

The measurements of the power conversion efficiency are carried out with the energy transmission coils operated in air. However, despite the low electrical conductivity of the living tissue, the alternating magnetic and electric fields in the vicinity of the energy transfer coils cause additional losses in the tissue. A model of the human skin and the energy transfer coils was used in a FE simulation, similar to the structure of the thermal model used in [23], to extract the total power losses in the tissue when the system is operated at maximum output power and a coil separation distance of 10 mm. For this operating point, the total power loss in the tissue due to the electromagnetic exposure is calculated to be lower than 50 mW, which would reduce the power conversion efficiency by about 0.15 %. These losses are, therefore, only of minor importance for the system performance and the heating of the human tissue, compared to the power losses generated within the secondary side coil. The data to describe the electrical properties of the relevant human tissues at the operating frequency were taken from [27].

## VII. Conclusion

In this paper, the design of a highly efficient wireless energy transfer system for high-power medical implant applications is described with the focus on the minimization of the power losses associated with the implanted electronics. The characteristics of the considered SS compensated IPT system are studied in detail and meaningful design equations are given, which allow for a simple determination of the resonant tank component values. In addition, the design for optimal load matching is explained and equations are derived to define the optimal operating conditions. Based on the design guidelines, a prototype TET system was built using latest GaN semiconductor technology to verify the theoretical considerations and the models used for the coil optimization process. It was shown that the parasitic capacitances of the rectifier circuit can alter the behavior of the IPT system at high operating frequencies significantly. Therefore, an extended load model and an accurate power loss model including the device parasitics must be used for the further optimization of the TET system. The presented models are validated with measurements and are given in a general form, which allows to use the models for SP and SSP systems as well.

It was shown that with a careful design of the synchronous rectifier, it is possible to reduce the secondary side power losses by up to 40 % and increase the overall dc-to-dc power conversion efficiency to more than 95 % at full load conditions and for a ratio of average coil diameter to the maximum considered coil separation distance of 3.5.

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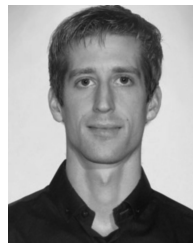
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