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Novel AC-Coupled Gate Driver for Ultrafast Switching of Normally Off SiC JFETs

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Novel AC-Coupled Gate Driver for Ultrafast Switching of Normally Off SiC JFETs

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***Abstract*—Over the last years, more and more SiC power semiconductor switches have become available in order to prove their superior behavior. A very promising device is the 1200 V 30 A JFET manufactured by SemiSouth. It features a very low on-resistance per die area (2.8 m$\Omega\cdot$cm^2), switching within 20 ns, normally off characteristic, high-temperature operation and has already been commercialized in contrast to many other SiC switches. To fully exploit the potential of the SiC normally off JFET, conventional gate drivers for unipolar devices must be adapted to this device due to its special requirements. During on-state, the gate voltage must not exceed 3 V, while a current of around 300 mA (depending on the desired on-resistance) must be fed into the gate; during switching operation, the transient gate–source voltage should be around $\pm$15 V and the low threshold voltage of less than 0.7 V requires a high noise immunity which is a severe challenge as the device has a comparably low gate–source but high gate–drain capacitance. To meet these requirements, several concepts have been published recently. They deal with the challenges mentioned, but they still show certain limitations (e.g., frequency and duty cycle limitations or need for additional cooling due to high gate driver losses). In this paper, a novel gate driver consisting of only one standard gate driver IC, resistors, capacitors, and diodes is designed and experimentally validated. It supplies enough gate current for minimum on-resistance, allows fast switching operation, features a high noise immunity, and can be used for any duty cycle and typical switching frequencies without significant self-heating.**

***Index Terms*—JFET switches, silicon carbide, power electronics, power semiconductor switches.**

I. Introduction

AGAINST the background of the continuing request for higher power density and efficiency of power electronic converters, an emerging interest in new semiconductor materials, especially wide bandgap semiconductors, has been observed. The group III-V compound semiconductor silicon carbide (SiC) is particularly promising for power electronic applications [1], [2].

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Compared to Silicon (Si), the conventional material for power semiconductors, SiC has a three times higher bandgap (the energy difference between the valence and the conduction band of the semiconductor) leading to an order of magnitude higher breakdown electrical field (328 MV/m for 4H-SiC, the most common SiC crystal structure for SiC power semiconductors, compared to 29 MV/m for Si) while having a comparable electron mobility [3]–[6].

This leads to lower conduction losses per chip area for unipolar SiC devices compared to Si devices of the same blocking voltage class. SiC field effect transistors (FETs) are feasible for high voltage ratings up to 10 kV [7] and are, in terms of losses, very competitive to Si insulated gate bipolar transistors (IGBTs), e.g., in the 1200 V blocking voltage class. Here, unipolar SiC devices offer, in particular, fast switching operation and thus lower switching losses compared to bipolar Si devices currently used in this voltage range [8], [9].

Additionally, SiC devices can be operated at junction temperatures significantly higher than 175 °C due to the several orders of magnitude lower intrinsic charge carrier concentration of SiC compared to Si and thus favoring them for applications with high ambient temperatures [10]–[13].

Currently, the main research and development focus concerning unipolar SiC devices is on Schottky barrier diodes, MOSFETs as well as normally on and off junction FETs (JFETs). While SiC Schottky diodes have already been commercially available for a few years and are increasingly deployed in applications where the absence of any reverse recovery charge can significantly improve the converter performance, the main issues with SiC MOSFETs are a low electron mobility at the channel surface and gate oxide reliability uncertainties [10], [14].

Considering the available SiC JFETs, in particular, enhancement mode (EM) devices are of interest. In contrast to normally on JFETs, no safety concerns for voltage source converters occur because the EM SiC JFET is a normally off device and blocks its nominal drain–source voltage at zero gate–source voltage. Nevertheless, it still features a pure SiC solution with all of its benefits (especially regarding high-temperature operation capability) compared to cascode approaches using an Si MOSFET connected in series to the SiC JFET, which additionally brings up the question of matching the right MOSFET to the JFET [14]. Furthermore, the available normally off device shows superior performance in terms of drain–source on-resistance per chip area (2.8 m$\Omega\cdot$cm^2 for a 1200 V device). The 1200 V 30 A normally off JFET was commercialized by SemiSouth Laboratories, Inc., in 2009 [15].

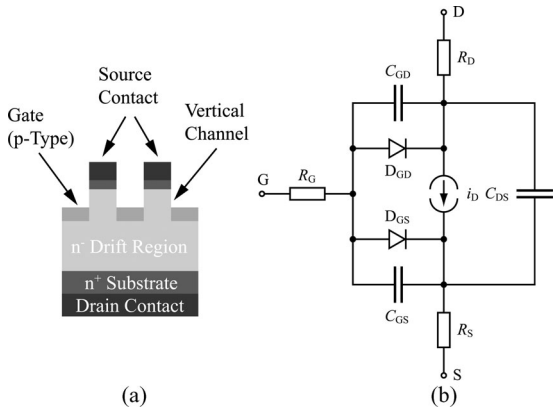

Fig. 1. SiC normally off 1200 V JFET: (a) cross section and (b) equivalent circuit diagram. Notable is with respect to the gate driver design in particular the p-n-junction diode at the gate as well as the purely vertical structure of the device leading to an inherently high gate-drain capacitance (Section II-A and Section II-B).

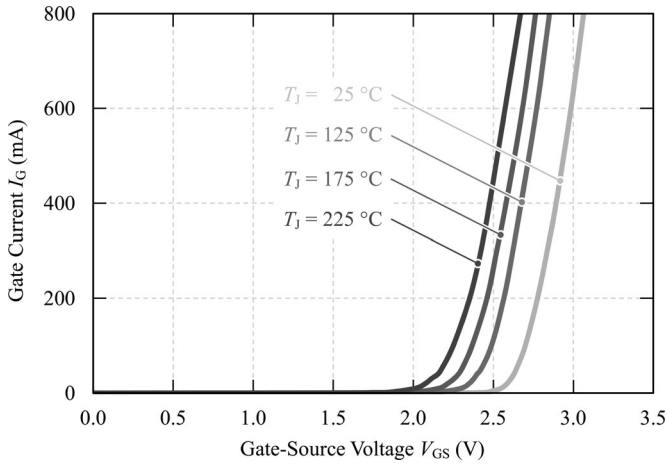

Fig. 2. Measured gate–source dc characteristic of the 1200 V 30 A SiC normally off JFET for different junction temperatures T_J. During the on-state of the SiC normally off JFET, the gate–source voltage V_{GS} should not exceed 3 V in order to avoid large currents flowing into the gate.

This device makes special demands on the gate driver circuit compared to other unipolar SiC or Si devices. To fully exploit the potential of SiC normally off JFETs, conventional gate driver circuits for unipolar switches need to be adapted for use with these switches: 1) during on-state, the gate–source voltage must not exceed 3 V, while a current of around 300 mA (depending on the desired on-resistance) must be fed into the gate; and 2) during switching operation, the transient gate voltage should be around ± 15 V and the low threshold voltage of less than 0.7 V requires a high noise immunity which is a severe challenge as the device has a comparably low gate–source but high gate–drain capacitance. Several concepts for adapted gate drivers have been presented in the literature. Some still have certain limitations, e.g., with respect to switching frequencies and possible duty cycles, and some are very complex solutions with the need for several integrated circuits, their own dc–dc converters or additional cooling due to high gate driver losses [15]–[22].

In this paper, a novel gate driver topology is presented that overcomes the current limitations while still having a low circuit complexity using one gate driver IC and passive components only. First, in Section II, the special gate driver requirements of the normally off JFET are described in detail together with their causes in order to reveal the differences to driving conventional power semiconductors. In Section III a short summary of the present concepts is given. In Section IV, the proposed novel gate driver concept is presented in detail. In Section V, the theoretical considerations are validated in a half-bridge test setup showing experimental waveforms of the switching transients. Conclusions are drawn in Section VI.

II. Gate Driver Requirements of the Normally Off JFET

Fig. 1 shows the cross section and equivalent circuit diagram of the SiC 1200 V normally off JFET. Compared to conventional power semiconductors such as MOSFETs and IGBTs, the structure of the investigated device involves special requirements for its gate driver, as will be shown in this section.

A. Requirements During On-State

From the cross section in Fig. 1(a), it can be seen that the major difference between a junction and a MOSFET is that the gate is not insulated from the channel by an oxide, but forms a p-n junction with the source [diode D_{GS} in the JFET model in Fig. 1(b)] and the drain D_{GD}, respectively. The resulting depletion layer in the channel makes sure that the device can block its nominal drain–source voltage, for the EM or normally off JFET without any reverse biasing of the p-n junction (and thus further extending the depletion region), i.e., with a gate–source voltage $V_{GS} = 0$.

Forward biasing the gate–source p-n junction reduces the width of the space charge region. The threshold gate–source voltage $V_{GS,th}$ of the device is typically around 1 V, decreasing with temperature at the rate of approximately 1.5 mV/°C to less than 0.7 V at 250 °C. If V_{GS} exceeds the built-in potential of the p-n junction $V_{bi} \approx 3$ V at room temperature, a significant amount of holes are injected into the channel. Fig. 2 shows the temperature-dependent forward characteristic of the gate–source diode. The consequence for the gate driver is the limitation that during the on-state, no more than 3 V should be applied to the JFET's gate with respect to the source (or to the drain, e.g., during synchronous rectification) to avoid large currents and thus unnecessarily high power flowing into the gate.

The correlation between the drain–source on-resistance $R_{DS,on}$ and the applied gate bias to D_{GS} (in this case in terms of the current, which can be related to the respective voltage using the diode characteristic in Fig. 2) is shown in Fig. 3 for different drain currents I_D and junction temperatures T_J. It can be seen that $R_{DS,on}$ depends on T_J and I_D. The latter dependence increases with temperature and the drain current saturation limit can be observed in Fig. 3 for junction temperatures of 175 °C and higher: while $R_{DS,on}$ increases at 175 °C for $I_D = 16$ A by 14% compared to $I_D = 7$ A, a drain current level of 24 A at a junction temperature of 175 °C (not shown in Fig. 3 for the sake

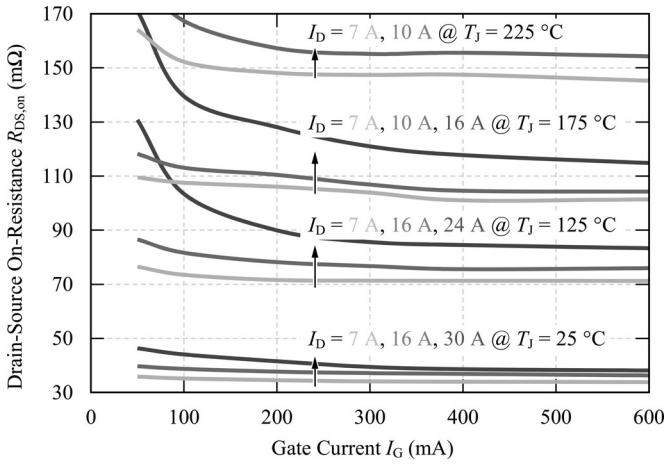

Fig. 3. Measured drain–source on-resistance $R_{\mathrm{DS,on}}$ of the 1200 V 30 A SiC normally off JFET for different drain currents I_{D} and different junction temperatures T_{J} against its gate current I_{G}. It can be clearly seen that a significant amount of gate current is necessary to operate the device with its minimum on-resistance. With increasing junction temperature, the difference in $R_{\mathrm{DS,on}}$ for different I_{G} increases. At high junction temperatures, a high drain current leads to very high values of $R_{\mathrm{DS,on}}$, and hence, $R_{\mathrm{DS,on}}$ at $T_{\mathrm{J}} = 225\,^{\circ}\mathrm{C}$ is only shown up to $I_{\mathrm{D}} = 10$ A.

of clarity) leads to a more than 50% increase in $R_{\mathrm{DS,on}}$, even for gate currents of 600 mA and more. For lower gate currents, the on-resistance is even higher.

The resulting requirement for the gate driver can be extracted from Fig. 4(a). It shows the required gate current for drain currents from 4 to 30 A and junction temperatures from 25 °C to 225 °C, if a minimum $R_{\mathrm{DS,on}}$ is desired. This gate current varies from 100 mA for $I_{\mathrm{D}} = 4$ A at 25 °C to 400 mA for $I_{\mathrm{D}} = 16$ A at 175 °C.

The required gate currents that have to be determined for the gate driver design in Section IV cannot be identified application independent. That is, the drain current (depending on the converter specifications), the available chip area (limited by cost constraints), and the maximum on-resistance (given by efficiency requirements) have to be determined for each application. This will be an iterative optimization as these different aspects interact. It has to be noted that at the mentioned gate current levels, the required power at the gate–source terminal can be more than 1 W for a single switch.

As can be seen from Fig. 3, the $R_{\mathrm{DS,on}}$ curve is very flat for a broad range of gate currents. Fig. 4(b) shows the required gate current for drain currents from 4 to 30 A and junction temperatures from 25 °C to 225 °C, if a 10% increase in the on-resistance is allowed. This leads to a significant reduction in gate current by much more than only a factor of 1.1: I_{G} varies from 50 mA for $I_{\mathrm{D}} = 4$ A at 25 °C to 200 mA for $I_{\mathrm{D}} = 16$ A at 175 °C. Taking the efficiency of the gate driver supply converters or restrictions with respect to self-heating of the drive components (e.g., due to high ambient temperature levels) into account, the gate current, which has to be delivered by the gate driver, and its influence on the on-resistance are also subject to the overall converter optimization.

To stay within the scope of this paper and to summarize the requirements for the gate driver during the on-state of the JFET, for this paper, the drain current limit is chosen as $I_{\mathrm{D}} = 10$ A at $T_{\mathrm{J}} = 225\,^{\circ}\mathrm{C}$ (see Fig. 3) and the upper limit of the gate current is chosen for minimum on-resistance at this operating point to 300 mA [see Fig. 4(a)] corresponding to a gate–source voltage of 2.42 V at $T_{\mathrm{J}} = 225\,^{\circ}\mathrm{C}$ (see Fig. 2).

This choice allows the design of a gate driver in Section IV that has challenging requirements meeting the needs of the SiC normally off JFET at high-temperature operation while being significantly different to those for MOSFET drivers. Additionally, choosing these values, a design is introduced that can be easily adapted for other applications toward lower or higher gate currents for other on-resistances or the parallelization of several chips.

B. Requirements During Off-State

The Miller effect causes special demands on the gate driver during the off-state. After turn-off of the JFET's channel, i.e., after discharging the gate–source capacitance C_{GS} from approximately 3 V to a value below the threshold voltage, and thus turning the JFET completely off, it can happen in half-bridge configurations, such as depicted in Fig. 9(a), that the gate–drain capacitance C_{GD} is charged to the actual blocking voltage V_{DC} significantly later than the turn-off of the switch.

This time delay between the turn-off of $\mathrm{JFET_{HS}}$ and the voltage rise across it occurs typically in the following situation: the inductor current i_{L} in Fig. 9(a) is freewheeling in $\mathrm{JFET_{HS}}$, before the channel of $\mathrm{JFET_{HS}}$ is turned off. The current i_{L} will continue to freewheel in $\mathrm{D_{HS}}$ after turn-off of $\mathrm{JFET_{HS}}$, until $\mathrm{JFET_{LS}}$ is turned on. Once $\mathrm{JFET_{LS}}$ is turned on, the source of $\mathrm{JFET_{HS}}$ (and thus also its gate, if the negative gate bias is negligible compared to V_{DC}) will be clamped by $\mathrm{JFET_{LS}}$ to the negative supply voltage rail, while the drain of $\mathrm{JFET_{HS}}$ remains at V_{DC}, resulting in quick charging of C_{GD} to approximately V_{DC}. Depending on the gate driver design, a certain portion of the capacitive current charging C_{GD} flows via C_{GS} or via the gate driver circuit to the source of the JFET.

Three factors increase the risk that this capacitive current leads to a voltage rise across C_{GS} above the threshold voltage resulting in an accidental turn-on of $\mathrm{JFET_{HS}}$ which would short circuit the dc link voltage.

As can be seen from the cross section in Fig. 1(a), the investigated normally off JFET has a vertical channel in contrast to typical SiC normally on JFETs [23] as well as (Si and SiC) MOSFETs [24]. This purely vertical structure leads first to a comparably low gate–source capacitance C_{GS} and second to an inherently high gate–drain (Miller) capacitance C_{GD}. This fact is illustrated in Fig. 5, which compares C_{iss} and C_{rss} of the 1200 V 30 A SiC normally off JFET with the C_{iss} and C_{rss} of a typical SiC MOSFET with similar voltage and current rating. C_{rss} is C_{GD} in the JFET model and is significantly higher for the JFET compared to the MOSFET (by a factor of 3 to 10 depending on the drain–source voltage V_{DS}). C_{iss} as the sum of C_{GS} and C_{GD} is lower for the JFET (by a factor of approximately 1.5), i.e., the JFET's C_{GS} is much smaller than that of the MOSFET, as expected from the device cross section. Then, even though the direct comparison of C_{GS} and C_{GD} of the JFET reveals

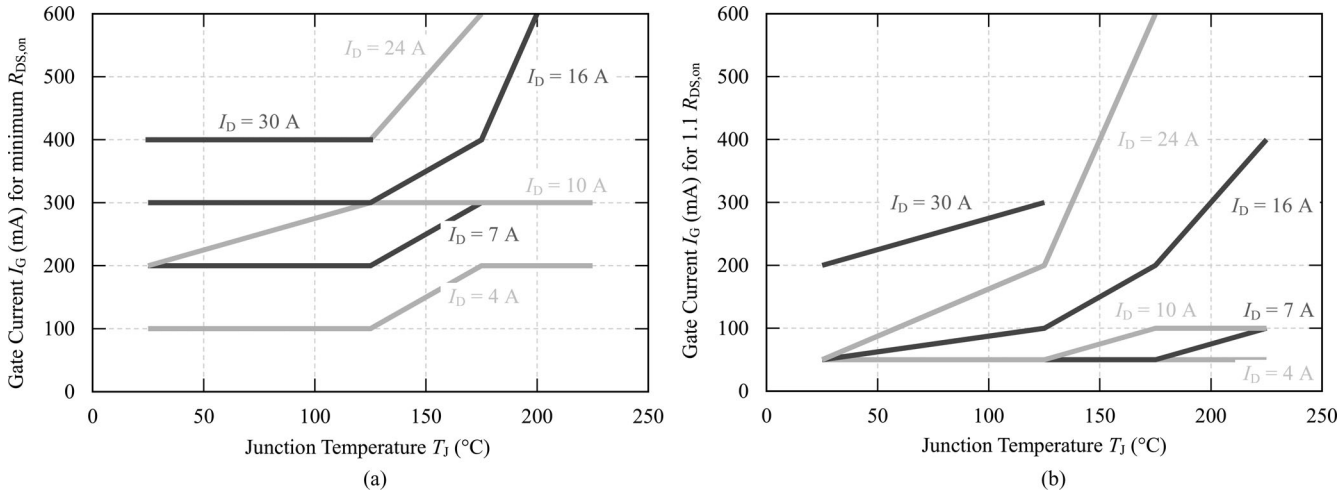

Fig. 4. Gate current I_G required to operate the 1200 V 30 A SiC normally off JFET for different drain current and junction temperature levels with (a) lowest possible drain–source on-resistance $R_{DS,on}$ and (b) drain–source on-resistance $R_{DS,on}$ that is 10% higher than the lowest possible $R_{DS,on}$. For the example gate driver design in this paper, a drain current limit of 10 A at 225 °C is assumed leading to a gate current of 300 mA for lowest possible $R_{DS,on}$ and to only 100 mA, if a 10% increase in on-resistance is accepted, reducing the power at the gate to one-third. This effect is due to the flat shape of the $R_{DS,on}$ curve in Fig. 3.

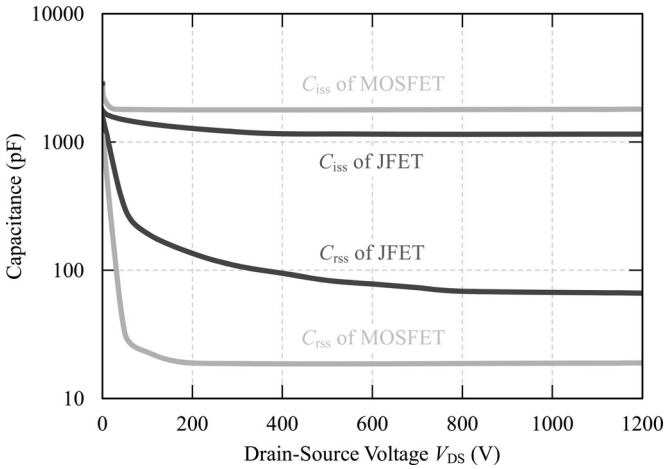

Fig. 5. Comparison of the measured input and reverse transfer capacitance (C_{iss} and C_{rss}, respectively) of an SiC normally off 1200 V 30 A JFET and a typical SiC MOSFET with similar voltage and current rating showing the high gate–drain and low gate–source capacitance of the JFET.

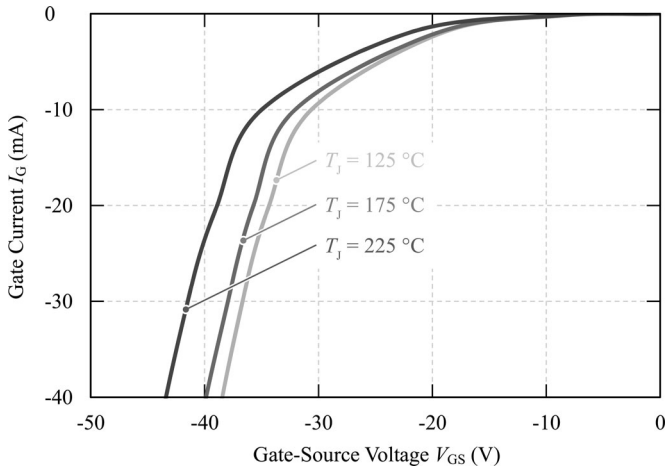

Fig. 6. Measured reverse gate–source dc characteristic of the 1200 V 30 A SiC normally off JFET for different junction temperatures T_J. A bias exceeding −15 V should not be applied to the gate in order to limit the losses during the off-state.

still a ratio of $C_{GS}/C_{GD} \approx 10$, the charge of C_{GD} can increase the gate–source voltage of the JFET as the voltage across the charged gate–drain capacitance is typically three orders of magnitude higher than the threshold voltage of the JFET which goes down to 0.7 V at 250 °C.

Hence, the gate driver circuit has to provide a low-impedance path for the capacitive current from the gate connection to the source of the normally off JFET to turn it reliably off. As this path will have parasitic resistances and inductances, a negative gate bias with respect to the source during the off-state is, thus, also needed. (This negative gate bias is not necessary during start-up of the converter and, hence, makes an important difference to the use of normally on devices.)

Fig. 6 shows the measured characteristic of the gate–source diode in reverse direction. Bearing in mind that the leakage currents occur in the off-state of the device and that the device may remain in the off-state for a longer time than only a few microseconds if, for example, the overall converter is in standby, the losses in the diode should be limited to a low level. Hence, the off-state bias is chosen to −15 V for this example design leading to a leakage current of less than 1 mA.

C. Requirements During Switching

During the switching transients, the gate driver must deliver the charge required by the parasitic input capacitance C_{iss}, which is the sum of the gate–source capacitance C_{GS} and the gate–drain capacitance C_{GD} of the JFET model in Fig. 1(b). To turn the device on, C_{GS} must be charged by the gate driver to approximately 3 V (see Section II-A) and C_{GD} (charged to approximately V_{DS} in the off-state of the device) must be discharged by feeding current from the gate terminal to the drain. To turn the device off, the opposite action is necessary. The gate driver must sink current in order to discharge C_{GS} and charge C_{GD} to approximately V_{DS}.

However, the finite conductivity of the bond wires and of the p- and n-doped SiC paths to the respective junction within the device leads to resistive portions R_{D}, R_{S}, and R_{G} of the impedance between the device terminals, as depicted in the JFET model in Fig. 1(b). The exact value depends on the operating point: the value during the on-state of the device can be extracted from the gate–source characteristic in Fig. 2 as a differential resistance. For the switching behavior, the resistivity for voltages between the threshold voltage and the negative bias during the off-state and frequencies up to the megahertz range (corresponding to the harmonics contained in the step function of the gate signal at turn-on or turn-off) are significant. The precise measurement of the resistance under these circumstances using an impedance analyzer with bias is possible only for frequencies above 1 MHz due to the small series capacitance in the JFET model leading to a load angle of close to 90° for lower frequencies and reveals a resistivity of approximately $3\,\Omega$ from the gate to the source with the drain shorted to the source to achieve a defined drain potential.

Due to this *RC* low-pass characteristic at the gate, the achievable switching speed of the JFET is limited. In order to be able to reach the desired voltage levels during turn-on ($V_{\mathrm{GS}} \geq V_{\mathrm{GS,th}}$) and turn-off ($V_{\mathrm{GS}} \leq V_{\mathrm{GS,th}}$) fast, the gate driver should apply voltages significantly higher than these steady-state values for a short period of time at each switch state transition, so that C_{GS} is rapidly charged to the desired voltage level with a higher current. SemiSouth allows transient gate–source voltages for turn-on of up to $+15$ V for a duration of less than 200 ns [25], and for turn-off, a voltage of -15 V equals the voltage level during the off-state in this gate driver design (see Section II-B).

In some applications, requirements given by electromagnetic interference, common mode or insulation issues, set limitations to the switching speed of power semiconductors. In such cases, a further gate driver requirement concerning the switching transients is the ability to switch with a preset switching speed, that is below the maximum achievable speed.

D. Gate Driver Temperature Behavior

Some of the requirements for the gate driver set by the switch characteristics investigated so far are temperature dependent, especially with respect to the gate current. Ideally, the gate driver behaves over the operating temperature range such that it caters to these changing requirements and does not induce any additional temperature variations itself. In this case, it is especially important with respect to the power loss of the gate driver that the gate current is always just as high as needed, i.e., if due to lower junction temperatures a gate current lower than the previously determined 300 mA is needed, the gate driver should supply less current.

To illustrate this requirement, the following example can be considered. If a converter design is such that the nominal rms value of the drain current is 10 A and the nominal junction temperature is 225 °C, the junction temperature is likely to be well below the nominal value of 225 °C at part load (i.e., at drain currents of less than 10 A), lowering also the gate current needed according to Fig. 4(a). (The precise value of the junction temperature at a given part load drain current level depends on the thermal impedance of the respective converter and thus cannot be calculated here.) Hence, for the example design of this paper, it is assumed that a nominal drain current of 10 A leads to a nominal junction temperature of 225 °C and a part load drain current of 7 A leads to a junction temperature of 125 °C only, mainly due to the decreasing conduction losses at lower drain currents. This means that, for the gate current supplied by the gate driver, 300 mA are needed at 225 °C ($I_{\mathrm{D}} = 10$ A) and only 200 mA at 125 °C ($I_{\mathrm{D}} = 7$ A) for minimum on-resistance [see Fig. 4(a)].

E. Gate Driver Standard Requirements

All of the aforementioned requirements for the investigated gate driver are given by the properties of the SiC normally off JFET. A novel, ubiquitous gate driver has to also fulfill standard requirements that apply to any gate driver used in power electronic converters:

1) low power consumption;
2) qualification for switching frequencies of standard power electronic converters in the investigated voltage range up to around 100 kHz;
3) enable arbitrary duty cycles from 0% to 100%;
4) robustness against steep voltage changes;
5) performance invariance against spread for factory standard models (of the gate driver IC itself as well as the switch); and
6) low (circuit) complexity and cost.

III. Existing Gate Drivers for the Normally Off JFET

Against the background of the summarized gate driver requirements for the SiC normally off JFET, existing solutions are briefly reviewed.

A. Existing Two-Stage Gate Drivers

To meet the different requirements for transient turn-on and turn-off, on the one hand, and the steady on-state, on the other hand, two-stage gate drivers have been introduced [15]–[19]. One stage supplies a short pulse with a high voltage (around 15 V) for turn-on and a second stage delivers the dc gate current for the on-state (at a gate–source voltage $V_{\mathrm{GS}} \approx 3$ V) from the same supply voltage rail via a resistor (causing high losses in that resistor due to high voltage drop of approximately 12 V across it and high gate current flowing through the resistor). The second stage is either realized by a second output of a dual gate driver IC or by low-voltage transistors connected to the supply voltage of the gate driver. The control of the second stage is realized by an additional logic IC.

To limit the power loss in the resistor during on-state, a dc–dc converter can be deployed that steps down the high voltage needed for turn-on to a lower value (e.g., around 6 V) and, thus, decreases the voltage drop across the resistor. Still, the power loss can become significant at duty cycles close to 100% and switching frequencies higher than 25 kHz [16]. This frequency limitation can be overcome with the newest implementation of

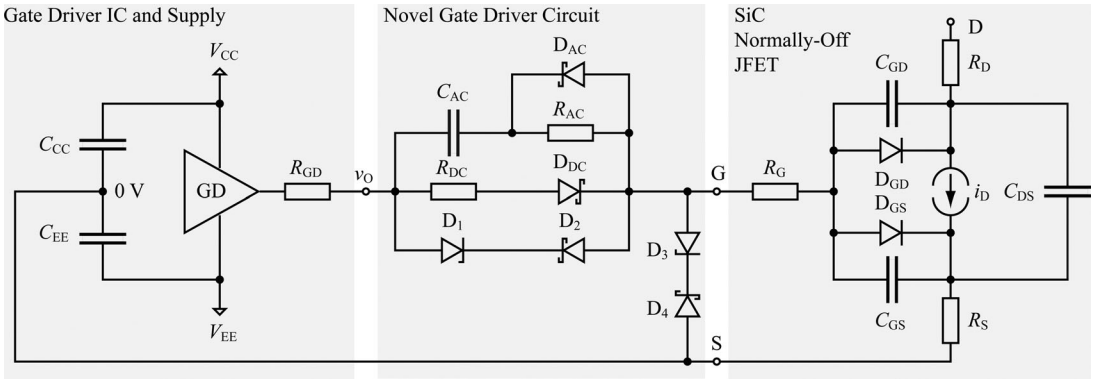

Fig. 7. Proposed novel ac-coupled gate driver for ultrafast switching of normally off SiC JFETs. During the on-state of the JFET, a dc current flows through R_{DC} and D_{DC} causing very low losses in these devices due to the low voltage drop. During turn-off, and the off-state $V_{\mathrm{Z,D3}}$ is applied to the gate for a high noise immunity making this gate driver together with D_1 and D_2 resistant against the Miller effect. During turn-on, the sum of V_{CC} and V_{CAC} is applied to the gate for fast turn-on. This gate driver does not have any duty cycle or frequency limitations and it does not suffer from significant self-heating.

this gate driver concept. However, it still features high circuit complexity, a high part count, and a large printed circuit board (PCB) footprint [17].

B. Existing AC-Coupled Gate Drivers

To reduce the high complexity of the two-stage gate drivers, ac-coupled gate drivers have been published [18]–[22], where the supply voltage is fed through a capacitor to the gate during the turn-on and turn-off and through a resistor (in parallel to the capacitor) during the on-state. The limitations of this concept include frequency and duty cycle limitations as the coupling capacitor needs to discharge during turn-off via a high impedance path [18], a high power loss in the dc current resistor, and the need for an external gate–source capacitor that can sink the current arising from the high gate–drain capacitance of the JFET [18], [22].

IV. Proposed Novel AC-Coupled Gate Driver

The proposed gate driver for the SiC normally off JFET is shown in Fig. 7. Based on the following description of the basic operation principle, detailed analytical expressions will be given for the dimensioning of the particular circuit elements and voltage levels.

A. Basic Operation Principle

A standard gate driver IC is supplied with a differential voltage $V_{\mathrm{CC}} - V_{\mathrm{EE}}$ with the midpoint (0 V) connected to the source of the JFET, V_{CC} being close to the desired gate–source voltage $V_{\mathrm{GS}} \approx 3$ V and V_{EE} in the range of -27 V (see Section IV-C and Section IV-F for the derivation of the exact values).

During the on-state of the switch, V_{CC} is applied to the gate through the output resistance R_{GD} of the gate driver IC, a resistor R_{DC}, and a Schottky diode D_{DC} in order to provide the required dc gate current to the JFET during the on-state [see Fig. 4(a)]. A value around 1 Ω results for the sum of the resistors R_{GD} and R_{DC} (see Section IV-C), compared to more than 5 Ω for the two-stage solution [17], and around 40 Ω for the existing ac-coupled drivers [20] mentioned in Section III. As the gate current depends on the desired on-resistance, it is the same for the different gate driver topologies, so the ohmic losses in the resistor scale directly with the resistor value and are, thus, at least a factor of 5 lower for the novel gate driver.

During the off-state of the device, the output v_{O} of the gate driver IC is at V_{EE}. The Zener voltage $V_{\mathrm{Z,D3}}$ of the Zener diode D_3 determines the sharing of the voltage V_{EE} between the gate–source terminals of the JFET and the capacitor C_{AC}. $V_{\mathrm{Z,D3}} \approx 15$ V fulfills the requirement of negative bias at the gate during the off-state (see Section II-B) and D_{DC} makes sure that no current flows through R_{DC} during the off-state.

To make sure that the Miller effect does not take influence and, thus, a large portion of the current charging C_{GD} during the off-state of the device can flow to the source of the JFET without flowing through C_{GS} (see Section II-B), the proposed gate driver has an antiseries connection of Zener diode D_1 and Schottky diode D_2. As the negative gate bias during the off-state is limited by leakage currents, the inductance from the gate to the source through the D_1–D_2 path has to be so low that the gate potential does not increase to the threshold voltage of the JFET for nanoseconds.

During turn-on of the JFET, the voltage $V_{\mathrm{CAC}} = -V_{\mathrm{EE}} - V_{\mathrm{Z,D3}} \approx 12$ V across C_{AC} is added to V_{CC}, making sure that a positive voltage around 15 V is applied to the gate terminal for fast charging of the JFET's input capacitance while discharging C_{AC}. To dampen oscillations or to slow down the switching speed, a resistor R_{AC} can be connected in series to C_{AC}.

During turn-off, the required negative bias can be applied to the gate by V_{EE} (limited to -15 V by D_3), and the diode D_{AC} provides with C_{AC} a low-impedance path for fast turn-off of the channel.

The state of charge of C_{AC} does not impose any duty cycle or frequency limitations in contrast to existing ac-coupled gate drivers as mentioned in Section III-B. If the on-time of the JFET is low, C_{AC} is still fully discharged as it is connected to D_{GS} through a low-impedance path. D_4, D_3, and D_{AC} form a low-impedance path that allows charging of C_{AC} also for very low off-times of the JFET (see Section V).

Having explained the basic functionality of the proposed gate driver and its elements, the design of appropriate components

and derivation of physical values is conducted in the following sections.

B. Choice of Gate Driver IC

When choosing the right gate driver IC for the proposed gate driver circuit, the output resistance R_{GD} is of special importance because during the on-state, the gate driver IC has to deliver a certain amount of current between 200 and 300 mA for this example design. During the switching transients, the IC has to deliver or sink current in order to charge or discharge C_{GS} and C_{GD} via a resistive path.

To limit the self-heating of the IC during the on-state of the JFET as well as during the large current peaks when switching the JFET and to minimize the *RC* time constant during the switching transients, R_{GD} should ideally be zero. However, the output stage of real gate driver ICs consists typically of p- and n-channel MOSFETs with nonzero on-resistance around 1 Ω. The maximum allowed value of R_{GD} can be calculated for a certain design by determining the maximum allowed temperature rise of the gate driver IC due to the described losses depending on the ambient temperature, the maximum IC junction temperature and the thermal resistance from the IC junction to its ambient.

The maximum output current that must be delivered or sunk by the IC is the second design criterion. During the on-state, a maximum of 300 mA is required for this example design. During the off-state, only leakage currents in the single-digit milliampere-range flow caused by the leakage currents of the JFET (see Section II-B) and the diodes $\mathrm{D_{DC}}$, $\mathrm{D_1}$, as well as $\mathrm{D_3}$. During switching, the capacitances C_{GS} and C_{GD} must be charged or discharged via a path with the total resistance R_{tot} consisting (during the switching transients) of R_{GD} (around 1 Ω), R_{AC} (assumed to 0 Ω to make sure the chosen gate driver IC is also applicable for designs where fastest switching is needed), and the internal resistances of the JFET accounting for approximately 3 Ω, (see Section II-C). Hence, the maximum output current I_{O} can be calculated by

$$I_{\mathrm{O}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{EE}}}{R_{\mathrm{tot}}} \approx \frac{30\ \mathrm{V}}{4\ \Omega} = 7.5\ \mathrm{A} \tag{1}$$

if R_{AC} is chosen to zero for fast switching in this design example and to reveal the maximum output current that can occur in this topology. Typically, the output resistance R_{GD} of the gate driver IC decreases with increasing output current rating, and hence, it can pay off to choose a gate driver IC with a higher output current rating than was calculated in (1).

The differential gate driver IC supply voltage of 30 V is not an uncommon value for gate drivers, but it is close to the recommended upper limit of many commercially available ICs. One advantage of a supply voltage level close to the upper limit is that the output resistance of the IC is typically smallest at this operating point. Here, the IXYS IXDE514SIA in an SO-8 package is chosen. Its peak output current is 14 A, the maximum output resistance for the high and low state is 1.25 Ω up to a junction temperature of 150 °C of the IC, and the maximum supply voltage is 35 V [26].

C. Determination of V_{CC}, R_{DC}, and $\mathrm{D_{DC}}$

The elements R_{DC} and $\mathrm{D_{DC}}$ as well as V_{CC} determine, together with R_{GD} and $\mathrm{D_{GS}}$, the gate current supplied to the JFET during the on-state of the device and, thus, the on-resistance of the JFET. The gate driver must deliver 300 mA at $T_{\mathrm{J}} = 225\,^{\circ}\mathrm{C}$ and 200 mA at $T_{\mathrm{J}} = 125\,^{\circ}\mathrm{C}$ for this design example according to Sections II-A and II-D, respectively.

For the choice of $\mathrm{D_{DC}}$, a low forward voltage drop at a current level close to the gate current during the on-state is important to minimize the losses during the on-state of the JFET, which is why a Schottky diode has been selected.

The drawback of a Schottky diode is its leakage current, which causes losses when the diode is blocking in the off-state of the JFET. Hence, the leakage current should ideally be zero but is typically higher for Schottky diodes than for p-n diodes. Still, there are Schottky diodes available that have a leakage current $I_{\mathrm{L}} \leq 3$ mA for the blocking voltage $V_{\mathrm{B,DDC}}$ needed in this gate driver circuit. $V_{\mathrm{B,DDC}}$ is given by

$$V_{\mathrm{B,DDC}} = -V_{\mathrm{EE}} - V_{\mathrm{F,D4}}\left(I_{\mathrm{L}}\right) - V_{\mathrm{Z,D3}} - I_{\mathrm{L}}\left(R_{\mathrm{DC}} + R_{\mathrm{GD}}\right). \tag{2}$$

The forward voltage drop $V_{\mathrm{F,D4}}\left(I_{\mathrm{L}}\right)$ of diode $\mathrm{D_4}$ and the voltage drop across the resistors R_{DC} and R_{GD} are negligible due to the low leakage current I_{L}; hence, (2) can be simplified and calculated to

$$V_{\mathrm{B,DDC}} \approx -V_{\mathrm{EE}} - V_{\mathrm{Z,D3}} = 12\ \mathrm{V} \tag{3}$$

using the numerical results from Sections IV-E and IV-F.

An oversized 60-V 1-A Schottky diode in SMB package (IR 10BQ060) is chosen because of the low forward voltage drop of 0.3 V for currents around 300 mA and the low leakage current of 3 mA for voltages around $V_{\mathrm{B,DDC}}$ [27].

If the gate driver circuit acted during the on-state of the switch as an ideal voltage source at the gate–source terminal of the JFET (i.e., a vertical line in a current-over-voltage diagram), it would supply significantly less current to its load $\mathrm{D_{GS}}$ at lower junction temperatures than at higher temperatures (see Fig. 2). If it was an ideal current source, it would supply the same current for all temperature levels, i.e., the gate driver would not fulfill the requirement of Section II-D to supply a gate current that is only as high as needed for the respective temperature level.

Using the $\mathrm{D_{GS}}$ characteristic (see Fig. 2, the values of the internal resistances R_{G} and R_{S} for dc current are already included as R_{G}, R_{S}, and $\mathrm{D_{GS}}$ can hardly be measured separately under dc conditions) and considering $\mathrm{D_{DC}}$ as part of the load the gate driver has to supply, V_{CC} as the no load voltage of a real voltage source and the sum of R_{GD} and R_{DC} as the internal resistance of this voltage source, the required values for V_{CC} and R_{DC} can be obtained graphically from Fig. 8: the two load lines, each one consisting of the Schottky diode $\mathrm{D_{DC}}$ and the impedance of the JFET from the gate to the source terminal, are shown for a diode junction temperature of 125 °C to facilitate gate driver operation even at high ambient temperatures, while one load line is based on a junction temperature of the JFET of 125 °C and the other on a temperature of 225 °C.

V_{CC} and the sum of R_{GD} and R_{DC} can now be derived by drawing the gate driver supply line from the 300 mA point of

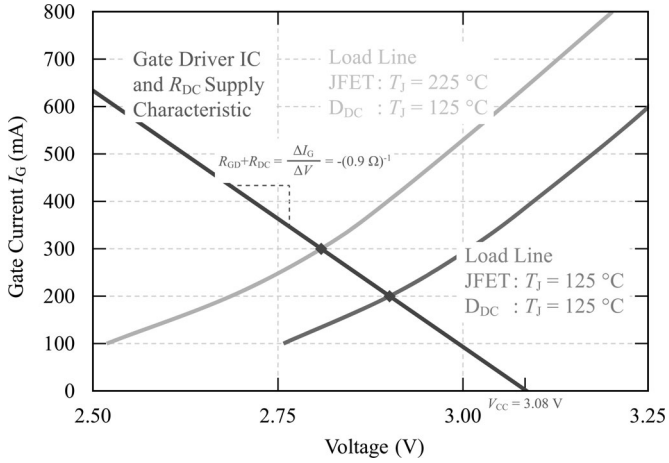

Fig. 8. Characteristic of series connection of gate–source diode D_{GS} and Schottky diode D_{DC} at junction temperatures of 125 °C and 225 °C for the JFET as well as 125 °C for diode D_{DC}. The voltage on the abscissa is the sum of the gate–source voltage V_{GS} of the JFET and the forward voltage V_F of D_{DC}. From these characteristics, the required gate driver supply characteristic (straight line) in terms of V_{CC} and R_{DC} can be derived.

the load line for the JFET junction temperature of 225 °C to the 200 mA point of the load line for the JFET junction temperature of 125 °C. The voltage axis intercept of the supply characteristic reveals $V_{CC} = 3.1$ V and the negative inverse of the slope gives 0.9 Ω for the sum of R_{GD} and R_{DC}. As R_{GD} is already in this range ($R_{GD} = 1.25\ \Omega$ of the chosen gate driver is its maximum value, see Section IV-B), R_{DC} can be chosen to zero for this example design. Fig. 8 also allows to directly analyze the impact of a slight change in V_{CC}, R_{GD}, or R_{DC} on the gate current and thus together with Fig. 3 on the on-resistance of the JFET.

Besides this intuitive graphical approach, analytical expressions can also be derived using formulas corresponding to the graphical approach: with the gate–source voltage V_{GS} of the JFET at the nominal junction temperature $T_{J,n}$ (in this design example 225 °C) and nominal gate current $I_{G,n}$ (300 mA) as well as at the part load junction temperature $T_{J,p}$ (125 °C) and part load gate current $I_{G,p}$ (200 mA) and the forward voltage V_F of diode D_{DC} at gate driver temperature level T_{GD}, R_{DC} and V_{CC} can be calculated as

$$R_{DC} = \frac{V_{GS}(I_{G,n}, T_{J,n}) + V_F(I_{G,n}, T_{GD})}{I_{G,p} - I_{G,n}} - \frac{V_{GS}(I_{G,p}, T_{J,p}) + V_F(I_{G,p}, T_{GD})}{I_{G,p} - I_{G,n}} - R_{GD} \quad (4)$$

$$V_{CC} = V_{GS}(I_{G,n}, T_{J,n}) + V_F(I_{G,n}, T_{GD}) + I_{G,n} \cdot (R_{GD} + R_{DC}). \quad (5)$$

The values for V_{GS} and for V_F for different temperature and current levels can be extracted from Fig. 2 and [27], respectively, or the sum of both can be read directly from Fig. 8. Equations (4) and (5) then reveal the same values as obtained graphically: $R_{DC} = 0$ and $V_{CC} = 3.1$ V.

D. Selection of D_{AC}, D_2, *and* D_4

To minimize the losses in the particular diode is the most important design criterion for the diodes D_{AC}, D_2, and D_4. Even though they conduct current (apart from leakage currents) only during turn-off and not during the on- or off-state of the JFET (in contrast to D_{DC}, see Section IV-C), a low forward voltage drop is desired, which is why again Schottky diodes are chosen. The blocking voltages of the three diodes are smaller than V_{CC}, and hence, the leakage currents are negligible for typical Schottky diodes. 40 V IR 10MQ040NPbF diodes in SMA packages are selected [28].

E. Selection of D_3

The Zener diode D_3 determines the negative bias at the gate during the turn-off of the JFET. It is limited to −15 V due to leakage currents of D_{GS}. The Zener voltage $V_{Z,D3}$ should be chosen to this voltage level, so that the immunity against the Miller Effect is as high as possible and a high voltage can be applied to the unavoidable inductances in the D_1–D_2 path in order to feed the Miller charge through this path (and not through C_{GS}). D_4 inhibits operation of D_3 in the forward direction.

F. Determination of V_{EE}, D_1, *and* R_{AC}

V_{EE} sets together with $V_{Z,D3}$ the voltage V_{CAC} that C_{AC} is charged to during the off-state for typical off-times during normal operation of power electronic converters. (For off-times longer than several tens of microseconds, the leakage currents of diodes D_1 and D_3 will match leading to a voltage distribution that is determined by their voltage-over-current characteristic and no longer simply by V_{EE} and $V_{Z,D3}$.) During turn-on, V_{CAC} is applied to the gate in addition to V_{CC}. Hence, to calculate V_{EE}, first V_{CAC} is calculated using the desired ac voltage $V_{GS,AC} = 15$ V during turn-on that can be applied to the gate (see Section II-C)

$$V_{CAC} = V_{GS,AC} - V_{CC} = 12\ \text{V}. \quad (6)$$

(During turn-off, the gate–source voltage is limited by the Zener voltage of diode D_3.) Now, the negative supply voltage level can be determined to

$$V_{EE} = -V_{CAC} - V_{Z,D3} = -27\ \text{V}. \quad (7)$$

$V_{Z,D1}$ should not be chosen to a significantly higher value than $-V_{EE} - V_{Z,D3} = 12$ V; otherwise, a larger portion of the capacitive current charging C_{GD} during the off-state (see Section II-B) would flow through C_{GS} to the source and not via D_1 and D_2 leading to a larger increase in the gate–source voltage. Hence, the Zener voltage $V_{Z,D1}$ is chosen to 12.5 V and thus only slightly above $-V_{EE} - V_{Z,D3} = 12$ V in order to make sure that no continuous current will flow through diodes D_1 to D_4 during the off-state.

The differential resistance in reverse direction of the diode D_1 should be as small as possible to guarantee a voltage drop across D_1 close to $V_{Z,D1}$ if the gate–drain capacitance is charged.

If the switching speed has to be limited, R_{AC} can be increased starting from its current value of 0 Ω.

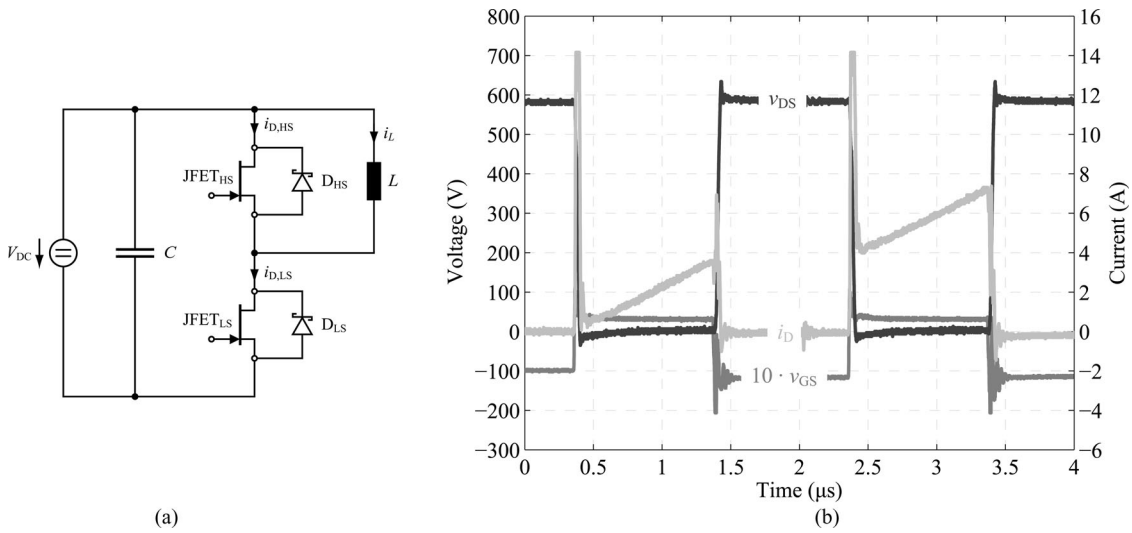

Fig. 9. (a) Test setup used for the validation of gate driver circuit. Half-bridge connection of two 1200 V 30 A SiC normally off JFETs with antiparallel freewheeling diodes (SiC Schottky Barrier Diodes Infineon IDH15S120) and an inductive load. (b) Measured time behavior of the drain current, drain–source, and gate–source voltage of the low-side switch.

G. Dimensioning of C_{AC}

To guarantee a fast switching of the JFET, the parasitic capacitances C_{GS} and C_{GD} of the JFET must be charged by the capacitor C_{AC}. If a freewheeling diode connected in antiparallel to the JFET is already conducting the load current before the JFET is switched, the difference in the voltage across C_{GD} before and after the switching action and, thus, the charge required for the voltage change across C_{GD} is low and C_{AC} must deliver the gate–source charge only. If the gate–drain potential difference increases rapidly when the devices switches, the charge in C_{AC} must equal the sum of the gate–source and gate–drain charge. This means, for turn-on of the JFET, that the capacitive current needed to charge C_{GS} and discharge C_{GD} should be able to flow through C_{AC}, which makes the voltage $V_{C\mathrm{AC}}$ decrease from its value during the off-state (12 V) to the voltage drop across R_{DC} (0 V in this design example) and $\mathrm{D_{DC}}$ (approximately 0.3 V). During turn-off, the capacitive current discharging C_{GS} and charging C_{GD} should also be able to flow through C_{AC}, increasing its value from the voltage drop across R_{DC} and $\mathrm{D_{DC}}$ to 12 V.

For a switched voltage of 600 V, the gate charge of the JFET is $Q_G = 60$ nC [29]. The required capacitance and, thus, the lower limit for C_{AC} can be calculated as

$$C_{\mathrm{AC}} = \frac{Q_{\mathrm{G}}}{V_{C\mathrm{AC}}} \approx 6 \text{ nF}. \tag{8}$$

The upper limit of the charge stored in C_{AC} is given by efficiency considerations as the energy stored in C_{AC} is dissipated in the resistances when switching. A capacitance value larger than the lower limit calculated in (8) helps slightly to achieve a faster turn-on as the voltage of capacitor decreases less fast in this case. Furthermore, a larger value for C_{AC} improves the gate driver's robustness against the Miller effect, as it leads to a smaller increase in the gate-source voltage when C_{GD} is charged. Here, 6 nF are chosen for C_{AC}.

V. Gate Driver Measurement Results

The gate driver circuit and resulting switching action has been tested in a half-bridge inductive test circuit with an SiC freewheeling diode as shown in Fig. 9(a) and switching patterns as shown in Fig. 9(b) to validate the theoretical considerations.

The switching waveforms for turn-on and turn-off are shown in Fig. 10. The switching times are slightly more than 30 ns for turn-on and 20 ns for turn-off in Fig. 10(a) and (b), respectively. Hence, this novel gate driver circuit enables similarly fast switching performance of the normally off SiC JFET as previously published for the existing two-stage [15], [19] and ac coupled [20], [22] gate drivers. Thus, this novel ac-coupled gate driver leads to switching losses of the JFET in the same range, if they are measured in a comparable (especially with respect to the parasitic capacitances) system layout, but the novel gate driver does not suffer from shortcomings in terms of circuit complexity and part count (for the two-stage gate drivers) and frequency or duty cycle limitation (for the existing ac-coupled gate drivers). The high power loss in the dc resistor R_{DC}, that all existing gate drivers suffer from, is avoided for this topology. This remains true even if a high gate current that is needed for operation of the device with lowest possible on-resistance is supplied to the JFET.

Two of the most important properties of the novel gate driver, the negative gate bias during the off-state and the significantly increased gate–source voltage during the switching transients, can also be observed in Fig. 10. As the gate–source voltage is measured directly at the TO-247 package, the inductive voltage drop resulting from the PCB tracks and the 10-mm-long pin of the package reduces the measured gate–source voltage slightly to less than 15 V.

Fig. 11 shows two examples of the experimental verification of the theoretical considerations and dimensioning in Section IV. In Fig. 11(a), the dimensioning of C_{AC} is proven

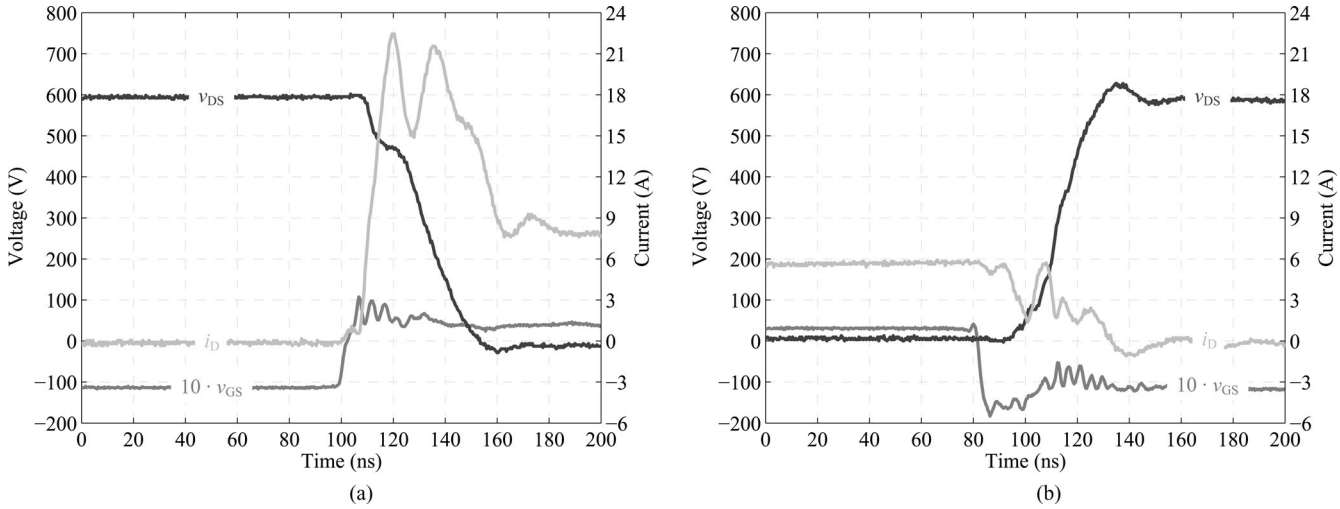

Fig. 10. Switching transient with the optimized gate driver circuit switching the JFET in an inductive load test circuit as shown in Fig. 9. (a) Turn-on and (b) turn-off are finished after 30 and 20 ns, respectively. The gate–source voltage waveform shows the negative bias during the off-state and the significantly increased voltage during the switching transients.

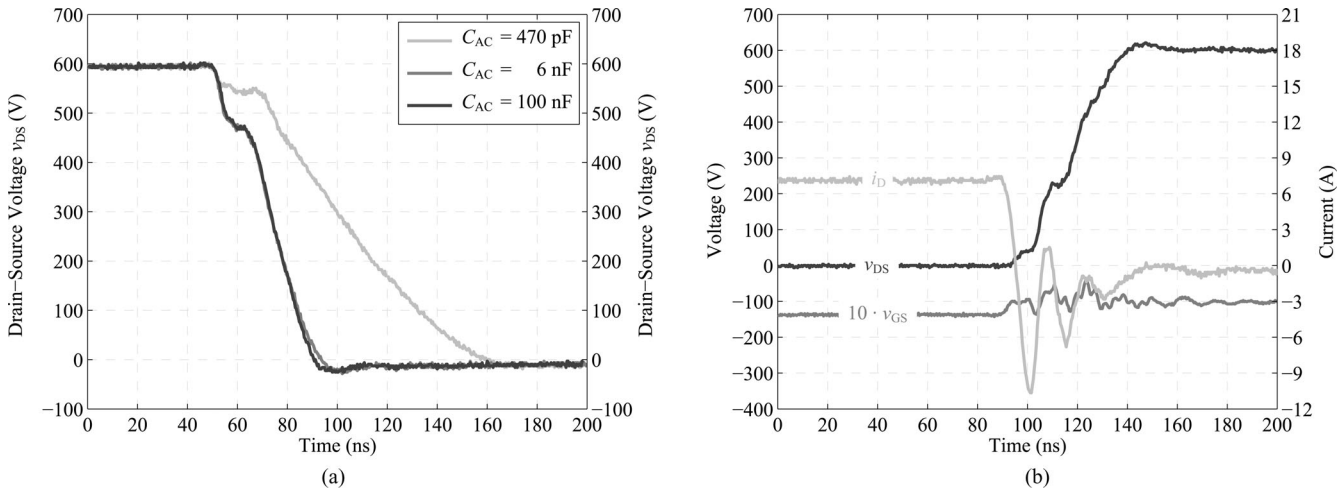

Fig. 11. (a) Drain–source voltage of $\mathrm{JFET_{LS}}$ during turn-on for different values of C_{AC}. As expected, a smaller value than $C_{\mathrm{AC}} = 6$ nF leads to a drastically slower turn-on while an increase does not yield a significant gain in switching speed. (b) Robustness against the Miller effect is proven by turning $\mathrm{JFET_{LS}}$ off as the negative gate–source voltage shows and turning $\mathrm{JFET_{HS}}$ on so that the load current i_{L} commutates from $\mathrm{D_{LS}}$ to the upper switch charging C_{GD} of $\mathrm{JFET_{LS}}$. It can be seen, that the gate–source voltage is less than -5 V, so that at every moment a safety margin of more than 5 V to an accidental turn-on of the JFET is maintained.

by measuring the drain–source voltage during turn-on of the JFET for different values of C_{AC}. As derived in Section IV-G, an increase in capacitance beyond the calculated value of $C_{\mathrm{AC}} = 6$ nF yields only a slightly faster turn-on (especially at the end of the turn-on transient, when the voltage across a larger C_{AC} does not increase as fast as across a smaller C_{AC}), but does not make a relevant difference. The consideration that a reduction significantly below 6 nF leads to a considerable extension of the switching time is also clearly shown.

The robustness of the novel gate driver circuit against the Miller effect is shown in Fig. 11(b). Charging the gate–drain capacitance to 600 V leads to a significant increase in the gate–source voltage, due to the presence of the low-impedance path to C_{AC} and the diodes $\mathrm{D_1}$ and $\mathrm{D_2}$, the gate–source voltage does not exceed -5 V at any time.

Furthermore, the optimized gate driver has been tested for varying JFET drain currents. No noticeable change in behavior was discovered. Switching speed is practically independent of drain current at turn-on, and turn-off is faster for increased currents, as they charge the intrinsic drain–source capacitance faster. Moreover, the JFET was subjected to elevated junction temperatures up to 250 °C in part showing reduced switching speed, e.g., slower turn-on transients of approximately 50 ns at 175 °C and 16 A, which is expected due to the on-resistance increasing with temperature and, therefore, slower discharge of the drain–source capacitance at turn-on.

The EM SiC JFET is suitable for parallelization in order to increase current rating because of the positive temperature coefficient of its on-resistance. The 30 A device is, in fact, a parallelization of two identical chips. Symmetrical setup is of great importance for balanced currents in the parallel

connections. If more chips are to be driven in parallel, the value of C_{AC} has to be increased due to the increased gate charge according to (8) and the design of V_{CC} as well as R_{DC} has to be conducted according to Section IV-C for the additional gate current needed.

VI. Conclusion

Against the background of the increasing importance of SiC as a semiconductor material for power electronic devices, appropriate gate drivers for the already commercialized normally off 1200 V 30 A SiC JFET with very promising performance in terms of the device losses have been of large interest and the subject of many recent publications. These publications mention certain limitations of proposed and partially complex gate drivers with respect to noise immunity, possible duty cycles, and switching frequencies as well as high gate driver losses which in turn lead to significant self-heating.

To fully exploit the potential of the SiC normally off JFET and to make sure that it can also be used in power electronic converters with high switching frequencies, a novel gate driver topology is presented and dimensioned in this paper. The exact demands for the gate driver are identified and analyzed in detail. The proposed gate driver meets the requirements of the SiC normally off JFET while using only one standard gate driver IC, one capacitor, two resistors, and six diodes. It delivers the required charge very fast during turn-on of the switch by means of a precharged capacitor. During turn-off, a low-impedance path quickly removes the charge from the gate, and negative biasing during the off state allows the gate–drain capacitance to be charged via a low-impedance path without the risk of turning the JFET on unintentionally. During the on-state, the gate driver delivers up to 300 mA at a gate–source voltage of only 2.4 V without significant self-heating to ensure that the JFET is operated with the lowest possible on-resistance.

Finally, measurement results are provided showing that this gate driver offers fast turn-on and turn-off of the switch while still having high noise immunity and allowing operation at all duty cycles and at high switching frequencies. The latter is especially important to enable promising SiC power semiconductors to make use of the superior performance of SiC in terms of high switching frequency capability in power electronic converters.

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