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***Abstract*—A comprehensive procedure for the derivation of optimal, full-operating-range zero voltage switching (ZVS) modulation schemes for single-phase, single-stage, bidirectional and isolated dual active bridge (DAB) ac–dc converters is presented. The converter topology consists of a DAB dc–dc converter, receiving a rectified ac line voltage via a synchronous rectifier. The DAB comprises primary and secondary side full bridges, linked by a high-frequency isolation transformer and a series inductor. ZVS modulation schemes previously proposed in the literature are either based on current-based or energy-based ZVS analyses. The procedure outlined in this paper for the calculation of optimal DAB modulation schemes (i.e., combined phase-shift, duty-cycle, and switching frequency modulation) relies on a novel, more accurate, current-dependent charge-based ZVS analysis, taking into account the amount of charge that is required to charge the nonlinear parasitic output capacitances of the switches during commutation. Thereby, the concept of "commutation inductance(s)" is shown to be an essential element in achieving full-operating-range ZVS. The proposed methods are applied to a 3.7 kW, bidirectional, and unity power factor electric vehicle battery charger which interfaces a 400 V dc-bus with the 230V_{ac}, 50-Hz utility grid. Experimental results obtained from a high-power-density, high-efficiency converter prototype are given to validate the theoretical analysis and practical feasibility of the proposed strategy.**

***Index Terms*—AC–DC power conversion, battery charger, circuit analysis, dual active bridge (DAB), optimal control.**

I. Introduction

SINGLE-PHASE, utility interfaced, isolated ac–dc converters with power factor correction (PFC) cover a wide range of applications such as chargers for plug-in hybrid electrical vehicles and battery electric vehicles [1], [2], interfaces for residential dc distribution systems and energy storage systems [3], [4], and inverters for photovoltaic modules. Bidirectional power flow is increasingly required since the traditional electricity grid is evolving from a rather passive to a smart interactive service network (customers/operators), where energy systems play an active role in providing different types of support to the grid [5] (e.g., vehicle-to-grid (V2G) concepts [6] and dc distribution systems [3]).

It is shown in [7] and [8] that the above mentioned unity power factor, isolated ac–dc conversions can be realized by combining a line voltage rectifier with a dual active bridge (DAB) dc–dc converter (single power conversion stage). For the line voltage rectifier, besides a passive diode bridge, an efficient synchronous rectifier (SR) can be used to further reduce the conduction losses and to enable bidirectional power flow. As no energy storage is present in the dc-link (a small high-frequency (HF) filter capacitor is placed between the SR and the DAB), the PFC is performed by the DAB, which has to actively shape the line current. The biggest advantage of these DAB topologies is that the ac–dc energy conversions take place in a single conversion stage (1-S), producing high quality waveforms and complying to regulations on low- and high-frequency distortions of the mains ac power lines [8]–[10]. Compared to the traditional dual-stage (2-S) approaches [4], a power factor correcting front-end as well as bulky failure prone electrolytic dc-link capacitors are omitted [11]. The 1-S DAB ac–dc converter topology implemented with a full bridge–full bridge (FBFB) DAB and SR (bidirectional power flow), as shown in Fig. 1, is the subject of this paper.

Research on the DAB mainly has been focusing on improved modulation schemes which facilitate increased converter efficiency and/or power density [12]. Whether the DAB is used in a dc–dc, a 1-S ac–dc (this paper), or any other configuration, one of the main goals has been to optimally (i.e., minimizing a certain, mostly loss related, cost function) operate the DAB within conditions where quasi-zero switching losses occur (i.e, by virtue of zero voltage switching, ZVS). Therefore, publications on DAB modulation schemes can be classified according to their ZVS considerations.

1) Current-based (CB) ZVS: The largest group of publications does not take into account the (parasitic) switch capacitances and assumes that ZVS of a bridge leg is achieved when the drain-to-source current of the switch which initiates the commutation (turn-off) is positive at the switching instant. Besides the traditional phase-shift-modulation (PSM[1]), where full-power-range CB ZVS is only possible at a voltage conversion ratio[2] d equal to one [8], [13], modulation schemes with increased degree of freedom regarding the search toward optimal CB ZVS operation

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[1] PSM: the active bridges of the DAB are operated to generate 50% duty-cycle high-frequency ac-link voltages which are phase-shifted relative to each other in order to achieve the required power transfer (one degree of freedom).

[2] According to Fig. 1, $d = n_1/n_2 \cdot V_{\mathrm{dc2}}/v_{\mathrm{dc1}}$.

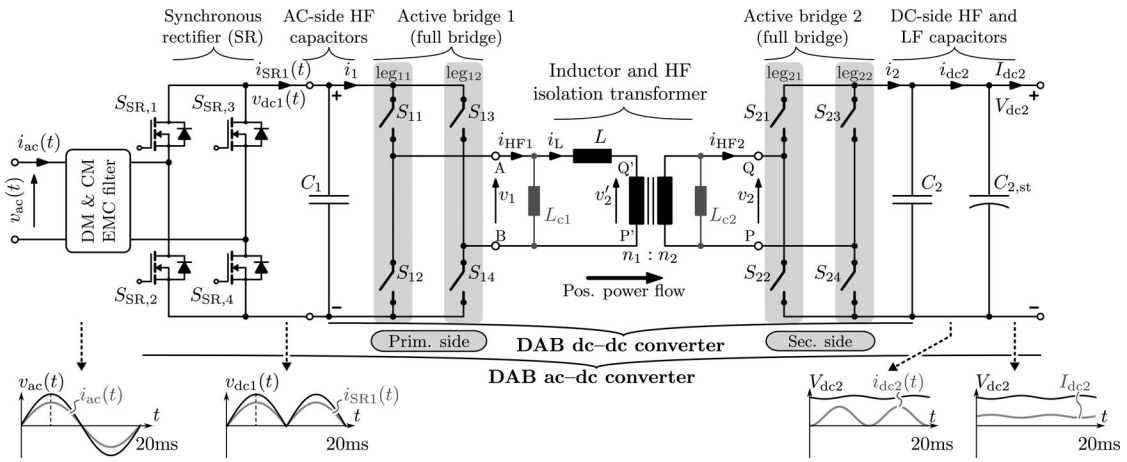

Fig. 1. Circuit schematic of the single-phase, single-stage (1-S), bidirectional and isolated DAB ac–dc converter topology.

of the DAB are introduced. These schemes combine PSM with either single-sided duty-cycle modulation (further referred to as SSPWM) or dual-sided duty-cycle modulation (further referred to as DSPWM; highest degree of freedom), and use a low-power and a high-power switching mode[3] in order to reduce the HF ac-link rms currents, to lower the transformer core flux, and to obtain full-operating-range CB ZVS [14]. Especially, DSPWM enables significant improvements for low-load operation and for widely varying input and/or output voltage ranges such as is the case for the investigated 1-S ac–dc converter, where the DAB input voltage is a rectified sinewave (see Fig. 1), and where d is highly variable [11]. Simple suboptimal solutions for the calculation of the modulation parameters in order to achieve full-operating-range CB ZVS are given in [15] and [16] using SSPWM, and in [9] using DSPWM. An SSPWM scheme for minimizing the reactive inductor power is presented in [17]. In [12], an optimal DSPWM scheme with respect to minimum inductor rms currents is proposed.

2) Energy-based (EB) ZVS: It was already shown in [18] that when considering CB ZVS, substantial parts of the ZVS regions involve incomplete bridge commutations due to the presence of (parasitic) switch capacitances. Consequently, above modulation schemes result in (partly) hard-switching operation for certain intervals of the DAB's operating range,[4] leading to reduced efficiency and in the worst case destruction of the semiconductor switching devices. The influence of the switch capacitances on the (resonant) bridge commutations is described in [10] and [18]–[21] by evaluating the energy balance between the switch capacitances and the HF ac-link inductances (EB ZVS). However, in [10] and [19], the state of the one active bridge is not taken into account in the ZVS verification of the other, leading to easy implementable but incomplete EB ZVS constraints. A simple suboptimal modulation scheme based on these simplified constraints is presented in [10] using SSPWM and variable switching frequency (f_s) control.[5] However, EB ZVS could not be fully achieved for the low-power mode, and the transition between the low- and high-power modes encompasses highly undesirable discontinuous steps in the modulation parameters. The harder to implement EB ZVS constraints given in [18], [20], and [21], are still incomplete as the state of the one active bridge is taken into account in the ZVS verification of the other but, however, a (quasi) simultaneous state change within the one and/or together with the other active bridge is not allowed. Therefore, in [20], simplifications had to be made, yielding a suboptimal modulation scheme which uses DSPWM and variable f_s. Full-operating-range EB ZVS was reported but, again, the mode transition involves discontinuous steps.

Regardless their objective, all DAB modulation schemes so far presented are based on "theoretical" CB or EB ZVS analyses. The latter are the most accurate but, as described previously, still involve difficulties, in particular concerning implementability and accuracy. As a consequence, the objective of this paper is twofold. On the one hand, this paper attempts to deal with the deficiencies of the CB and EB ZVS considerations by proposing a current-dependent charge-based (CDCB) ZVS analysis (see Section III) that takes into account the commutation charge of the (parasitic) switch capacitances[6] as well as the time dependence of the commutation currents. Therewith, the state and the simultaneous and nonsimultaneous state changes of the active bridges are inherently dealt with, resulting in a more accurate description of the DAB's ZVS conditions. On the other hand, a procedure to derive optimal ZVS modulation schemes (see Section IV) for DAB converters is introduced and illustrated for the investigated 1-S DAB ac–dc converter. This procedure combines DSPWM and frequency modulation in order to minimize a cost function related to the converter losses, and relies on the proposed CDCB ZVS analysis in order to assure full-operating-range ZVS. Furthermore, the concept

[3]The low-power and high-power modes are similar to, respectively, mode 2 and mode 1 in this paper (cf. Fig. 7).

[4]This effect is most pronounced in the regions where $d \gg 1$ and $d \ll 1$, and along the boundary between the low- and the high-power mode [18].

[5]In [22], it was shown that the use of a variable switching frequency f_s enables improved DAB efficiency.

[6]The EB ZVS analyses are typically based on constant energy-equivalent switch capacitances [10]. As this can result in significant errors [23], in this paper the voltage dependent nonlinear switch capacitances are correctly modeled using data-sheet small-signal measurements (see Section III).

TABLE I
CONVERTER SPECIFICATIONS AND REQUIREMENTS

Property		*Value*
ac side	$V_{\rm ac}$ ($V_{\rm rms}$)	230 (nominal) $207 \leqslant V_{\rm ac} \leqslant 253$
	$I_{\rm ac,P,nom}$ ($A_{\rm rms}$)	16 (nominal)
	$f_{\rm L}$ (Hz)	50
dc side	$V_{\rm dc2}$ (V)	$370 \leqslant V_{\rm dc2} \leqslant 470$
EMC compliance		CISPR 22 Class B
PF		> 0.9 (at $I_{\rm ac,P} \geqslant 0.1 \cdot I_{\rm ac,P,nom}$)

of "commutation inductance(s),"[7] which is implemented in the calculation procedure, is introduced as an essential element in achieving both full-operating-range ZVS and smooth, continuous mode transitions. As explained previously and reaffirmed in Section IV, these two objectives are normally problematic for DAB converters with large input and/or output voltage variations and large power variations such as is the case for the single-stage DAB ac–dc converter investigated in this paper.

The paper is further organized as follows. In Section II, after a brief discussion of the general operating principle of the single-stage DAB ac–dc converter, a simplified representation of the DAB converter is given and the operating modes are detailed. The implications on the model and the expressions by adding commutation inductance(s) in the HF ac-link are described. In Section III, the CDCB ZVS analysis is introduced, followed by the procedure to determine optimal ZVS modulation schemes and optimal system level component values in Section IV. In Section IV-B, the results obtained from numerical optimizations are given for different HF ac-link configurations, highlighting the necessity of commutation inductance(s) in achieving full-operating-range ZVS. The actual implementation of the calculated modulation schemes (see Section V-A) and the experimental results (see Ssection V-B) obtained from a 3.7 kW, bidirectional, and unity power factor 1-S DAB ac–dc prototype system are presented in Section V.

The specifications (see Table I) of the investigated DAB ac–dc converter shown in Fig. 1 are based on the requirements for future electric vehicle on-board battery chargers, interfacing a 400 V dc-bus with the single-phase 230 $V_{\rm rms}$/50 Hz mains. Compliance with domestic power sockets results in a nominal (active) ac input current of $I_{\rm ac,P} = 16\ A_{\rm rms}$ and a nominal power of $P_{\rm nom} = 3.7$ kW. The voltage ranges are further listed in Table I. The dc-bus voltage level was chosen based on the forecasts that the vehicular power system voltages tend to rise. Bidirectional power flow enables V2G functionality, while galvanic isolation ensures safety. Other requirements are a high conversion efficiency, a high power density, EMC compliance to the CISPR 22 Class B standard, a high power factor (PF), and low total harmonic distortion (THD) of the ac input current (see Table I).

[7]It has been mentioned in inter alia [9], [16], [18] that the magnetizing inductance of the transformer can be used to provide additional commutation charge in the switches. However, no detailed investigation (and subsequent modulation scheme) concerning EB (or CDCB) ZVS is given.

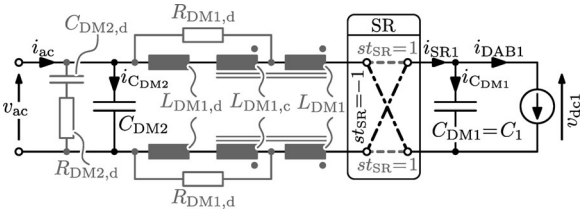

Fig. 2. Equivalent circuit of the converter's ac input side, with a controllable current source $i_{\rm DAB1}$, the SR, and the two-stage DM EMC filter.

II. ANALYSIS OF THE DAB MODEL

A. DAB ac–dc Converter Topology

Fig. 1 shows the schematic of the single-phase, single-stage, bidirectional and isolated DAB ac–dc converter topology, consisting of an SR followed by a DAB dc–dc converter. During operation, the state $st_{\rm SR}$ of the SR changes two times each period of the ac line voltage $v_{\rm ac}(t)$, according to

$$st_{\rm SR} = \begin{cases} 1 & \text{if } v_{\rm ac}(t) > 0 \ (\rm S_{SR,1} \ \& \ S_{SR,4} \text{ are on}) \\ -1 & \text{if } v_{\rm ac}(t) < 0 \ (\rm S_{SR,2} \ \& \ S_{SR,3} \text{ are on}). \end{cases} \quad (1)$$

Due to this continuous state change, the ac line voltage $v_{\rm ac}(t)$ is folded into a dc voltage $v_{\rm dc1}(t)$ that is pulsating twice the ac line frequency $f_{\rm L}$ (i.e., $v_{\rm dc1}(t) = |v_{\rm ac}(t)| = |\hat{V}_{\rm ac} \sin(\omega_{\rm L} t)|$) and that is directly fed to the input of the DAB dc–dc converter. Note that the voltage drop across the differential mode (DM) input filter inductors can be neglected in a steady state. As explained in Section II-B, the DAB draws a net dc current i_1 at its input. The HF components of i_1 are bypassed by a small HF filter capacitor C_1 that is placed between the SR and the DAB, while the dc component $i_{\rm DAB1}$ (not shown in Fig. 1) of i_1 propagates to the SR. In the *ideal case*, i.e., neglecting the reactive power consumed by the HF filter capacitor C_1,[8] the SR's output current $i_{\rm SR1}(t)$ equals $i_{\rm DAB1}(t)$. By proper modulation of the DAB's active bridges this current $i_{\rm DAB1}(t)$, and thus $i_{\rm SR1}(t)$, can be actively controlled to be in phase with $v_{\rm dc1}(t)$. As $i_{\rm SR1}(t)$ is unfolded toward the ac input side by the SR, a sinusoidal ac input current $i_{\rm ac}(t)$ that is in phase (unity power factor) with the ac input voltage $v_{\rm ac}(t)$ is obtained. However, in the *nonideal case,* the reactive (capacitive) power consumed by C_1 and by the other DM EMC input filter capacitor(s) needs to be compensated in order to meet the PFC requirement given in Table I. This can be done by controlling $i_{\rm DAB1}(t)$ slightly lagging to $v_{\rm dc1}(t)$, requiring a certain reactive power transfer capability of the DAB. For the exact calculation of $i_{\rm DAB1}(t)$, in Fig. 2 the DAB is represented by a variable current source $i_{\rm DAB1}$ connected in parallel with the DM EMC input filter and the SR (note that C_1 is the capacitive part of the first DM filter stage, $C_{\rm DM1} = C_1$). It can be shown[9] that for a given amplitude of the (active) ac input current $\hat{I}^*_{\rm ac,P}$ and PF ($=\cos(\varphi)$; see Fig. 3),

[8]Voltage $v_{\rm dc1}(t)$ induces a small capacitive current in C_1.
[9]In a steady state $i_{\rm SR1} = i_{\rm DAB1} + i_{C_{\rm DM1}}$ (see Figs. 1 and 2).

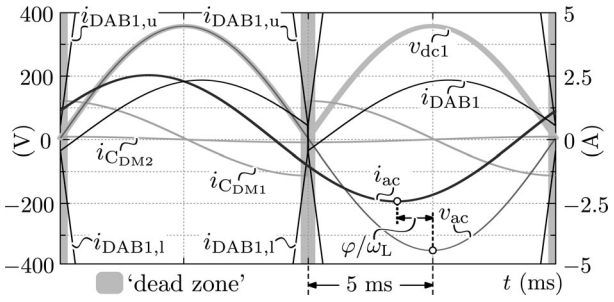

Fig. 3. Ideal input-side quantities for the worst case PF condition: $\hat{I}^*_{\mathrm{ac,P}} = \sqrt{2}\cdot 0.1\cdot I_{\mathrm{ac,P,nom}} = 2.26$ A; $\hat{V}_{\mathrm{ac}} = \hat{V}_{\mathrm{ac,max}} = 357.8$ V; PF $= 0.9$.

i_{DAB1} needs to be controlled according to

$$i_{\mathrm{DAB1}} = st_{\mathrm{SR}}\Big[dir\cdot(\hat{I}^*_{\mathrm{ac,P}}/\mathrm{PF})\sin(\omega_{\mathrm{L}}t + dir\cdot\arccos(\mathrm{PF})) - \omega_{\mathrm{L}}(C_{\mathrm{DM1}}+C_{\mathrm{DM2}})\hat{V}_{\mathrm{ac}}\sin(\omega_{\mathrm{L}}t+\pi/2)\Big] \quad (2)$$

where $\omega_{\mathrm{L}} = 2\pi f_{\mathrm{L}}$ with f_{L} the 50 Hz ac line frequency, $\hat{V}_{\mathrm{ac}}$ the amplitude of the ac input voltage, st_{SR} the state of the SR [according to (1)], and dir the power flow direction (see Fig. 1)

$$dir = \begin{cases} 1 & \text{if } p(t) > 0 : \text{prim.} \rightarrow \text{sec. side,} \\ -1 & \text{if } p(t) < 0 : \text{sec.} \rightarrow \text{prim. side.} \end{cases} \quad (3)$$

The ideal converter's input-side quantities for the worst case PF condition (Table I; $\hat{I}^*_{\mathrm{ac,P}} = \sqrt{2}\cdot 0.1\cdot I_{\mathrm{ac,P,nom}} = 2.26$ A; $\hat{V}_{\mathrm{ac}} = \hat{V}_{\mathrm{ac,max}} = 357.8$ V; PF $= 0.9$) are depicted in Fig. 3. The values of C_{DM1} $(=C_1)$ and C_{DM2} are listed in Table IV. In order to meet the PFC requirements (see Table I) under all input conditions, including enough current margin for component variances, an upper DAB input current limit $i_{\mathrm{DAB1,u}}$ is calculated. Assuming PF $= 1, dir = 1$, and $C_{\mathrm{DM1}} = C_{\mathrm{DM2}} = 0$, the instantaneous i_{DAB1} according to (2) becomes $i_{\mathrm{DAB1}} = st_{\mathrm{SR}}\hat{I}^*_{\mathrm{ac,P}}\sin(\omega_{\mathrm{L}}t) = |\hat{I}^*_{\mathrm{ac,P}}\sin(\omega_{\mathrm{L}}t)|$. This means that the i_{DAB1}, which corresponds with a certain value of the DAB input voltage $v_{\mathrm{dc1}} = |v_{\mathrm{ac}}| = |\hat{V}_{\mathrm{ac}}\sin(\omega_{\mathrm{L}}t)|$ and ac input current $\hat{I}^*_{\mathrm{ac,P}}$, can be calculated with $i_{\mathrm{DAB1}} = \hat{I}^*_{\mathrm{ac,P}}\cdot v_{\mathrm{dc1}}/\hat{V}_{\mathrm{ac}}$. Consequently i_{DAB1} at a certain v_{dc1} and for a certain $\hat{I}^*_{\mathrm{ac,P}}$ is highest if $\hat{V}_{\mathrm{ac}} = \hat{V}_{\mathrm{ac,min}}$. Using $\hat{I}^*_{\mathrm{ac,P}} = 24$ A $(=\sqrt{2}\cdot I_{\mathrm{ac,P,nom}} + \text{margin})$, adding a margin of 0.5 A, and clamping the result to 24 A, $i_{\mathrm{DAB1,u}}$ is defined as[10]

$$i_{\mathrm{DAB1,u}}(v_{\mathrm{dc1}}) = \min\left(\frac{24\cdot v_{\mathrm{dc1}}}{\hat{V}_{\mathrm{ac,min}}} + 0.5, 24\ \mathrm{A}\right). \quad (4)$$

Taking the lower limit $i_{\mathrm{DAB1,l}} = -i_{\mathrm{DAB1,u}}$ yields the complete converter's operating range[11] shown in Fig. 4. Note that the DAB handles the double-line frequency power component, which in the 2-S ac-dc topologies is buffered by the (electrolytic) dc-link capacitor. Due to the absence of this dc-link capacitor in the investigated single-stage converter, an electrolytic capacitor $C_{2,\mathrm{st}}$ was placed at the dc output side in order to (partly) filter the 100-Hz power component.

[10]Given the specifications in Table I, the current margins were chosen to be able to satisfy (2) at any possible input condition (V_{ac}, $I_{\mathrm{ac,P}}$, and PF) that may occur, taking into account component variances. The selection of the margins thus depends on the final hardware design.

[11]Around the zero crossing (-30 V$\leqslant v_{\mathrm{ac}} \leqslant 30$ V) the bridges of the DAB are inactive (dead zone) as ZVS power conversion is quasi-impossible within this voltage interval (see also Section IV).

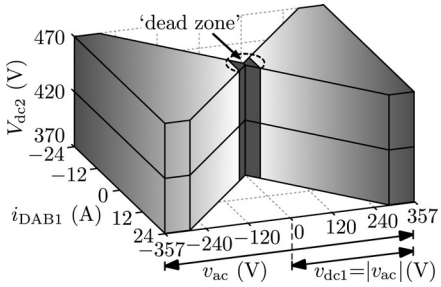

Fig. 4. Complete operating range of the investigated DAB converter.

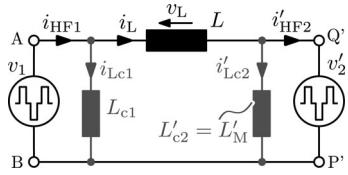

Fig. 5. Simplified (lossless) electrical model of the DAB.

B. Simplified DAB Model

The DAB in Fig. 1 comprises HF transformer-coupled primary and secondary side full bridges, performing the PFC [via active control of i_{DAB1} according to (2)] and the regulation of dc output voltage V_{dc2}. Therefore, they produce phase-shifted edge resonant square wave voltages v_1 and v_2 at the terminals of the HF ac-link (inductor L and HF transformer), resulting in an inductor current i_{L}. Both active bridges act as ac–dc converters to their respective dc side, transforming the ac currents i_{HF1} and i_{HF2} into net dc currents i_1 and i_2. Filter capacitors C_1 and C_2 bypass the HF components of i_1 and i_2. The respective dc components (i_{DAB1} and i_{DAB2}; not shown in Fig. 1) propagate to the input and the output of the DAB, and are obtained by averaging $i_1(t)$, respectively. $i_2(t)$ over the one switching period $T_{\mathrm{s}} = 1/fs$, e.g.

$$i_{\mathrm{DAB1}} = i_{1,\mathrm{avg}} = \frac{1}{T_{\mathrm{s}}}\int_{t_0}^{t_0+T_{\mathrm{s}}} i_1(t)\mathrm{d}t. \quad (5)$$

On the assumption of ideal components and by referring the model to the primary side of the transformer, a simplified (lossless) electrical representation of the DAB is obtained (see Fig. 5). The primary side referred voltage v'_2 is given by $v'_2 = v_2\cdot n_1/n_2$. By applying an appropriate phase shift angle[12] ϕ between the voltages v_1 and v'_2 and additionally adjusting the respective pulse width modulation angles τ_1 and τ_2 (i.e., DSPWM; τ_1, τ_2 are defined in Fig. 6), i_{DAB1} can be controlled. A last parameter that can be freely adjusted (within a reasonable

[12]The phase shift angle ϕ is defined as the angle between the first falling edge of v_1 and the first falling edge of v'_2 (see Fig. 6).

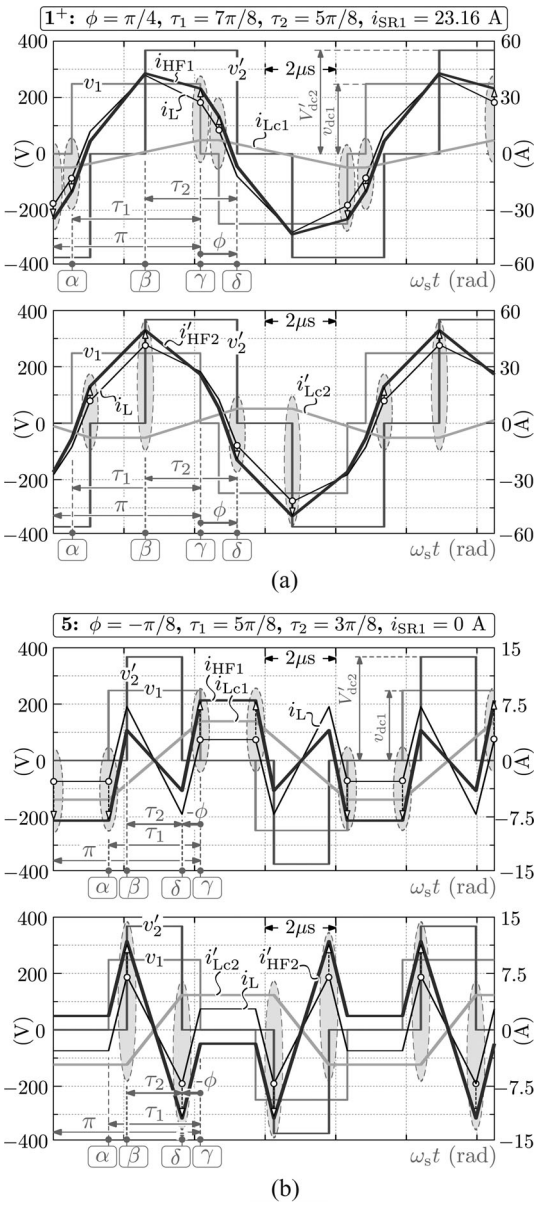

Fig. 6. Influence of L_{c1} and L_{c2} on the HF ac-link currents for (a) mode 1^+ and (b) mode 2, using the same conditions as in Fig. 7 (see caption). (a) Mode 1^+; with primary side commutation current (top inset); with secondary side commutation current (bottom inset). (b) Mode 2; with primary side commutation current (top inset); with secondary side commutation current (bottom inset).

range) is the switching frequency f_s, resulting in a total of four modulation parameters: $\mathbf{x} = (\phi, \tau_1, \tau_2, f_s)$.

C. Switching Modes and Commutation Inductance(s)

As presented in [12, Fig. 2], depending on the sequence in time of the falling and rising edges of the voltages v_1 and v_2', twelve different switching modes[13] can be generated with the DAB shown in Fig. 1. It is shown in Section IV that only two out of the twelve possible modes are feasible for efficient ZVS

[13]The total of 12 switching modes contains 4 unique modes for each power flow direction and 4 modes that are common for both power flow directions [12]; power flow direction, dir, according to (3) and Fig. 1.

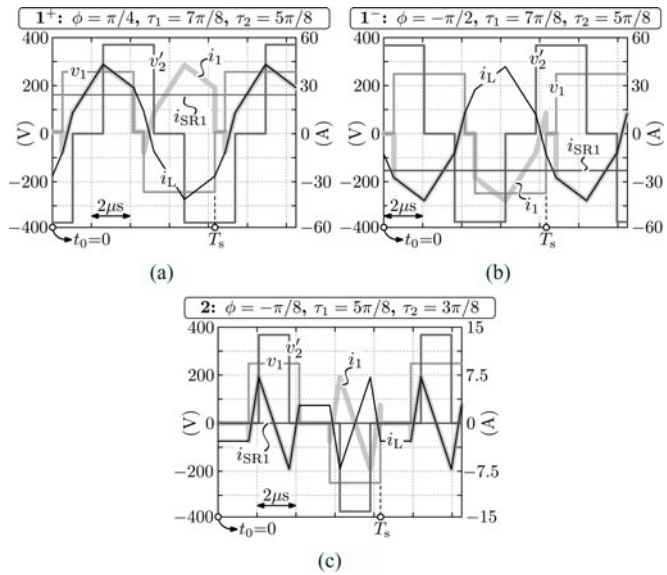

Fig. 7. Ideal voltage and current waveforms for (a) mode 1^+, (b) mode 1^-, and (c) mode 2. The waveforms are derived using: $v_{dc1} = 250$ V, $V_{dc2} = 370$ V, $L = 13\,\mu$H, $L_{c1} = L_{c2} = 62.1\,\mu$H, $n_1/n_2 = 1$, and $f_s = 120$ kHz.

operation. These two modes are further referred to as mode 1 (high power mode) and mode 2 (low power mode) and form the basis of the final modulation schemes derived in this paper. Mode 1 can be subdivided into a submode for positive power flow [i.e., mode 1^+; Fig. 7(a)] and a similar submode for negative power flow [i.e., mode 1^-; Fig. 7(b)], whereas mode 2 [see Fig. 7(c)] can be used for both positive and negative power flow. For the reason of clarity, below the mode equations are presented for mode 1^+ and mode 2 only.[14] Nevertheless, in the scope of the search toward optimal ZVS modulation schemes, the expressions for all 12 modes were derived and implemented.

It is explained in Section IV that, considering CDCB ZVS (see Section III) or EB ZVS, full-operating-range ZVS involving smooth mode transitions cannot be achieved with the traditional implementation of the DAB converter (i.e., a DAB with a transformer and optionally a series inductor L in the HF ac-link). To overcome this problem, an inductance can be placed in parallel with active bridge 1 (L_{c1}; between nodes A and B) and/or with active bridge 2 (L_{c2}; between nodes Q and P), as shown in Figs. 1 and 5. These bridge-paralleled inductances, which are further referred to as *commutation inductances*, always have a beneficial contribution to the ZVS conditions due to the injection of a small reactive current[15] in the respective bridge (i.e., i_{Lc1} resp. i_{Lc2}, Fig. 6)[16]. In the following, L_{c2} is implemented by the magnetizing inductance of the transformer ($L_{c2} = L_M$), avoiding the increased volume and costs. Different scenarios (i.e., using zero, one, or two commutation inductances) are discussed in Section IV-B.

[14]Note that the equations for mode 1^- are similar to those of mode 1^+.

[15]The addition of commutation inductance(s) does not necessarily lead to higher conduction losses since the freedom to optimally control $\mathbf{x}$ under ZVS conditions becomes bigger.

[16]Although only shown for mode 1^+ and mode 2, commutation inductances L_{c1} and L_{c2} benefit the ZVS commutation for all 12 switching modes.

TABLE II
HF AC-LINK CURRENTS i_{L}, i_{Lc1}, AND i'_{Lc2} FOR MODE 1^+ AND MODE 2

Mode 1^+	i_{L}	i_{Lc1}	i'_{Lc2}
α	$\frac{v_{\mathrm{dc1}}\left(d(-\tau_1+\tau_2/2-\phi+\pi)-\tau_1/2\right)}{\omega_{\mathrm{s}}L}$	$\frac{-v_{\mathrm{dc1}}\tau_1/2}{\omega_{\mathrm{s}}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{dc2}}\left(\tau_1-\tau_2/2+\phi-\pi\right)}{\omega_{\mathrm{s}}L'_{\mathrm{c2}}}$
β	$\frac{v_{\mathrm{dc1}}\left(d\tau_2/2+\tau_1/2-\tau_2+\phi\right)}{\omega_{\mathrm{s}}L}$	$\frac{v_{\mathrm{dc1}}\left(\tau_1/2-\tau_2+\phi\right)}{\omega_{\mathrm{s}}L_{\mathrm{c1}}}$	$\frac{-V'_{\mathrm{dc2}}\tau_2/2}{\omega_{\mathrm{s}}L'_{\mathrm{c2}}}$
γ	$\frac{v_{\mathrm{dc1}}\left(d(-\tau_2/2+\phi)+\tau_1/2\right)}{\omega_{\mathrm{s}}L}$	$\frac{v_{\mathrm{dc1}}\tau_1/2}{\omega_{\mathrm{s}}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{dc2}}\left(\tau_2/2-\phi\right)}{\omega_{\mathrm{s}}L'_{\mathrm{c2}}}$
δ	$\frac{v_{\mathrm{dc1}}\left(-d\tau_2/2-\tau_1/2-\phi+\pi\right)}{\omega_{\mathrm{s}}L}$	$\frac{v_{\mathrm{dc1}}\left(-\tau_1/2-\phi+\pi\right)}{\omega_{\mathrm{s}}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{dc2}}\tau_2/2}{\omega_{\mathrm{s}}L'_{\mathrm{c2}}}$

Mode 2	i_{L}	i_{Lc1}	i'_{Lc2}
α	$\frac{v_{\mathrm{dc1}}\left(d\tau_2/2-\tau_1/2\right)}{\omega_{\mathrm{s}}L}$	$\frac{-v_{\mathrm{dc1}}\tau_1/2}{\omega_{\mathrm{s}}L_{\mathrm{c1}}}$	$\frac{-V'_{\mathrm{dc2}}\tau_2/2}{\omega_{\mathrm{s}}L'_{\mathrm{c2}}}$
β	$\frac{v_{\mathrm{dc1}}\left(d\tau_2/2+\tau_1/2-\tau_2+\phi\right)}{\omega_{\mathrm{s}}L}$	$\frac{v_{\mathrm{dc1}}\left(\tau_1/2-\tau_2+\phi\right)}{\omega_{\mathrm{s}}L_{\mathrm{c1}}}$	$\frac{-V'_{\mathrm{dc2}}\tau_2/2}{\omega_{\mathrm{s}}L'_{\mathrm{c2}}}$
γ	$\frac{v_{\mathrm{dc1}}\left(-d\tau_2/2+\tau_1/2\right)}{\omega_{\mathrm{s}}L}$	$\frac{v_{\mathrm{dc1}}\tau_1/2}{\omega_{\mathrm{s}}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{dc2}}\tau_2/2}{\omega_{\mathrm{s}}L'_{\mathrm{c2}}}$
δ	$\frac{v_{\mathrm{dc1}}\left(-d\tau_2/2+\tau_1+\phi\right)}{\omega_{\mathrm{s}}L}$	$\frac{v_{\mathrm{dc1}}\left(\tau_1/2+\phi\right)}{\omega_{\mathrm{s}}L_{\mathrm{c1}}}$	$\frac{V'_{\mathrm{dc2}}\tau_2/2}{\omega_{\mathrm{s}}L'_{\mathrm{c2}}}$

For the modulation parameter conventions shown in Fig. 6, the modulation parameter relations for achieving the mode 1^+ and mode 2 voltage patterns (i.e., the mode boundary conditions) are

$$\text{mode } 1^+: \quad -\tau_1+\pi \leqslant \phi \leqslant \tau_2 \tag{6}$$

$$\text{mode } 2: \quad \tau_2-\tau_1 \leqslant \phi \leqslant 0. \tag{7}$$

According to Fig. 5, neglecting the transformer leakage inductances $L_{\sigma 1}$ and $L_{\sigma 2}$, for each mode the dynamics of the currents $i_{\mathrm{L}}(t)$, $i_{\mathrm{Lc1}}(t)$, and $i'_{\mathrm{Lc2}}(t)$ can, respectively, be expressed as

$$\frac{\mathrm{d}i_{\mathrm{L}}(t)}{\mathrm{d}t}=\frac{v_{\mathrm{L}}(t)}{L}, \quad \frac{\mathrm{d}i_{\mathrm{Lc1}}(t)}{\mathrm{d}t}=\frac{v_1(t)}{L_{\mathrm{c1}}}, \quad \text{and} \frac{\mathrm{d}i'_{\mathrm{Lc2}}(t)}{\mathrm{d}t}=\frac{v'_2(t)}{L'_{\mathrm{c2}}}$$

with $v_{\mathrm{L}}(t)=v_1(t)-v'_2(t)$. The bridge currents $i_{\mathrm{HF1}}(t)$ and $i_{\mathrm{HF2}}(t)$ are calculated using

$$i_{\mathrm{HF1}}(t)=i_{\mathrm{L}}(t)+i_{\mathrm{Lc1}}(t) \tag{8}$$

$$i_{\mathrm{HF2}}(t)=i'_{\mathrm{HF2}}(t)\cdot\frac{n_1}{n_2}=\left(i_{\mathrm{L}}(t)-i'_{\mathrm{Lc2}}(t)\right)\cdot\frac{n_1}{n_2}. \tag{9}$$

Solving above equations in each interval within half the switching period $T_{\mathrm{s}}/2$, as defined in Fig. 6, under the assumption of steady-state operation (i.e., $i_{\mathrm{L}}(t)=-i_{\mathrm{L}}(t+T_{\mathrm{s}}/2)$; $i_{\mathrm{Lc1}}(t)=-i_{\mathrm{Lc1}}(t+T_{\mathrm{s}}/2)$; and $i'_{\mathrm{Lc2}}(t)=-i'_{\mathrm{Lc2}}(t+T_{\mathrm{s}}/2)$), and evaluating the resulting systems of equations yields the expressions in Table II for the HF ac-link currents at the different switching instances $\theta_i=\{\alpha,\beta,\gamma,\text{and }\delta\}$[17], where $\theta=\omega_{\mathrm{s}}t$, with $\omega_{\mathrm{s}}=2\pi f_{\mathrm{s}}$, and f_{s} the switching frequency. V'_{dc2} is the primary side referred dc output voltage, and d the primary side referred voltage conversion ratio: $d=V'_{\mathrm{dc2}}/v_{\mathrm{dc1}}$. Currents i_1 and i_2 can be derived from i_{HF1} and i_{HF2}, respectively, by analyzing the conduction states[18] of the switches S_{xx}. Applying (5), the expressions for the instantaneous DAB input current i_{DAB1} respectively for

[17] α and β correspond with the positive rising edge of respectively v_1 and v'_2 while γ and δ correspond with the respective positive falling edges (Fig. 6).

[18] The conduction states can be found in [9], Fig. 4.

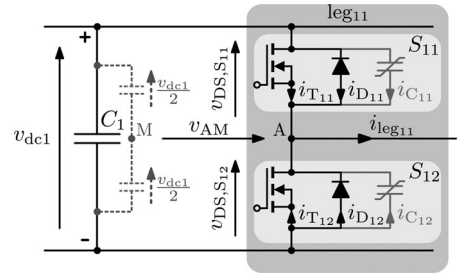

Fig. 8. Bridge leg of the DAB converter.

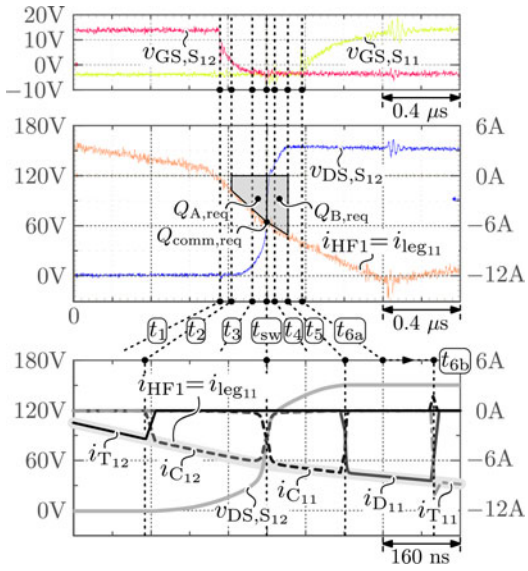

Fig. 9. Example of a commutation of current $i_{\mathrm{leg}_{11}}=i_{\mathrm{HF1}}$ from the bottom switch S_{12} to the top switch S_{11} of bridge leg_{11}. The dc-bus voltage of the bridge, v_{dc1}, is 150 V for this example.

mode 1^+ and mode 2 are

$$i_{\mathrm{DAB1},1^+}=\frac{-V'_{\mathrm{dc2}}}{2\omega_{\mathrm{s}}L\pi}\cdot\left((\phi-\tau_2)^2+(\phi+\tau_1)^2-\tau_1\tau_2+\pi(\pi-2(\tau_1+\phi))\right) \tag{10}$$

$$i_{\mathrm{DAB1},2}=\frac{-V'_{\mathrm{dc2}}}{2\omega_{\mathrm{s}}L\pi}\cdot\left(\tau_2^2-\tau_1\tau_2-2\tau_2\phi\right). \tag{11}$$

The DAB input power $p_1(t)$ over one switching cycle T_{s} can now be calculated with

$$p_1(t)=i_{\mathrm{DAB1}}(t)v_{\mathrm{dc1}}(t). \tag{12}$$

Commutation inductances L_{c1} and L_{c2} do not contribute to the power transfer and are therefore not present in any of the expressions for i_{DAB1} and p_1.

III. CURRENT-DEPENDENT CHARGE-BASED ZVS (CDCB ZVS)

The zero voltage switching (ZVS) principle is explained using Figs. 8 and 9, considering the commutation of current $i_{\mathrm{leg}_{11}}=i_{\mathrm{HF1}}$ from the bottom switch S_{12} to the top switch[19]

[19] The same principle applies for commutation from the top to the bottom switch of leg_{11}.

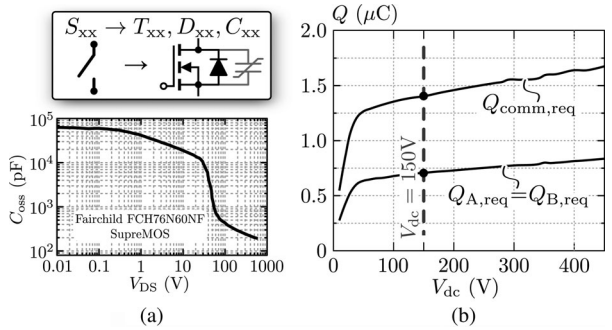

Fig. 10. (a) Top inset: representation of the HF high-voltage switches S_{xx} (MOSFETs) of the DAB's active bridges. Bottom inset: parasitic output capacitance $C_{oss}(V_{ds})$ of the used MOSFETs. (b) Charges required to achieve a voltage change of the full dc-bus voltage (V_{dc}) and of half the dc-bus voltage ($V_{DC}/2$) during commutation of a bridge leg (i.e., charging/discharging of the parasitic leg capacitance C_{leg}). The 150-V line corresponds with the example in Fig. 9.

S_{11} of bridge leg_{11} ($i_{\text{leg}_{11}}$ is negative at the switching instant t_{sw}; Fig. 9). As shown in Fig. 10(a) (top inset), each switch[20] S_{xx} consists of a power transistor T_{xx}, a diode D_{xx}, and a nonlinear parasitic capacitance C_{xx} (i.e., $C_{oss}(V_{DS})$; Fig. 10(a), bottom inset). The total parasitic leg capacitance to be considered for the commutation is highly nonlinear and can be calculated with

$$C_{\text{leg}_{11}}(v_{AM}) = C_{12}(v_{DS,S_{12}}) + C_{11}(v_{DS,S_{11}}) \quad (13)$$

$$v_{AM}(t) = v_{DS,S_{12}}(t) - \frac{v_{dc1}}{2} \quad (14)$$

$$v_{dc1} = v_{DS,S_{11}}(t) + v_{DS,S_{12}}(t). \quad (15)$$

The top inset of Fig. 9 depicts the measured gate voltages of the two leg switches, while the middle inset shows the measured leg current $i_{\text{leg}_{11}} (= i_{HF1})$ and the measured drain-to-source voltage $v_{DS,S_{12}}$ of the bottom switch S_{12}. The simulation in Fig. 9 (bottom inset), performed using the same conditions as for the measurements, is a zoomed image (finer time scale) of the middle figure inset, enabling discussion of the currents (according to Fig. 8) flowing in the individual switch components (T_{xx}, D_{xx}, and C_{xx}).

Quasi-lossless ZVS turn-off: At time instant t_1 (see Fig. 9) the gate of switch S_{12}, carrying a positive drain-to-source current ($i_{DS,S_{12}}(t = t_1) = -i_{T_{12}}(t = t_1) = -i_{\text{leg}_{11}}(t = t_1) > 0$), is turned OFF. After a small delay ($= t_2 - t_1$), the gate threshold voltage is reached and the channel resistance $R_{DS,S_{12}}$ of S_{12} starts to increase rapidly. This causes the leg current $i_{\text{leg}_{11}}$ to start flowing through $C_{\text{leg}_{11}}$ (current divider network consisting of $R_{DS,S_{12}}$ and $C_{\text{leg}_{11}}$), and in particular through C_{12} [$i_{C_{12}} \approx i_{\text{leg}_{11}}$, Fig. 9 (bottom inset); C_{12} is big and C_{11} is small at low $v_{DS,S_{12}}$, Fig. 10(a) (bottom inset)]. Quasi-lossless turn-off of switch S_{12} is achieved if the drain-source channel of T_{12} is fully opened before $i_{\text{leg}_{11}}$ has provided enough charge to $C_{\text{leg}_{11}}$ for causing a significant rise of drain-to-source voltage $v_{DS,S_{12}}$ (quasi-zero voltage turn-off of switch S_{12}). This can be seen in Fig. 9 where at time instant t_3 the gate of S_{12} is completely

[20]In this study metaloxidesemiconductor field-effect transistors (MOSFETs) are considered.

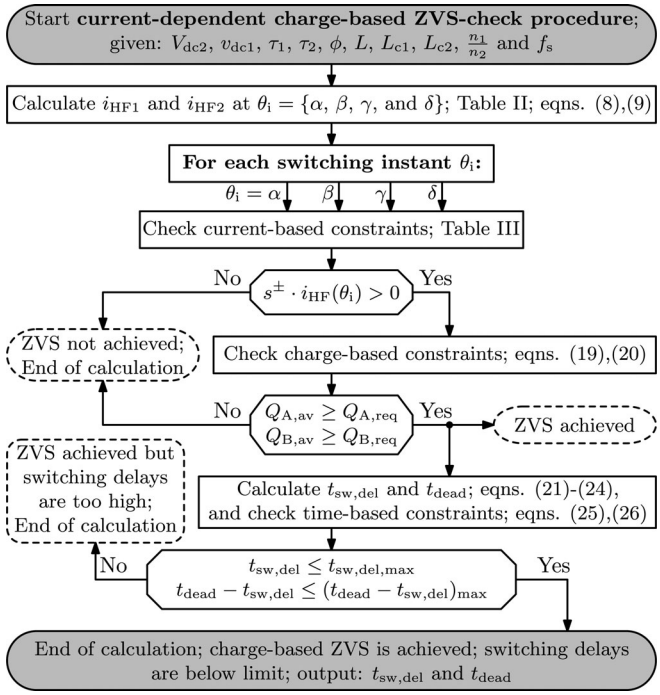

Fig. 11. Procedure to check if current-dependent charge-based (CDCB) ZVS is achieved and if the switching delays are below an upper limit.

OFF while $v_{DS,S_{12}}$ is still low (C_{12} is bypassing $i_{\text{leg}_{11}}$, keeping $v_{DS,S_{12}}$ low at turn-off).

Quasi-lossless ZVS turn-on: After time instant t_2 (see Fig. 9) a resonance occurs between $C_{\text{leg}_{11}}$ and the HF ac-link inductances during which $C_{\text{leg}_{11}}$ is charged by $i_{\text{leg}_{11}}$ (t_2–t_5). Due to the resulting increase of $v_{DS,S_{12}}$, the value of C_{12} drops while that of C_{11} rises, causing the leg current $i_{\text{leg}_{11}}$ to transfer from C_{12} to C_{11} [around t_{sw}, Fig. 9 (bottom inset)]. At t_5 the resonant transition completes ($v_{DS,S_{12}}$ has reached the dc-bus voltage v_{dc1}), putting diode D_{11} into conduction. Now, transistor T_{11} can be turned on under (quasi) zero voltage (time instant t_6; anti-parallel diode is conducting). ZVS turn-on is thus achieved when the resonant transition (t_2–t_5) of drain-to-source voltage $v_{DS,S_{12}}$ from ≈ 0 V to v_{dc1} completes before switch S_{11} is turned ON. This requires a negative leg current (i.e., into the leg) at minimum (see further).

Procedure for verifying CDCB ZVS: Based on above considerations a general procedure is introduced in order for a given set of input parameters ($V_{dc2}, v_{dc1}, \tau_1, \tau_2, \phi, L, L_{c1}, L_{c2}, n_1/n_2$ and f_s) to ascertain whether quasi-lossless ZVS commutation is achieved in all DAB bridges. Fig. 11 summarizes the complete procedure which relies on a *current-dependent charge-based ZVS analysis*.

Step 1: Starting from the given set of input parameters, i_{HF1} and i_{HF2} at the different switching instances $\theta_i = \{\alpha, \beta, \gamma, \text{and } \delta\}$ are calculated using the expressions in Table II and (8)–(9). The sign of these currents is verified, keeping in mind that for the commutation from a bottom switch to a top switch of a bridge leg, the current needs to flow into the leg (charging of C_{leg}) and out of the leg (discharging of C_{leg}) when commutation from top to bottom switching is required. By inspecting the waveforms

TABLE III
CB AND EB ZVS CONSTRAINTS

Edge type	Multiplier	CB ZVS	EB ZVS acc. to [10]
Pos. rising edge of v_1	$s^{\pm}=-1$	$s^{\pm}\cdot i_{\mathrm{HF1}}(\alpha)>0$	$s^{\pm}\cdot i_{\mathrm{HF1}}(\alpha)>\frac{v_{\mathrm{dc1}}}{\sqrt{\frac{L}{C_{\mathrm{Eeq,p}}}}}$
Pos. falling edge of v_1	$s^{\pm}=1$	$s^{\pm}\cdot i_{\mathrm{HF1}}(\gamma)>0$	$s^{\pm}\cdot i_{\mathrm{HF1}}(\gamma)>\frac{v_{\mathrm{dc1}}}{\sqrt{\frac{L}{C_{\mathrm{Eeq,p}}}}}$
Pos. rising edge of v_2	$s^{\pm}=1$	$s^{\pm}\cdot i_{\mathrm{HF2}}(\beta)>0$	$s^{\pm}\cdot i_{\mathrm{HF2}}(\beta)>\frac{V_{\mathrm{dc2}}}{\sqrt{\frac{L}{C_{\mathrm{Eeq,s}}}}}$
Pos. falling edge of v_2	$s^{\pm}=-1$	$s^{\pm}\cdot i_{\mathrm{HF2}}(\delta)>0$	$s^{\pm}\cdot i_{\mathrm{HF2}}(\delta)>\frac{V_{\mathrm{dc2}}}{\sqrt{\frac{L}{C_{\mathrm{Eeq,s}}}}}$

in Fig. 6 this yields the set of *CB constraints* listed in Table III (CB ZVS).

Step 2: The total charge needed to complete the commutation of a bridge leg (charging/discharging of C_{leg}), $Q_{\mathrm{comm,req}}(V_{\mathrm{dc}})$, can be subdivided into charges $Q_{\mathrm{A,req}}(V_{\mathrm{dc}})$ and $Q_{\mathrm{B,req}}(V_{\mathrm{dc}})$, each required to achieve a voltage change of half the dc-bus voltage ($V_{\mathrm{DC}}/2$)

$$Q_{\mathrm{A,req}}(V_{\mathrm{dc}})=Q_{\mathrm{B,req}}(V_{\mathrm{dc}})=\frac{Q_{\mathrm{comm,req}}(V_{\mathrm{dc}})}{2}. \tag{16}$$

$Q_{\mathrm{comm,req}}(V_{\mathrm{dc}})$, $Q_{\mathrm{A,req}}(V_{\mathrm{dc}})$, and $Q_{\mathrm{B,req}}(V_{\mathrm{dc}})$ for the used MOSFETs[21] are depicted in Fig. 10(b) which was obtained using the circuit simulator GeckoCIRCUITS$^{\mathrm{TM}}$ [24], where a nonlinear capacitor $C(u)$ that is based on small-signal measurements (such as in Fig. 10(a), bottom inset) can be directly employed [23]. Note that $Q_{\mathrm{comm,req}}$, $Q_{\mathrm{A,req}}$, and $Q_{\mathrm{B,req}}$ do not only depend on V_{dc} but also slightly on the leg current. Therefore, they are derived based on an average $i_{\mathrm{leg,AVG}}$, applying a margin ($0.05\,\mu$C and $0.1\,\mu$C) for component variances and circuit imperfections

$$Q_{\mathrm{comm,req}}(V_{\mathrm{dc}})=Q_{\mathrm{comm}}(V_{\mathrm{dc}},i_{\mathrm{leg,AVG}})+0.1\,\mu\mathrm{C} \tag{17}$$

$$Q_{\mathrm{A/B,req}}(V_{\mathrm{dc}})=Q_{\mathrm{A/B}}(V_{\mathrm{dc}},i_{\mathrm{leg,AVG}})+0.05\,\mu\mathrm{C}. \tag{18}$$

Lossless ZVS commutation of a bridge leg occurs when the charges $Q_{\mathrm{A,av}}$ and $Q_{\mathrm{B,av}}$ which are available in the leg-current before (i.e., $Q_{\mathrm{A,av}}$) and after (i.e., $Q_{\mathrm{B,av}}$) the switching instant θ_i are higher than or equal to, respectively, $Q_{\mathrm{A,req}}(V_{\mathrm{dc}})$ and $Q_{\mathrm{B,req}}(V_{\mathrm{dc}})$. $Q_{\mathrm{A,av}}$ and $Q_{\mathrm{B,av}}$ are calculated using, respectively, a backward and a forward integration of the leg current, starting at θ_i

$$Q_{\mathrm{A,av}}=s^{\pm}\cdot\left[\left(\sum_{j=1}^{n_{\mathrm{B}}}\int_{\theta_{i-j+1}}^{\theta_{i-j}}\frac{i_{\mathrm{HF}}}{\omega_{\mathrm{s}}}\mathrm{d}\theta\right)+\int_{\theta_{i-n_{\mathrm{B}}}}^{\theta_x}\frac{i_{\mathrm{HF}}}{\omega_{\mathrm{s}}}\mathrm{d}\theta\right]\geqslant Q_{\mathrm{A,req}} \tag{19}$$

$$Q_{\mathrm{B,av}}=s^{\pm}\cdot\left[\left(\sum_{j=1}^{m_{\mathrm{F}}}\int_{\theta_{i+j-1}}^{\theta_{i+j}}\frac{-i_{\mathrm{HF}}}{\omega_{\mathrm{s}}}\mathrm{d}\theta\right)+\int_{\theta_{i+m_{\mathrm{F}}}}^{\theta_y}\frac{-i_{\mathrm{HF}}}{\omega_{\mathrm{s}}}\mathrm{d}\theta\right]\geqslant Q_{\mathrm{B,req}} \tag{20}$$

with:

1) θ_x first instant prior to θ_i where i_{HF} crosses zero;
2) θ_y first instant after θ_i where i_{HF} crosses zero;
3) $\theta_{\mathrm{i-j}}$ and $\theta_{\mathrm{i+j}}$ switching instances of the three remaining bridges;
4) n_{B} number of switching instances between θ_x and θ_i;
5) m_{F} number of switching instances between θ_i and θ_y;
6) $i_{\mathrm{HF}}=i_{\mathrm{HF1}}$ for $\theta_i=\{\alpha,\gamma\}$, $i_{\mathrm{HF}}=i_{\mathrm{HF2}}$ for $\theta_i=\{\beta,\delta\}$.

These *CDCB constraints* need to be met at each switching instant $\theta_i=\{\alpha,\beta,\gamma,\text{ and }\delta\}$. θ_x, θ_y, n_{B}, and m_{F} are calculated using the given set of input parameters.

Step 3: In order to achieve switching at the predicted moment, the switching delay $t_{\mathrm{sw,del}}$ ($=t_{\mathrm{sw}}-t_2$, Fig. 9) has to be dynamically compensated in the controller. Moreover, a dynamic deadtime (t_{dead}) adaptation is required for each bridge leg, avoiding back commutation. At each switching instant θ_i, $t_{\mathrm{sw,del}}$ and t_{dead} are, respectively, calculated as

$$t_{\mathrm{sw,del}}=\frac{\theta_i-\theta_A}{\omega_{\mathrm{s}}} \tag{21}$$

$$t_{\mathrm{dead}}=\frac{\theta_B-\theta_A}{\omega_{\mathrm{s}}} \tag{22}$$

where θ_{A} and θ_{B} are the instances where the backward and forward integration [(19) and (20); starting point θ_i] of the corresponding leg current equals the charge needed to achieve a voltage change of half the dc-bus voltage ($V_{\mathrm{dc}}/2$). θ_{A} and θ_{B} are found by, respectively, solving

$$s^{\pm}\cdot\int_{\theta_i}^{\theta_A}\frac{i_{\mathrm{HF}}}{\omega_{\mathrm{s}}}\mathrm{d}\theta=Q_{\mathrm{A,req}} \tag{23}$$

$$s^{\pm}\cdot\int_{\theta_i}^{\theta_B}\frac{-i_{\mathrm{HF}}}{\omega_{\mathrm{s}}}\mathrm{d}\theta=Q_{\mathrm{B,req}}. \tag{24}$$

Step 4: Finally, it is verified if $t_{\mathrm{sw,del}}$ and ($t_{\mathrm{dead}}-t_{\mathrm{sw,del}}$) are smaller than an upper limit, avoiding too long commutation delays. This yields a set of *time-based constraints*[22]

$$t_{\mathrm{sw,del}}\leqslant t_{\mathrm{sw,del,max}} \tag{25}$$

$$t_{\mathrm{dead}}-t_{\mathrm{sw,del}}\leqslant(t_{\mathrm{dead}}-t_{\mathrm{sw,del}})_{\mathrm{max}}. \tag{26}$$

The error due to the linear approximation of the HF ac-link currents is small as, due to the strong nonlinearity of the leg capacitances, the energy transfer to and from the capacitances during commutation is almost fully concentrated in time intervals t_2–t_3 and t_4–t_5 (see Fig. 9). During these intervals $v_{\mathrm{DS,S_{12}}}$ remains quasi-constant. Therefore, the momentaneous resonant transition has a negligible influence on the linear shape of the HF ac-link currents (see Figs. 9 and 21) and the expressions in Table II are still valid. Qausi simultaneously with this study, a similar charge-based ZVS analysis for a TCM PFC rectifier has been proposed in [25], strengthening the validity.

IV. OPTIMAL MODULATION SCHEMES

For determining an optimal modulation scheme for the DAB an optimization algorithm is proposed which is based on a

[21]The FAIRCHILD FCH76N60NF SupreMOS high voltage super-junction MOSFETs were selected for the active bridges of the final DAB converter prototype due to their excellent soft-switching performance, inter alia the nonlinear output capacitance, in combination with a low on-resistance.

[22]A reasonable value for these limits is 500 ns (for the used MOSFETs).

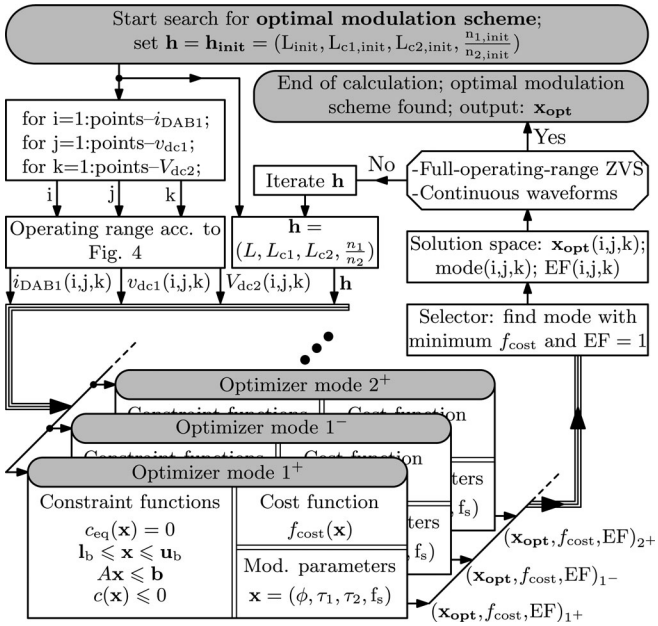

Fig. 12. Procedure to determine an optimal modulation scheme and the optimal modulation parameters $\mathbf{x_{opt}}$, using a constrained numerical optimization.

constrained numerical minimum search (i.e., a constrained nonlinear optimization[23]). Closed form solutions, such as presented in [12], for the optimal modulation parameters $\mathbf{x_{opt}} = (\phi_{opt}, \tau_{1,opt}, \tau_{2,opt}, f_{s,opt})$ are not directly feasible because of the three following reasons:

1) *User definability of the cost-function $f_{cost}(\mathbf{x})$:* according to their needs, users can predefine a cost function to be minimized. This allows us to include all converter related losses, but also requirements concerning system volume, weight, control, EMI,... A closed form solution for $\mathbf{x_{opt}}$ would require a fixed cost function.
2) *Discontinuity of the ZVS conditions:* the CDCB ZVS criterion (see Section III) introduces discontinuities [i.e., $0 \leqslant n_B, m_F \leqslant 3$, (19), (20)] in the constraints for ZVS, as well as additional boundaries due to the time-based constraints [(25), (26)].
3) *Increased complexity:* additional terms appear in the "mode equations" (see Section II-C) due to the inclusion of commutation inductances (L_{c1} and L_{c2}). Moreover, the use of a variable switching frequency adds a degree of freedom to modulate the active bridges of the DAB.

Fig. 12 summarizes the optimization procedure which starts from an initial set of circuit level variables $\mathbf{h} = \mathbf{h_{init}} = (L_{init}, L_{c1,init}, L_{c2,init}$, and $n_{1,init}/n_{2,init})$. Then, it iterates through the operating range, passing variables $i_{DAB1}(i,j,k), v_{dc1}(i,j,k), V_{dc2}(i,j,k)$, and $\mathbf{h}$ to the core algorithm. Here, for each switching mode an optimizer is applied to find the minimum of a cost function $f_{cost}(\mathbf{x})$, while satisfying the constraint functions for that mode. The results ($\mathbf{x_{opt}}, f_{cost}$, and exitflag EF) from each mode optimizer are inputted to a selector for detecting which mode satisfies the constraint functions (i.e., exit flag EF $= 1$) and has the "best value" for the cost function, outputting $\mathbf{x_{opt}}(i,j,k)$, mode(i,j,k), and EF(i,j,k). The circuit level variables $\mathbf{h} = (L, L_{c1}, L_{c2},$ and$n_1/n_2)$ are varied in a top level iteration loop until full-operating-range ZVS is achieved (i.e., all EF $= 1$), and until the resulting solution is continuous (no discontinuous steps in $\mathbf{x_{opt}}$), yielding the optimal modulation scheme.

A. Implementation of the Constrained Nonlinear Optimization

First, for each mode the constraint functions and the cost function $f_{cost}(\mathbf{x})$ need to be defined.

1) Constraint Functions: These can be subdivided into:

1) functions describing the relation $i_{DAB1} = f(\mathbf{x})$; e.g. (10)–(11). These are nonlinear and can be rewritten to subject the optimizer to nonlinear equality $c_{eq}(\mathbf{x}) = 0$;
2) functions describing the physical limitations on $\mathbf{x}$ (e.g., $0 \leqslant \tau_1 \leqslant \pi$ and $f_{s,min} \leqslant f_s \leqslant f_{s,max}$). This yields a set of lower and upper bounds so that the solution of the optimization is always in the range $\mathbf{l_b} \leqslant \mathbf{x} \leqslant \mathbf{u_b}$;
3) functions describing the mode boundaries [e.g., (6)-(7)], assuring that the resulting $\mathbf{x_{opt}}$ for a certain mode does not result in a different mode of operation. These can be written as a set of linear inequalities, $A\mathbf{x} \leqslant \mathbf{b}$;
4) functions describing the ZVS[24] boundaries according to Section III (19)–(26) and Fig. 11. These can be written as nonlinear inequalities $c(\mathbf{x}) \leqslant 0$.

2) Cost Function $f_{cost}(\mathbf{x})$: For investigations of the DAB topology, most often converter losses are chosen for $f_{cost}(\mathbf{x})$, and the impact of HF losses caused by current harmonics is neglected in a first design phase [12], [17]. According to [11], [12], under ZVS operation, the transistor's conduction losses account for the biggest part ($> 50\%$) of the total converter losses. For this reason, only the DAB MOSFET conduction losses are considered for illustrating the optimization procedure proposed in this paper (similar to [12]). These are proportional to $(I_{HF1}^2 + I_{HF2}^2)$ as both active bridges use the same type of MOSFETs, yielding

$$f_{cost}(\mathbf{x}) = (I_{HF1}^2 + I_{HF2}^2). \tag{27}$$

3) Switching Frequency Range: An upper limit of $f_{s,max} = 120$ kHz was selected to accommodate a compact converter design without causing excessive switching frequency related losses such as conduction losses due to high-frequency effects, core losses, and switching losses. Moreover, thermal limitations apply at high-switching frequencies, resulting in an increased total converter volume. $f_{s,max}$ was chosen to stay well below these thermal limits. The choice of $f_{s,min}$ is based on design considerations related to the DM EMC input filter which is designed according to [26] and [27] for compliance to CISPR 22 Class B in the frequency range of 150 kHz – 30 MHz. A two-stage DM filter with optimized damping is selected (see Fig. 2, Table IV). $f_{s,min} = 75$ kHz, which is doubled toward

[23]The final algorithm was implemented in MATLAB^{TM} using the 'fmincon'-function of the Optimization Toolbox^{TM}, and verified using a Genetic Algorithm of the Global Optimization Toolbox^{TM}.

[24]The DAB operation is assumed/recommended to be, but not limited to ZVS. Alternatively hard-switching operation could be allowed and the switching losses could be included in the cost function.

TABLE IV
COMPONENT VALUES OF THE DM EMC FILTER

Stage 1		Stage 2	
L_{DM1} (μH)	34.6	$L_{\mathrm{DM2}} = L_{\mathrm{mains}}$ (μH)	5 … 150
$L_{\mathrm{DM1,d}}$ (μH)	6.9	C_{DM2} (μF)	1
$L_{\mathrm{DM1,c}}$ (μH)	1.64	$C_{\mathrm{DM2,d}}$ (μF)	0.47
$C_{\mathrm{DM1}} = C_1$ (μF)	13.2	$R_{\mathrm{DM2,d}}$ (Ohm)	20
$R_{\mathrm{DM1,d}}$ (Ohm)	0.19		

the input port of the DAB converter, is chosen so that $2 \cdot f_{\mathrm{s,min}}$ is well beyond the maximum second filter cut-off frequency, assuring enough margin to attenuate the lower HF harmonics of the input current. However, for an optimal DM filter design it might be advantageous to select $f_{\mathrm{s,min}}$ higher than 75 kHz, enabling higher filter cut-off frequencies [28]. Allowing a variable switching frequency has the same effect as changing the inductance values. Therefore, investigations with other inductances are implicitly covered.

4) Circuit Level Variables $\mathbf{h}$*:* For allowing a clear comparison of the different scenarios discussed in Section IV-B, n_1/n_2 and L are taken the same for each scenario:

Transformer's turns ratio: n_1/n_2 is determined such that $V'_{\mathrm{dc2,min}} > (\hat{v}_{\mathrm{dc1,max}} + 10V\mathrm{margin})$ is always satisfied.[25] Given the specifications in Table I, with $V'_{\mathrm{dc2,min}} = 370$ V (minimum primary side referred output voltage) and $\hat{v}_{\mathrm{dc1,max}} = 358$ V (maximum DAB input voltage), a ratio of $n_1/n_2 = 1$ is chosen. Note that the valley in V'_{dc2}, due to the 100-Hz voltage ripple occurs 45° out of phase with $\hat{v}_{\mathrm{dc1}}$.

Main inductance L: The maximum positive DAB input current[26] $i_{\mathrm{DAB1,max}}$ is achieved at $\tau_1 = \tau_2 = \pi$; $\phi = \pi/2$; mode 1^+ [12], and needs to be higher than the maximum required DAB input current according to (4)

$$\left(i_{\mathrm{DAB1,max}} = \frac{V_{\mathrm{dc2}}\frac{n_1}{n_2}}{8 f_{\mathrm{s}} L}\right) \geqslant (\max(i_{\mathrm{DAB1,u}}) = 24\ \mathrm{A}). \quad (28)$$

The upper limit of L can be calculated with (28) by setting $f_{\mathrm{s}} = f_{\mathrm{s,max}} = 120$ kHz, $V_{\mathrm{dc2}} = V_{\mathrm{dc2,min}} = 370$ V, $n_1/n_2 = 1$, yielding $L_{\mathrm{max}} = 16.06\,\mu$H. A good choice is to take $L_{\mathrm{init}} \approx (0.75 \ldots 0.85) \cdot L_{\mathrm{max}}$, i.e., leaving some margin to optimally modulate $\mathbf{x}$. The final value, $L = 13\,\mu$H, is the result of an iteration performed during the converter's design phase.

B. Results of the Numerical Optimizations

The search toward optimal modulation parameters $\mathbf{x_{opt}}$ using the proposed optimization procedure (see Fig. 12) is illustrated for different scenarios concerning commutation inductances (L_{c1} and L_{c2}) and ZVS conditions. For each scenario $\mathbf{x_{opt}}$ is calculated for the whole DAB operating range according to Fig. 4, applying $75\ \mathrm{kHz} \leqslant f_{\mathrm{s}} \leqslant 120\ \mathrm{kHz}$, $n_1/n_2 = 1$, and

[25]The DAB can also be operated with other settings (e.g., allowing $V'_{\mathrm{dc2,min}} \leqslant \hat{v}_{\mathrm{dc1,max}}$) [12]. For the 1-S DAB ac–dc converter, operated under variable d, this implies crossing of $d = 1$. However, in the vicinity of $d = 1$, CDCB ZVS is hard to obtain as the inductor volt-seconds product needed to achieve the required current crossing in interval $\beta - \delta$ (Fig. 6(b); low power mode) is too small. Low inductance values for L_{c1} and/or L_{c2} would be needed, leading to increased rms values of the HF ac-link currents.

[26]For maximum negative current: $\tau_1 = \tau_2 = \pi$; $\phi = \pi/2$; mode 1^-; this yields an equation similar to (28).

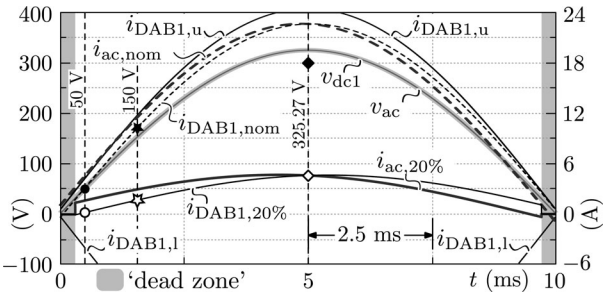

Fig. 13. DAB input currents i_{DAB1}, required to achieve $I_{\mathrm{ac,P}} = I_{\mathrm{ac,P,nom}} = 16\ \mathrm{A_{rms}}$; PF $= 0.999$, respectively, $I_{\mathrm{ac,P}} = 0.2 \cdot I_{\mathrm{ac,P,nom}} = 3.2\ \mathrm{A_{rms}}$; PF $= 0.983$. Here, $V_{\mathrm{ac}} = 230\ \mathrm{V_{rms}}$ (nominal ac input voltage). Vertical dashed lines: $v_{\mathrm{dc1}} = \{50\ \mathrm{V}; 150\ \mathrm{V}; 325.27\ \mathrm{V}\}$.

$L = 13\,\mu$H (cf. Section IV-A). Remind that the optimizer outputs $\mathbf{x_{opt}}$. Other quantities (graphs below) are calculated using $\mathbf{x_{opt}}$ in the analytical models of Section II.

1) Scenario 1, no Use of Commutation Inductances (Infinite L_{c1}*; Infinite* L_{c2}*):* This is the way the DAB converter is traditionally implemented: $i_{\mathrm{Lc1}}(t) = i_{\mathrm{Lc2}}(t) = 0$; $i_{\mathrm{HF1}}(t) = i_{\mathrm{L}}(t)$ according to (8); $i_{\mathrm{HF2}}(t) = i_{\mathrm{L}}(t) \cdot n_1/n_2$ according to (9); no injection of additional reactive currents in the active bridges of the DAB.

1st run: Illustratively the optimization is performed a first time applying the theoretical *CB ZVS constraints* (see Table III). In Fig. 14, the results for $\tau_{2,\mathrm{opt}}$ [see Fig. 14(a)] and $f_{\mathrm{s,opt}}$ [see Fig. 14(b)] at an output voltage of $V_{\mathrm{dc2}} = 400$ V are given as an example. Although the CB ZVS conditions are met within the whole operating range, the CDCB ZVS conditions (see Section III) are mostly violated as indicated by the ZVS areas in Fig. 14(c). The same goes for the EB ZVS constraints given in [10] (listed in Table III, EB ZVS). In Fig. 16(a) and (b), the trajectories (solid lines) of, respectively, the modulation angles and the switching frequency are depicted which are run through during a half-cycle of the nominal ac input voltage ($V_{\mathrm{ac}} = 230\ \mathrm{V_{rms}}$) at the nominal input current of $I_{\mathrm{ac,P}} = I_{\mathrm{ac,P,nom}} = 16\ \mathrm{A_{rms}}$ and a power factor of PF $= 0.999$ (according to Fig. 13). Fig. 16(c) and (d) (solid lines) show $s^{\pm} \cdot i_{\mathrm{HF1}}(\alpha)$ and $s^{\pm} \cdot i_{\mathrm{HF1}}(\gamma)$, respectively $s^{\pm} \cdot i_{\mathrm{HF2}}(\beta)$ and $s^{\pm} \cdot i_{\mathrm{HF2}}(\delta)$ which clearly satisfy the CB ZVS constraints (i.e. they need to be bigger than zero). However, they are below the limit for EB ZVS (according to [10]) during the major part of the half cycle. The same goes for the commutation charges[27] which do not reach the CDCB ZVS limit [according to equations (19), (20)], as shown in Fig. 16(e) and (f) (solid lines). The solution for $\mathbf{x_{opt}}$ is similar to the one presented in [12], validating the optimization algorithm. As expected, only mode 1 (low power mode) and mode 2 (high power mode) are used [see Fig. 16(a)]. Moreover, the modulation parameter trajectories are continuous.

2nd run: A second optimization is performed using the same conditions as in the first run, with the difference that now the optimizer is subjected to the *CDCB ZVS constraints* proposed in this paper (see Section III). From Fig. 15, it can be seen

[27]For convenience only $Q_{A,\mathrm{av}}$ and $Q_{\mathrm{B,av}}$ for commutation instances $\theta_i = \{\alpha$ and $\delta\}$ are shown, being the most critical for ZVS operation.

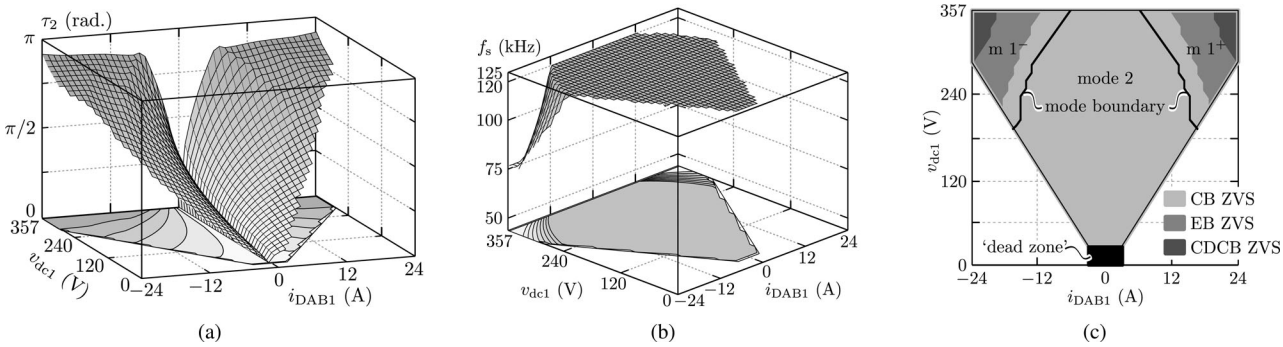

Fig. 14. Results of the numerical search for optimal modulation schemes according to scenario 1 (1^{st} run): no use of commutation inductances ($Lc1 = Lc2 = \infty$). The optimizer is subjected to the CB ZVS conditions, using all possible modes. The output voltage for this example is $V_{\mathrm{dc2}} = 400$ V.

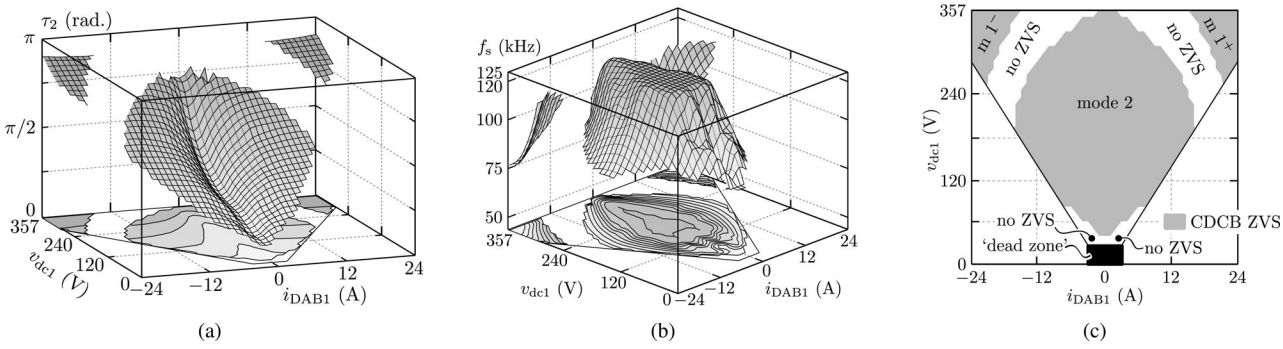

Fig. 15. Results of the numerical search for optimal modulation schemes according to scenario 1 (2^{nd} run): no use of commutation inductances ($Lc1 = Lc2 = \infty$). The optimizer is subjected to the CDCB ZVS conditions, using mode 1 and mode 2 only. The output voltage for this example is $V_{\mathrm{dc2}} = 400$ V.

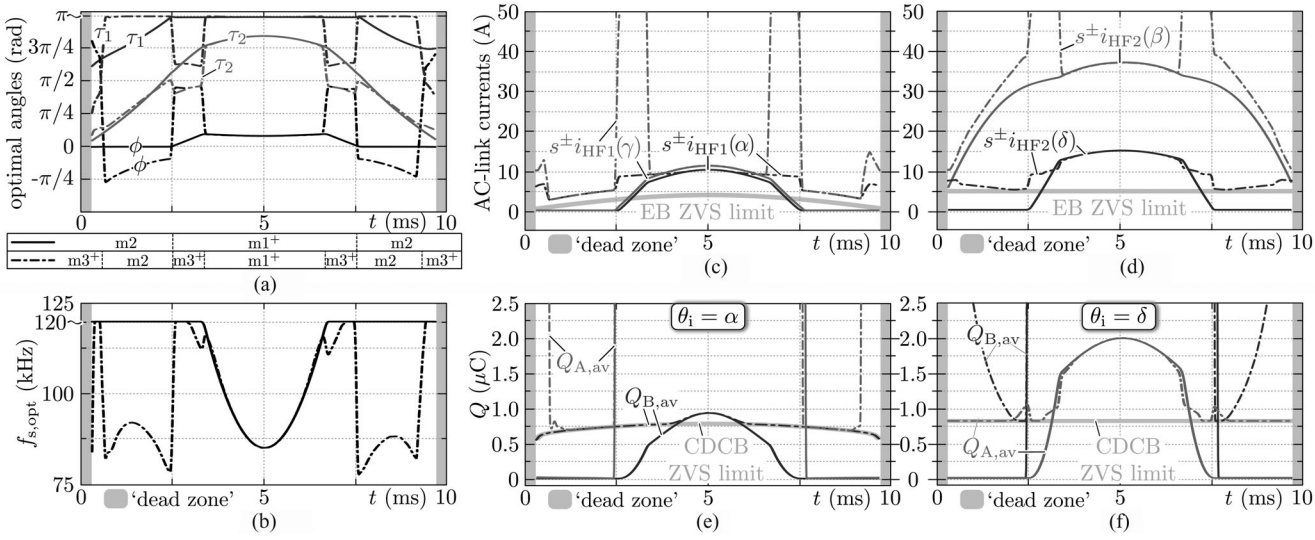

Fig. 16. AC trajectories for achieving $I_{\mathrm{ac,P}} = I_{\mathrm{ac,P,nom}} = 16\ \mathrm{A_{rms}}$, and PF $= 0.999$, at $V_{\mathrm{dc2}} = 400$ V (half cycle of the nominal ac input voltage $V_{\mathrm{ac}} = 230\ \mathrm{V_{rms}}$; according to Fig. 13). Solid lines: conditions cf. scenario 1, 1^{st} run (all modes included). Dot dashed lines: conditions cf. scenario 1, 2^{nd} run (all modes included).

that there are regions in the operating range (especially along the mode boundary and at low v_{dc1}) where the CDCB ZVS conditions cannot be met. Note that for the results in this figure, only mode 1 and mode 2 are used in the optimizer. In Fig. 16 (dot dashed lines), using all possible modes in the optimizer, these region are now covered by a very inefficient mode 3, resulting in full-operating-range CDCB ZVS [see Figs. 16(e) and (f)]. However, highly discontinuous modulation parameter trajectories and inefficient operation are obtained. It is a clear indication that it is impossible to achieve "efficient" (i.e., mode 1 and 2 only) full-operating-range CDCB ZVS with the traditional DAB (i.e., without L_{c1} and L_{c2}).

2) Scenario 2, Primary and Secondary Side Commutation Inductances (Fnite L_{c1}; Fnite L_{c2}): As proposed in this paper,

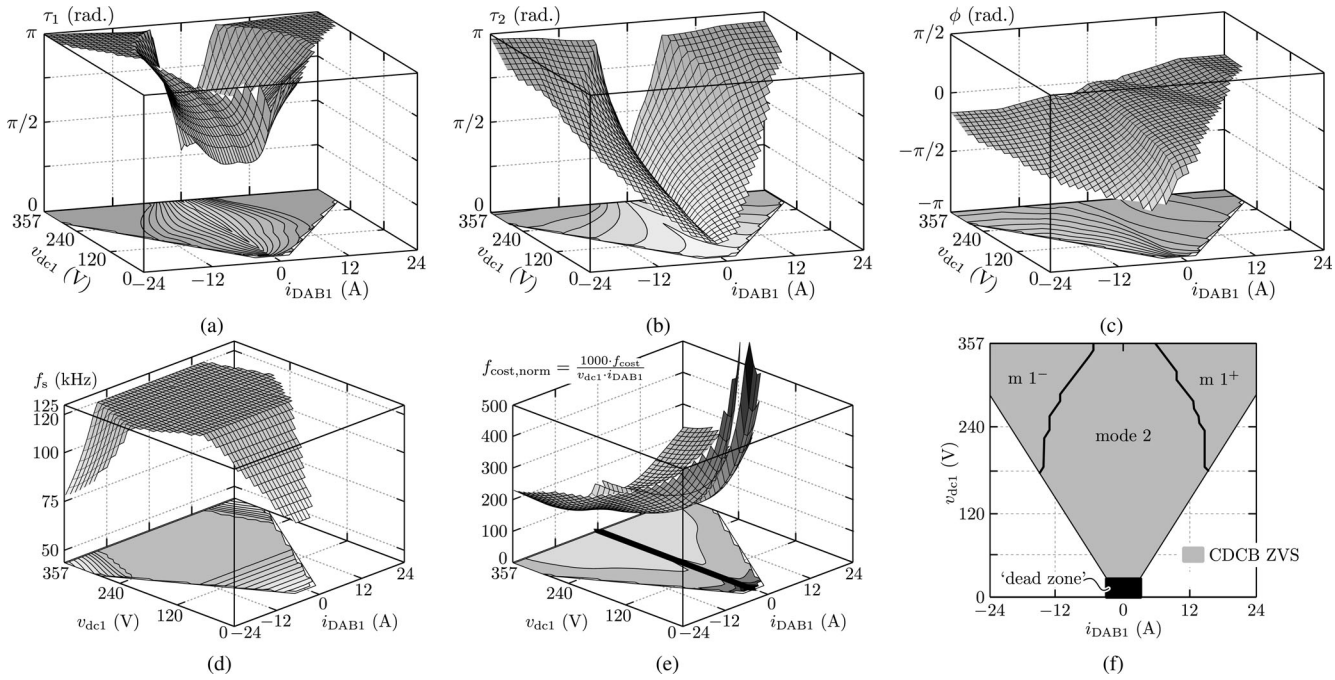

Fig. 17. Results of the numerical search for optimal modulation schemes according to scenario 2: primary and secondary side commutation inductances ($Lc1 = Lc2 = 62.1\mu$H). The optimizer is subjected to the CDCB ZVS conditions, using all possible modes and an output voltage of $V_{dc2} = V_{dc2,min} = 370$ V.

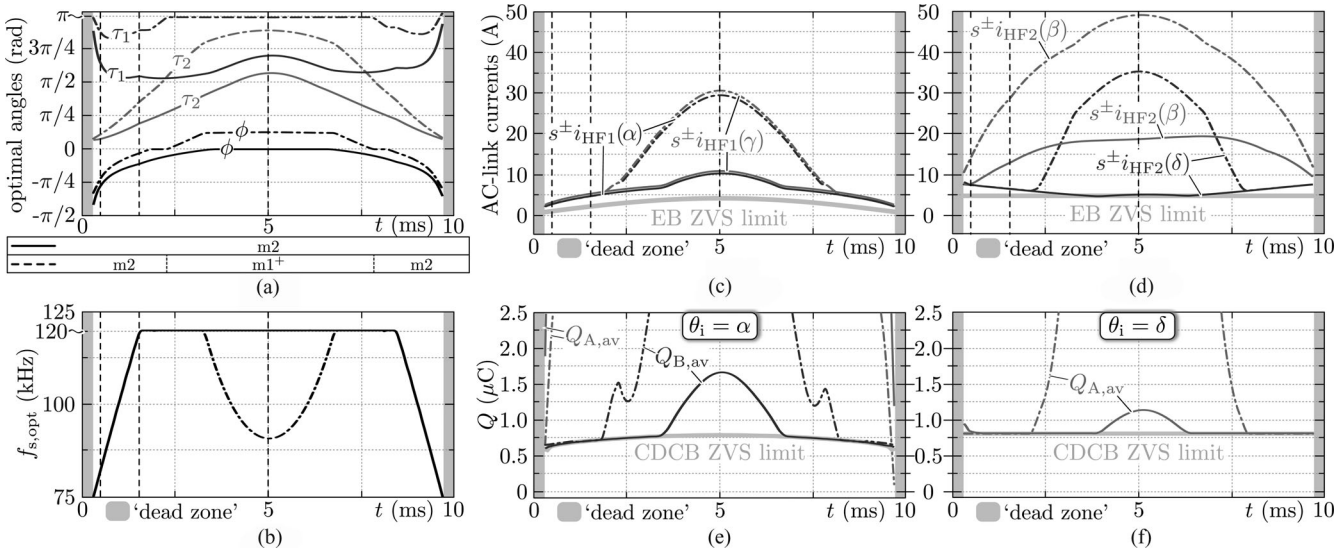

Fig. 18. AC trajectories for achieving $I_{ac,P} = I_{ac,P,nom} = 16$ A$_{rms}$, PF $= 0.999$ (dot dashed lines), and $I_{ac,P} = 0.2 \cdot I_{ac,P,nom} = 3.2$ A$_{rms}$, PF $= 0.983$ (solid lines), at $V_{dc2} = V_{dc2,min} = 370$ V (half-cycle of the nominal ac input voltage $V_{ac} = 230$ V$_{rms}$; according to Fig. 13). Conditions cf. scenario 2 (all modes included). Vertical dashed lines: $v_{dc1} = \{50\text{ V}; 150\text{ V}; 325.27\text{ V}\}$ cf. Fig. 13.

the DAB is now implemented with finite L_{c1} and L_{c2}, and the optimization (including all possible modes) is performed applying the *CDCB ZVS constraints* (see Section III). Equal commutation inductances are assumed, which are top-level-iterated until full-operating-range ZVS under the efficient modes 1 and 2 is achieved, yielding ($L_{c1} = L_{c2} = 62.1\mu$H). The results for the worst case output voltage $V_{dc2} = V_{dc2,min} = 370$ V and the nominal ac input voltage $V_{ac} = 230$ V$_{rms}$ are shown in Figs. 17 (full operating range) and 18 (ac trajectories for $I_{ac,P} = I_{ac,P,nom} = 16$ A$_{rms}$; PF $= 0.999$; dot dashed lines, and for $I_{ac,P} = 0.2 \cdot I_{ac,P,nom} = 3.2$ A$_{rms}$; PF $= 0.983$; solid lines). Full-operating-range CDCB ZVS is achieved under efficient modes 1 and 2 only, while the modulation parameter trajectories are continuous. Similar results can be obtained using only one commutation inductance (i.e., finite L_{c1}, infinite L_{c2} or infinite L_{c1}, finite L_{c2}), which however yield more unbalanced HF ac-link current values. The case with infinite L_{c1}, finite L_{c2} for example would require $L_{c2} = 29.7\,\mu$H.

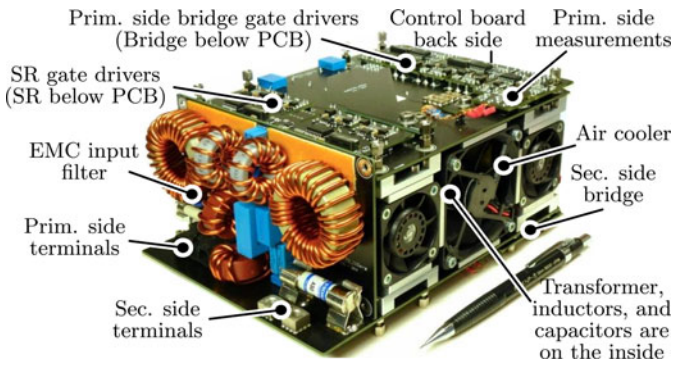

Fig. 19. 3.7 kW, single-phase, single-stage, bidirectional and isolated DAB ac–dc converter prototype (177 mm × 130 mm × 72 mm).

Measurements of the HF ac-link voltage and current patterns at different points of the ac-trajectories are shown in Fig. 21 and briefly discussed in Section V-B1. There it is also explained how these measurements can be validated by comparing the current values at the different switching instances in Fig. 21 with the values on the trajectories shown in Fig. 18(c) and (d). Together with Fig. 18(a) and (b) this gives a clear view on how the modulation angles, the frequency, the modes, . . ., evolve during sinusoidal operation.

V. Experimental Results

The experimental results are obtained from the DAB ac–dc hardware prototype depicted in Fig. 19, which is designed according to the specifications given in Table I. Providing detailed information about the design of each subcomponent is for the reason of clarity not within the scope of this paper. In fact, the final prototype is designed using a recursive design procedure. The basic technical data of the system are:

1) power PCB's: 2-layers, 105 μm copper per layer; auxiliary and other PCB's: 4-layers, 35 μm copper per layer;
2) HF DAB switches: FCH76N60NF (SupreMOS$^{\mathrm{TM}}$);
3) SR switches: STY112N65M5 (PowerMESH$^{\mathrm{TM}}$);
4) HF caps. C_2: 7 × 1.5 μF/630 $\mathrm{V_{dc}}$ in parallel (MKP);
5) HF caps. C_1: 6 × 2.2 μF/305 $\mathrm{V_{ac}}$/X2 in parallel (MKP);
6) LF caps. $C_{2,\mathrm{st}}$: 3 × 390 μF/500 $\mathrm{V_{dc}}$ in parallel (ELCO);
7) transformer: turns ratio $n_1/n_2 = 1$, N97 core material, 2 × 2 planar ELP58 cores, magnetizing inductance (i.e., commutation inductance L_{c2}) $L_{\mathrm{c2}} = L_{\mathrm{M}} = 62.1\,\mu$H (using an airgap), Litz wire;
8) main inductor: $L = 13\,\mu$H, N97 core material, 3 × 2 planar ELP38 cores, Litz wire;
9) commutation inductance $L_{\mathrm{c1}} = 62.1\,\mu$H, N97 core material, 1 × 2 planar ELP58 cores, Litz wire;
10) DM EMC filter: see Table IV and Fig. 2;
11) CM EMC filter: out of the scope of this paper.

It should be noted that the primary side commutation inductance L_{c1} was originally not included in the hardware design, but added in a later phase in order to achieve full-operating-range CDCB ZVS according to the analysis given in this paper. Although not shown in Fig. 19, during testing it was connected to the hardware with the screws that are located on the top power PCB (i.e., using the connection points of the transformer and inductor L). Also, the volume of this inductor is included in the results for the system's power density, which are listed in Table V. As a consequence, a further design iteration with optimized ac-link would certainly yield even higher efficiencies and power densities than presented below.

TABLE V
Prototype Power Density Values (at 3.7 kW Nominal Power)

Total system, incl. EMC filter (DM & CM), incl. $C_{2,\mathrm{st}} = 1170\ \mu$F	2.2 kW/liter
Total system, incl. EMC filter (DM & CM), excl. $C_{2,\mathrm{st}} = 1170\ \mu$F	2.7 kW/liter
Total system, excl. EMC filter (DM & CM), excl. $C_{2,\mathrm{st}} = 1170\ \mu$F	3.2 kW/liter

A. Practical Implementation of the Controller

1) Controller Hardware: The control hardware consists of an on-board FPGA, in particular the ALTERA EP3C25E144C8N CYCLONE III, which is operated with a clock frequency of 62.5 MHz and programmed in the VHDL hardware description language. The FPGA is responsible for generating the PWM gate drive signals, for reading in the current and voltage measurement peripherals (A/D converters), and for "fast" overcurrent and overvoltage protection. Moreover, it communicates over Ethernet with an off-board PC-based real-time target (RTT) from Triphase [29].[28] The RTT can be programmed and operated through MATLAB/Simulink, where the controllers, the "slow" protection, the start-stop procedures, the control parameter generation, and the delay and dead-time compensation are implemented (see Section V-A2). The Real-TimeWorkshop automatic code generator translates the MATLAB/Simulink model into C-code which is compiled and executed by the RTT.

2) Controller Software: The cascaded control structure used to control the DAB input current i_{DAB1} in accordance to (2) is shown in Fig. 20. The dashed lines indicate which part of the controller hardware (see Section V-A1) performs each particular task. The measured quantities (index m) that are available in the PFGA as digital signals are also indicated in Fig. 20. A PI current control loop controls i_{DAB1} based on a reference value $i_{\mathrm{DAB1,ref}}$ which is generated using a phase locked loop and calculation of (2). The set values $\hat{I}^*_{\mathrm{ac,P}}$, dir^*, and PF^* origin from an external source such as the battery management system or the vehicle power management system. For testing of the prototype system, a fixed voltage was used at the output of the DAB and the set values were manually applied. Optionally, an outer PI voltage controller can be used to control the output voltage V_{dc2}.

The control parameters needed for the DAB to generate the set current $i_{\mathrm{DAB1,set}}$ are determined using lookup tables which are calculated for the whole converter's operating range, as explained in Section IV. Based on $[i_{\mathrm{DAB1,set}}; v_{\mathrm{dc1,m}}; V_{\mathrm{dc2,m}}]$, the modulation parameters $\mathbf{x_{set}}$, the delay vector $\mathbf{t_{sw,del,set}}$, and the dead time vector $\mathbf{t_{dead,set}}$ are determined using linear table interpolation. $\mathbf{t_{sw,del,set}}$ and $\mathbf{t_{dead,set}}$ consist of respectively the switching delays $t_{\mathrm{sw,del}}$ (21) and dead times $t_{\mathrm{dead,min}}$

[28]The use of the Triphase RTT allows flexible implementation of different control algorithms. In a next phase the functions of the RTT can be implemented on the 3C25 FPGA by means of an embedded CPU [29].

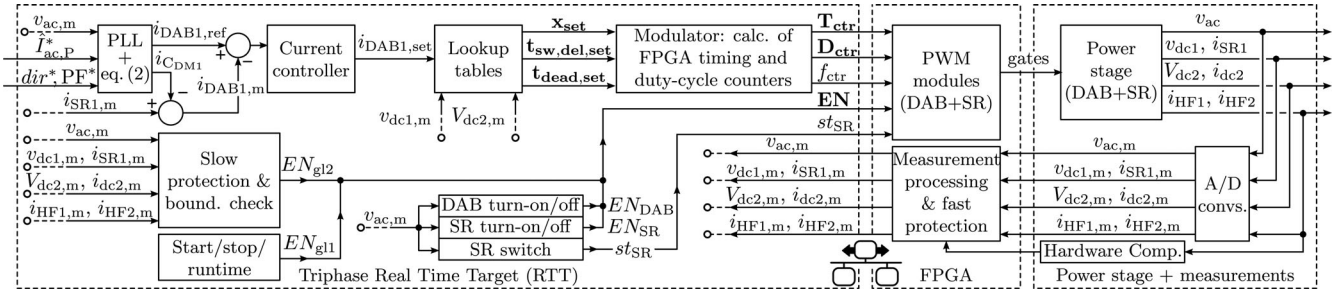

Fig. 20. Control structure employed to control the input current i_{DAB1} in accordance to (2) as well as the modulator function, the SR switch, and the enabling/disabling units (i.e. the start/stop/runtime, overcurrrent and overvoltage protection, and boundary check). The dashed lines indicate which part of the controller hardware (RRT, FPGA, or power stage/measurements) performs each particular task.

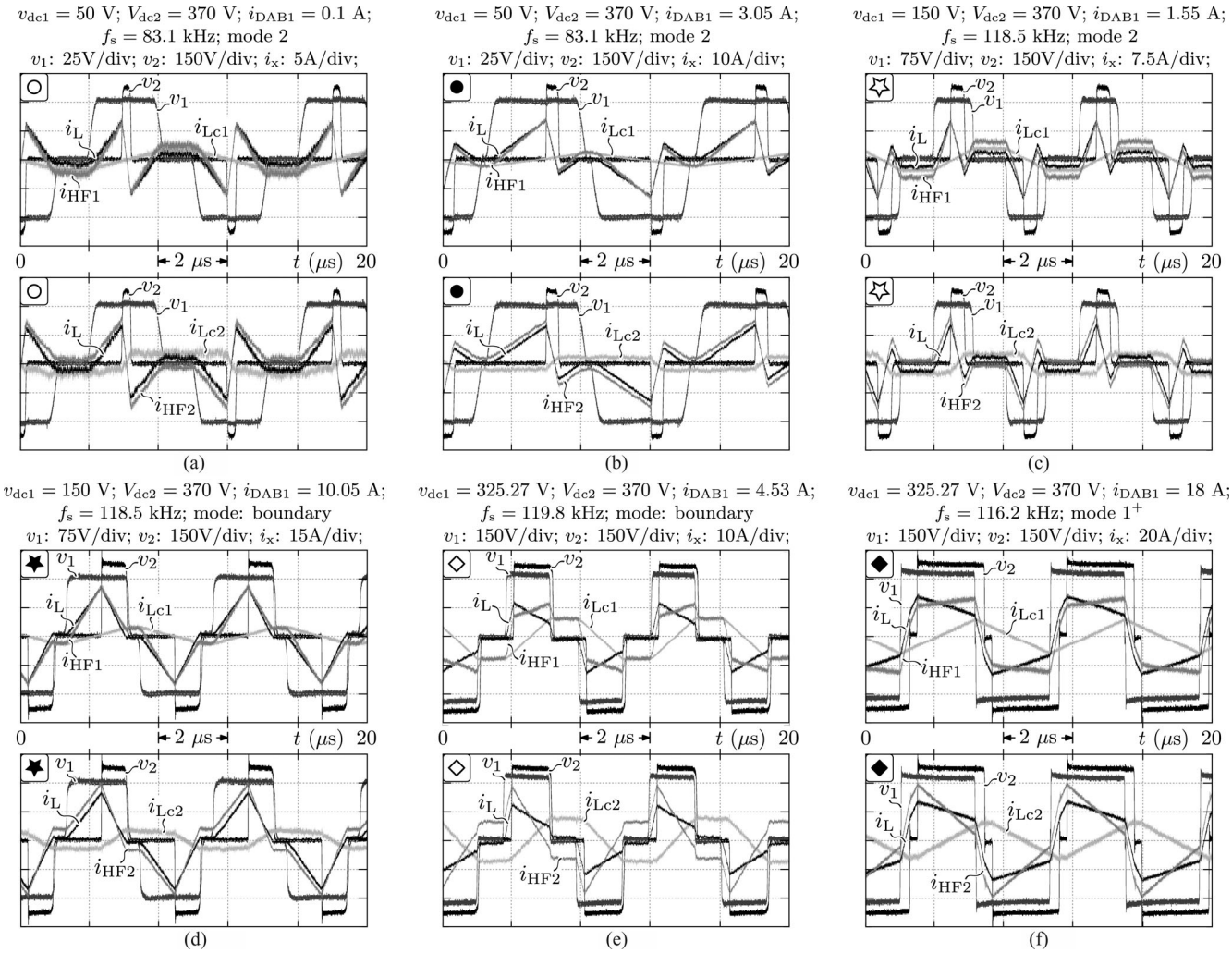

Fig. 21. Measured HF ac-link currents/voltages at six different points of the ac trajectories in Fig. 13 ($V_{\mathrm{dc2}} = V_{\mathrm{dc2,min}} = 370$ V: i.e. the, for ZVS, worst case output voltage). The top inset of each subfigure contains the DAB primary side currents, and the bottom inset the DAB secondary side currents.

(22) at the different commutation instances $\theta_i = \{\alpha, \beta, \gamma,$ and $\delta\}$. Finally, the modulator function calculates the frequency counter f_{ctr}, and the timing and duty-cycle counters for each bridge leg: $\mathbf{T_{ctr}} = [T_{\mathrm{ctr},11}; T_{\mathrm{ctr},12}; T_{\mathrm{ctr},21}; T_{\mathrm{ctr},22}]$; $\mathbf{D_{ctr}} = [D_{\mathrm{ctr},11}; D_{\mathrm{ctr},12}; D_{\mathrm{ctr},21}; D_{\mathrm{ctr},22}]$. These, as well as the enable signals $\mathbf{EN}$ and the SR state st_{SR}, are inputted to the FPGA PWM-generation modules.

B. Measurements

Below, the results of a dc–dc and ac–dc characterization of the prototype system at room temperature ($T_{\mathrm{A}} = 22\,^{\circ}$C) are presented. Although the power supply did not allow to sink power, and therefore only positive power flow could be applied, the results for negative power flow would be similar as the DAB is completely symmetric. The conversion efficiency is evaluated

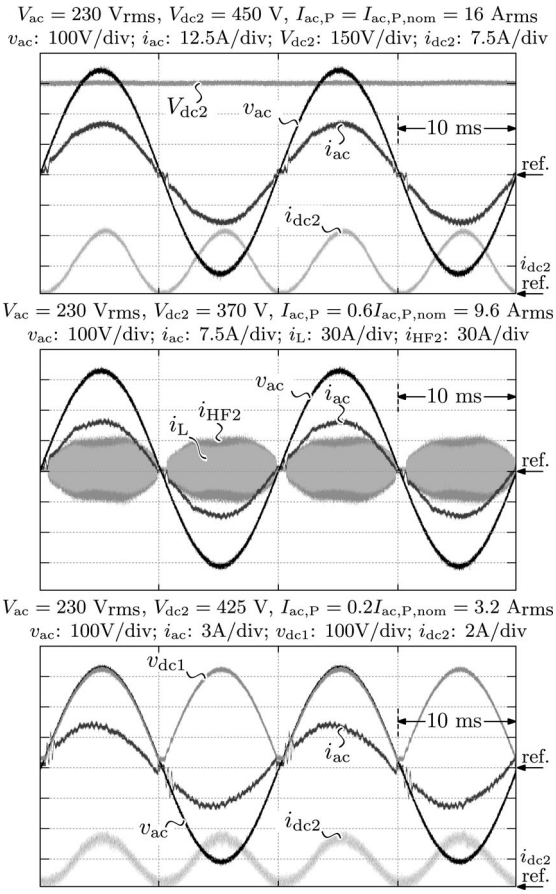

Fig. 22. Measured waveforms in ac–dc operation at different input currents and output voltages, and at the nominal ac input voltage $V_{\rm ac} = 230\ {\rm V_{rms}}$.

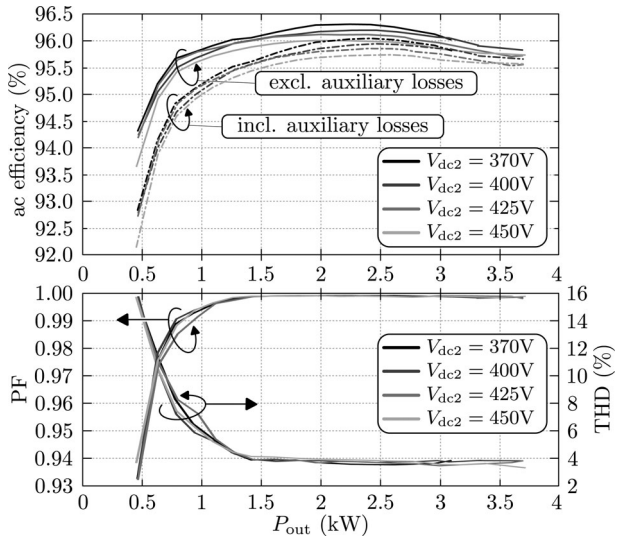

Fig. 23. Measured efficiency, THD, and (true) PF in ac–dc operation. Measurements are taken at the nominal ac input voltage $V_{\rm ac} = 230\ {\rm V_{rms}}$, in the whole power range and at different output voltages.

using the Yokogawa WT3000 precision power analyzer, having a power accuracy reading of $\pm 0.02\%$.

1) DC–DC Operation: A first prototype characterization is performed applying dc voltages at both the input (ac-side) and at the output (dc-side) terminals of the ac–dc converter. Fig. 21 shows the HF ac-link currents and voltages at six different points of the ac trajectories depicted in Figs. 13 and 18 (i.e., cf. scenario 2, Section IV-B2). A subfigure in Fig. 21 and its corresponding point in Fig. 13 are equally marked. For each voltage $v_{\rm dc1} = \{50\ {\rm V}; 150\ {\rm V}; 325.27\ {\rm V}\}$ (vertical dashed lines in Figs. 13 and 18) two different points (one on the line $I_{\rm ac,P} = I_{\rm ac,P,nom} = 16\ {\rm A_{rms}}$, and one on the line $I_{\rm ac,P} = 0.2 \cdot I_{\rm ac,P,nom} = 3.2\ {\rm A_{rms}}$) are captured. For $v_{\rm dc1} = 325.27$ V, the point on the line $I_{\rm ac,P} = I_{\rm ac,P,nom} = 16\ {\rm A_{rms}}$ is not measured as here the power transfer would be as high as 7.4 kW. In continuous dc–dc operation this would cause an overtemperature, and therefore $i_{\rm DAB1}$ is limited to 18 A [Figs. 13 and 21(f)]. The values of the HF-link currents ($i_{\rm HF1}$ and $i_{\rm HF2}$) at the different switching instants $\theta_i = \{\alpha, \beta, \gamma,$ and $\delta\}$ in Fig. 21 show very good agreement with the calculated values in Fig. 18(c) and (d). The same goes for the modulation angles and the switching frequency, validating the CDCB ZVS analysis method and practical implementation of the strategy. Additionally CDCB ZVS operation was successfully verified by visual inspection of the waveforms, according to Section III.

Also remind that here the, for ZVS, worst case output voltage $V_{\rm dc2} = V_{\rm dc2,min} = 370$ V is applied.

2) AC–DC Operation: For the ac–dc characterization the nominal ac input voltage $V_{\rm ac} = 230\ {\rm V_{rms}}$ is provided to the input (ac-side) of the converter by an ac power source, while the output (dc-side) is connected to a 5.9 mF dc-bus and a load. Fig. 22 depicts the measured waveforms at different input currents and output voltages. Note that the maximum output voltage that could be applied with the measurement setup is $V_{\rm dc2} = 450$ V. The system was successfully tested in the full power range (up until an output power of 3.7 kW), showing waveforms with little distortion [see Fig. 22 and Fig. 23 (bottom inset, THD)], a (true) PF close to unity [see Fig. 23 (bottom inset, PF)], and a high conversion efficiency in the whole power and output voltage range [see Fig. 23 (top inset)]. The latter is measured including and excluding auxiliary (i.e., gate drivers, fans, and control board) losses. An improved THD would be achieved by replacement of the on-board sample-based measurements circuits by Delta-Sigma measurements. Moreover, optimization of the ac-link components would yield even higher efficiencies.

3) Further Remarks on the Practical Realization: The closed-loop control of DAB converters is typically performed using lookup tables in which precalculated values for the modulation parameters (i.e., the duty-cycles, the phase-shift angle, the dead-times, and the delay compensation) are stored. However, table entries are dedicated results for one particular DAB converter. In practice, the system may be sensitive to changes of inductance values, and care should be taken when using high-performance MOSFET's. Loss of ZVS can easily cause device destruction. The DAB inductances, however, could be considered as another dimension of the lookup table.

Due to the presence of an SR, the investigated ac–dc converter might be identified as a "quasi" single-stage converter rather than a "single-stage" converter. However, alternatively the SR can be integrated in the primary side active bridge of the

DAB by placing the SR switches $S_{\mathrm{SR,x}}$ in antiseries with the equally indexed HF switches $S_{1\mathrm{x}}$, yielding a real single-stage ac–dc converter [7], [10], [19], [30]. Also here, one of the SR switches of each primary side bridge leg must be continuously ON during a half-period of the sinusoidal input voltage, resulting in the exact same operation as with the quasi-single-stage implementation (i.e., with a separate SR). Nevertheless, it is advantageous to not integrate the SR switches with the DAB's primary side bridge since in that case they have to conduct the HF components of the DAB input current $i_1(t)$. This is not the case when using a separate SR where the HF components of $i_1(t)$ are filtered by C_1, yielding lower overall conduction losses, while the component count remains the same.

VI. Conclusion

This paper presents a general procedure for the derivation of optimal, full-operating-range ZVS modulation schemes for DAB converters. The numerical nature of the proposed optimization algorithm allows users to freely define the cost function to be minimized. Thereby converter related losses, but also requirements concerning system volume, weight, control, EMI,... can be included. Moreover, a novel CDCB ZVS verification method was introduced, taking into account the commutation charge (switch capacitances) as well as the time dependence of the commutation currents. This ZVS verification method is implemented in the optimization algorithm in the form of constraint functions, assuring quasi-zero transistor switching losses.

Although applicable for any DAB implementation (minor adjustments), the optimization procedure is demonstrated for a FBFB DAB used in a single-phase, single-stage, bidirectional and isolated ac–dc topology. In a first scenario, using the traditional DAB ac-link implementation (i.e., a transformer and optional series inductor), considering "theoretical" CB-ZVS, and minimizing with respect to inductor and transformer rms current, a similar modulation scheme as in [12] was outputted, validating the algorithm. By changing the ZVS constraints from CB to CDCB ZVS, it was shown that an efficient full-operating-range ZVS modulation scheme which involves continuous modulation parameter trajectories cannot be achieved with the traditional DAB. In a second scenario, commutation inductance(s) were added in the DAB ac-link, benefiting the ZVS conditions due to the injection of small reactive currents in the bridges. As a result, a full-operating-range CDCB ZVS scheme with continuous modulation parameter trajectories is obtained.

The practical value of the optimization procedure is demonstrated with a 3,7 kW, bidirectional, and unity power factor electric vehicle battery charger which interfaces a 400 V dc-bus with the 230 $\mathrm{V_{ac}}$, 50-Hz utility grid. The calculated modulation scheme was successfully implemented on a high-power-density prototype converter, yielding high conversion efficiencies (full load and low load; $>96\%$ peak efficiency), a high PF, and low THD. Further optimization of the ac-link components would yield even higher efficiencies. Therewith the single-stage DAB ac–dc converter can be considered as a valuable competitor for the 2-S ac–dc topologies. A T-type HF ac-link and/or use of the transformer's leakage inductances are the subject of further optimization.

References

[1] S. Haghbin, S. Lundmark, M. Alakula, and O. Carlson, "Grid-connected integrated battery chargers in vehicle applications: Review and new solution," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 459–473, Feb. 2013.

[2] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[3] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, "Grid-interface bidirectional converter for residential DC distribution systems—Part 1: High-density two-stage topology," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1655–1666, Apr. 2013.

[4] H.-S. Kim, M.-H. Ryu, J.-W. Baek, and J.-H. Jung, "High-Efficiency Isolated Bidirectional AC–DC Converter for a DC Distribution System," *IEEE Trans. on Power Electron.*, vol. 28, no. 4, pp. 1642–1654, Apr. 2013.

[5] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodriguez, "Control of power converters in AC microgrids," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4734–4749, Nov. 2012.

[6] K. Clement-Nyns, E. Haesen, and J. Driesen, "The impact of vehicle-to-grid on the distribution grid," *Elect. Power Syst. Res.*, vol. 81, no. 1, pp. 185–192, Jan. 2011.

[7] K. Vangen, T. Melaa, S. Bergsmark, and R. Nilsen, "Efficient high-frequency soft-switched power converter with signal processor control," in *Proc. IEEE 13th Int. Telecommun. Energy Conf.*, Nov. 1991, pp. 631–639.

[8] M. H. Kheraluwala and R. W. De Doncker, "Single phase unity power factor control for dual active bridge converter," in *Proc. IEEE Ind. Appl. Soc. Annu. Meet.*, Oct. 1993, vol. 2, pp. 909–916.

[9] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J. W. Kolar, "Switching control strategy for full ZVS soft-switching operation of a dual active bridge AC/DC converter," in *Proc. IEEE 27th Ann. Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 1048–1055.

[10] F. Jauch and J. Biela, "Single-phase single-stage bidirectional isolated ZVS AC–DC converter with PFC," in *Proc. 15th Int. Power Electron. Motion Control Conf.*, Sep. 2012, pp. 1–8, Paper LS5d.1.

[11] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Comparative evaluation of soft-switching, bidirectional, isolated AC/DC converter topologies," in *Proc. IEEE 27th Ann. Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 1067–1074.

[12] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.

[13] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high power density DC/DC converter for high power applications," in *Proc. IEEE Ind. Appl. Soc. Annu. Meet.*, Oct. 1988, vol. 1, pp. 796–805.

[14] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1215–1227, Apr. 2011.

[15] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformer-coupled multiport ZVS bidirectional DC–DC converter with wide input range," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 771–781, Mar. 2008.

[16] J. Everts, J. Van den Keybus, and J. Driesen, "Switching control strategy to extend the ZVS operating range of a dual active bridge AC/DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 4107–4114.

[17] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC–DC converter under soft switching in the whole operating range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228–1236, Apr. 2011.

[18] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.

[19] K. Vangen, T. Melaa, and A. K. Adnanes, "Soft-switched high-frequency, high power DC/AC converter with IGBT," in *Proc. IEEE 23rd Annu. Power Electron. Spec. Conf.*, 1992, vol. 1, pp. 26–33.

[20] G. Guidi, A. Kawamura, Y. Sasaki, and T. Imakubo, "Dual active bridge modulation with complete zero voltage switching taking resonant transitions into account," in *Proc. 14th Europ. Conf. Power Electron. Appl.*, Sep. 2011, pp. 1–10.

[21] Z. Shen, R. Burgos, D. Boroyevich, and F. Wang, "Soft-switching capability analysis of a dual active bridge DC–DC converter," in *Proc. IEEE Elec. Ship Techn. Symp.*, Apr. 2009, pp. 334–339.
[22] G. Guidi, M. Pavlovsky, A. Kawamura, T. Imakubo, and Y. Sasaki, "Improvement of light load efficiency of dual active bridge DC–DC converter by using dual leakage transformer and variable frequency," in *Proc. IEEE Ener. Convers. Congr. Expo.*, Sep. 2010, pp. 830–837.
[23] U. Drofenik, A. Musing, and J. W. Kolar, "Voltage-dependent capacitors in power electronic multi-domain simulations," in *Proc. Int. Power Electron. Conf.*, June 2010, pp. 643–650.
[24] Gecko-Simulations AG—GeckoCIRCUITS. Free version available. [Online]. Available: www.gecko-simulations.com
[25] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.
[26] T. Nussbaumer, M. L. Heldwein, and J. W. Kolar, "Differential mode input filter design for a three-phase buck-type PWM rectifier based on modeling of the EMC test receiver," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1649–1661, Oct. 2006.
[27] R. W. Erickson, "Optimal single resistors damping of input filters," in *Proc. IEEE 14th Ann. Appl. Power Electron. Conf. Expo.*, Mar. 1999, vol. 2, pp. 1073–1079.
[28] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics," in *Proc. 7th Int. Conf. Integr. Power Electron. Sys.*, Mar. 2012, pp. 1–22.
[29] Triphase NV. 3PExpress^{TM}, Rapid System Development for Power Conversion Applications. [Online]. Available: www.triphase.com
[30] D. Chen and J. Liu, "The uni-polarity phase-shifted controlled voltage mode AC-AC converters with high frequency AC link," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 899–905, Jul. 2006.

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