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Extended Smart-Link Quasi-Single-Stage 3-Phase AC-DC Power Supply Module for AI-Driving Data Centers

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***Abstract*—In the rapidly evolving landscape of artificial intelligence (AI), the demand for computational power has surged, placing data centers at the forefront of technological progress. This increasing need for computational resources has led to a corresponding rise in energy consumption, currently estimated between 450 and 650 TWh/year and expected to reach 1000 TWh/year, driven by the emergence of next-generation 2 kW GPUs. Wide-bandgap (WBG) devices, including gallium nitride (GaN) and silicon carbide (SiC), offer the potential for up to a 1% efficiency improvement in applications such as state-of-the-art two-stage ac-dc converters, which currently achieve efficiencies of up to 98%. This paper presents a novel quasi-single-stage ac-dc topology leveraging partial power processing to precisely control the input ac current and output dc voltage, ensuring unity power factor under constant power load conditions, while maintaining LLC converter operation at its resonant frequency despite input voltage variations. The eXtended Smart-Link (XS-Link) integrates both voltage and current regulation across the two stages of ac-dc converters, effectively improving efficiency.**

***Index Terms*—ac-dc conversion, data centers, galvanic isolation, partial power processing, three-phase grid.**

I. Introduction

The widespread and rapidly expanding use of artificial intelligence (AI) drives an unprecedented demand for computing power. Thus, large-scale data centers are at the forefront of technological advancements. The growth in computational power has been accompanied by a parallel increase in energy consumption. Current estimates place the annual global energy usage of data centers, including data computing and transmission, between 450 TWh and 650 TWh, accounting for up to 2.2% of the global electricity generation [1]. However, future hyperscale data centers are expected to contribute to more than a doubling of the energy consumption, reaching 1000 TWh/year, e.g., resulting from the next-generation of 2 kW GPUs [2]. New cutting-edge power supplies tailored for data center applications are thus needed, delivering exceptional efficiency, scalability, and reliability, while lowering operational costs and reducing environmental impact. For example, wide-bandgap (WBG) devices, such as gallium nitride (GaN) and silicon carbide (SiC), promise up to a 1% improvement in efficiency [2]. Due to their higher operating temperatures and greater thermal conductivity, they positively affect the liquid-based cooling system in terms of performance and volume [3].

The state-of-the-art power distribution architecture in modern data centers incorporates includes a shared three-phase low-frequency transformer (3Φ-LFT) that steps down the medium-voltage ac (MVAC) grid voltage (e.g., 13.4 kV) to low-voltage ac (LVAC, e.g., 400 V...690 V line-to-line rms), which is then distributed throughout the data center to the individual server racks [4]. At the rack level, a two-stage conversion system, consisting of an ac-dc converter followed by a dc-dc converter, is usually adopted. While single-phase ac-dc converters were predominant until recently, three-phase ac-dc converters are now the preferred choice due to higher power levels. This configuration supplies a 50 V backplane power bus of each CPU/GPU rack, providing up to 25 kW for the latest generation of processors. The front-end (FE) stage is designed to rectify the three-phase grid to an HVDC voltage (e.g., 800 V or ± 400 V), and provide power factor correction functionality through phase current control [5]. Then, the back-end (BE) dc-dc step-down stage must only provide voltage scaling and galvanic separation and regulate the output voltage, facing rapid fluctuations in the load power due to the high dynamics of the CPU/GPU current consumption depending on the computational load. The LLC converter is commonly used as the BE stage due to its outstanding performance. When operating at its optimum operating point (i.e., at the resonant frequency, known as DCX operation), the LLC converter shows constant voltage gain and guarantees zero voltage/current switching (ZVS/ZCS) commutations, drastically reducing the losses [6]–[9]. To overcome the limitation of fixed voltage gain, an additional partial power (PP) processing converter can be used to adjust the LLC input voltage [10], [11]. Alternatively, a dual active bridge (DAB) converter can be employed as a BE stage, providing performance comparable to the LLC converter but with increased control complexity [12]–[14]. Other approaches discussed in the literature feature single-phase single-stage ac-dc converters utilizing three-level converters [15], modified Cuk topologies [16], [17], and flying capacitors [18], as well as three-phase isolated single-stage ac-dc matrix converters with monolithic bidirectional switches [19] or anti-series connections of SiC transistors [20]; the latter achieves an efficiency of 99% but requires relatively complex modulation and commutation schemes. Finally, today, industrial state-of-the-art power supply units with power levels of up to 12 kW show rated efficiencies in the order of 97.5% [21].

This paper proposes a novel isolated quasi-single-stage three-phase ac-dc power converter that has the potential to achieve efficiencies of 99%. The output voltage and input current regulation are integrated through a PP auxiliary converter (i.e., the "eXtended Smart dc-Link" or "XS-Link" concept), while ensuring that the LLC converter operates as DCX even under input voltage variations.

In the following, **Section II** introduces the XS-link concept and explains the operating principle. Then, **Section III** discusses design guidelines and the control method, before **Section IV** verifies the proposed XS-Link with detailed closed-loop circuit simulations. Finally, **Section V** concludes the paper.

II. Operating Principle

The proposed XS-Link concept is depicted in **Fig. 1**, alongside its predecessor, the "Smart dc-Link" (S-Link) introduced in [22].[1] In both cases, two-stage ac-dc power converters comprising an ac-dc front-end stage performing power factor correction (PFC) and an isolated dc-dc back-end stage that ensures the required galvanic isolation for the targeted application. For a first conceptual explanation of the operating principle, it is convenient to model the S/XS-Link circuit as a single current source in the S-Link configuration or as a pair of power-linked current sources in the XS-Link configuration, as shown in **Figs. 1a** and **Figs. 1b**, respectively. The interaction of the S/XS-Link with both FE and BE converters enables to select the best topology for each of these stages and operating them at their maximum-efficiency operating point. The considered hardware implementation of the proposed ac-dc converter based on the XS-Link circuit is reported in **Fig. 2**. **Fig. 1** reports the key voltage, current, and power waveforms to describe and highlight the main differences and capabilities of both concepts (S-Link and XS-Link), neglecting the switching-frequency components. In the following analysis, unity power factor and lossless power conversion is assumed.

A. Ac-dc FE Stage

Under the assumption of unity power factor and symmetric grid voltages, the input three-phase voltages and currents of the ac-dc PFC stage are defined as

$$\begin{aligned} v_i(t) &= \hat{V}_{ac}\cos(2\pi f_{ac}t + \varphi_i), \\ i_i(t) &= \hat{I}_{ac}\cos(2\pi f_{ac}t + \varphi_i), \end{aligned} \tag{1}$$

where $i = \{a, b, c\}$, $\varphi_i = \{0, -\frac{2}{3}\pi, \frac{2}{3}\pi\}$ are the phase angles, $\hat{V}_{ac}$ and $\hat{I}_{ac}$ are the peak line voltage and current, respectively, and f_{ac} is the grid frequency. To minimize losses, a three-phase rectifier employing an active third-harmonic current injection circuit is considered [23], i.e., an integrated active filter (IAF) rectifier, as shown in **Fig. 2**. The operating principle of the IAF is recalled next for completeness.

[1]Note that the S-Link in [22] is used in combination with a Vienna rectifier ac-dc FE stage, and advantageously facilitates so-called 1/3-PWM operation of that Vienna rectifier, reducing switching losses. Here, the S-Link is combined with an IAF rectifier front-end, as discussed below.

The dc-link $1\bar{1}$-port is connected through diodes (or switches) to the maximum line-to-line voltage, following the typical six-pulse-shaped voltage (see $v_{1\bar{1}}$ voltage in **Fig. 1**). Due to its periodicity, the analysis is reduced to its fundamental period $T_{ac}/6$. Within the interval $[0, T_{ac}/6]$, voltage $v_{1\bar{1}}$ is expressed as

$$\begin{aligned} v_{1\bar{1}}(t) &= \max(v_a(t), v_b(t), v_c(t)) - \min(v_a(t), v_b(t), v_c(t)) \\ &= \sqrt{3}\hat{V}_{ac}\sin\left(2\pi f_{ac}t + \tfrac{\pi}{3}\right), \end{aligned} \tag{2}$$

where $v_{1\bar{1}}(t) = v_a(t) - v_c(t)$ in this sector.

Using the hypothesis of a unity power factor, the absorbed power from the grid under balanced and sinusoidal conditions (i.e., $P_{ac} = p_{ac}(t) = p_a(t) + p_b(t) + p_c(t) = \frac{3}{2}\hat{V}_{ac}\hat{I}_{ac}$) must be equal to the power at the $1\bar{1}$-port, imposing the dc-link current i_1. Since lossless power conversion is assumed, the input and output power are equal, such that $p_{ac}(t) = p_{1\bar{1}}(t) = P_o$, allowing to define the dc-link current i_1 as

$$i_1(t) = \frac{P_o}{v_{1\bar{1}}(t)} = \frac{P_o}{\sqrt{3}\hat{V}_{ac}\sin\left(2\pi f_{ac}t + \frac{\pi}{3}\right)}. \tag{3}$$

The downstream converter stages must thus shape the dc-link current i_1 accordingly. Then, the third-harmonic current injection circuit must ensure symmetric three-phase currents at the input, such that $i_i(t) = G^* \cdot v_i(t)$ where $i \in \{a, b, c\}$ and G^* represents the equivalent input conductance. For this purpose, the smallest phase current (i.e., i_b in the considered time-interval $t \in [0, T_{ac}/6]$) is injected by modulating the L_j-inductor current with the auxiliary half-bridge $S_{j,x}$ and closing the related path of the bidirectional phase selector switch (PSS) $S_{abc,x}$. Thus, within interval $[0, T_{ac}/6]$, $i_b = G^* \cdot v_b$. Note that the PSSs are switched at line frequency.

To validate the aforementioned control strategy, the necessary i_1 current is derived. Consider negligible voltage drop across the L_j-inductor at low frequency (i.e., $\bar{v}_{kj} \simeq 0$), the half-bridge $S_{j,x}$ is modulated so that

$$v_{kn} \simeq v_b = d_j v_{1n} + (1 - d_j)v_{\bar{1}n} = d_j v_a + (1 - d_j)v_c \tag{4}$$

where d_j is the duty-cycle of the upper switch $S_{j,1}$. From (4), the definition of d_j is unique and given by $d_j = v_{bc}/v_{ac}$. Under the unity power factor assumption, the i_1 current is constrained to be equal to

$$i_1 = i_a - d_j i_j = i_a + \frac{v_{bc}}{v_{ac}} i_b = G^*\left(v_a + \frac{v_{bc}}{v_{ac}} v_b\right) = \frac{G^* \sum_i v_i^2}{v_{ac}}. \tag{5}$$

Recalling $P_{ac} = G^* \sum_i v_i^2$ and $v_{ac} = v_{1\bar{1}}$ in $t \in [0, T_{ac}/6]$, the equivalence between (3) and (5) is verified, highlighting that unity power factor is achieved only with a downstream converter stage that draws constant power [24].

In particular, the IAF FE stage combines low complexity with high efficiency. Further, since the inductor L_j always carries the smallest phase current, triangular current mode (TCM) modulation can be exploited to achieve ZVS of the $S_{j,x}$ switches for almost the entire sector.

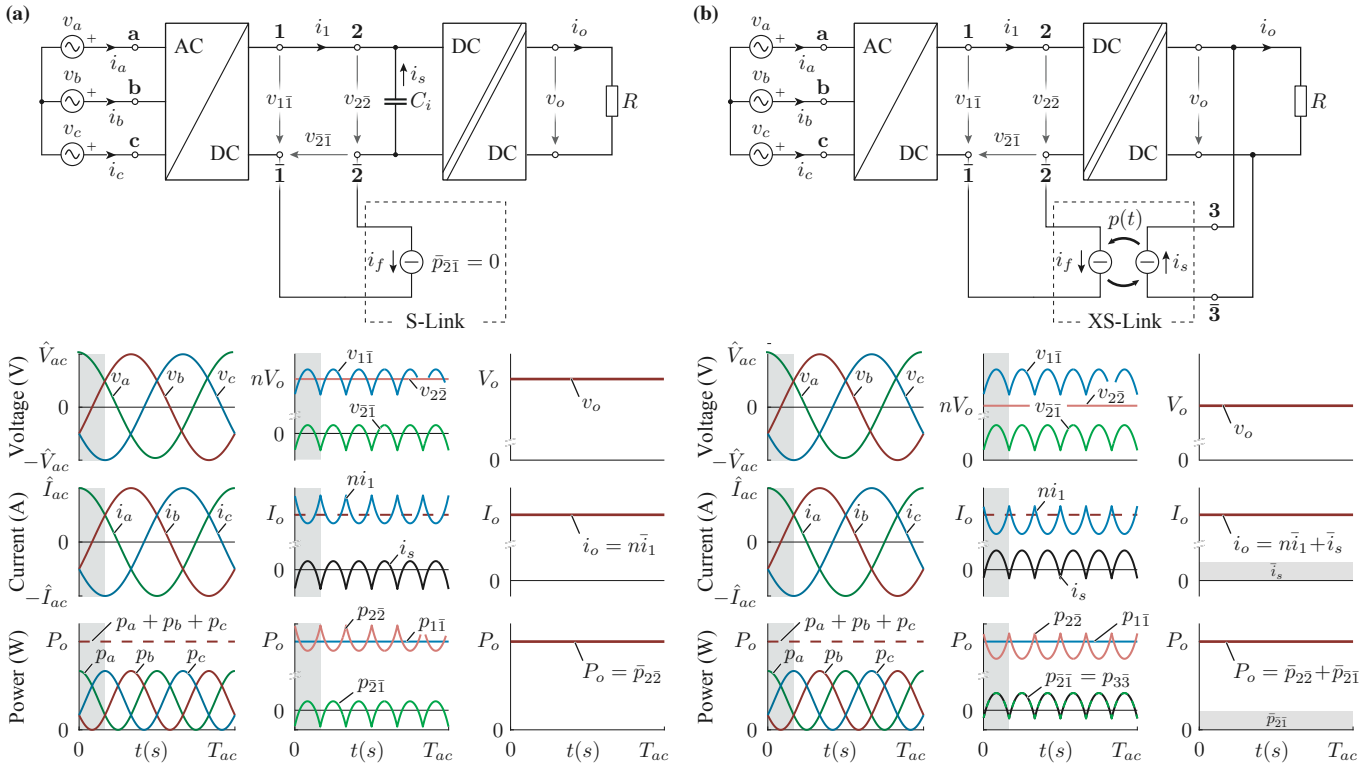

Fig. 1. Quasi-single-stage ac-dc power converters comprising an IAF PFC front-end and an isolated DCX-LLC dc-dc converter as BE stage. **(a)** The "S-Link" concept introduced in [22] can be utilized to achieve sinusoidal mains currents and constant power flow to the output; however, the output dc voltage is tied (fixed ratio) to the mains voltage amplitude. **(b)** Proposed eXtended Smart dc-Link (XS-Link) concept, where the partial-power stage can exchange active power with the dc output. This allows tight regulation of that output dc voltage to a fixed value independent of the mains voltage. The shown parameter n is the voltage gain of the isolated dc-dc converter, i.e., $n = v_{2\bar{2}}/v_o$.

B. Dc-dc BE Stage

As in the FE stage, the simplicity of control and minimization of loss are the most significant decision elements for the chosen topology. For this reason, the LLC converter is selected for its well-known high-efficiency performance operating at its resonant frequency f_r (i.e., DCX mode) achieving ZVS for the primary-side switches and ZCS for the secondary-side ones. In this operating mode, the LLC acts like a dc-transformer where the voltage gain depends only on the selected transformer turn ratio $n_{12} = N_1/N_2$. The related circuit is reported in **Fig. 2** as the DCX-LLC block.

The two full bridges $S_{1,x}$ and $S_{2,x}$ are synchronously controlled and produce two identical square voltage waveforms across the L_rC_r resonant tank of amplitude $\pm v_{2\bar{2}} = \pm n_{12}v_o$. To increase DCX-LLC performance, the transformer can be designed as a matrix transformer offering excellent power density and better integration of the XS-Link stage.

It is important to note that the DCX-LLC stage operates in open-loop configuration, without any closed-loop control. As a result, the output voltage remains unregulated, and the voltage regulation must be implemented in the upstream converter stages.

C. S/XS-Link Circuit

The presented "S/XS-Link" concepts addresses the shortcomings of the two cascade converters: on one hand, the IAF FE stage requires constant power load, i.e., an impressed current as defined in (3), and on the other, the DCX-LLC stage lacks output voltage regulation.

Given the strict constraint on the dc-link current i_1, the S/XS-Link stage interfaced with the $\bar{2}\bar{1}$-port must be designed as a current generator. For its realization, the inductor L_f is placed in series to the i_1 current path, and its current is controlled by the means of a full-bridge (FB) circuit $S_{4,x}$ connected to an energy storage capacitor C_h, as shown in **Fig. 2**.

As shown in [22], the S-Link circuit must process zero net power at its input port (i.e., $\bar{p}_{\bar{2}\bar{1}} = 0$)[2]. Within interval $[0, T_{ac}/6]$, the instantaneous input power expression at the $\bar{2}\bar{1}$-port from (2) and (3) is

$$p_{\bar{2}\bar{1}}(t) = p_{1\bar{1}}(t) - p_{2\bar{2}}(t) = P_o\left[1 - \frac{\bar{v}_{2\bar{2}}}{\sqrt{3}\hat{V}_{ac}\sin(2\pi f_{ac}t + \frac{\pi}{3})}\right] \tag{6}$$

and averaging over the considered sector, the net input power

[2]Note that the S-Link is designed solely to implement the circuit described here, without incorporating any additional ports. In contrast, the XS-Link circuit includes an extra port, enabling it to handle a net input power.

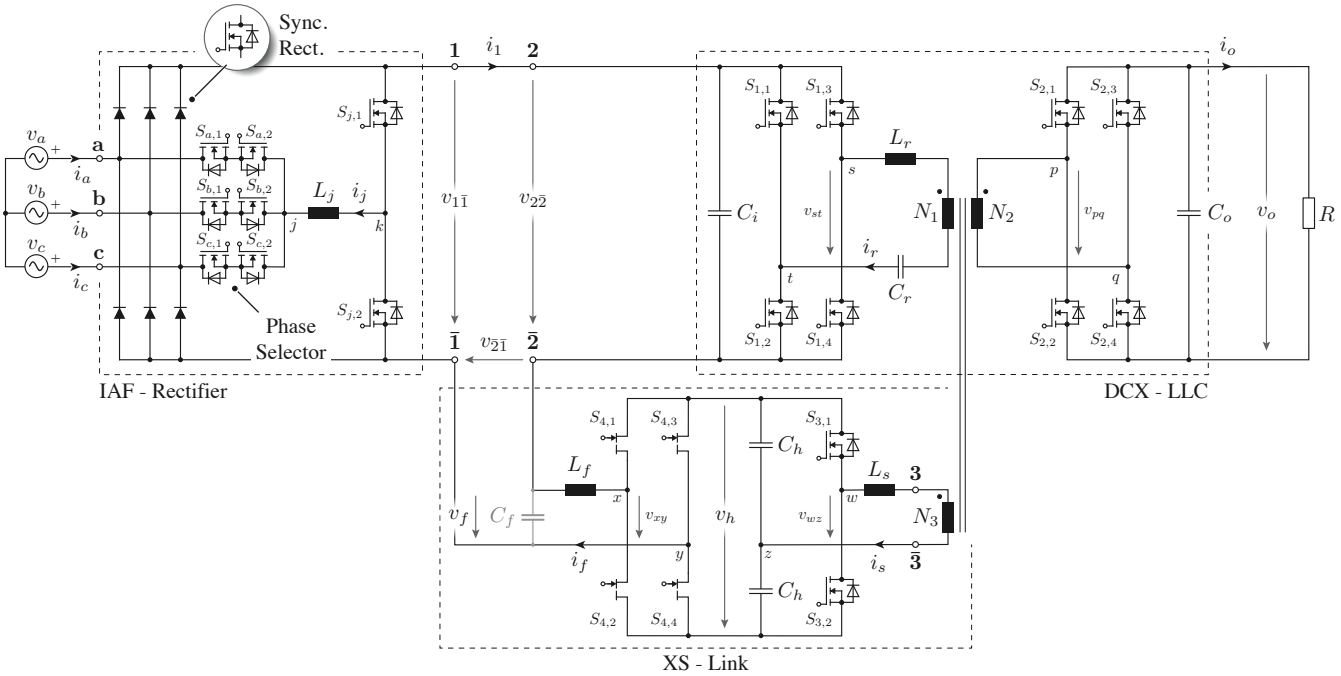

Fig. 2. Implementation example of the proposed quasi-single-stage isolated ac-dc power converter comprising an IAF PFC front-end, a DCX-LLC isolated dc-dc converter as back-end stage, and the proposed eXtended Smart dc-Link (XS-Link) partial-power converter (see also **Fig. 1b**. The exchange of power between the PPC stage and the dc output is implemented via a third winding on the DCX-LLC transformer as done in [10].

is found as

$$\bar{p}_{\bar{2}\bar{1}} = P_o \frac{6}{T_{ac}} \left[t - \frac{\bar{v}_{2\bar{2}}/\sqrt{3}\hat{V}_{ac}}{2\pi f_{\text{ac}}} \ln \left| \tan\left(\pi f_{ac} t + \frac{\pi}{6}\right) \right| \right]_0^{T_{\text{ac}}/6} = P_o \left[1 - \frac{\bar{v}_{2\bar{2}}}{\hat{V}_{ac}} \frac{\sqrt{3}\ln 3}{\pi} \right]. \tag{7}$$

It is worth noting that the zero net power constraint can be satisfied only for a specific value of the $v_{2\bar{2}}$ voltage, fixing inevitably the the output voltage at

$$V_o = \frac{\bar{v}_{2\bar{2}}}{n_{12}} = \frac{1}{n_{12}} \frac{\pi}{\sqrt{3}\ln 3} \hat{V}_{ac}\,. \tag{8}$$

As emphasized in (8), the output voltage cannot be independently controlled relative to the grid voltage, meaning any fluctuation in the grid voltage directly impacts the output voltage V_o. However, as shown in **Fig. 1**, a buffer capacitor C_i must be added at the $2\bar{2}$-port to filter the ac component of i_1, such that $i_s = i_1 - I_o$. Otherwise, the output power should not be constant, which would violate the constant power load requirement required by the IAF stage.

To overcome the imposed voltage limitation at the $2\bar{2}$-port of the S-Link circuit, which enables an output voltage regulation scheme, the net-power setpoint of $p_{\bar{2}\bar{1}}$ must be moved from zero, as highlighted in (7). Therefore, the S-Link must be extended to enable partial processing of the input power $p_{1\bar{1}}$. Partial power (PP) architectures are well-suited for this purpose. As proposed in [10], a third port was added to the DCX transformer and connected through a phase shift modulated (PSM) half-bridge. This created a power path for a voltage pre-regulator, which was connected in series with the DCX input port. Similarly, the S-Link is now equipped with a third port (i.e., $3\bar{3}$ in **Fig. 2**), interfacing an additional DCX transformer winding with a PSM half-bridge connected to the energy storage capacitor C_h, currently split into two. The obtained circuit is the implementation of the "XS-Link" concept.

As shown in **Fig. 1**, the additional circuit allows to share the input power $p_{1\bar{1}}$ among the DCX and the XS-Link without violating the constant power requirement at the IAF FE stage for output voltages differing from (8). The power processed by the XS-Link can be easily set with the additional half-bridge $S_{3,x}$ as in a DAB converter. Imposing a square voltage waveform of amplitude $\pm\frac{1}{2}v_h$ on $v_{wz}(t)$, leading in phase relative to voltage $v_{pq}(t)$ of φ_{32} angle, the power exchanged at $3\bar{3}$-port is regulated according to the following relation:

$$p_{3\bar{3}} = \frac{\frac{1}{2}v_h \cdot n_{32} v_o}{2\pi^2 f_r L_s} \varphi_{32}(\pi - |\varphi_{32}|), \tag{9}$$

where $n_{32} = N_3/N_2$ is the winding turn ratio between the transformer ports connected to the XS-Link and output, respectively, L_s is the leakage inductance of the third winding or a coupling impedance intentionally connected, and f_r is the resonance frequency of the DCX converter corresponding to the switching frequency of all bridge circuits connected to the DCX transformer.

III. Design Guidelines

This section outlines general design considerations for determining the XS-Link parameters and the critical com-

ponents of the front-end and back-end stages. Detailed design methodologies fall outside the scope of this paper. The reported guidelines are referred to the circuit implementation done in **Fig. 2**.

A. IAF Rectifier

The power semiconductor devices must be selected to block at least the maximum line-to-line grid voltage, i.e., $\sqrt{3}\hat{V}_{ac}$. Taking into account voltage fluctuations of ±10% relative to the nominal grid voltage and a 50% safety margin above the maximum operating voltage, the rated voltage for the switches and diodes of the IAF stage should be $V_R > 3/2(\sqrt{3}\hat{V}_{ac}+10\%)$.

The injection inductor L_j is designed to guarantee ZVS of the $S_{j,x}$ switches for almost the entire sector. At the sector boundaries, i.e., at the crossings of the grid voltages, the duty cycle d_j saturates to 0 or 1, reducing the magnitude of the current ripple and loosing ZVS conditions.

B. DCX-LLC Converter

The voltage rating of the semiconductor devices connected to the $2\bar{2}$-port is selected following the same approach as the one used in the previous section. Likewise, the same safety margin can be considered for devices connected to the output port, that is, $V_R > 3/2\hat{V}_o$ with $\hat{V}_o$ the maximum allowed output voltage.

The resonant tank can be designed to limit the maximum voltage $\hat{V}_{Cr}$ reached by the resonant capacitor at the nominal power P_o, defining a minimum capacitance value equal to $C_r = P_o/(4n_{12}V_o f_r \hat{V}_{Cr})$. The related resonant inductor is derived from the switching frequency chosen for the DCX-LLC stage, which corresponds to the resonance one. The selection of the n_{12} turn-ratio value will be addressed in the following section as a key aspect of the XS-Link circuit.

The input and output capacitances, C_i and C_o in the are **Fig. 2**, respectively, are designed to filter the high-frequency component of the resonant current, limiting the voltage ripple at the DCX ports[3].

C. XS-Link

In the next step, all parameters for the XS-Link implementation are defined, starting with the n_{12} turn ratio value.

This parameter is responsible for the net power processed by the XS-Link, tuning the $v_{2\bar{2}}$ voltage, (i.e., $n_{12}v_o$) in (7). As demonstrated in [10], the PP approach is advantageous when the auxiliary circuit processes positive power, as the power handled by the PP circuit is directly transferred to the output port rather than recirculating between the input and output ports. For this reason, the turn ratio should be chosen as $n_{12} < \frac{3}{2}\hat{V}_{ac}/V_o$, accordingly to (6). However, lowering the $v_{2\bar{2}}$ voltage increases the average voltage at $v_{\bar{2}\bar{1}}$, at the expense of a higher voltage stress on the input full-bridge of the XS-Link circuit. Since the final target is the use of high-performance GaN MOSFETs to reduce the L_f inductor volume allowed by very-high-switching frequency, the most significant design-driving parameter will be the maximum absolute voltage at $\bar{2}\bar{1}$-port. It follows that the turn ratio n_{12} is chosen close to the average voltage value of $v_{2\bar{2}}$ as $n_{12} \simeq \frac{3\sqrt{3}}{\pi}\hat{V}_{ac}/V_o$.

Once the turn ratio n_{12} is defined, the buffer capacitor voltage V_h is determined to keep the duty-cycle $d_{xy} = v_{\bar{2}\bar{1}}/V_h$ in its linear range (i.e. $d_{xy} \in [-1, 1]$) with a sufficient margin to ensure enough current control capability during transient (i.e. $|d_{xy}| < \hat{d}_{xy}$). Then, the buffer voltage is selected as $V_h = \hat{v}_{\bar{2}\bar{1}}/\hat{d}_{xy}$, and, consequently, the maximum voltage rating V_R of the XS-Link power semiconductor devices, keeping a reasonable safety margin like $V_R > 3/2V_h$.

The buffer capacitors C_h are designed to compensate for the power mismatch between the $\bar{2}\bar{1}$ and $3\bar{3}$-ports during grid voltage transient or output load step. Unlike the S-Link concept, where buffer capacitors serve as energy storage elements to absorb power fluctuations at the $\bar{2}\bar{1}$-port, the XS-Link circuit is power-transparent, meaning $p_{\bar{2}\bar{1}}(t) = p_{3\bar{3}}(t)$ as shown in **Fig. 1**. This enables a significant reduction in the minimum required stored energy and, consequently, in the C_h capacitance value.

The input inductor L_f is designed in a consistent manner with the selected modulation scheme of the full-bridge $S_{4,x}$. A three-level modulation can be employed, doubling the effective switching frequency of the $v_{xy}(t)$ voltage. Triangular current modulation can be also implemented to guarantee ZVS commutations at the cost of an increased rms value. The input capacitor C_f is dimensioned as a return path for the high-frequency components of the current i_f.

Since the XS-Link output stage operates equivalently to a DAB, the same design rules are applied: the turn ratio n_{23} is chosen closest to the voltage ratio V_h/V_o, while the leakage inductance L_s is selected to transfer the maximum rated power of the XS-Link circuit at maximum allowed phase-shift $\hat{\varphi}_{32}$ according to (9).

D. Control

Fig. 3 describes the closed-loop control structure of the quasi-single-stage three-phase ac-dc power module implementing the XS-Link concept. The output voltage $\mathrm{Rv_o}$ regulator sets an input power reference $p^*_{1\bar{1}}$, which is converted into the dc-link current i^*_1 reference. This current is then tracked by the XS-Link current $\mathrm{Ri_{Lf}}$ regulator, incorporating appropriate feedforward terms (see **Fig. 3 a**). The additional voltage $\mathrm{Rv_h}$ regulator is used to maintain the buffer voltage v_h around its reference V^{*}_h[4] (**Fig. 3 b**), generating a power mismatch between the input and output processed by the XS-Link (i.e., $p_{\bar{2}\bar{1}}$ and $p_{3\bar{3}}$, respectively). Lastly, the input power reference $p^*_{1\bar{1}}$ is converted into a grid conductivity reference $G^* = \hat{I}^*_{ac}/\hat{V}_{ac}$, which is used to define the injection current reference i^*_j. This current is then tracked by the IAF current $\mathrm{Ri_{Lj}}$ regulator, incorporating appropriate feedforward terms (see **Fig. 3 c**). For the sake of completeness, the closed-loop control structure of the power module implementing the S-Link is reported in **Fig. 3 d**. In

[3]The input capacitance C_i of the S-Link must be over-designed to compensate also the low-frequency ac component of the input current i_1.

[4]The control bandwidth of $\mathrm{Rv_h}$ regulator is limited to not interfere with the wide-bandwidth current $\mathrm{Ri_{Lf}}$ regulator.

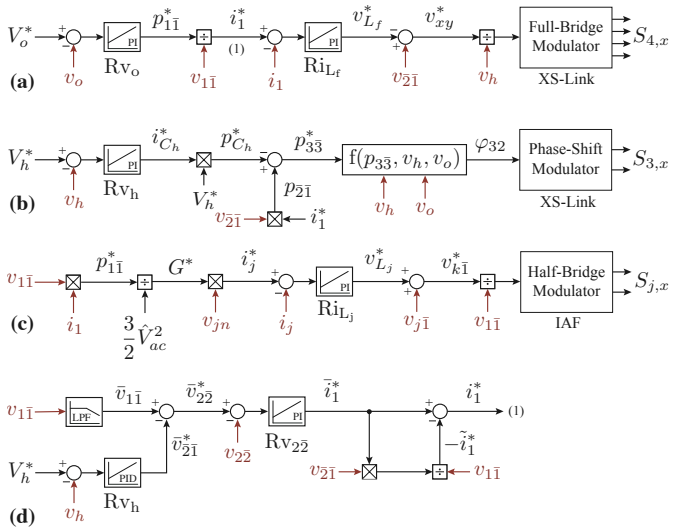

Fig. 3. Control structure of the XS-Link concept: **(a)** cascaded control structure with internal current i_1 control, and external output voltage v_o control; **(b)** buffer voltage v_h control; **(c)** injection current i_j control. The $\mathrm{Ri_{L_j}}$ regulator always controls the current only in one phase (j), which is selected by the phase selector switches (PSS); **(d)** i_1-current reference for the S-Link concept replacing i_1^* in **(a)**.

this case, the dc-link current i_1^* reference is obtained starting from its average value $\bar{i}_1^*$, which is provided by the $v_{2\bar{2}}$ voltage regulator $\mathrm{Rv}_{2\bar{2}}$. The $v_{2\bar{2}}^*$ voltage reference is then built by the average value of the input voltage $\bar{v}_{1\bar{1}}$ and XS-Link $v_{\bar{2}\bar{1}}$ voltage reference. The latter is provided by the voltage $\mathrm{Rv_h}$ regulator.

IV. Verification

To validate the effectiveness of the proposed XS-Link concept, a performance evaluation is carried out using numerical simulations. These simulations confirm the operation of the proposed converter and the effectiveness of the control architecture, even in the critical transient conditions due to input voltage variations, and perform an evaluation of the conduction losses. To increase modularity, and limit the device voltage stress, the converter BE stage is split in 2.5 kW modules each. Two DCX + XS-Link modules are connected in series to share the six-pulse-shaped voltage, then paralleled to reach the required 25 kW. Conversely, the IAF rectifier is shared among all the BE modules. The considered module arrangement is depicted in **Fig. 4**.

A. Verification of converter operation

Tab. I lists the system specifications and key converter parameters considered in this section.

The main XS-Link converter waveforms simulated in PLECS for S-Link [22] (i.e., $p_{3\bar{3}} = 0$) and the proposed XS-Link operation (i.e., $p_{3\bar{3}} \approx p_{\bar{2}\bar{1}}$) are reported in **Fig. 6a** and **Fig. 6b**, respectively. In **Fig. 6-1** and **Fig.6-2**, the line voltages and currents are reported, respectively, under a grid voltage steps of +10% and −10% with respect to the nominal value. In **Fig. 6-3**, the HV-side voltages are reported for a single DCX+XS-Link module: as mentioned, during the grid voltage steps, the XS-Link is able to keep the output voltage v_o constant, as well as

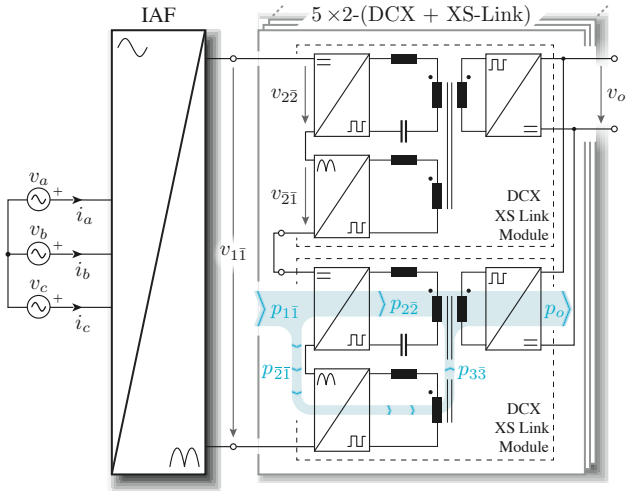

Fig. 4. Simulated structure of the quasi-single-stage three-phase ac-dc power module implementing the XS-Link concept. The simulation parameters are reported in **Tab. I.**

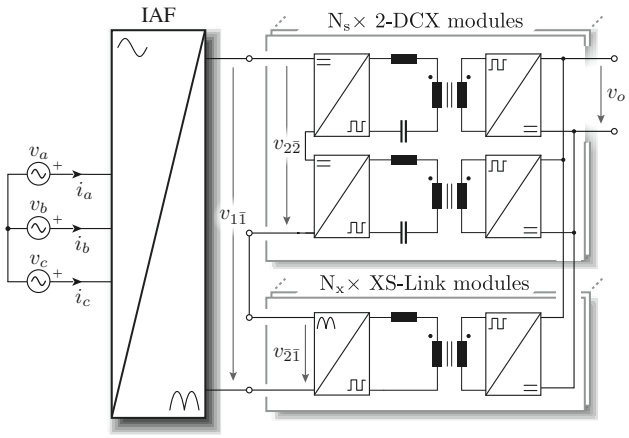

Fig. 5. Different arrangement of the quasi-single-stage ac-dc power module with N_s dc-dc stage in parallel composed of 2 DCX-LLC and N_x XS-Link module in parallel.

the input DCX voltage (i.e., $v_{2\bar{2}}$ - see **6b-3**). Unlike the S-Link, which, being unable to sustain a dc voltage offset at the $\bar{2}\bar{1}$-port, constraints the voltage $v_{2\bar{2}}$ to follow the grid voltage variation (see **6a-3**). In **Fig. 6-5**, the dc-link current i_1 and the DCX input current (i.e., i_o/n_{12}) are shown, demonstrating how the XS-Link ensures a seamless output current during grid transients. This is attributed to the XS-Link's ability to handle active power, as demonstrated in **Fig. 6-5**. By constraining $p_{3\bar{3}} = 0$ (refer to **6a-5**), the S-Link is limited to compensating only the ac component of the $v_{1\bar{1}}$ voltage. Notably, since constant power load is considered, the input power $p_{1\bar{1}}$ fluctuates accordingly with $p_{\bar{2}\bar{1}}$, causing a small variation in the output and grid currents (see **Fig. 6a-2**.). On the other side, when the XS-Link operates, the module is power-transparent keeping both input and output power constants (i.e., $p_{1\bar{1}} \simeq p_o$). Finally, the output voltage v_o and the buffer voltage v_h are shown in the **Fig. 6-6**.

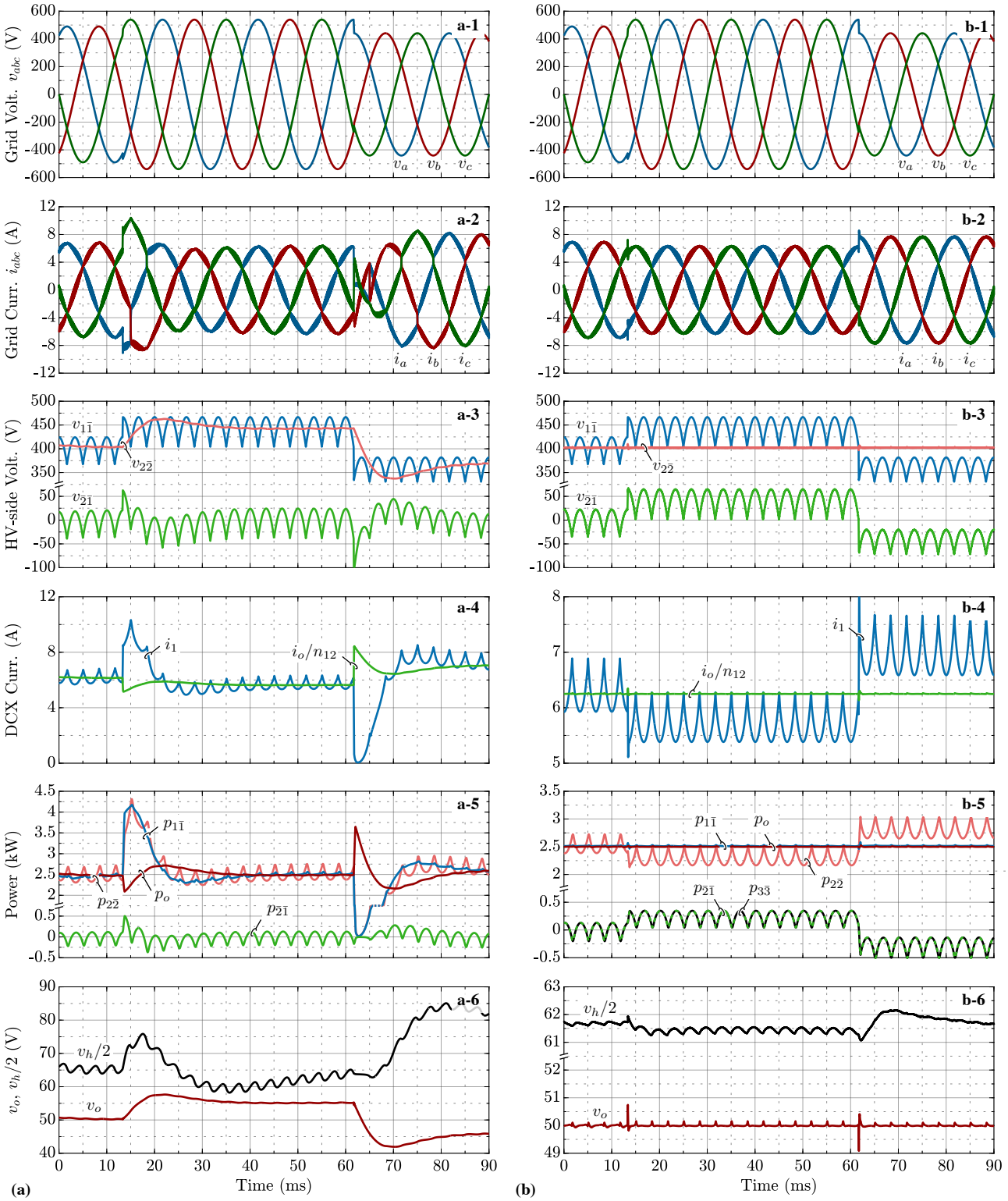

Fig. 6. Main XS-Link converter waveforms simulated in PLECS for **(a)** $p_{3\bar{3}} = 0$ (i.e., S-Link operation [22]) and **(b)** $p_{3\bar{3}} = p_{\bar{2}\bar{1}}$ (i.e., XS-Link operation), under grid voltage step transitions (±10%). The simulation parameters are reported in **Tab. I**. The vertical scale of **(4)**, **(5)** and **(6)** are different between S-Link**(a)** and XS-Link**(b)** operations to improve the visibility.

B. Performance Evaluation

To evaluate whether the proposed XS-Link approach can break the 99%-efficiency limit, the total conduction losses are estimated considering the following power transistors: Infineon CoolSiC 1200 V (10 mΩ) for $S_{abc,x}$ and $S_{j,x}$; Infineon CoolSiC

TABLE: I: MAIN SYSTEM SPECIFICATIONS FOR XS-LINK

Parameter	Value	Parameter	Value
Grid volt.[1]	V_{ac} = 600 V±10%	DC volt.	V_o = 50 V±1%
Grid curr.	$\hat{I}_{ac}$ = 6.8 A	DC curr.	I_o = 500 A
Grid freq.	f_{ac} = 50 Hz	DC power	P_o = 25 kW
$S_{j,x}$ freq.	$f_{sw,j}$ = 72 kHz	IAF ind.	L_j = 86 µH
$S_{12,x}$ freq.	$f_{sw,12}$ = 144 kHz	DCX ind.	L_r = 20 µH
DCX cap.	C_o = 57 µF	DCX cap.	C_r = 610 nF
DCX cap.	C_i = 710 nF (105 µF for S-Link)		
$S_{3,x}$ freq.	$f_{sw,3}$ = 144 kHz	XS ind.	L_s = 1.5 µH
$S_{4,x}$ freq.	$f_{sw,4}$ = 288 kHz	XS volt.	V_h = 125 V
XS ind.	L_f = 8.9 µH	XS cap.	C_f = 330 nF
XS cap.	C_i = 67 µF (100 µF for S-Link)		
Transf.	$N_1 : N_2 : N_3$ = 8:1:1		

[1]line-to-line rms voltage

650 V (7.6 mΩ) for $S_{1,x}$; Infineon OptiMOS 5-80 V (1.5 mΩ) for $S_{2,x}$; Infineon OptiMOS 5 200 V(7.8 mΩ) for $S_{3,x}$; and EPC2304(200 V - 4.65 mΩ) for $S_{4,x}$. A junction temperature of 100° is considered for the evaluation of the on-state resistances. Then, the total conduction losses amount to 130 W (0.52%), allowing to allocate 120 W for the other loss contributions, e.g., switching losses, magnetics, EMI filter.

C. Alternative Realization Options

Thanks to the modularity allowed by the XS-Link concept, different arrangements of the quasi-single-stage three-phase ac-dc converter can be implemented, as shown in **Fig. 5**. In the reported solution, the ac-dc FE stage is kept unvaried, while the BE stage is substituted with N_s-paralleled modules of 2 series-connected DCX-LLC converter to split the dc-link voltage $v_{1\bar{1}}$ across the 2 dc-dc converters. Since single transformer integration is not possible with the used BE stage, N_x-paralleled modules of the XS-Link circuit are connected to the output with a dedicated full-bridge inverter which replaces the DCX-LLC output-side one of the arrangement of **Fig. 4**.

V. CONCLUSION

To address the rising energy demand driven by the increasing computational needs of next-generation datacenters, advancements in power distribution architectures utilizing wide-bandgap devices like GaN and SiC are crucial. This paper presents a three-phase quasi-single-stage ac-dc converter, designed to step down from 600 V ac to 50 V dc, which leverages the significant advantages of the partial power processing concept.

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