Analysis of a Synergetically Controlled Two-Stage Three-Phase DC/AC Buck-Boost Converter

Michael Antivachis, Jon Azurza Anderson, Dominik Bortis, and Johann Walter Kolar

***Abstract*—Three-phase DC/AC power electronics converter systems used in battery-powered variable-speed drive systems or employed in three-phase mains-supplied battery charger applications usually feature two power conversion stages. In both cases, typically a DC/DC stage is attached to a three-phase DC/AC stage in order to enable buck-boost functionality and/or a wide input-output voltage operating range. However, a two-stage solution leads to a high number of switched bridge-legs and hence, results in high switching losses, if the degrees of freedom available for controlling the overall system are not utilised. If the DC/DC stage is used to vary the DC link voltage with six times the AC-side frequency, a pulse width modulation (PWM) of always only one phase of the DC/AC stage is sufficient to achieve three-phase sinusoidal output currents. The clamping of two phases (denoted as 1/3 PWM) leads to a drastic reduction of the DC/AC stage switching losses, which is further accentuated by a DC link voltage which is lower than for the conventional modulation schemes. This paper details the operating principle of a three-phase buck-boost converter system using 1/3 PWM and outlines an appropriate control system design. Subsequently, the switching losses and the voltage/current stresses on the converter components are analytically derived. There, a more than 66% reduction of the DC/AC stage switching losses is calculated without any increase of the stress on the remaining converter components. The theoretical considerations are finally verified on a hardware demonstrator, where the proposed modulation strategy is experimentally compared against several conventional modulation techniques and its clear performance advantages are validated.**

***Index Terms*—Battery charger, control system design, modulation strategy, variable-speed drives, wide input-output voltage range.**

I. Introduction

THREE-PHASE DC/AC converter systems for E-mobility applications are currently in high demand. Such three-phase converters appear either in inverter systems, such as variable-speed motor drives [1], [2], or in three-phase pulse width modulation (PWM) rectifier systems, used for fast battery charging [3], [4]. Since both power electronics systems are typically installed on a vehicle, it is required that the converters are highly efficient while maintaining a high power density. At the same time, three-phase inverters and/or rectifiers in E-mobility applications have to cope with a wide input-output voltage range.

In particular, a motor drive supplied by a battery must generate a controllable three-phase output AC voltage in an amplitude range $\hat{U}_m = 0...\hat{U}_{m,max}$. Simultaneously, the input battery DC voltage varies depending on the state-of-charge, loading and temperature between $U_b = U_{b,min}...U_{b,max}$. Accordingly, the operation area of the inverter system is defined by all possible combinations of the DC input and the AC output voltage. As the motor line-to-line voltage amplitude $\hat{U}_{m,LL} = \sqrt{3}\,\hat{U}_m$ can exceed the battery voltage U_b, a boost-type DC/DC converter stage that generates an adequately high DC link voltage u_{DC}, is typically placed in front of the buck-type three-phase DC/AC converter stage as shown in Fig. 1(a).

In analogy, three-phase fast battery chargers also have to operate within a wide voltage operating area. There, the output DC battery voltage varies in a range $U_b = U_{b,min}...U_{b,max}$ depending on the vehicle type and charging status, while the input three-phase grid AC voltage can also fluctuate in a range $\hat{U}_m = \hat{U}_{m,min}...\hat{U}_{m,max}$. The level of U_b can be lower than the input grid line-to-line voltage amplitude $\hat{U}_{m,LL} = \sqrt{3}\,\hat{U}_m$. Therefore, a buck-type DC/DC stage that adapts the DC link voltage u_{DC} to U_b is typically placed after the three-phase boost-type PFC rectifier stage as is shown in Fig. 1(b). All in all, both systems, i.e., the variable-speed motor drive and the battery charging system, feature the same two-stage converter structure, just with opposite direction of the power flow. Unfortunately, this two-stage solution suffers from high switching losses and large heatsink volume originating from the fact that both converter stages are typically independently modulated with a high switching frequency. In the following, the example of a variable-speed motor drive system shown in Fig. 1(a) is analysed in detail, however, the same considerations also apply to the battery charging system of Fig. 1(b).

For conventional sinusoidal PWM [5] of the DC/AC stage shown in Fig. 1(a), purely sinusoidally varied duty cycles are employed for all phases (i.e., no third harmonic component [6] is injected), as illustrated in Fig. 2(a.ii). This modulation strategy results in continuous switching of all three DC/AC stage half-bridges (in the following denoted as 3/3 PWM) and accordingly leads to high switching losses (cf., Fig. 2(a.i)). At the same time, 3/3 PWM requires a high DC link voltage u_{DC} equal or larger than $2\hat{U}_m$($\hat{U}_m$ denotes the motor phase voltage

Manuscript received August 12, 2019; revised October 25, 2019; accepted November 27, 2019. Date of publication March 31, 2020; date of current version February 8, 2020.

All authors are with the Power Electronic Systems Laboratory, ETH Zurich, Switzerland (e-mail: antivachis@lem.ee.ethz.ch).

Digital Object Identifier 10.24295/CPSSTPEA.2020.00004

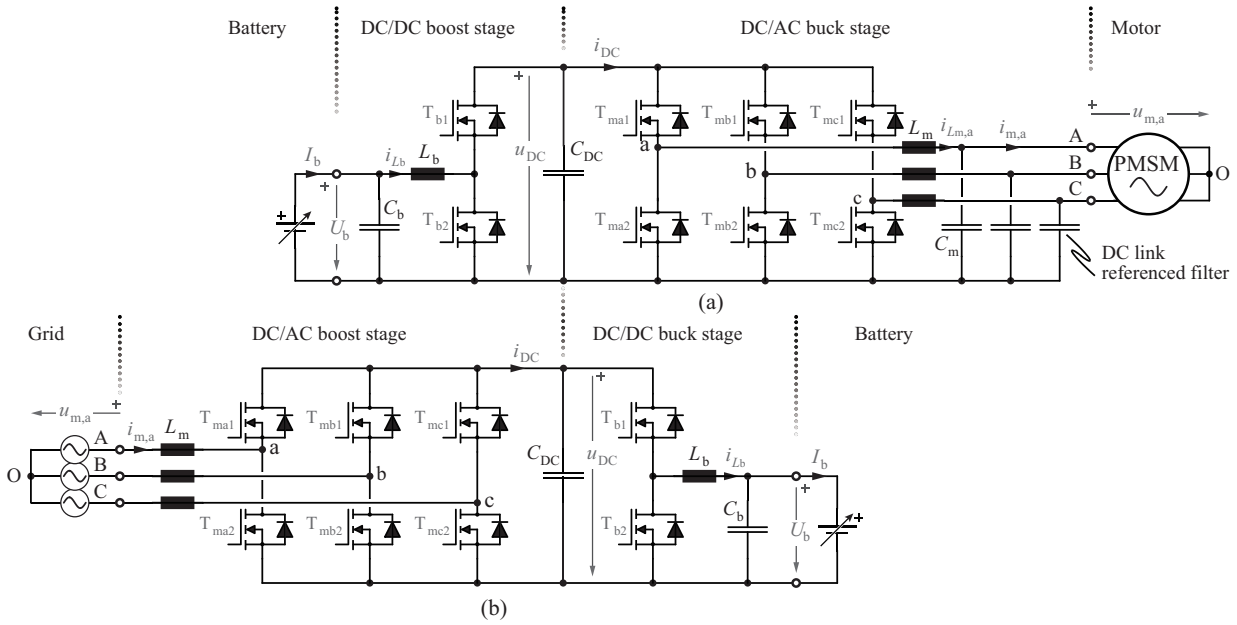

Fig. 1. For a variable speed motor drive application (a) supplied by a battery, a DC/DC boost-type converter stage is typically placed in front of the DC/AC converter stage in order to adapt the battery voltage U_b to the DC link voltage u_{DC} required for generating the (speed dependent) motor voltage $\hat{U}_m$. For a battery charging application (b) supplied from a three-phase AC grid, the battery voltage U_b can be higher or lower than the grid line-to-line voltage $\sqrt{3}\,\hat{U}_m$. For this reason, a buck-type DC/DC stage is placed after the boost-type DC/AC (rectifier) stage in order to generate a DC output voltage U_b lower than the DC link voltage u_{DC}.

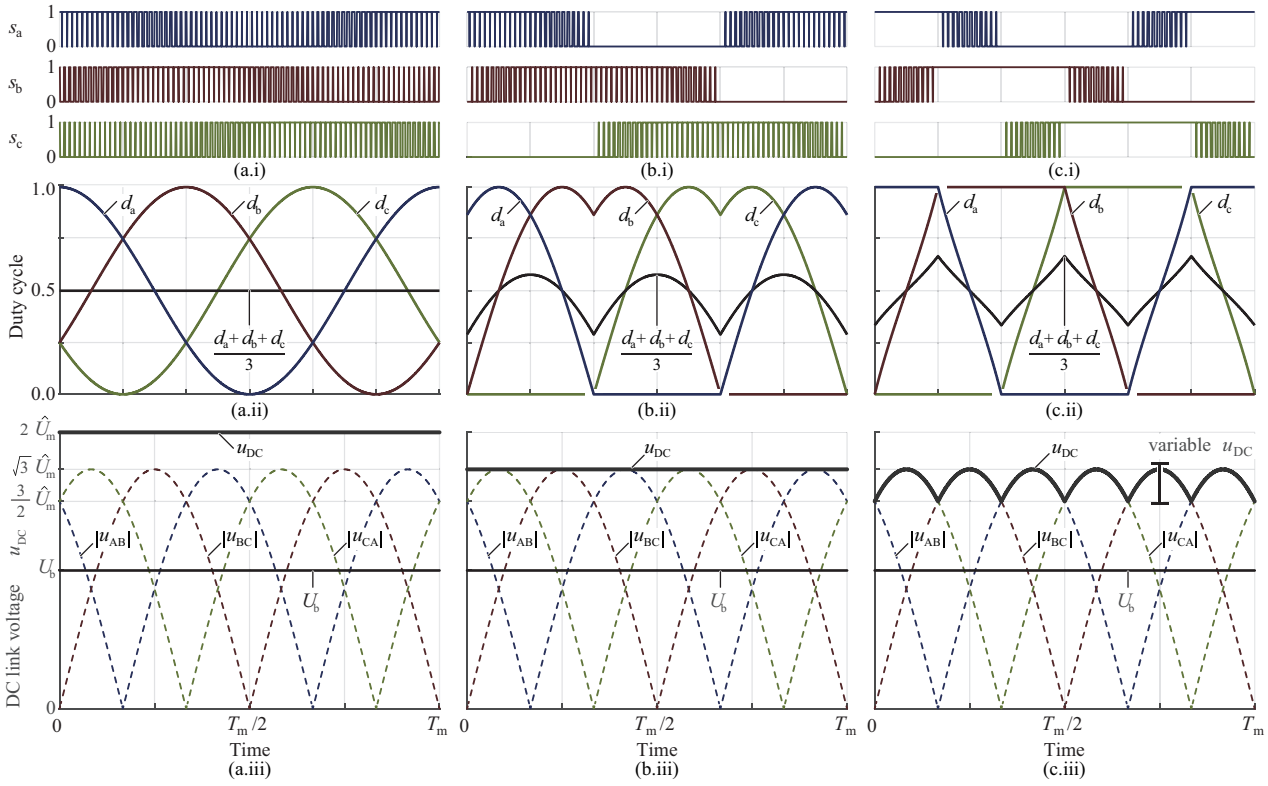

Fig. 2. Different PWM strategies of a three-phase two-level DC/AC inverter. (i) Gate signals of the three DC/AC stage bridge-legs. (ii) Duty cycles of the bridge-legs. (iii) DC link voltage u_{DC}. In (a) the characteristic waveforms of 3/3 PWM are shown, which is characterized by purely sinusoidally varying duty cycles, continuous switching of all three-phases and a high DC link voltage $u_{DC} = 2\hat{U}_m$. In (b) the properties for 2/3 PWM are depicted, which allow for the switching of always only two out of three-phases and leaves the third phase clamped to the negative DC link rail. The DC link voltage can be lowered to $u_{DC} = \sqrt{3}\,\hat{U}_m$. In (c) the proposed 1/3 PWM scheme is illustrated, where always only one out of the three-phases is switched. The DC link voltage is varying over time, has a six-pulse shape (resulting from proper control of the DC/DC stage) and is equal to the largest instantaneous motor line-to-line voltage.

amplitude) which is generated by the DC/DC stage, as shown in Fig. 2(a.iii). In order to reduce the switching losses, different clamping methods have been proposed in literature such as discontinuous PWM [7], [8], which always operates only two out of the three DC/AC half-bridges (denoted as 2/3 PWM, cf., Fig. 2(b.i)) and results at least in a 33% reduction of the DC/AC stage switching losses [9]. Typical duty cycles for 2/3 PWM are illustrated in Fig. 2(b.ii). There, negative clamping is used, i.e., at any given point in time, one of the low-side switches of the DC/AC stage is permanently turned-on and clamps the corresponding phase to the negative DC rail. It is noted that 2/3 PWM employs non-sinusoidal duty cycles and/or output phase voltages of the DC/AC stage (measured against the negative DC rail) but still allows to generate a purely sinusoidal three-phase line-to-line voltage system thanks to the open motor star point O (cf., Fig. 1(a)). Besides lower switching losses, 2/3 PWM results in a lower DC link voltage requirement for the same output voltage modulation range, compared to 3/3 PWM and accordingly leads to a lower voltage stress on the converter components. In particular, the DC link voltage in the case of 2/3 PWM should be equal or higher than the line-to-line motor voltage amplitude $u_{DC} \geqslant \sqrt{3}\,\hat{U}_m$ as depicted in Fig. 2(b.iii).

Both, 3/3 PWM and 2/3 PWM, employ a constant DC link voltage u_{DC} and the DC/DC stage and DC/AC stage are controlled independently. However, a constant DC link voltage u_{DC} is actually not required. As shown in [10]–[14] the modulation of the DC/DC and DC/AC stages can be synergetically combined which results in a significant performance improvement. If the DC/DC stage is used to vary the DC link voltage with six times the output frequency f_m, a PWM of always only one phase of the DC/AC stage is sufficient to achieve three-phase sinusoidal output currents. The clamping of two phases (denoted as 1/3 PWM in the following) leads to a 66% reduction of the DC/AC stage switching losses compared to 3/3 PWM [15]–[18], and the corresponding DC link voltage is lower than, the conventional modulation schemes. The gating signals and the duty cycles for 1/3 PWM are plotted in Fig. 2(c.i) and (c.ii) respectively, while the time-varying DC link voltage is depicted in Fig. 2(c.iii).

In the following, the 1/3 PWM strategy is explained in more detail (Section II) and an appropriate control structure for the overall converter system is presented. Subsequently, the switching losses of 1/3 PWM are analytically derived and compared against traditional PWM modulation strategies in Section III. Furthermore, the voltage and/or current stresses on the different converter components are calculated in order to allow a complete assessment of the 1/3 PWM scheme. In Section IV, a versatile hardware demonstrator is assembled and tested, employing either 1/3 PWM, 2/3 PWM or 3/3 PWM which enables a comprehensive comparison among the different modulation strategies. Accordingly, the drastic switching loss reduction achieved by means of 1/3 PWM is experimentally verified. Finally, conclusions are drawn in Section V.

II. Operation Principle

The DC/AC stage operated with 1/3 PWM generates the three-phase sinusoidal motor voltages which are plotted in Fig. 3(b.iii)

$$\begin{aligned} u_{m,a} &= u_{AO} = \hat{U}_m \cos(2\pi f_m t) \\ u_{m,b} &= u_{BO} = \hat{U}_m \cos\left(2\pi f_m t - \frac{2\pi}{3}\right) \\ u_{m,c} &= u_{CO} = \hat{U}_m \cos\left(2\pi f_m t + \frac{2\pi}{3}\right), \end{aligned} \tag{1}$$

where f_m is the fundamental motor frequency. The 1/3 PWM features a variable DC link voltage $u_{DC}(t)$ generated by the preceding DC/DC stage, whose shape is always defined by the largest absolute motor line-to-line voltage u_{AB}, u_{BC} or u_{CA}. Therefore, the DC link voltage has a six-pulse shape that varies between a minimum value of $\sqrt{3}\,\hat{U}_m \cos(\pi/6) = 3/2\hat{U}_m$ and a maximum value of $\sqrt{3}\,\hat{U}_m$. The accordingly required duty cycle d of the DC/DC stage high-side switch is shown in Fig. 3(a.ii) and the gating signal is plotted in Fig. 3(a.i). In Fig. 3(a.iv) the battery current I_b and the DC link current $\bar{i}_{DC}$ are depicted. The local average value of the DC link current $\bar{i}_{DC}$ also fluctuates because the DC link voltage u_{DC} is not constant. The product $p(t) = u_{DC}(t) \cdot \bar{i}_{DC}(t)$ of DC link voltage and current is constant in order to ensure a constant instantaneous power delivery $p(t)$ to the motor.

Using the 1/3 PWM scheme, the DC/AC stage is controlled by the duty cycles d_a, d_b, d_c depicted in Fig. 3(b.ii). For the first 60° interval of the fundamental period, (highlighted in grey, cf., Fig. 3), where the line-to-line voltage $|u_{CA}|$ is the largest, the duty cycle of phase a is $d_a = 1$ (i.e., phase a is clamping to the positive DC link rail), the duty cycle of phase c is $d_c = 0$ (i.e., phase c is clamping to the negative DC link rail), while only the duty cycle of the middle phase b varies within $d_b = 0$, 1. This means that the six-pulse shaped DC link voltage u_{DC} is directly applied between phases a and c i.e., $u_{ac} = u_{DC}$ and only phase b i.e., the phase with the middle voltage value, is actively switched with PWM. Hence, neglecting the reactive voltages/currents of the L_m-C_m filter, the motor line-to-line voltage results as $u_{AC} \backsimeq u_{ac} = u_{DC}$. Therefore, during the first 60° an appropriate sinusoidal line-to-line voltage is applied between the motor terminals A and C, even though in the DC/AC stage no switching action for the corresponding phases a and c is taking place. Accordingly, only the remaining motor terminal B voltage must be actively generated by the DC/AC stage by means of switching phase b. It is noted that, the open star connection of the motor O, $u_{m,a} + u_{m,b} + u_{m,c} = 0$, is a prerequisite for 1/3 PWM, since it allows to generate a three-phase voltage system by actively controlling only two voltages at any point in time. For the considered example, only the line-to-line voltage u_{ac} and the phase voltage u_b are actively controlled. The same principle applies for the remaining 60° intervals of the fundamental period T_m, while the roles of phases a, b and c are exchanged. The sinusoidal motor currents and currents in the filter inductor L_m are plotted in Fig. 3(b. iv). As can be noticed, always only the inductor current of the middle (PWM operated) phase exhibits a pronounced high-

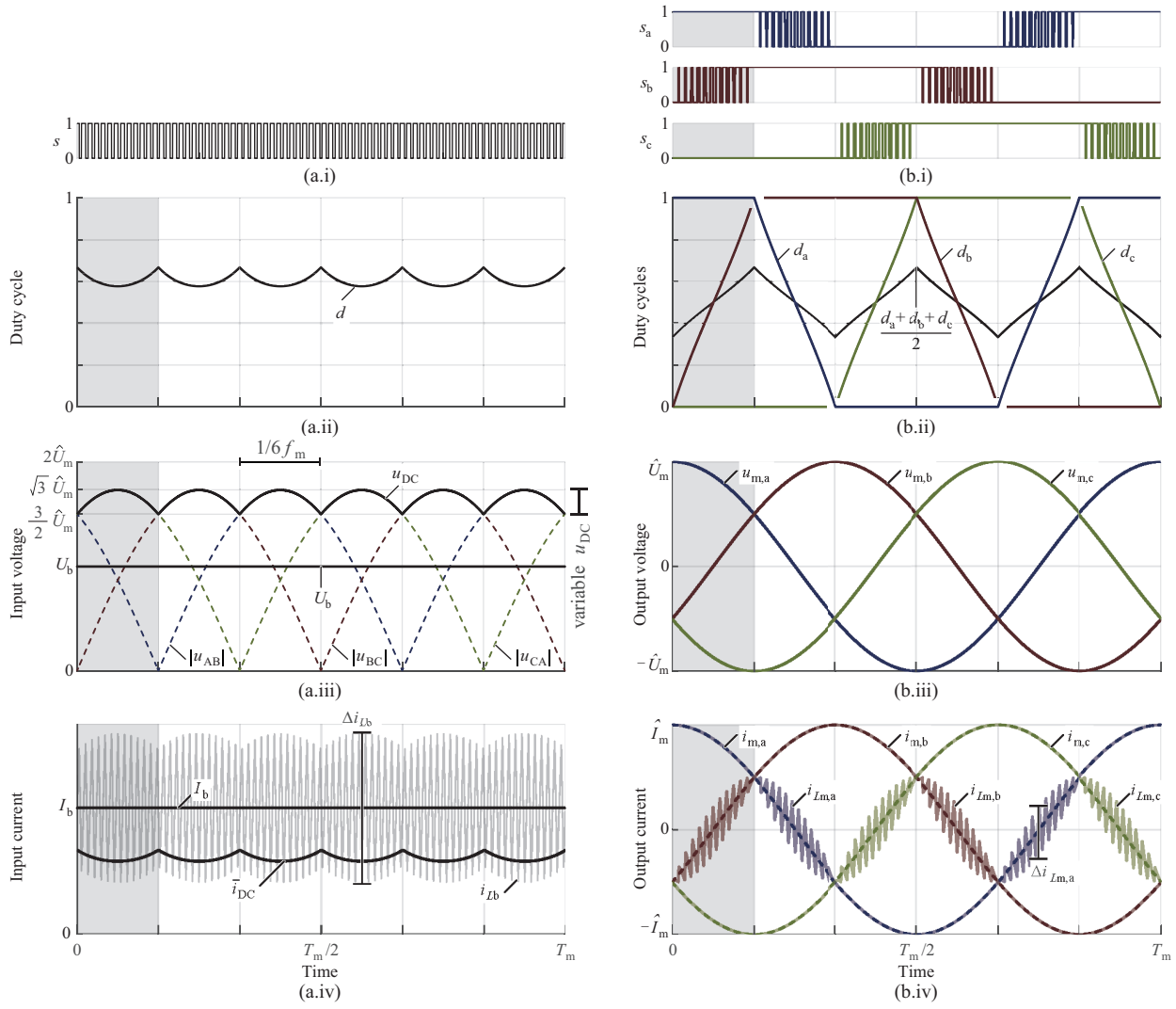

Fig. 3. Characteristic waveforms for 1/3 PWM operation of the converter system of Fig. 1(a), where (a) corresponds to the DC/DC stage and (b) refers to the DC/AC stage and low switching frequency f_s is assumed for the visualisation. In (a.i) the gate signal of the DC/DC stage high-side switch and in (a.ii) the duty cycle are depicted. In (a.iii) the variable DC link voltage u_{DC} featuring a six-pulse shape is highlighted and in (a.iv) the battery current and DC link current are plotted. The gate signals and the duty cycles of the DC/AC stage are illustrated in (b.i) and (b.ii), respectively. Finally, the motor terminal voltages are plotted in (b.iii), while the motor phase currents and filter inductor currents are shown in (b.iv).

frequency current ripple, while the two other inductors conduct smooth sinusoidal motor currents, which in turn also reduces the high-frequency losses in the filter inductors. The DC/AC stage inductor current ripple shape is unique to the DC link referenced filter of Fig. 1(a), i.e., for filter capacitors C_m connected to the negative DC link rail [19].

In the following, the analytic calculation of fundamental quantities and/or waveforms for the 1/3 PWM is performed. In a first step, the time behaviour of the DC link voltage u_{DC} is formulated. To this end, the maximum instantaneous line-to-line motor voltage is required which based on (1) has a six-pulse shape and is

$$u_{m,LL,max}(t) = u_{m,max}(t) - u_{m,min}(t), \tag{2}$$

where $u_{m,max}(t) = \max\{u_{m,a}, u_{m,b}, u_{m,c}\}$ and $u_{m,min}(t) = \min\{u_{m,a}, u_{m,b}, u_{m,c}\}$. The DC link voltage is subsequently derived (cf., Fig. 3(a.iii)) as

$$u_{DC}(t) = \begin{cases} U_b & \text{for } u_{m,LL,max}(t) \leqslant U_b \\ u_{m,LL,max}(t) & \text{for } u_{m,LL,max}(t) > U_b \end{cases}. \tag{3}$$

As long as the actual maximum line-to-line motor voltage $u_{m,LL,max}(t)$ is below the battery voltage U_b, the boost-type DC/DC converter cannot control the DC link voltage to a six-pulse shape and thus clamps the DC link voltage $u_{DC} = U_b$ by permanently turning-on the high-side switch T_{b1}. On the other hand, as soon as the line-to-line motor voltage amplitude $\sqrt{3}\hat{U}_m$ exceeds the battery voltage U_b (for higher speeds), the DC/DC stage can control the DC link voltage to the six-pulse voltage $u_{DC} = u_{m,LL,max}(t)$. The duty cycle of the high-side switch

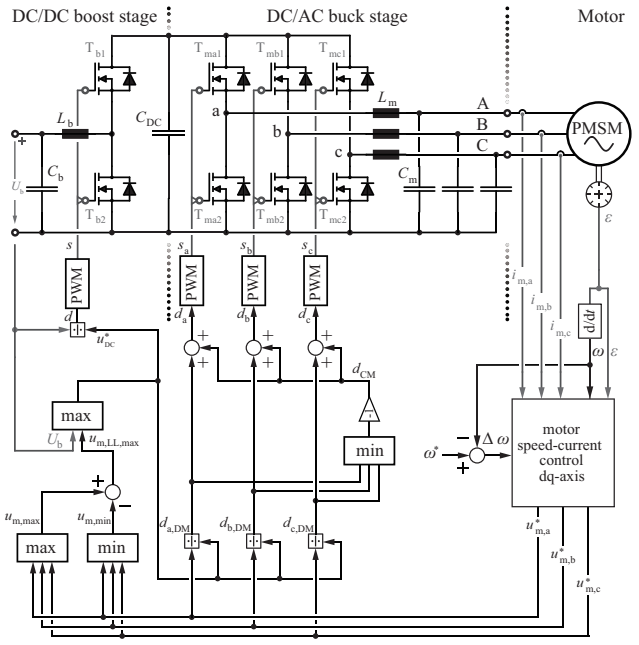

Fig. 4. Block diagram of the proposed control scheme. A cascaded control of the motor speed ω^* with an underlying motor torque and/or motor phase current control (reference values $i^*_{\mathrm{m},\{\mathrm{a,b,c}\}}$) is assumed, which finally outputs the three machine terminal voltage references $u^*_{\mathrm{m},\{\mathrm{a,b,c}\}}$ which must be generated. Subsequently, the corresponding duty cycles of the DC/DC stage and DC/AC stage are derived and are translated into gating signals.

$\mathrm{T_{b1}}$ of the DC/DC stage is then given as (cf., Fig. 3(a.i) and (a.ii))

$$d(t) = \frac{U_\mathrm{b}}{u_\mathrm{DC}(t)}. \tag{4}$$

In a second step, the duty cycles d_a, d_b and d_c of the DC/AC stage for 1/3 PWM are calculated, which is based on the same algorithm as used for 2/3 PWM [20] (cf., Fig. 2(b)). The duty cycle of each phase ranges within 0−1 and is split into a differential-mode (DM) and a common-mode (CM) part. The DM part is purely sinusoidal and is calculated for phases a, b and c based on (1), (3) as

$$d_{\{\mathrm{a,b,c}\},\mathrm{DM}}(t) = \frac{U_{\mathrm{m},\{\mathrm{a,b,c}\}}(t)}{u_\mathrm{DC}(t)}. \tag{5}$$

The CM part or offset of the duty cycle, which is common to all three phases, is

$$d_\mathrm{CM}(t) = -\min\{d_{\mathrm{a,DM}}(t),\, d_{\mathrm{b,DM}}(t),\, d_{\mathrm{c,DM}}(t)\}. \tag{6}$$

The total duty cycle is the sum of both components

$$d_{\{\mathrm{a,b,c}\}}(t) = d_{\{\mathrm{a,b,c}\},\mathrm{DM}}(t) + d_\mathrm{CM}(t). \tag{7}$$

Based on these duty cycle calculations, when the instantaneous motor line-to-line voltage is lower than the battery voltage $u_{\mathrm{m,LL,max}}(t) \leqslant U_\mathrm{b}$, the DC/DC stage clamps the DC link voltage to the battery voltage $u_\mathrm{DC} = U_\mathrm{b}$. Then, the DC/AC stage operates with 2/3 PWM resulting in the waveforms shown in Fig. 2(b). On the other hand, for $u_{\mathrm{m,LL,max}}(t) \geqslant U_\mathrm{b}$, the

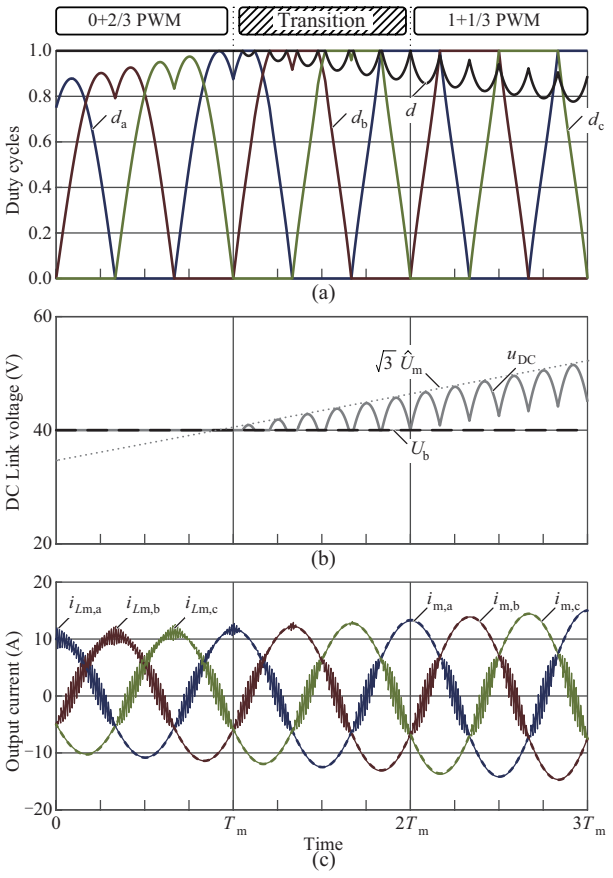

Fig. 5. Simulation results showing a smooth transition from 2/3 PWM to 1/3 PWM, where the motor voltage is gradually increased. When the motor voltage is low ($\hat{U}_\mathrm{m} \leqslant U_\mathrm{b}/\sqrt{3}$), 2/3 PWM is employed. When the motor voltage is high ($\hat{U}_\mathrm{m} > 2U_\mathrm{b}/3$), exclusively 1/3 PWM is used. During the transition, where $U_\mathrm{b}/\sqrt{3} < \hat{U}_\mathrm{m} \leqslant 2U_\mathrm{b}/3$ is valid, 2/3 PWM and 1/3 PWM are occurring alternately.

DC/DC stage is activated and generates a DC link voltage $u_\mathrm{DC} = u_{\mathrm{m,LL,max}}(t)$, which in case of $\hat{U}_\mathrm{m} \geqslant 2U_\mathrm{b}/3$ shows a six-pulse shape. Then, the DC/AC stage is operating with 1/3 PWM (cf., Fig. 3(b.ii)). In other words, the 1/3 PWM results from the generalization of 2/3 PWM, since the same algorithm (cf., Fig. 4) is used for the calculation of the DC/AC stage duty cycles throughout the whole DC link operation range. Depending on the relationship between the battery voltage U_b and the motor voltage $\hat{U}_\mathrm{m}$, the converter can transition continuously from 2/3 PWM to 1/3 PWM and vice-versa.

The 1/3 PWM is incorporated in a block diagram of a cascaded motor speed control in Fig. 4. There, the three-phase motor currents $i_\mathrm{m,a}$, $i_\mathrm{m,b}$, $i_\mathrm{m,c}$ as well as the motor rotation angle ε and the motor speed ω are measured and fed as input to the motor controller. A standard cascaded speedtorque/current motor controller in a d-q reference frame is employed. The motor controller defines the motor terminal AC voltage references $u^*_\mathrm{m,a}$, $u^*_\mathrm{m,b}$, $u^*_\mathrm{m,c}$ which must be generated. According to the reference voltages, the DC/DC stage duty cycle d is calculated employing (2)−(4). At the same time, the DC/AC stage duty cycles d_a, d_b and d_c are derived based on (5)−(7).

A transition example from 2/3 PWM to 1/3 PWM is shown in Fig. 5. There, the motor voltage and current is gradually

increased, as highlighted in Fig. 5(c). During $t < T_m$, the motor voltage is low, $\hat{U}_m \leqslant U_b/\sqrt{3}$, therefore exclusively 2/3 PWM is employed. In particular, the DC/DC stage is deactivated, which means that the battery is directly connected to the DC link $u_{DC} = U_b$. This operating regime is denoted as 0+2/3 PWM in Fig. 5, '0' indicating that the DC/DC stage is not switched and '2/3' denoting that two out of three DC/AC half-bridges are switched. In contrast, for $t > 2T_m$, the motor voltage is high, $\hat{U}_m \geqslant 2U_b/3$, therefore exclusively 1/3 PWM is employed. In this case, the DC/DC stage is activated and controls the DC link voltage to $u_{DC} = u_{m,LL,max}(t)$. This operating regime is denoted as 1+1/3 PWM, with '1' indicating that the DC/DC stage is switched. During $T_m < t \leqslant 2T_m$, the motor voltage is $U_b/\sqrt{3} < \hat{U}_m \leqslant 2U_b/3$ and both modulation schemes are alternatively employed, while a smooth transition between the two modulation regimes is achieved without unwanted transients.

It is noted that during 1/3 PWM operation of the DC/AC stage, the motor voltage cannot be abruptly increased. In order to increase the motor line-to-line voltage, a higher, six-pulse shaped DC link voltage $u_{DC}(t)$ must first be generated by the DC/DC stage. Therefore, the maximum rate at which the motor line-to-line voltage can be increased is defined by the dynamic response of the DC/DC stage. Consequently, 1/3 PWM exhibits a limited control bandwidth of the motor line-to-line voltage, depending on the value of the DC link capacitor C_{DC}. A large C_{DC} value would slow down the dynamics of the DC/DC stage and hence would impede the converter from quickly changing the motor line-to-line voltage. For this reason, a careful selection of the DC link capacitor C_{DC} is necessary, as described later in Section III-E. The 1/3 PWM is hence not suitable for drive systems where high dynamic response of the motor torque/speed is required. Instead, 1/3 PWM is more suitable for drive systems with low dynamics that are mostly operated under steady state conditions, as compressor drives.

III. Component Stresses

In this section, the switching losses and the voltage/current stresses on the different converter components are calculated for the drive system with the specifications of Table I. The analysis is performed for the 1/3 PWM modulation strategy as well as for the conventional 2/3 PWM and 3/3 PWM over the whole operating range of the motor. For the considered application example, the battery voltage ranges within U_b = 40...60 V, however, for the following analysis the lowest battery voltage U_b = 40 V is considered, where the highest current stress in the DC/DC stage appears. The motor voltage ranges within $\hat{U}_m$ = 0...40 V (phase amplitude), while the maximum motor voltage $\hat{U}_m$ = 40 V operation yields the highest component stresses. For the sake of simplicity a resistive load $R = 3\hat{U}_{m,max}/2P_{max}$ = 4.8 Ω is assumed and hence a unity power factor (PF), cos (φ) = 1, is obtained. A comprehensive analysis of the component stresses for a PF cos (φ) < 1 is given in Appendix A. In order to further simplify the analysis, the current ripple of the DC/DC stage inductor L_b and the DC/AC stage filter inductors L_m is neglected, unless stated otherwise.

TABLE I
Motor Drive Specifications. The Worst Case Operating Condition of the Two-Stage DC/AC Converter, Where the Highest Component Stresses Appear, Is Highlighted in Bold.

Parameter	Value
Battery voltage (U_b)	**40**–60 V
Battery current (I_b)	0–**12.5**A (for U_b = 40 V)
Motor fundamental frequency (f_m)	0–**400** Hz
Motor voltage amplitude ($\hat{U}_m$)	0–**40** V (phase)
Motor current amplitude ($\hat{I}_m$)	0–**8.3** A
Modulation index $\left(M = \frac{\hat{U}_m}{\frac{1}{2}U_b}\right)$	0–**2** (for U_b = 40 V)
Power (P)	0–**500** W

In a typical DC/AC two-level inverter, the modulation index is defined as the ratio between motor phase voltage amplitude and half the DC link voltage, $M_m = 2\hat{U}_m/u_{DC}$ and ranges within 0–1.15. However, since a DC/DC stage precedes the DC/AC stage in the case at hand, it is desirable to relate $\hat{U}_m$ to the battery supply voltage U_b instead of u_{DC}. Therefore, the modulation index is redefined as the ratio between motor and half of the battery voltage

$$M = \frac{\hat{U}_m}{\frac{1}{2}U_b}. \tag{8}$$

The modulation index M can exceed the value of 1.15 thanks to the DC/DC stage that can boost the supplying battery voltage. For the system at hand (cf., Table I) the modulation index ranges within M = 0...2. Thereby, the transferred power P, battery current I_b and motor fundamental phase current amplitude $\hat{I}_m$ can be derived as a function of the modulation index

$$P = M^2\frac{3U_b^2}{8R},\ I_b = M^2\frac{3U_b}{8R},\ \hat{I}_m = M\frac{U_b}{2R}. \tag{9}$$

A. Semiconductor Voltage Stress

Firstly, the voltage stress on the power semiconductor devices is analysed. The semiconductors of the DC/DC and of the DC/AC stage are blocking and/or switching the DC link voltage u_{DC}. A higher DC link voltage u_{DC} results in higher switching losses and hence a higher thermal stresses on the semiconductor devices. Furthermore, the maximum DC link voltage $u_{DC,max}$ with some additional safety margin dictates the voltage rating of the employed semiconductor devices. The maximum DC link voltage always appears for the maximum motor voltage (in the case at hand represented by ($M = M_{max} = 2$), and is

$$\begin{aligned} U_{\mathrm{DC,max}}\big|_{\mathrm{3/3\ PWM}} &= 2\hat{U}_{\mathrm{m,max}} = M_{\mathrm{max}} U_{\mathrm{b}} \\ U_{\mathrm{DC,max}}\big|_{\mathrm{2/3\ PWM}} &= \sqrt{3}\,\hat{U}_{\mathrm{m,max}} = M_{\mathrm{max}} \frac{\sqrt{3}}{2} U_{\mathrm{b}} \\ U_{\mathrm{DC,max}}\big|_{\mathrm{1/3\ PWM}} &= \sqrt{3}\,\hat{U}_{\mathrm{m,max}} = M_{\mathrm{max}} \frac{\sqrt{3}}{2} U_{\mathrm{b}}. \end{aligned} \tag{10}$$

Therefore, both the 1/3 PWM and 2/3 PWM schemes lead to a 13% voltage stress reduction compared to 3/3 PWM.

B. Semiconductor Switching Losses

The reduction of the switching losses P_{sw} of the DC/AC stage is the main advantage of the 1/3 PWM modulation, compared to conventional 2/3 PWM. In the following, the switching losses for the 1/3 PWM are analytically derived and compared against the conventional modulation strategies. To this end, the switching energy dissipation E_{sw} for each hard switching transition is approximated as a linear function of the commutation current I_{sw} as

$$E_{\mathrm{sw}}(I_{\mathrm{sw}}) = k_0 + k_1 I_{\mathrm{sw}}. \tag{11}$$

Accordingly, the switching power dissipation for a switching frequency f_{s} is

$$P_{\mathrm{sw}}(I_{\mathrm{sw}}) = f_{\mathrm{s}} E_{\mathrm{sw}} = f_{\mathrm{s}} (k_0 + k_1 I_{\mathrm{sw}}). \tag{12}$$

The parameters k_0 and k_1 depend on the switched voltage U_{sw}. Namely the parameter k_0 represents the constant part of the switching losses and is calculated in literature [21] (assuming unipolar power semiconductors) as

$$k_0(U_{\mathrm{sw}}) = Q_{\mathrm{oss}}(U_{\mathrm{sw}}) \cdot U_{\mathrm{sw}}, \tag{13}$$

where Q_{oss} is the electric charge stored in the non-linear output parasitic capacitance C_{oss} of the MOSFET

$$Q_{\mathrm{oss}}(U_{\mathrm{sw}}) = \int_0^{U_{\mathrm{sw}}} C_{\mathrm{oss}}(u)\mathrm{d}u. \tag{14}$$

For the case at hand, the parameter $k_1(U_{\mathrm{sw}})$ depends on the semiconductor technology and the gate driver configuration [22], [23]. Since the DC link voltage does not drastically change for the different modulation strategies as shown in (10), it can be assumed for a first step worst case consideration that the parameters k_0 and k_1 are the same regardless of the modulation strategy.

The expression given in (12) is used for the calculation of the switching losses of the DC/DC stage, which are the same regardless of the modulation strategy

$$P_{\mathrm{sw}} = f_{\mathrm{s,b}} (k_0 + k_1 I_{\mathrm{b}}). \tag{15}$$

Subsequently the expression (12) for the switching losses is applied to the DC/AC stage, where the commutation current varies over time in a sinusoidal fashion. In order to account for the sinusoidal current waveform, an integration of (12) over the fundamental period T_{m} is performed. In the case of 3/3 PWM, the resulting sum of the switching losses for all three bridge-legs of the DC/AC stage (for assumed unity power factor cos (φ) = 1 load condition) is

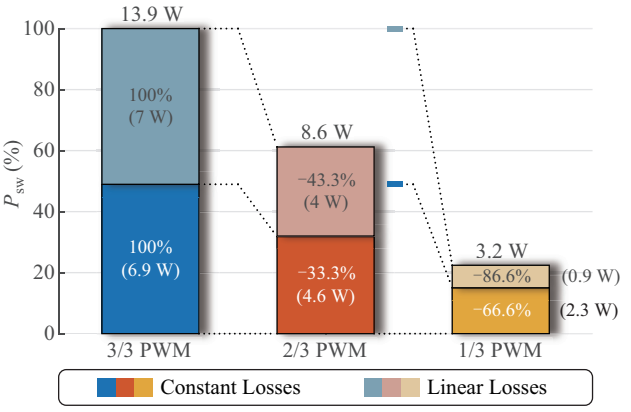

Fig. 6. Switching losses of the DC/AC stage under maximum motor voltage, i.e., $M = 2$ for the case at hand. For the calculations a unity power factor cos (φ) = 1 is assumed. Numerical values are derived for the worst case operating conditions of Table I and the parameters of Table VI.

$$P_{\mathrm{sw}}\big|_{\mathrm{3/3\ PWM}} = 3 f_{\mathrm{s,m}} \left(k_0 + k_1 \frac{2}{\pi} \hat{I}_{\mathrm{m}} \right). \tag{16}$$

The switching losses comprise two components, a constant part $3f_{\mathrm{s,m}}k_0$ which is independent of the converter load and a linear part $3f_{\mathrm{s,m}}k_1 2/\pi\, \hat{I}_{\mathrm{m}}$ (proportional to the average value of a sinusoidal current half cycle) which increases linearly with the output current $\hat{I}_{\mathrm{m}}$ and is used to characterise the load state. The maximum switching losses of the DC/AC stage occur for maximum motor voltage/power i.e., $M = 2$ and are illustrated in Fig. 6. Similarly, the switching losses of the DC/AC stage employing the 2/3 PWM are derived using (12)

$$P_{\mathrm{sw}}\big|_{\mathrm{2/3\ PWM}} = 3 f_{\mathrm{s,m}} \left[\underbrace{\frac{2}{3}}_{-33.3\%} k_0 + \underbrace{\left(1 - \frac{\sqrt{3}}{4}\right)}_{-43.3\%} k_1 \frac{2}{\pi} \hat{I}_{\mathrm{m}} \right]. \tag{17}$$

The 2/3 PWM yields a reduction of the constant part of the switching losses by 33.3% and of the linearly current dependent part of the switching losses by 43.3%, compared to 3/3 PWM, since each phase is switched for $2T_{\mathrm{m}}/3$ of the fundamental period T_{m}. Finally, the switching losses for 1/3 PWM are calculated,

$$P_{\mathrm{sw}}\big|_{\mathrm{1/3\ PWM}} = 3 f_{\mathrm{s,m}} \left[\underbrace{\frac{1}{3}}_{-66.6\%} k_0 + \underbrace{\left(1 - \frac{\sqrt{3}}{2}\right)}_{-86.6\%} k_1 \frac{2}{\pi} \hat{I}_{\mathrm{m}} \right]. \tag{18}$$

With 1/3 PWM a drastic reduction of the switching losses is achieved, since each phase is switched only for $T_{\mathrm{m}}/3$ of the fundamental period T_{m}. Namely, a 66.6% reduction of the constant part and a 86.6% reduction of the linear part is possible compared to 3/3 PWM. Furthermore, 1/3 PWM notably outperforms 2/3 PWM in terms of switching losses.

The switching losses of 2/3 PWM and 1/3 PWM for maximum motor voltage/current and $M = 2$ are plotted in Fig. 6. It is noted, that the switching losses reduction achieved by means of 1/3 PWM, simultaneously enables a lower semiconductor heatsink volume [24].

C. Semiconductor Current Stress

For the calculation of the conduction losses, the current ripple of the DC/DC stage inductor L_b and DC/AC stage filter inductor L_m is neglected. Accordingly, the resulting total conduction losses are independent of the modulation strategy of both stages and are equal to

$$P_{cd} = I_b^2 R_{Tb,on} + \frac{3}{2} I_m^2 R_{Tm,on}, \tag{19}$$

where $R_{Tb,on}$ and $R_{Tm,on}$ are the on-state resistances of the DC/DC and DC/AC stage (unipolar) power semiconductor devices, respectively. However, the sharing of the conduction losses among the semiconductor devices, i.e., the sharing of the RMS current stress between the high-side and low-side switches, changes depending on the modulation strategy. It is therefore important to analyse the current stress for each semiconductor device individually in order to provide a basis for the proper selection of the components in the design process.

The RMS current stress of T_{b1} and T_{b2} of the DC/DC stage is analytically derived for the different modulation techniques over the whole modulation range and results as

$$I_{Tb1,RMS}\big|_{3/3\ PWM} = \begin{cases} I_b & \text{for } M \leqslant 1 \\ I_b\sqrt{\dfrac{1}{M}} & \text{for } M > 1 \end{cases} \tag{20}$$

$$I_{Tb2,RMS}\big|_{3/3\ PWM} = \begin{cases} 0 & \text{for } M \leqslant 1 \\ I_b\sqrt{1-\dfrac{1}{M}} & \text{for } M > 1 \end{cases} \tag{21}$$

$$I_{Tb1,RMS}\big|_{2/3\ PWM} = \begin{cases} I_b & \text{for } M \leqslant \dfrac{2}{\sqrt{3}} \\ I_b\sqrt{\dfrac{2}{\sqrt{3}\,M}} & \text{for } M > \dfrac{2}{\sqrt{3}} \end{cases} \tag{22}$$

$$I_{Tb2,RMS}\big|_{2/3\ PWM} = \begin{cases} 0 & \text{for } M \leqslant \dfrac{2}{\sqrt{3}} \\ I_b\sqrt{1-\dfrac{2}{\sqrt{3}\,M}} & \text{for } M > \dfrac{2}{\sqrt{3}} \end{cases} \tag{23}$$

$$I_{Tb1,RMS}\big|_{1/3\ PWM} = \begin{cases} I_b & \text{for } M \leqslant \dfrac{2}{\sqrt{3}} \\ I_b\sqrt{\dfrac{6\ln(3)}{\sqrt{3}\,\pi M}} & \text{for } M > \dfrac{4}{3} \end{cases} \tag{24}$$

$$I_{Tb2,RMS}\big|_{1/3\ PWM} = \begin{cases} 0 & \text{for } M \leqslant \dfrac{2}{\sqrt{3}} \\ I_b\sqrt{1-\dfrac{6\ln(3)}{\sqrt{3}\,\pi M}} & \text{for } M > \dfrac{4}{3} \end{cases} \tag{25}$$

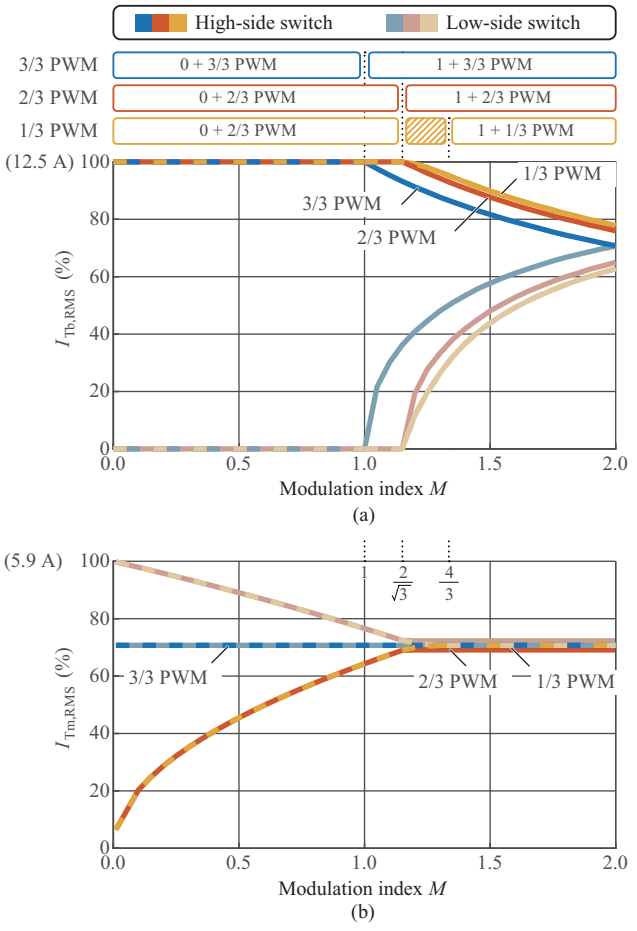

Fig. 7. Semiconductor device current stress for the three modulation strategies over the whole operating range, $M = 0...2$ considered in the case at hand. (a) Normalized RMS current of DC/DC stage high- and low-side semiconductor devices, with respect to the DC/DC stage RMS inductor current $I_{Lb,RMS}$. (b) Normalized RMS current of DC/AC stage high-and low-side semiconductor devices, with respect to the DC/AC stage RMS inductor current $I_{Lm,RMS}$. Numerical values are derived for the worst case operating conditions of Table I and the parameters of Table VI.

The semiconductor devices current stresses, normalized with respect to the DC/DC stage inductor (L_b) RMS current $I_{Lb,RMS} = I_b$, are shown in Fig. 7(a). It should be noted that the sum of the instantaneous currents of the T_{b1} and T_{b2} semiconductor devices is equal to the L_b inductor current

$$i_{Tb1}(t) + i_{Tb2}(t) = i_{Lb}(t). \tag{26}$$

However, the relationship between the RMS currents is nonlinear,

$$I_{Tb1,RMS}^2 + I_{Tb2,RMS}^2 = I_{Lb,RMS}^2. \tag{27}$$

When the modulation index is low and the DC/DC stage is deactivated (e.g., 1/3 PWM and $M \leqslant 2/\sqrt{3}$), the high-side switch T_{b1} of the DC/DC stage is clamped and therefore experiences the whole RMS current stress. However, this is typically not a problem since for low modulation indexes

(low DC/AC stage output voltage and/or motor speed) the power P and thus battery current I_b is anyway low. The 1/3 PWM leads to asymmetric current distribution between the high-side and the low-side switches similar to the 2/3 PWM, while the asymmetry reduces as the modulation index and/or the transferred power increases. In summary, the asymmetric current distribution caused by 1/3 PWM for low modulation index M, does not require over-dimensioning of the DC/DC stage semiconductor devices. The (symmetric) stresses for high modulation indexes M are higher than the (asymmetric) stresses for low values of M, and hence dominate the dimensioning of the DC/DC stage semiconductors.

Similarly, the RMS current stress of the semiconductor devices T_{m1} and T_{m2} of the DC/AC stage is analytically calculated as

$$I_{\mathrm{Tm1,RMS}}\big|_{\text{3/3 PWM}} = I_{\mathrm{Tm2,RMS}}\big|_{\text{3/3 PWM}} = \frac{\hat{I}_m}{\sqrt{2}}\frac{1}{\sqrt{2}} \tag{28}$$

$$I_{\mathrm{Tm1,RMS}}\big|_{\text{2/3 PWM}} = \begin{cases} \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{\dfrac{3\sqrt{3}M}{4\pi}} & \text{for } M \leqslant \dfrac{2}{\sqrt{3}} \\ \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{\dfrac{3}{2\pi}} & \text{for } M > \dfrac{2}{\sqrt{3}} \end{cases} \tag{29}$$

$$I_{\mathrm{Tm2,RMS}}\big|_{\text{2/3 PWM}} = \begin{cases} \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{1-\dfrac{3\sqrt{3}M}{4\pi}} & \text{for } M \leqslant \dfrac{2}{\sqrt{3}} \\ \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{1-\dfrac{3}{2\pi}} & \text{for } M > \dfrac{2}{\sqrt{3}} \end{cases} \tag{30}$$

$$I_{\mathrm{Tm1,RMS}}\big|_{\text{1/3 PWM}} = \begin{cases} \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{\dfrac{3\sqrt{3}M}{4\pi}} & \text{for } M \leqslant \dfrac{2}{\sqrt{3}} \\ \dfrac{\hat{I}_m}{\sqrt{2}}\dfrac{1}{\sqrt{2}} & \text{for } M > \dfrac{4}{3} \end{cases} \tag{31}$$

$$I_{\mathrm{Tm2,RMS}}\big|_{\text{1/3 PWM}} = \begin{cases} \dfrac{\hat{I}_m}{\sqrt{2}}\sqrt{1-\dfrac{3\sqrt{3}M}{4\pi}} & \text{for } M \leqslant \dfrac{2}{\sqrt{3}} \\ \dfrac{\hat{I}_m}{\sqrt{2}}\dfrac{1}{\sqrt{2}} & \text{for } M > \dfrac{4}{3} \end{cases}. \tag{32}$$

The semiconductor devices current stresses, normalized with respect to the DC/AC stage inductor (L_m) RMS current $I_{Lm,RMS} = \hat{I}_m/\sqrt{2}$, are shown in Fig. 7(b). The 3/3 PWM modulation results in symmetric current sharing between the high-side and low-side semiconductor devices of the DC/AC stage (28). In contrast, 2/3 PWM and 1/3 PWM both lead to a similar asymmetric current stress on the semiconductor devices (29)–(32). In particular, higher current stress appears on the low-side switch of the DC/AC stage T_{ma2} when the modulation index is low (e.g., $M \leqslant 2/\sqrt{3}$ and 1/3 PWM). As the modulation index increases (e.g., $M > 4/3$ and 1/3 PWM) the RMS current sharing becomes symmetric. The asymmetric current stress for low modulation indexes (i.e., low motor voltage $\hat{U}_m$ and/or motor speed) is critical. Care has to be taken with the thermal design of the low-side switches T_{m2}, such that they can conduct the nominal motor current $\hat{I}_m$ and hence ensure nominal motor torque during motor acceleration, starting from standstill. It is noted that there is an alternative 1/3 PWM and 2/3 PWM implementation which ensures symmetric current distribution for the whole operating range and is analysed in Appendix B.

D. Inductive Components

The inductor losses are investigated, in a first step. It is assumed that a two-stage DC/AC converter system is designed for conventional 3/3 PWM (e.g., features a cooling system that can withstand the high switching losses of the 3/3 PWM) and that the inductive components cannot be changed. In particular, the DC/DC stage features an inductance L_b and the DC/AC stage employs an inductance L_m, regardless of the modulation scheme.

In general, there is a direct relation between the inductor losses and the RMS inductor current ripple $\Delta I_{L,RMS}$, as a high RMS current ripple results in a high frequency RMS flux density and hence substantial core losses [25]. In addition, high RMS current ripple causes high-frequency winding losses due to skin and proximity effect. Therefore, the RMS inductor current ripple $\Delta I_{L,RMS}$ is a reasonable performance indicator for the design of the inductive components and is calculated in the following for the different modulation strategies over the whole operating range.

For the DC/DC stage the same inductance value L_b is considered regardless of the modulation strategy. Subsequently, the RMS inductor current ripple $\Delta I_{Lb,RMS}$ is calculated for the considered modulation strategies based on a numeric solver (i.e., no analytical solution). The RMS inductor current ripple, normalized with respect to the worst case local RMS current ripple,

$$\Delta I_{\mathrm{Lb,RMS,max}} = \frac{\hat{U}_{\mathrm{m,max}}}{4\sqrt{3}\,f_{\mathrm{s,b}}L_b}, \tag{33}$$

is plotted in Fig. 8(a). When the modulation index is low and the DC/DC stage is deactivated (e.g., 1/3 PWM for $M \leqslant 2/\sqrt{3}$), the high-side switch T_{b1} of the DC/DC stage is clamped and therefore no current ripple appears on the inductor L_b. As the modulation index increases (e.g., 1/3 PWM for $M > 2/\sqrt{3}$) the inductor gradually conducts a current with increasing ripple. Due to the lower DC link voltage for the same DC/AC stage output voltage, 1/3 PWM exhibits significantly lower RMS inductor current ripple compared to 3/3 PWM but only slightly lower ripple compared to 2/3 PWM.

Similarly, for the DC/AC stage the same inductance value L_m is considered independent of the modulation strategy. The RMS inductor current ripple $\Delta I_{Lm,RMS}$ is calculated for all modulation strategies over the complete operating range based on a numeric solver (i.e., no analytic solution). The RMS

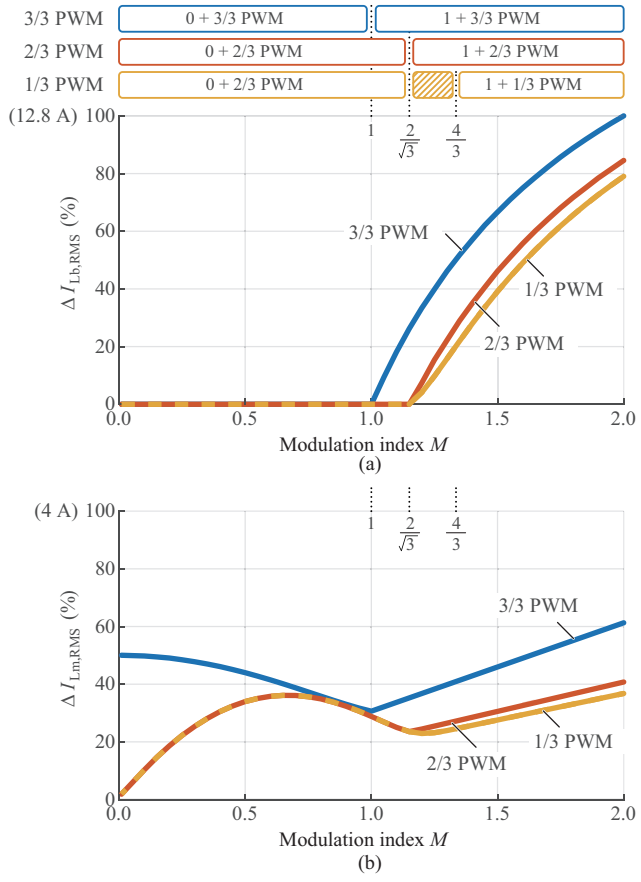

Fig. 8. Inductor RMS current ripple for different modulation strategies over the whole operating range $M = 0, ..., 2$ considered in the case at hand. (a) The normalized RMS current ripple of the DC/DC stage inductor L_b is depicted. (b) The normalized RMS current ripple of the DC/AC stage filter inductor L_m is plotted. Numerical values are derived for the worst case operating conditions of Table I and the parameters of Table VI.

inductor current ripple, normalized with respect to the worst case local RMS current ripple

$$\Delta I_{Lm,RMS,max} = \frac{\hat{U}_{m,max}}{4\sqrt{3} f_{s,m} L_m}, \tag{34}$$

is depicted in Fig. 8(b). In particular for 1/3 PWM, when the modulation index is low, $M \leqslant 2/\sqrt{3}$, the DC link voltage is constant and equal to the battery voltage $u_{DC} = U_b$. As the modulation index gradually increases (i.e., $M = 0 \rightarrow 2/\sqrt{3}$), the current ripple RMS value initially increases, reaches a local maximum value and then decreases [19]. When the modulation index exceeds the threshold value of $M = 2/\sqrt{3}$, the DC/DC stage is activated and the DC link voltage increases. Accordingly, the ripple of the DC/AC filter inductor which is proportional to the DC link voltage also increases. In general, 1/3 PWM yields similar current ripple RMS value as the 2/3 PWM but lower current ripple compared to 3/3 PWM (21% reduction of $\Delta I_{Lm,RMS}$% occurs for $M = 2$).

In a more general case, where there is not a pre-existing converter designed for 3/3 PWM, different inductance values can be advantageously selected for the different modulation strategies. Besides a smaller heatsink volume for the DC/AC stage (thanks to the low switching losses), the 1/3 PWM allows for smaller inductance values, which translates into further volume reduction [26]. Accordingly, the minimum required inductance value L_b of the DC/DC stage and the inductance L_m of the DC/AC stage are analytically calculated.

In order to calculate the required inductance L_b, a worst case current ripple amplitude $\Delta I_{Lb,PK}$ (single side peak value) is assumed. The same current ripple limit applies regardless of the modulation strategy and the required inductance is given by

$$L_b \geqslant \frac{d_{min}(1 - d_{min})U_{DC,max}}{2\Delta I_{Lb,PK} f_{s,b}}, \quad d_{min} = \frac{U_b}{U_{DC,max}}, \tag{35}$$

where $f_{s,b}$ is the switching frequency of the DC/DC stage. Applying (35) to 3/3 PWM, where $U_{DC,max} = 2\hat{U}_{m,max}$ (10), the required inductance is

$$L_b\big|_{3/3\ PWM} \geqslant \frac{\hat{U}_{m,max}}{4\Delta I_{Lb,PK} f_{s,b}}. \tag{36}$$

Subsequently, (35) is applied to 1/3 PWM and 2/3 PWM. The 1/3 PWM and 2/3 PWM schemes require the same inductance value because both modulation schemes feature the same maximum instantaneous DC link voltage $U_{DC,max} = \sqrt{3}\hat{U}_{m,max}$ (10). The inductance is calculated as

$$L_b\big|_{1/3\ PWM} = L_b\big|_{2/3\ PWM} \geqslant \frac{\left(1 - \frac{1}{\sqrt{3}}\right)\hat{U}_{m,max}}{2\Delta I_{Lb,PK} f_{s,b}}. \tag{37}$$

Consequently, 2/3 PWM and 1/3 PWM require 15% lower inductance compared to 3/3 PWM for the DC/DC stage, resulting in an accordingly higher power density.

For the calculation of the DC/AC stage filter inductance L_m, a worst case current ripple amplitude $\Delta I_{Lm,PK}$ (single side peak value) is considered. The same limit applies for all possible modulation strategies and the required inductance is given by

$$L_m \geqslant \frac{U_{DC,max}}{8\Delta I_{Lm,PK} f_{s,m}}, \tag{38}$$

where $f_{s,m}$ is the switching frequency of the DC/AC stage. Applying (38) to 3/3 PWM, the required inductance is

$$L_m\big|_{3/3\ PWM} \geqslant \frac{\hat{U}_{m,max}}{4\Delta I_{Lm,PK} f_{s,m}}. \tag{39}$$

The 2/3 PWM and 1/3 PWM schemes require the same DC/AC stage inductance L_m, which based on (38) is

$$L_m\big|_{1/3\ PWM} = L_m\big|_{2/3\ PWM} \geqslant \frac{\sqrt{3}\,\hat{U}_{m,max}}{8\Delta I_{Lm,PK} f_{s,m}}. \tag{40}$$

Accordingly, 2/3 PWM and 1/3 PWM are reducing the DC/AC stage filter inductance requirement by 13% and hence yield a smaller inductor volume compared to 3/3 PWM.

E. DC Link Capacitor

The DC link capacitor C_{DC} must be carefully selected. On the one hand, the capacitance value should be small in order to allow the DC/DC stage to accurately control the DC link voltage to a six-pulse shape during 1/3 PWM operation (cf., Fig. 3(a.iii)). In particular, the resonant frequency of the L_b −C_{DC} filter $f_{r,DC}$, must be $a_f \sim 10$ times higher compared to the repetition frequency $6f_m$ of the six-pulse shaped DC link voltage, under 1/3 PWM operation

$$f_{r,DC} \geqslant a_f \cdot 6f_m, \text{ where } f_{r,DC} = \frac{1}{2\pi\sqrt{L_b C_{DC}}}. \quad (41)$$

Solving the inequality for C_{DC} provides an upper bound for the DC link capacitance

$$C_{DC} \leqslant \frac{1}{144\pi^2 L_b a_f^2 f_m^2}. \quad (42)$$

On the other hand, the capacitance value should be large enough in order to limit the DC link voltage ripple amplitude ΔU_{DC} to a sufficiently low value. In particular, the capacitor C_{DC} conducts the switched output current of the DC/DC stage as well as the switched input current of the DC/AC stage, both contributing to the DC link voltage ripple $\Delta u_{DC}(t)$. Therefore, the DC link capacitance value must be

$$C_{DC} \geqslant \frac{I_{b,max}}{8f_{s,b}\Delta U_{DC}} + \frac{\hat{I}_{m,max}}{8f_{s,m}\Delta U_{DC}}, \quad (43)$$

independent of the modulation strategy, in order to ensure a DC link voltage ripple amplitude less or equal to ΔU_{DC}. The design constraints of (42) and (43) define a design space within which the capacitance C_{DC} must be selected. The resulting DC link capacitance value is typically small since there is no need for energy storage in a three-phase system (in contrast to a single-phase system). An upper bound for the DC link capacitor RMS current stress is

$$I_{C_{DC},RMS,max} = \sqrt{\frac{I_{b,max}^2}{4} + \frac{\hat{I}_{m,max}^2}{4}}. \quad (44)$$

A detailed analysis of the DC link capacitor current stress can be found in [27]. In summary, the DC link capacitor must conduct a high-frequency switched current with high peak values, while a low capacitance value is typically required. For this reason, ceramic or film capacitors are suggested for the DC link implementation.

F. Motor Common-Mode Voltage

The motor CM voltage resulting from the different modulation strategies is now analysed. A motor CM voltage with high du/dt would results in parasitic CM currents which would partly flow through the motor bearings and could result in bearing damage [28]. For this reason, a DC link referenced output filter L_m−C_m is employed (cf., Fig. 1(a)) which protects the motor against CM (and differential-mode) voltages with high du/dt [29]–[33]. In particular, the DC link referenced output filter directly attenuates the switching frequency CM voltage generated by the DC/AC stage and hence only a small residual high-frequency (HF) motor CM voltage with an amplitude

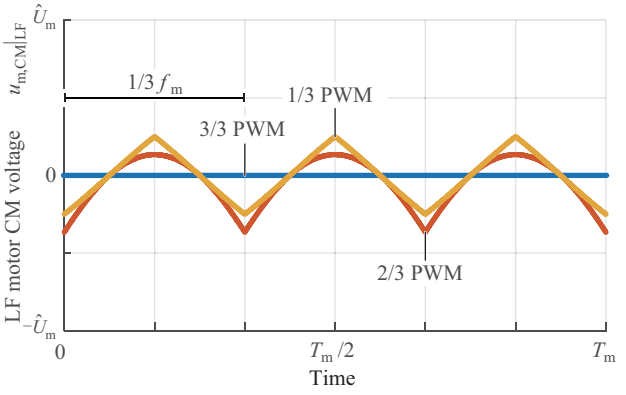

Fig. 9. Low-frequency component of the motor CM voltage $u_{m,CM}|_{LF}(t)$, for the three examined modulation strategies cf., Fig. 2(a)–(c). Waveforms shown for maximum motor voltage, i.e., $M = 2$ for the case at hand.

$$\hat{U}_{m,CM}|_{HF} = \frac{1}{64}\frac{U_{DC,max}}{L_m C_m f_{s,m}^2} \quad (45)$$

remains at the motor terminals, where $U_{DC,max}$ is given by (10). When a DC link referenced output filter is employed, $\hat{U}_{m,CM}|_{HF}$ is noncritical concerning bearing currents and is marginally higher for 3/3 PWM as opposed to 2/3 PWM and 1/3 PWM because of the marginally higher DC link voltage $U_{DC,max}$ of the former.

Furthermore, the motor CM voltage can feature a low-frequency (LF) component

$$u_{m,CM}|_{LF}(t) = u_{DC}(t) \cdot \left(\frac{d_a + d_b + d_c}{3} - \frac{1}{2}\right), \quad (46)$$

depending on the employed modulation scheme, as depicted in Fig. 9. In particular, 3/3 PWM features zero LF motor CM voltage $u_{m,CM}|_{LF}(t) = 0$, because the sum of the three-phase DC/AC stage duty cycles is constant over time (cf., Fig. 2(a.ii)). In contrast, 2/3 PWM and 1/3 PWM feature a time varying LF motor CM voltage [9] with a repetition frequency equal to $3f_m$, since the sum of the three-phase DC/AC stage duty cycles is different from 0 (cf., Fig. 2(b.ii) and (c.ii), respectively). The LF motor CM voltage is also noncritical concerning motor bearing currents.

G. Design Guidelines

For designing the two-stage DC/AC converter shown in Fig.

TABLE II
DC/DC STAGE SEMICONDUCTOR DESIGN/STRESS SUMMARY FOR THE WORST CASE OPERATING CONDITIONS OF TABLE I. NUMERICAL VALUES ARE DERIVED FOR THE PARAMETERS OF TABLE VI.

	DC/DC stage			
	$U_{\mathrm{DC,max}}$	P_{sw}[1]	$I_{\mathrm{Tb1,RMS}}$[1]	$I_{\mathrm{Tb2,RMS}}$[1]
3/3 PWM	$2\hat{U}_{\mathrm{m}} = 80\ \mathrm{V}$	$f_{\mathrm{s,b}}(k_0 + k_1 I_{\mathrm{b}}) = 10.1\ \mathrm{W}$	$I_{\mathrm{b}}\sqrt{\frac{1}{M}} = 8.8\ \mathrm{A}$	$I_{\mathrm{b}}\sqrt{1-\frac{1}{M}} = 8.8\ \mathrm{A}$
2/3 PWM	$\sqrt{3}\hat{U}_{\mathrm{m}} = 69\ \mathrm{V}$	$f_{\mathrm{s,b}}(k_0 + k_1 I_{\mathrm{b}}) = 10.1\ \mathrm{W}$	$I_{\mathrm{b}}\sqrt{\frac{2}{\sqrt{3}M}} = 9.5\ \mathrm{A}$	$I_{\mathrm{b}}\sqrt{1-\frac{2}{\sqrt{3}M}} = 8.1\ \mathrm{A}$
1/3 PWM	$\sqrt{3}\hat{U}_{\mathrm{m}} = 69\ \mathrm{V}$	$f_{\mathrm{s,b}}(k_0 + k_1 I_{\mathrm{b}}) = 10.1\ \mathrm{W}$	$I_{\mathrm{b}}\sqrt{\frac{6\ln(3)}{\sqrt{3}\pi M}} = 9.7\ \mathrm{A}$	$I_{\mathrm{b}}\sqrt{1-\frac{6\ln(3)}{\sqrt{3}\pi M}} = 7.8\ \mathrm{A}$

[1] DC/DC stage inductor L_{b} current ripple is neglected for the calculations.

TABLE III
DC/AC STAGE SEMICONDUCTOR DESIGN/STRESS SUMMARY FOR THE WORST CASE OPERATING CONDITIONS OF TABLE I. NUMERICAL VALUES ARE DERIVED FOR THE PARAMETERS OF TABLE VI.

	DC/AC stage		
	P_{sw}[1]	$I_{\mathrm{Tm1,RMS}}$[1]	$I_{\mathrm{Tm2,RMS}}$[1]
3/3 PWM	$3f_{\mathrm{s,m}}(k_0 + k_1\frac{2}{\pi}\hat{I}_{\mathrm{m}}) = 13.9\ \mathrm{W}$	$\frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\frac{1}{\sqrt{2}} = 4.2\ \mathrm{A}$	$\frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\frac{1}{\sqrt{2}} = 4.2\ \mathrm{A}$
2/3 PWM	$3f_{\mathrm{s,m}}[\frac{2}{3}k_0 + (1-\frac{\sqrt{3}}{4})k_1\frac{2}{\pi}\hat{I}_{\mathrm{m}}] = 8.6\ \mathrm{W}$	$\frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\sqrt{\frac{3}{2\pi}} = 4.1\ \mathrm{A}$	$\frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\sqrt{1-\frac{3}{2\pi}} = 4.3\ \mathrm{A}$
1/3 PWM	$3f_{\mathrm{s,m}}[\frac{1}{3}k_0 + (1-\frac{\sqrt{3}}{2})k_1\frac{2}{\pi}\hat{I}_{\mathrm{m}}] = 3.3\ \mathrm{W}$	$\frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\frac{1}{\sqrt{2}} = 4.2\ \mathrm{A}$	$\frac{\hat{I}_{\mathrm{m}}}{\sqrt{2}}\frac{1}{\sqrt{2}} = 4.2\ \mathrm{A}$

[1] DC/AC stage filter inductor L_{m} current ripple is neglected for the calculations.

TABLE IV
INDUCTOR DESIGN SUMMARY FOR A PRE-EXISTING DRIVE SYSTEM DESIGNED FOR 3/3 PWM. NUMERIC RESULTS DERIVED FOR THE WORST CASE OPERATING CONDITIONS OF TABLE I AND THE PARAMETERS OF TABLE VI.

	DC/DC stage		DC/AC stage	
	L_{b}	$\Delta I_{L\mathrm{b,RMS}}$[1]	L_{m}	$\Delta I_{L\mathrm{m,RMS}}$[1]
3/3 PWM	$\frac{\hat{U}_{\mathrm{m}}}{4\Delta I_{L\mathrm{b,PK}} f_{\mathrm{s,b}}} = 1.5\ \mu\mathrm{H}$	12.8 A	$\frac{\hat{U}_{\mathrm{m}}}{4\Delta I_{L\mathrm{m,PK}} f_{\mathrm{s,m}}} = 4.7\ \mu\mathrm{H}$	2.5 A
2/3 PWM	1.5 μH	10.8 A	4.7 μH	1.6 A
1/3 PWM	1.5 μH	10.1 A	4.7 μH	1.5 A

[1] The values are based on numerical solver.

1(a), the worst case stresses on the DC/DC stage and the DC/AC stage must be identified. The worst case component stress appears for maximum motor voltage and/or transferred power as shown in Table I. In Table II the analytic expressions for the semiconductor voltage/current stresses and the switching losses are summarized for the DC/DC stage. Accordingly, in Table III the analytic expressions are provided for the DC/AC stage. Numerical values are given for the application at hand with the parameters of Table VI. Note that the analytic expressions are general and thus can be easily used for the selection of semiconductor devices of a system with different specifications.

If a drive system designed for conventional 3/3 PWM pre-exists, then 1/3 PWM can be retrofitted to the system by means of a firmware update. In this case, the drive system features a cooling system that can withstand the high DC/AC stage switching losses of the 3/3 PWM and there is no possibility to change the DC/DC stage inductor L_{b} and the DC/AC stage filter inductors L_{m}. The use of the 1/3 PWM scheme leads to a significant switching losses reduction and thus a substantial overall efficiency η improvement. The inductor losses also decrease, since 1/3 PWM results in an RMS current ripple reduction of the DC/DC stage inductor L_{b} and DC/AC stage inductor L_{m}. The inductor performance is summarized in Table IV.

In a more general case, where there is not a pre-existing drive system designed for 3/3 PWM, different inductance values can be selected for the different modulation strategies. Besides a smaller semiconductor heatsink volume of the DC/AC stage, thanks to the low switching losses, the 1/3 PWM allows for smaller inductance values. The inductor values and the resulting inductor RMS current ripple are summarized in

TABLE V
INDUCTOR DESIGN SUMMARY FOR A SYSTEM WHICH IS PURPOSELY DESIGNED FOR THE EMPLOYED MODULATION. NUMERIC RESULTS DERIVED FOR THE WORST CASE OPERATING CONDITIONS OF TABLE I AND THE PARAMETERS OF TABLE VI.

	DC/DC stage		DC/AC stage	
	L_b	$\Delta I_{Lb,RMS}$[1]	L_m	$\Delta I_{Lm,RMS}$[1]
3/3 PWM	$\frac{\hat{U}_m}{4\Delta I_{Lb,PK} f_{s,b}} = 1.5\,\mu H$	12.8 A	$\frac{\hat{U}_m}{4\Delta I_{Lm,PK} f_{s,m}} = 4.7\,\mu H$	2.5 A
2/3 PWM	$\frac{(1-\frac{1}{\sqrt{3}})\hat{U}_m}{2\Delta I_{Lb,PK} f_{s,b}} = 1.27\,\mu H$	12.8 A	$\frac{\sqrt{3}\hat{U}_m}{8\Delta I_{Lm,PK} f_{s,m}} = 4.1\,\mu H$	1.8 A
1/3 PWM	$\frac{(1-\frac{1}{\sqrt{3}})\hat{U}_m}{2\Delta I_{Lb,PK} f_{s,b}} = 1.27\,\mu H$	11.9 A	$\frac{\sqrt{3}\hat{U}_m}{8\Delta I_{Lm,PK} f_{s,m}} = 4.1\,\mu H$	1.7 A

[1] The values are based on numerical solver.

TABLE VI
PARAMETER VALUES OF THE HARDWARE PROTOTYPE SHOWN IN FIG. 10 CORRESPONDING TO THE SCHEMATIC DIAGRAM NOTATION OF FIG. 1(A).

Parameter	Value
DC/DCstage	
Switching frequency ($f_{s,b}$)	300 kHz
Switches (2 in parallel)	200 V EPC 2034
Switching parameters [23]	$k_0 = 15.4\,\mu J$, $k_1 = 1.5\,\mu J/A$
Inductance (L_b)	1.5 μH
Capacitance (C_b)	10 μF
Capacitance (C_{DC})	25 μF, ($\Delta U_{DC} = 0.8$ V, $a_f = 10$)
DC/ACstage	
Switching frequency ($f_{s,m}$)	300 kHz
Switches	200 V EPC 2034
Switching parameters [23]	$k_0 = 7.7\,\mu J$, $k_1 = 1.5\,\mu J/A$
Inductance (L_m)	4.7 μH
Capacitance (C_m)	2 μF

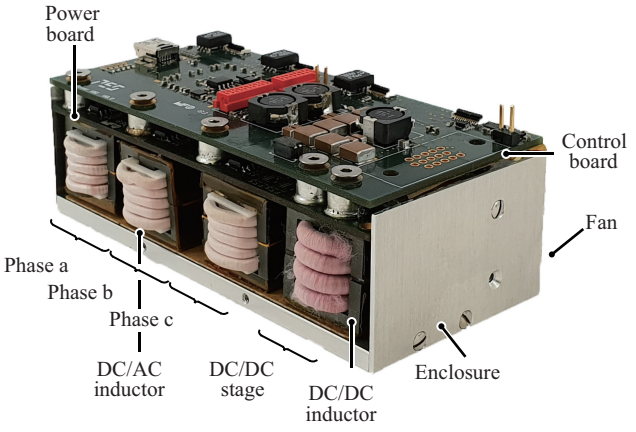

Fig. 10. Three-phase converter hardware prototype employed for experimentally verifying the main characteristics of 3/3, 2/3 and 1/3 PWM. The system comprises a boost-type DC/DC stage and a buck-type DC/AC stage (cf., Fig. 1(a)) and is thus suitable for drive applications with a wide input-output voltage variation. Furthermore, modulation can be easily switched between the different modulation strategies. Dimensions 35 × 50 × 106 mm^3 (11.32 in^3).

Table V. There, the 1/3 PWM not only employs a smaller DC/DC stage inductance L_b and DC/AC inductance L_m, but also features lower RMS current ripples. Therefore, the inductors L_b and L_m can be realised in a more compact way, which translates into a lower overall volume for 1/3 PWM compared to 3/3 PWM.

Finally, the DC link capacitor value must be selected considering a maximum allowed DC link voltage ripple amplitude of $\Delta U_{DC} = 0.8$ V (~ 1% of the DC link voltage) and the operating parameters of Tables I and VI. Based on (42) and (43) this results in 11 μF $\leqslant C_{DC} \leqslant$ 29 μF and/or finally selected value of $C_{DC} = 25\,\mu$F.

IV. HARDWARE VERIFICATION

In order to verify the performance potential of 1/3 PWM modulation, a hardware demonstrator has been built according to the specifications of Table I. The demonstrator system is shown in Fig. 10, while the selected parameter values are summarized in Table VI. The hardware prototype comprises a power and a control board. The power board includes the DC/AC stage and the DC/DC stage half-bridges and the respective gate drivers. Each half-bridge of the DC/AC stage features two 200 V rated EPC 2034 semiconductor devices (i.e., single device per switch) while the DC/DC stage half-bridge employs four EPC 2034 semiconductor devices (i.e., two devices in parallel per switch). The four inductors as well as a custom aluminium heatsink which is optimally designed for the given application, are placed below the power board. Four 25 mm fans are used for forced air cooling. A custom control board which is used for the generation of the appropriate gating signals and the current/voltage measurements is placed on top of the power board.

The 1/3 PWM modulation strategy is implemented in software and tested according to the control diagram of Fig. 4. The experimentally measured waveforms are shown in Fig. 11 for maximum transferred power $P = 500$ W and maximum motor phase voltage amplitude $\hat{U}_m = 40$ V, i.e., modulation index $M = 2$. There, the six-pulse shape of the DC link voltage u_{DC} is clearly visible. Furthermore, the three motor line-to-line voltages are depicted. The DC link voltage is equal to the highest instantaneous motor line-to-line voltage. In addition, the gate signal of phase a of the DC/AC stage is shown, which reveals that the corresponding half-bridge is switched only for 1/3 of the fundamental period T_m.

Subsequently, a transition from 2/3 PWM to 1/3 PWM is shown in Fig. 12. There, the output motor line-to-line voltages are gradually increased and a seamless transition (without unwanted transients) from 2/3 PWM to 1/3 PWM is achieved.

The experimental measurements are verifying the theoretical

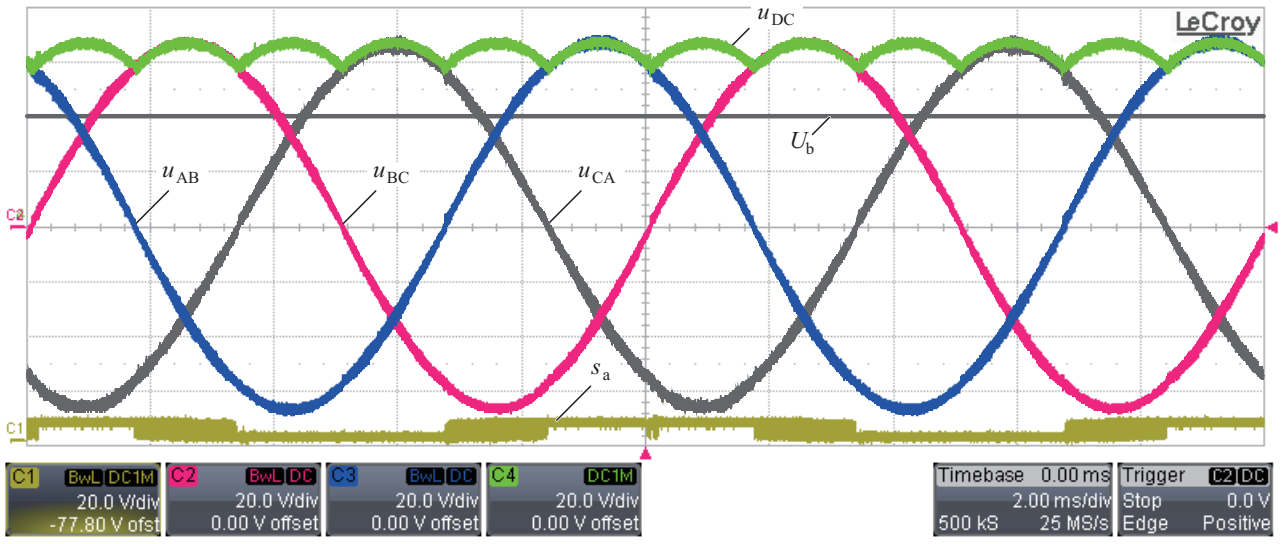

Fig. 11. Experimentally measured waveforms of 1/3 PWM for maximum power $P = 500$ W, maximum motor voltage $\hat{U}_m = 40$ V, modulation index $M = 2$ and a fundamental frequency of $f_m = 100$ Hz. The motor line-to-line voltages u_{AB}, u_{BC} and u_{CA}, the DC link voltage u_{DC} and the gating signal of phase a (s_a) are also depicted. The line-to-line voltage u_{CA} is not directly measured, but instead is reconstructed based on the two other measured line-to-line voltages u_{AB} and u_{BC}.

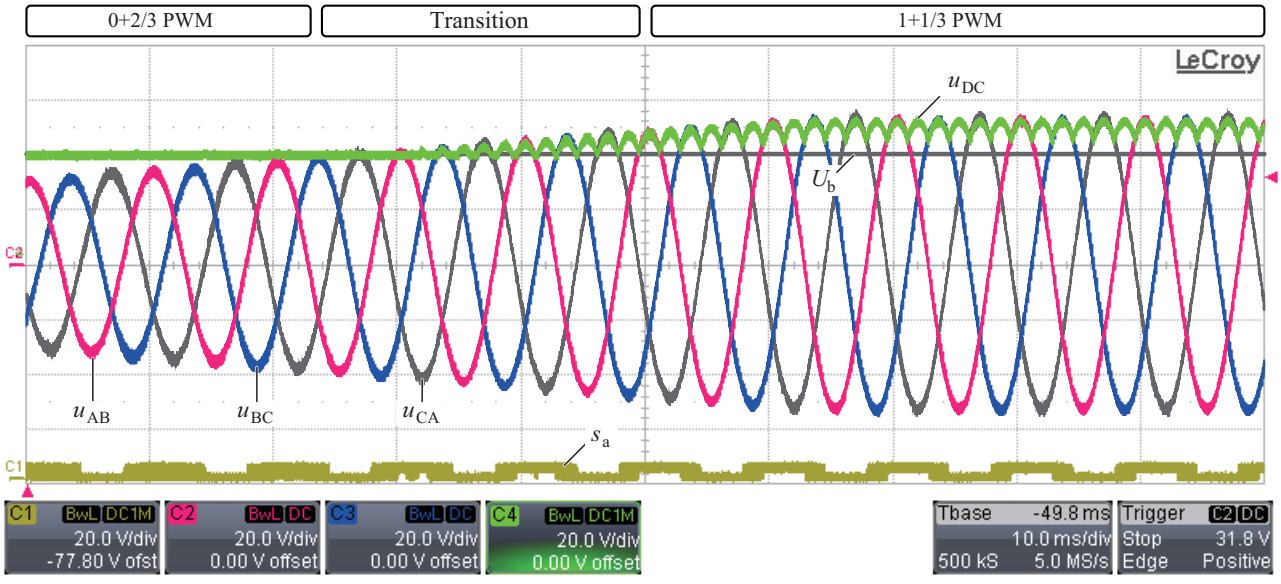

Fig. 12. Experimentally measured transition from 2/3 PWM to 1/3 PWM, where the modulation index (and hence the output AC voltage) is gradually increased: $M = 0.5 \rightarrow 1.5$. The motor line-to-line voltages u_{AB}, u_{BC} and u_{CA}, the DC link voltage u_{DC} and the gating signal of phase a (s_a) are also depicted. The line-to-line voltage u_{CA} is not directly measured, but instead is reconstructed based on the two other measured line-to-line voltages u_{AB} and u_{BC}.

consideration of Section II. It should be pointed out that 1/3 PWM can be applied on existing converter systems as a firmware update. That is, no hardware modifications are needed in order to accommodate the 1/3 PWM scheme.

The converter efficiency characteristic is now measured over the whole output power range, $P = 0...500$ W, in order compare 1/3 PWM against the conventional modulation strategies 2/3 PWM and 3/3 PWM. The results are illustrated in Fig. 13(a). The 3/3 PWM exhibits the worst performance of $\eta \backsimeq 96\%$ nominal efficiency due to the continuous switching of all three DC/AC stage half-bridges. Furthermore, when the modulation index exceeds $M > 1$, the DC/DC stage is activated, resulting in additional losses due to the DC/DC stage semiconductor devices and inductor. Therefore, a sharp decrease in efficiency appears for $M > 1$. The 2/3 PWM out-performs 3/3 PWM with a nominal efficiency of $\eta \backsimeq 97.2\%$.When the modulation index exceeds $M > 2/\sqrt{3}$, the DC/DC stage is activated causing a steep drop in efficiency. The 1/3 PWM features the highest nominal efficiency, $\eta \backsimeq 98\%$, thanks to the drastic reduction of the DC/AC stage switching losses. Note that 1/3 PWM does not suffer from an efficiency reduction for $M > 2/\sqrt{3}$ when the DC/DC stage is activated. This is attributed to the continuous transition between the 0+2/3 and the 1+1/3 modulation regimes of Fig. 5. Namely, for 0+2/3 modulation

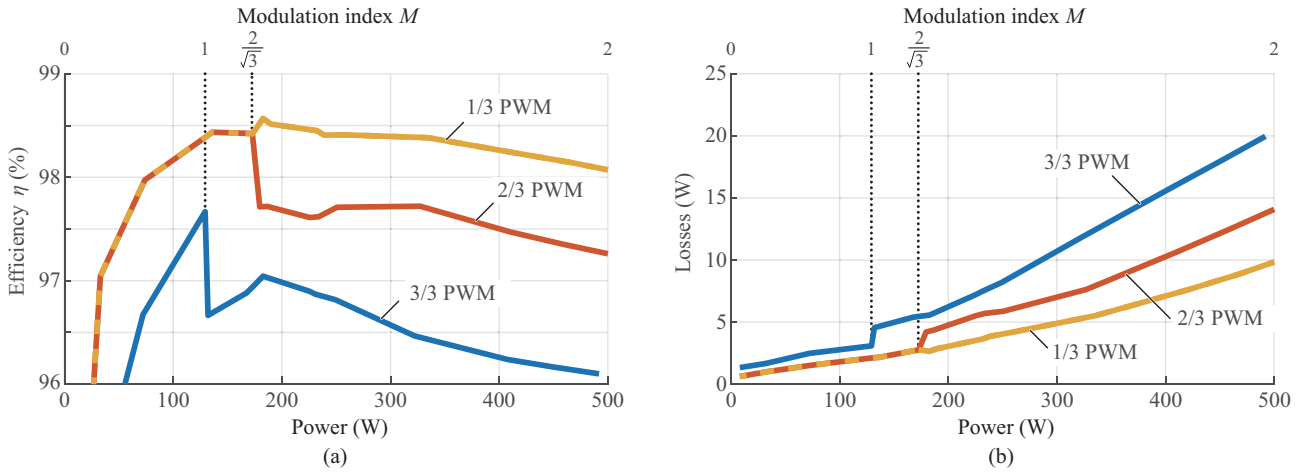

Fig. 13. (a) Efficiency of the hardware prototype employing the 1/3 PWM modulation strategy in the whole operating power range P = 0...500 W. The efficiency measurement is also performed for the conventional 2/3 PWM and 3/3 PWM, and a clear comparative advantage in favour of the 1/3 PWM is deduced. (b) Corresponding losses of the hardware prototype for the different modulation strategies. The converter operating parameters are given in Table VI.

regime the DC/DC stage is not operated, while two phases of the DC/AC stage are switching. For 1+1/3 modulation regime the DC/DC stage half-bridge is switching, while only one phase of the DC/AC stage is operated. Therefore, in any case in total two half-bridges (including the DC/DC and DC/AC stage) are switching, resulting in a smooth efficiency curve. In Fig. 13(b), the losses associated with each modulation strategy are plotted.

There, a 10 W (50%) reduction of the overall converter losses is experimentally achieved with 1/3 PWM compared to 3/3 PWM. It can be assumed that this 10 W losses reduction originates mainly from the DC/AC stage switching losses reduction under 1/3 PWM, while the rest of the loss contributions either remain the same (e.g., DC/DC stage semiconductor switching/conduction losses and DC/AC stage semiconductor conduction losses), or slightly decrease (e.g., DC/DC stage and DC/AC stage inductor losses), compared to 3/3 PWM. Therefore, the experimentally measured 10 W reduction of the DC/AC stage switching looses with 1/3 PWM, matches well with the respective theoretically calculated value of 10.7 W from Fig. 6.

Experimentally measured waveforms of the DC/DC stage inductor (L_b) current are shown in Fig. 14(i), while the DC/AC stage inductor (L_m) current and the inductor current ripple component are depicted in Fig. 14(ii) and (iii), respectively. The results are plotted for the three considered modulation strategies and for a modulation index of M = 1.75. It should be noted that the DC/AC stage inductor current ripple shape is unique to the DC link referenced filter of Fig. 1(a), i.e., for filter capacitors C_m connected to the negative DC link rail [19]. The 3/3 PWM induces the highest current ripple for both the DC/DC stage inductor L_b and for the DC/AC stage inductors L_m. On the contrary, 1/3 PWM generates the lowest overall current ripple and hence the lowest inductor losses. The 2/3 PWM current ripple performance lies in between the values achieved for 1/3 PWM and 3/3 PWM.

Finally, the experimentally measured RMS inductor current ripple is compared against the theoretically calculated values of Fig. 8. The results are shown in Fig. 15(a) and (b) for the DC/DC and DC/AC stage, respectively. An excellent matching between the theoretical analysis and the experimental measurements is verified.

V. Conclusions

As shown in this paper, 1/3 PWM can be applied to three-phase DC/AC converter systems which feature a separate DC/DC and DC/AC stage and are designed to cope with a wide input-output voltage variation. 1/3 PWM utilizes a variable DC link voltage instead of a constant DC link voltage used in conventional PWM modulation schemes. Thereby, it is possible to generate three-phase sinusoidal line-to-line output voltages by switching always only one out of the three DC/AC stage half-bridges. A main advantage of the 1/3 PWM modulation is that it can be easily retrofitted to existing three-phase converter systems by means of a firmware update. In order to quantify the performance advantage of 1/3 PWM, the semiconductor switching losses are analytically calculated and the remaining converter component stresses are comprehensively analysed. It is deduced that 1/3 PWM reduces the switching losses of the DC/AC stage by more than 66% compared to the conventional 3/3 PWM modulation strategy. The 1/3 PWM also outperforms the more advanced 2/3 PWM by reducing the switching losses of the latter by at least a factor of two. Besides the lower switching losses, 1/3 PWM exhibits similar if not slightly lower current and/or voltage stresses on the remaining converter components compared to the 2/3 PWM modulation strategy. Therefore, 1/3 PWM is a promising modulation technique with substantial advantages over state-of-the-art approaches. Finally, a hardware demonstrator is assembled and tested. There, the uncomplicated operation of 1/3 PWM is experimentally validated. Furthermore, 3/3 PWM, 2/3 PWM and 1/3 PWM are applied to the same hardware demonstrator and the corresponding losses are measured over a wide power

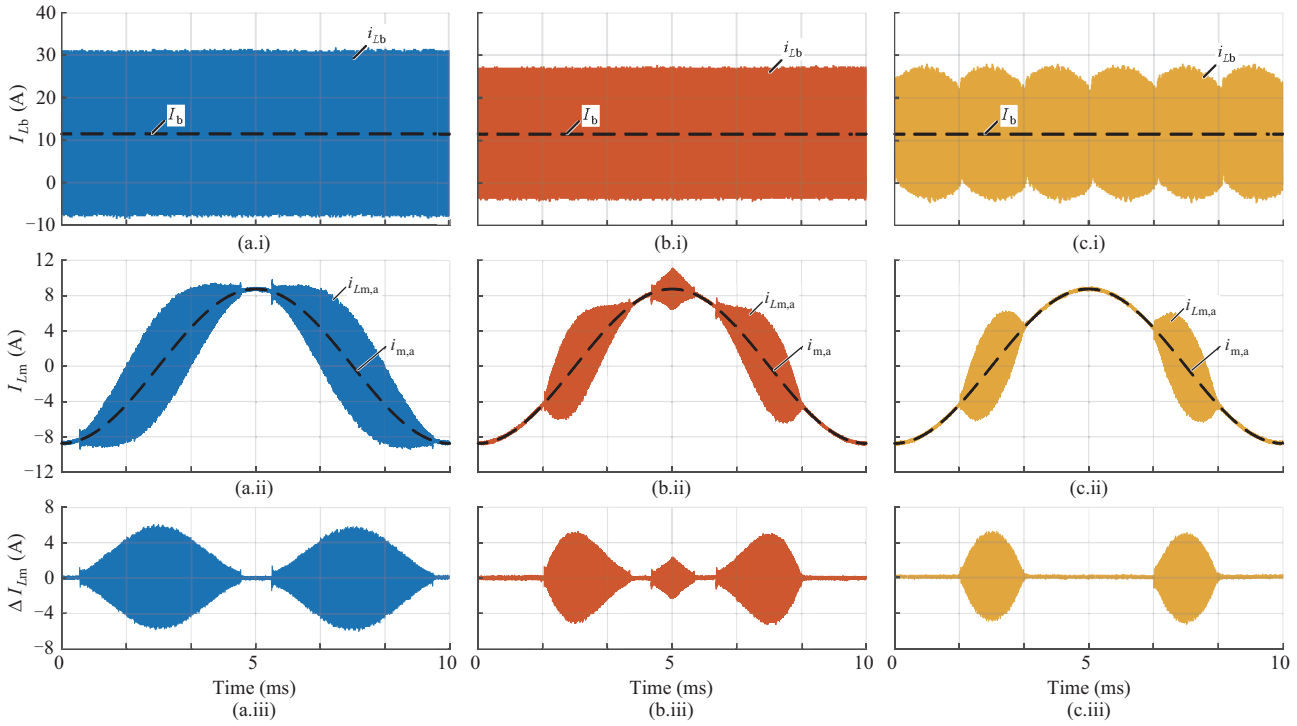

Fig. 14. Inductor currents for different modulation strategies measured using the hardware demonstrator of Fig. 10 for a modulation index of $M = 1.75$ ($P = 460$ W) and a fundamental frequency of $f_m = 100$ Hz. (i) The DC/DC stage inductor L_b current is shown. (ii) The current in an output filter inductor of the DC/AC stage L_m is plotted. (iii) The respective DC/AC stage inductor current ripple is illustrated. (a), (b) and (c) refer to the 3/3 PWM, 2/3 PWM and 1/3 PWM, respectively.

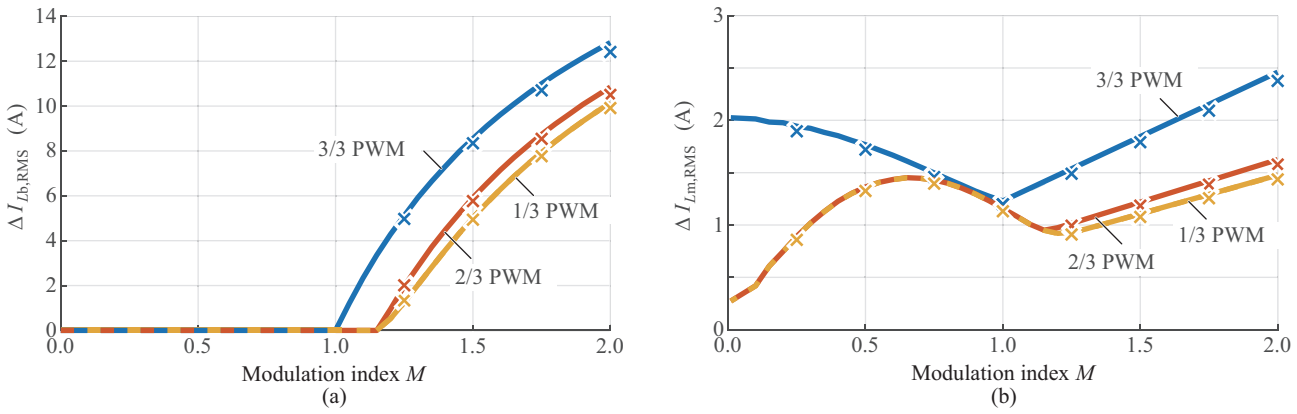

Fig. 15. Theoretically calculated inductor RMS current ripple (continuous lines) compared against experimental measurements (x marks). (a) Corresponds to the DC/DC stage while (b) refers to the DC/AC stage.

range. A 2% increase of efficiency, i.e., a loss reduction of 50% is measured for the 1/3 PWM compared to 3/3 PWM for the considered application.

Appendix A: Component Stresses for cos (φ) < 1

The impact of a low load PF on the overall design of the two-stage converter system is discussed. A converter system that can operate under any load voltage-current phase shift φ is desirable in this case study. Therefore, the stresses on the different system components are now analysed for a PF cos (φ) < 1. In particular, the load current is assumed to either lead or lag the load voltage by a phase shift angle $\varphi = -90°...90°$ (i.e., capacitive or inductive load behaviour). Accordingly, the transferred apparent power $S = 0...500$ W, active power P, battery current I_b and load fundamental phase current amplitude $\hat{I}_m$ can be derived as a function of the modulation index M and PF cos (φ) as

$$S = M^2 \frac{3U_b^2}{8R}, \quad P = M^2 \frac{3U_b^2}{8R}\cos(\varphi),$$
$$I_b = M^2 \frac{3U_b}{8R}\cos(\varphi), \quad \hat{I}_m = M\frac{U_b}{2R}, \tag{47}$$

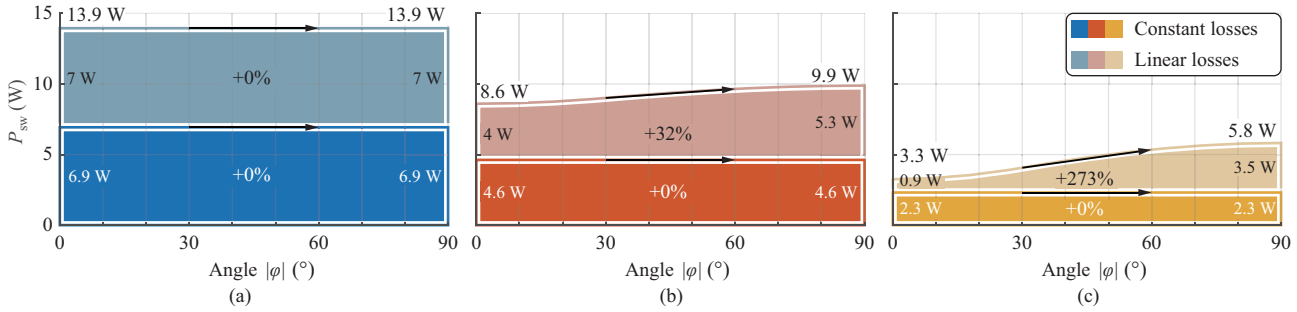

Fig. 16. Switching losses of the DC/AC stage as a function of the voltage-current phase shift φ of the load and the modulation scheme. (a) 3/3 PWM. (b) 2/3 PWM. (c) 1/3 PWM. There, the worst case operating point with the maximum motor voltage ($M = 2$ for the case at hand) is considered, while numerical values are derived for the worst case operating conditions of Table I and the parameters of Table VI.

where $R = 3\hat{U}_{m,max}/2S_{max} = 4.8\ \Omega$.

The switching losses of the DC/DC stage can directly be derived by substituting I_b from (47) in (15). Since the battery current I_b decreases as the PF reduces, the DC/DC stage switching losses also decrease. The switching losses of the DC/AC stage for 3/3 PWM are independent from the PF and are therefore given by using (16). On the other hand, the switching losses of the DC/AC stage for 2/3 PWM and 1/3 PWM depend on the PF and hence the phase shift φ has to be considered in the derivation of the local switching losses (12) of the DC/AC stage as

$$p_{sw}(\theta) = f_{s,m}\left[k_0 + k_1 \hat{I}_m \left|\cos(\theta - \varphi)\right|\right]. \quad (48)$$

By averaging $p_{sw}(\theta)$ over a 2π wide fundamental period the global average switching losses can be derived. For 2/3 PWM, the switching losses are calculated as

$$P_{sw}\big|_{2/3\ PWM} = \frac{3}{2\pi}\left[\int_0^{\frac{2\pi}{3}} p_{sw}(\theta)\mathrm{d}\theta + \int_{\frac{4\pi}{3}}^{2\pi} p_{sw}(\theta)\mathrm{d}\theta\right], \quad (49)$$

for a voltage-current phase shift of $|\varphi| \leqslant 30°$ results in

$$P_{sw}\big|_{2/3\ PWM} = 3f_{s,m}\left[\frac{2}{3}k_0 + \left(1 - \frac{\sqrt{3}\cos|\varphi|}{4}\right)k_1\frac{2}{\pi}\hat{I}_m\right], \quad (50)$$

and for $|\varphi| > 30°$ gives

$$P_{sw}\big|_{2/3\ PWM} = 3f_{s,m}\left[\frac{2}{3}k_0 + \left(\frac{1}{2} + \frac{\sin|\varphi|}{4}\right)k_1\frac{2}{\pi}\hat{I}_m\right]. \quad (51)$$

The same procedure can be applied to calculate the DC/AC stage switching losses for 1/3 PWM where

$$P_{sw}\big|_{1/3\ PWM} = \frac{3}{2\pi}\left[\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} p_{sw}(\theta)\mathrm{d}\theta + \int_{\frac{4\pi}{3}}^{\frac{5\pi}{3}} p_{sw}(\theta)\mathrm{d}\theta\right], \quad (52)$$

for a voltage-current phase shift of $|\varphi| \leqslant 30°$ results in

$$P_{sw}\big|_{1/3\ PWM} = 3f_{s,m}\left[\frac{1}{3}k_0 + \left(1 - \frac{\sqrt{3}\cos|\varphi|}{2}\right)k_1\frac{2}{\pi}\hat{I}_m\right], \quad (53)$$

while for $|\varphi| > 30°$ gives

$$P_{sw}\big|_{1/3\ PWM} = 3f_{s,m}\left(\frac{1}{3}k_0 + \frac{\sin|\varphi|}{2}k_1\frac{2}{\pi}\hat{I}_m\right). \quad (54)$$

In Fig. 16, the switching losses for all modulation schemes depending on the phase shift φ of the load are plotted. Compared to the load independent losses obtained with 3/3 PWM, the losses for 2/3 PWM and 1/3 PWM slightly increase with increasing phase shift, since in the middle phase a higher current has to be switched than with $\cos(\varphi) = 1$. It is noted, that the switching losses are symmetric with respect to φ, i.e., the losses for a voltage-current phase shift $+\varphi$ are equal to the respective losses for $-\varphi$. It can be deduced from Fig. 16, that although the switching losses for 2/3 PWM and 1/3 PWM increase as the PF reduces, both still generate by far lower overall switching losses compared to 3/3 PWM.

For a complete converter system design, the stresses on the remaining components must be considered. The total conduction losses of the converter system can still be calculated from (19) over the whole PF range, where the battery current I_b is substituted from (47). Similarly, the mathematical formulas which describe the current stresses on the semiconductor devices of the DC/DC stage (20)–(25) and DC/AC stage (28)–(32) are still valid. The DC/DC stage semiconductor devices must hence be designed for the worst case operating conditions with the maximum load voltage ($M = 2$) and unity PF ($\varphi = 0°$), independent of the modulation strategy. For these operating conditions, the maximum switching losses and conduction losses appear simultaneously on the DC/DC stage semiconductors, since I_b is maximum (47). The same worst case operating conditions apply for the DC/AC stage semiconductor devices, if they are designed for 3/3 PWM operation. However, if the DC/AC stage semiconductor devices are designed for 2/3 PWM or 1/3 PWM the worst case operating conditions appear for the maximum load voltage but zero PF ($|\varphi| = 90°$). For these operating conditions, the maximum

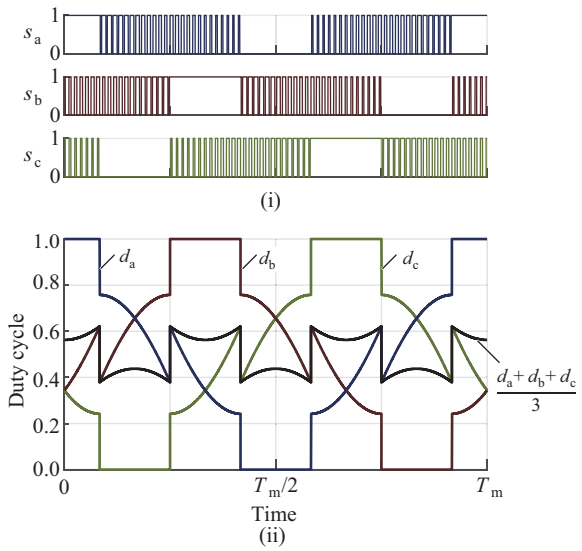

Fig. 17. Alternative 2/3 PWM strategy with positive & negative (p & n) clamping. (i) Gate signals and (ii) duty cycles of the DC/AC stage.

switching losses (cf., Fig. 16) and conduction losses (maximum load current $\hat{I}_m$) appear simultaneously on the DC/AC stage semiconductors. Finally, the proposed inductor values L_b for the DC/DC stage and L_m for the DC/AC stage ((36)–(37) and (39)–(40), respectively), as well as the recommended DC link capacitor value C_{DC} ((42) and (43)), are applicable for $\cos(\varphi) < 1$.

Appendix B: Alternative 1/3 PWM Scheme

The total duty cycle is the sum of both duty cycle components (7). This paper focuses on a negative clamping 2/3 PWM algorithm (5)–(7), which is accordingly extended for 1/3 PWM. However, an alternative positive & negative (p & n) clamping 2/3 PWM scheme [7] could be used, i.e., at any given moment one of the high-side or low-side switches of the DC/AC stage is permanently turned-on and clamps the corresponding phase to the positive or the negative DC rail, respectively. Typical duty cycles and gate signals for such 2/3 PWM scheme are depicted in Fig. 17. The p & n clamping 2/3 PWM duty cycle calculation algorithm is similar to the respective calculations for the negative clamping 2/3 PWM scheme. Namely, the DC/AC stage duty cycles are split into a DM and a CM part. The DM part is purely sinusoidal and is given by (5), while the CM part is

$$d_{CM} = 0.5 + \left[0.5 - \max\left\{\left|d_{a,DM}\right|, \left|d_{b,DM}\right|, \left|d_{c,DM}\right|\right\}\right] \cdot \operatorname{sign}\left[\max\left\{d_{a,DM}, d_{b,DM}, d_{c,DM}\right\} - \left|\min\left\{d_{a,DM}, d_{b,DM}, d_{c,DM}\right\}\right|\right]. \quad (55)$$

The main advantage of p & n clamping 2/3 PWM is that it ensures equal current distributions between the high-side and the low-side semiconductor devices of the DC/AC stage, in contrast to negative clamping 2/3 PWM which suffers from an asymmetric current stress for low modulation indexes (29). Namely, the RMS current of the DC/AC stage devices in case of p & n clamping 2/3 PWM is

$$I_{Tma1,RMS}\big|_{2/3\ PWM} = I_{Tma2,RMS}\big|_{2/3\ PWM} = \frac{\hat{I}_m}{\sqrt{2}}\frac{1}{\sqrt{2}}. \quad (56)$$

Thereby, the drive system can always conduct the nominal motor current amplitude $\hat{I}_m$ without overstressing the low-side switches $T_{m\{a,b,c\}2}$ and hence ensures nominal motor torque during motor acceleration, starting from standstill.

The disadvantage of the p & n clamping 2/3 PWM is that the discontinuous duty cycles (cf., Fig. 17) lead to abrupt CM voltage steps at the inverter output. Such CM voltage steps can excite the DC link referenced output filter of Fig. 1(a) and hence p & n clamping 2/3 PWM is not suitable for the application at hand.

References

[1] T. M. Jahns and H. Dai, "The past, present, and future of power electronics integration technology in motor drives," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 197–216, Sep. 2017.

[2] A. Stippich, C. H. Van Der Broeck, A. Sewergin, A. H. Wienhausen, M. Neubert, P. Schülting, S. Taraborrelli, H. V. Hoek, and R. W. De Doncker, "Key components of modular propulsion systems for next generation electric vehicles," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 249–258, Dec. 2017.

[3] P. Hertzke, N. Muller, S. Schenk, and T. Wu, "The global electric vehicle market is amped up and on the rise," [Online]. Available: https://autoassembly. mckinsey. com/article/the-global-electric-vehicle-market-is-amped-up-and-on-the-rise.

[4] K. A. Kim, Y. Liu, M. Chen, and H. Chiu, "Opening the box: Survey of high power density inverter techniques from the little box challenge," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 131–139, Dec. 2017.

[5] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a pwm converter system," in *IEEE Transactions on Industry Applications*, vol. 27, no. 6, pp. 1063–1075, Nov.-Dec. 1991.

[6] A. M. Hava, S. Sul, R. J. Kerkman, and T. A. Lipo, "Dynamic overmodulation characteristics of triangle intersection PWM methods," in *IEEE Transactions on Industry Applications*, vol. 35, no. 4, pp. 896–907, Jul.-Aug. 1999.

[7] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," in *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[8] F. Liu, K. Xin, and Y. Liu, "An adaptive discontinuous pulse width modulation (DPWM) method for three phase inverter," in *Proceedings of IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 1467–1472..

[9] C. Charumit and V. Kinnares, "Discontinuous SVPWM techniques of three-leg VSI-fed balanced two-phase loads for reduced switching losses and current ripple," in *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2191–2204, Apr. 2015.

[10] F. Antunes and A. M. Torres, "A three-phase grid-connected PV system," in *Proceedings of 26th Annual Conference of the IEEE Industrial Electronics Society (IECON). IECON 2000. 2000 IEEE International Conference on Industrial Electronics, Control and Instrumentation. 21st Century Technologies*, Nagoya, Japan, 2000, pp. 723–728, vol.1.

[11] P. Luerkens, M. Wendt, T. Duerbaum, and H. V. D. Broeck, "3-phase solar converter circuit and method," U.S. Patent 7 539 029 B2, 2005.

[12] K. Rigbers, S. Schroder, R. W. de Doncker, P. Lurkens, M. Wendt, and U. Boke, "High-efficient soft-switching converter for three-phase grid connections of renewable energy systems," in *Proceedings of 2005 International Conference on Power Electronics and Drives Systems*, Kuala Lumpur, Malaysia, 2005, pp. 246–250.

[13] K. Rigbers, S. Thomas, U. Boke, and R. W. De Doncker, "Behavior and

loss modeling of a three-phase resonant pole inverter operating with 120° double flattop modulation," in *Proceedings of the Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, Tampa, FL, USA, 2006, pp. 1694–1701.

[14] Q. Lei and F. Z. Peng, "Space vector pulsewidth amplitude modulation for a buck–boost voltage/current source inverter," in *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 266–274, Jan. 2014.

[15] D. Menzi, D. Bortis, and J. W. Kolar, "Three-phase two-phase-clamped boost-buck unity power factor rectifier employing novel variable dc link voltage input current control," in *Proceedings of 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen, 2018, pp. 1–8.

[16] H. Fujita, "A three-phase voltage-source solar power conditioner using a single-phase PWM control method," in *Proceedings of 2009 IEEE Energy Conversion Congress and Exposition (ECCE-USA)*, San Jose, CA, 2009, pp. 3748–3754.

[17] J. Shen, K. Rigbers, C. P. Dick, and R. W. De Doncker, "A dynamic boost converter input stage for a double 120° flattop modulation based three-phase inverter," in *Proceedings of 2008 IEEE Industry Applications Society Annual Meeting (IAS)*, Edmonton, AB, 2008, pp. 1–7.

[18] T. B. Soeiro and P. Bauer, "Fast DC-type electric vehicle charger based on a quasi-direct Boost-Buck rectifier," in *Proceedings of 2019 AEIT International Conference of Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE)*, Torino, Italy, 2019, pp. 1–6.

[19] M. Antivachis, D. Bortis, A. Avila, and J. W. Kolar, "New optimal common-mode modulation for three-phase inverters with DC-link referenced output filter," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 4, pp. 331–340, Dec. 2017.

[20] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis [three-phase inverters]," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 1, pp. 186–196, Feb. 2002.

[21] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[22] G. Deboy, O. Haeberlen, and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 89–100, Aug. 2017.

[23] M. Guacci, J. A. Anderson, K. L. Pally, D. Bortis, J. W. Kolar, M. J. Kasper, J. Sanchez, and G. Deboy, "Experimental characterization of silicon and gallium nitride 200 V power semiconductors for modular/multi-level converters using advanced measurement techniques," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

[24] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight optimization of a cooling system composed of fan and extruded-fin heat sink," in *IEEE Transactions on Industry Applications*, vol. 51, no. 1, pp. 509–520, Jan. -Feb. 2015.

[25] P. Papamanolis, F. Krismer, and J. W. Kolar, "Minimum loss operation of high-frequency inductors," in *Proceedings of 2008 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 1756–1763.

[26] M. Antivachis, D. Bortis, D. Menzi, and J. W. Kolar, "Comparative evaluation of Y-inverter against three-phase two-stage buck-boost DC-AC converter systems," in *Proceedings of 2008 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, Niigata, 2018, pp. 181–189.

[27] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," in *IEE Proceedings - Electric Power Applications*, vol. 153, no. 4, pp. 535–543, Jul. 2006.

[28] S. Schroth, D. Bortis, and J. W. Kolar, "Impact of stator grounding in low power single-phase EC-motors," in *Proceedings of 2014 IEEE Applied Power Electronics Conference and Exposition (APEC 2014)*, Fort Worth, TX, 2014, pp. 783–790.

[29] D. Rendusara and P. Enjeti, "New inverter output filter configuration reduces common mode and differential mode dv/d*t* at the motor terminals in PWM drive systems," in *Proceedings of PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference. Formerly Power Conditioning Specialists Conference 1970-71. Power Processing and Electronic Specialists Conference 1972*. Saint Louis, MO, USA, 1997, pp. 1269–1275, vol.2.

[30] D. A. Rendusara and P. N. Enjeti, "An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in PWM drive systems," in *IEEE Transactions on Power Electronics*, vol. 13, no. 6, pp. 1135–1143, Nov. 1998.

[31] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved triangular current mode (TCM) resonant transition, single phase PFC rectifier with high efficiency and high power density," in *Proceedings of the 2010 International Power Electronics Conference (ECCE ASIA)*, Sapporo, 2010, pp. 1725–1732.

[32] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," in *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

[33] M. Kaufmann, A. Tüysüz, and J. W. Kolar, "New optimum modulation of three-phase ZVS triangular current mode GaN inverter ensuring limited switching frequency variation," in *Proceedings of 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, Glasgow, 2016, pp. 1–6.

Michael Antivachis received the B.Sc. degree in electrical engineering from the National Technical University of Athens (NTUA) in 2014 and the M.Sc. degree in energy science and technology from the Swiss Federal Institute of Technology (ETH) in 2016. Since June 2016 he is with the Power Electronic Systems Laboratory (PES) of ETH Zurich as a Ph.D. candidate. His research interests include high-speed motor drives for commercial applications, highly compact inverter systems which enable inverter-motor integration in the same housing and low EMI emission profile inverters.

Jon Azurza Anderson received the B.Sc. degree in industrial technology engineering from TECNUN School of Engineering of the University of Navarra in 2014, and the M.Sc. degree in electrical engineering from ETH Zurich (with distinction) in 2016, specializing in energy and power electronics. In 2013 and 2014 he worked for Fraunhofer IIS in Nuremberg, Germany, developing software in the RFID & Radio Systems group. In November 2016 he joined the Power Electronics Systems Laboratory (PES) of ETH Zurich as a scientific assistant, where in February 2017 he began his Ph.D. studies, focusing on ultra-high efficiency three-phase multi-level PWM converters.

Dominik Bortis received the M.Sc. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Postdoctoral Fellow and from 2011 to 2016 a Research Associate with PES, co-supervising Ph.D. students and leading industry research projects. Since January 2016 Dr. Bortis is heading the research group Advanced Mechatronic Systems at PES, which concentrates on ultra-high speed motors, magnetic bearings and bearingless drives, new linear-rotary actuator and machine concepts with integrated power electronics. In this context, multi-objective optimizations concerning weight/volume/efficiency/costs, the analysis of in-teractions of power electronics and electric machines, and EMI are given special attention. Targeted applications include advanced industry automation and manufacturing, e.g., highly dynamic and precise positioning systems, medical and pharmaceutical systems, e.g., ultra-high purity and blood pumps, and future mobility concepts, including motors and actuators for hybrid and electric vehicles, more electric aircraft and satellites. Dr. Bortis has published more than 90 scientific papers in international journals and conference proceedings. He has filed 32 patents and has received 6 IEEE Conference Prize Paper Awards.

Johann Walter Kolar received the M.Sc. and Ph.D. degrees (summa cum laude/promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria, in 1997 and 1999, respectively. Since 1984, he has been working as an independent researcher and international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drive systems. He has proposed numerous novel PWM converter topologies, modulation and control concepts and has supervised 70+ Ph.D. students. He has published 880+ scientific papers in international journals and conference proceedings, 4 book chapters, and has filed 190+ patents. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultra-high speed and bearingless motors. Dr. Kolar has received 28 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award and two ETH Zurich Golden Owl Awards for excellence in teaching. He initiated and/or is the founder of four ETH Spin-off companies. He is a member of the steering committees of several leading international conferences in the field and has served from 2001 through 2013 as an Associate Editor of the *IEEE Transactions on Power Electronics*. Since 2002 he also is an Associate Editor of the *Journal of Power Electronics of the Korean Institute of Power Electronics* and a member of the Editorial Advisory Board of the *IEEJ Transactions on Electrical and Electronic Engineering*.