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Classification and Comparative Evaluation of PV Panel Integrated DC-DC Converter Concepts

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Classification and Comparative Evaluation of PV Panel Integrated DC-DC Converter Concepts

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***Abstract*—Strings of photovoltaic panels have a significantly reduced power output when mismatch between the panels, such as partial shading, occurs since integrated diodes are then partly bypassing the shaded panels. With the implementation of DC-DC converters on panel level, the maximum available power can be extracted from each panel regardless of any shading. In this paper, different concepts of PV panel integrated DC-DC converters are presented, comparative evaluation is given and the converter design process is shown for the buck-boost converter which is identified as the best suited concept. Furthermore, the results of high precision efficiency measurements of an experimental prototype are presented and compared to a commercial MIC.**

***Index Terms*—Panel integrated DC-DC converters, Pareto front, prototype.**

I. Introduction

In state of the art photovoltaic (PV) energy systems, the PV-panels are connected in series so that the output voltages of the panels add up to generate the desired bus voltage which is necessary in order to feed power into the grid with an inverter. Each PV panel has one or more integrated bypass diodes depending on the number of substrings in a panel. In case no panel in a string is shaded, the whole string of panels has only one maximum power point (MPP) and all panels contribute to the total power of the string (**Fig. 1(a)**). In contrast, if one or more panels are shaded, the string will show multiple MPPs as (cf. **Fig. 1(b)**). None of those MPPs will deliver the total power $P_{\text{tot,th}}$ that theoretically could be harvested which would be the sum of the individual MPPs of each panel,

$$P_{\text{tot,th}} = n_{\text{sh}} \cdot P_{\text{PV,sh}} + (n_{\text{tot}} - n_{\text{sh}}) \cdot P_{\text{PV,unsh}} \qquad (1)$$

with n_{sh} and n_{tot} being the number of shaded panels respectively the total number of panels and $P_{\text{PV,th}}$ and $P_{\text{PV,unsh}}$ the maximum power point of shaded resp. unshaded panels, assuming that the shaded panels are uniformly shaded.
By drawing the MPP current of the unshaded panels, which is higher than the maximum current of the shaded panels, the shaded panels are shorted out by the bypass diodes and their power is lost. The other option is drawing the MPP current of the shaded panels which would allow every panel to feed power into the string. However, then the unshaded panels would not be operating in their MPP and thus also power would be lost. In addition, the occurrence of multiple MPPs poses a challenge for any MPP tracking device connected to the string, which is usually the central inverter for multiple strings or a string converter for each string of PV panels. The above mentioned problem is not only caused by shading of panels but also by other factors of mismatch between the panels e.g. different orientation, aging of panels, different panel manufactures, debris, dust etc.
Those causes of power loss can be eliminated by applying DC-DC converters on panel level, thus allowing to track the MPP of each panel without bypassing any panel. Hence with those module integrated converters (MIC) the theoretically available power $P_{\text{tot,th}}$ of the string can be extracted.

In this work, a classification of possible DC-DC converter topologies for PV panel integration is introduced. Furthermore, the two most promising concepts for series connected PV panels are selected for a comparative evaluation and the best suited concept is fully dimensioned and finally verified by

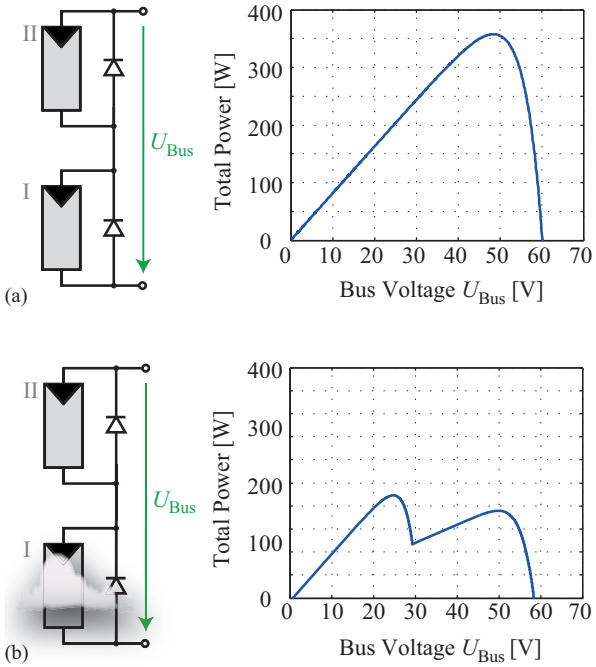

Fig. 1: Impact of shading on a simplified string of two PV panels: (a) Output power of a PV string with only unshaded panels and (b) with one shaded panel (plotted vs. the bus voltage U_{Bus}).

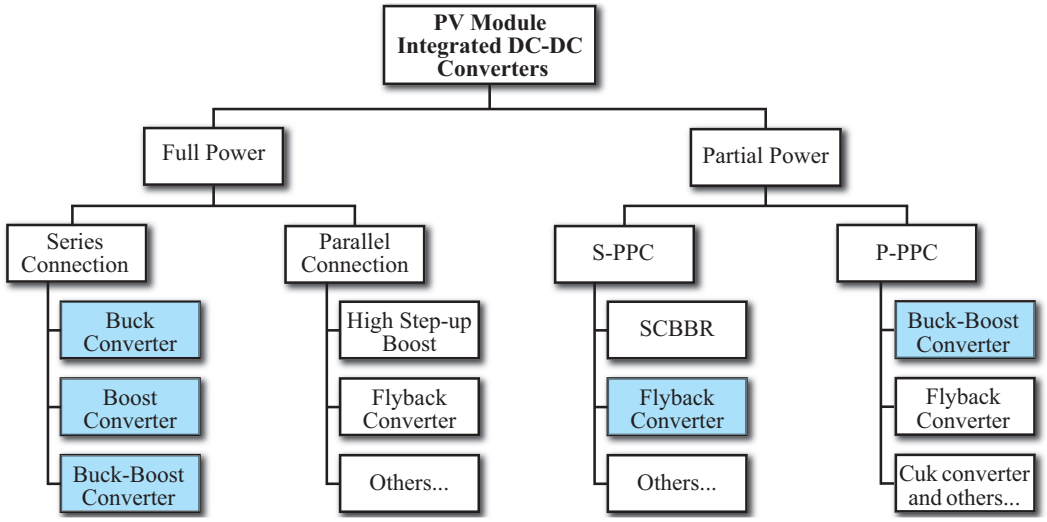

Fig. 2: Classification of PV module integrated DC-DC converters. Converter categories highlighted in blue are examined in this paper.

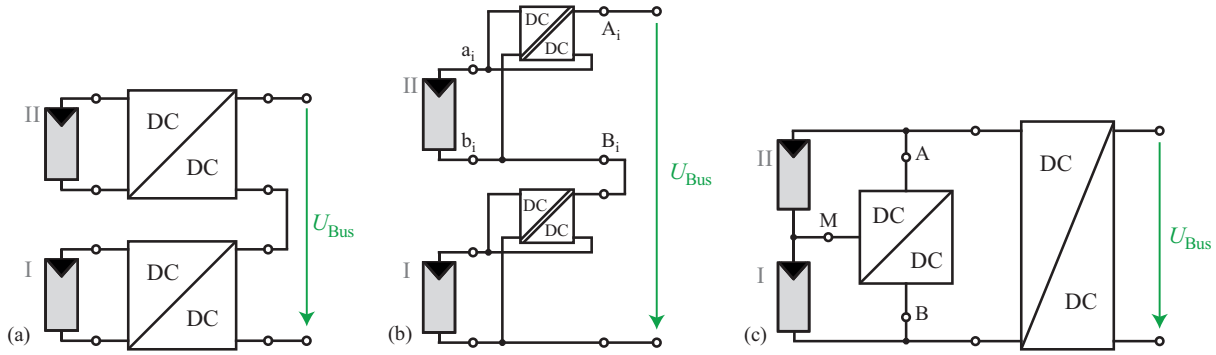

Fig. 3: Possible DC-DC converter topologies for string series connection: (a) Full power converters, (b) series connected partial power converters (S-PPC) and (c) parallel connected partial power converter (P-PPC).

measurements on a prototype.

An overview of the converter configurations for DC-DC converters on panel level can be divided into two categories: (1) Full power converters [1] with subcategories for series and parallel connected PV panels and (2) partial power converters, again with subcategories for Series connected Partial Power Converters (S-PPC) and Parallel connected Partial Power Converters (P-PPC), as shown in **Fig. 2**. Other terms for the P-PPC concept are ”energy shuffler” or ”current diverter”.

II. Evaluation of Converter Topologies

Since in nowadays PV installations the PV panels are connected in series, only those topologies will be regarded in this paper, that still allow for series connection of PV panels, as shown in **Fig. 3**. In future work the concept of parallel connection will be examined.

A. Full power converters

For full power conversion (**Fig. 3(a)**) either buck, boost or buck-boost converters can be used (**Fig. 4**). When shading of a panel occurs, the current of the shaded panel has to be matched to the string current since all panels are connected in series. A buck converter (**Fig. 4(a)**) thereby increases the current of the shaded panel (red curve) until it matches the MPP current of the unshaded panels (blue curves) and thus lowers its output voltage. With a boost converter (**Fig. 4(b)**) the current of the unshaded panels is decreased until it matches the MPP current of the shaded panels and thus increases its output voltage. The greatest flexibility is given with a buck-boost converter (**Fig. 4(c)**) where any given current value can be matched by the converters.

These three different concepts have also different implications on the number of PV panels per string which are required in order to still reach a bus voltage U_{Bus} of $400\,\mathrm{V}$. In a string where all panels are equipped with buck converters, the string voltage may drop below $400\,\mathrm{V}$ if panels get shaded, since the adaption to the string current is achieved by lowering the voltage of shaded panels. Thus a minimum number of panels per string is required. The upper limit of PV panels with buck converter in a string depends on the maximum output current rating of the converters.

For boost converters, the problem occurs vice versa, i.e. the

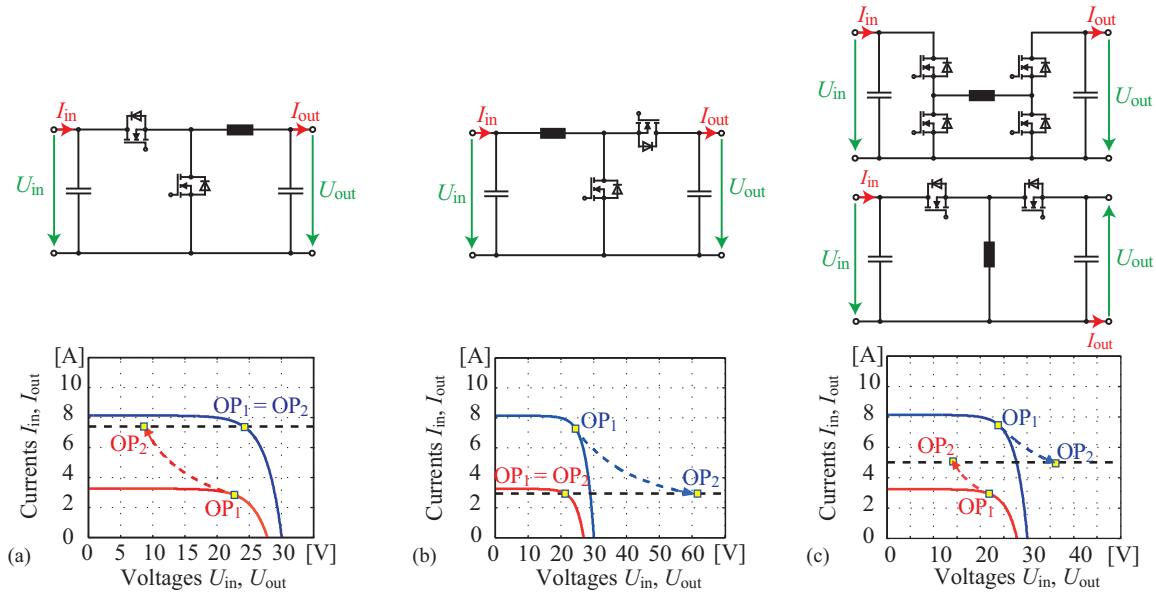

Fig. 4: Working principles of full power converters in series connection of shaded (red) and unshaded (blue) panels: (a) Buck converter, (b) boost converter and (c) buck-boost converter. OP_1: Converter input (U_{in}, I_{in}) related to MPP of a PV panel. OP_2: Operating point characterizing the converter output (U_{out}, I_{out}).

string voltage is prone to exceed the level of 400 V during shading since unshaded panels increase their output voltage to reach the current level of shaded panels. This leads to a maximum number of PV panels per string. The lower limit of PV panels with boost converters in each string depends on the maximum output voltage rating of the converters.

With the buck-boost converters the bus voltage can be kept constant since any current level can be set. Thus the upper limit of PV panels per string for the buck-boost converter concept depends on the maximum output current rating and the lower limit depends on the maximum output voltage rating of the buck-boost converters.

In **Tab. I** the maximum and minimum numbers of PV panels per string are calculated for the three different full power converters under the assumption that all panels should be able to feed power in the string under a given shading intensity Δ i.e. $\frac{P_{PV,unsh}}{P_{PV,sh}}$. An example of those limitations is given in **Fig. 5**.

For this example the number of panels per PV string when only boost converters are used has to be in the range of 6 to 11. If all PV panels are equipped with buck converters only, the number of panels has to be between 25 and 32. So, if only one or the other converter type is chosen, there is no possibility to have between 12 and 24 PV panels in the string. However, with a combination of buck and boost converters, any number of PV panel between 6 and 32 can be connected in series.

Thus, based on the limitations that both buck and boost converter topologies imply on the number of panels in a PV string, the buck-boost concept is chosen for further consideration. Since MICs in general target residential applications

TABLE I: Maximum resp. minimum number of PV panels per string for different MIC topologies where $I_{out,max}$ denotes the maximum output current of the converter, U_{MPP} the PV panel voltage in a typical MPP, Δ the fraction $\frac{P_{PV,unsh}}{P_{PV,sh}}$ and $P_{PV,max}$ the maximum output power of the PV panel.

Type	Maximum nr. of panels	Minimum nr. of panels
Buck	$\frac{U_{Bus}}{P_{PV,max}} I_{out,max}$	$\left(\frac{U_{Bus}}{U_{MPP}}\right) \Delta + 1$
Boost	$\frac{U_{Bus}+(\Delta-1)U_{MPP}}{\Delta \cdot U_{MPP}}$	$\left(\frac{U_{Bus}}{U_{out,max}} - 1\right) \Delta + 1$
Buck-boost	$\frac{U_{Bus}}{P_{PV,max}} I_{out,max}$	$\left(\frac{U_{Bus}}{U_{out,max}} - 1\right) \Delta + 1$

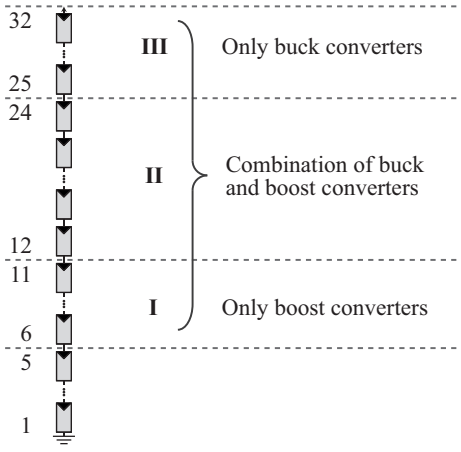

Fig. 5: Example of maximum and minimum number of PV panels per string when either only buck converters (**III**) or only boost converters (**I**) are used. The combination of buck and boost converters combines those two regions and extends it to the previously unreachable area **II**. (Numbers used for this example: $U_{Bus} = 400\,V$, $U_{MPP} = 25\,V$, $P_{PV} = 250\,W$, $\Delta = 1.5$, $I_{out,max} = 20\,A$, $U_{out,max} = 100\,V$.)

which are more prone to shading than industrial applications, the flexibility provided by buck-boost converters is not only advantageous for the design of a PV system regarding shading but also allows to fully utilize the available space on a rooftop by setting up multiple PV string with different lengths.

B. Partial power converters

With series connected partial power converters (S-PPC) (**Fig. 6(b)**) the output voltage of the converter is added (boost operation) to or subtracted (buck operation) from the solar panel output. One concept with boost functionality which is based on a bidirectional flyback converter is shown in (**Fig. 6(a)**). Another concept which allows buck and boost operation is described in [2].

The S-PPC has the same functionality (i.e. buck and/or boost operation) as the series connected full power converter and is advantageous when only a slight adjustment of the output voltage is required since then the components in a S-PPC can be smaller in size and value than in the full power converter. The total efficiency η_{tot} of the conversion of the panel current to the string current depends only to a limited extent on the efficiency of the converter η_{conv} itself [12]. The ratio of the power which is processed by the converter P_c and the total panel power P_{PV} determines the influence of the converter efficiency on the total efficiency. The less power is processed by the partial power converter the higher is the system efficiency, as reflected in following equation

$$\eta_{\text{tot}} = 1 - \frac{P_{\text{c}}}{P_{\text{PV}}}(1 - \eta_{\text{conv}}). \tag{2}$$

In the ideal case, converters are not working and thus theoretically 100% efficiency can be achieved (neglecting conduction losses). Furthermore, since a partial power converter is usually only processing some share of the full panel power, the efficiency can be optimized on partial load operation.

However, calculations have shown that an output to input voltage boost ratio capability of 4:1 for any full or partial power buck-boost converter as module integrated DC-DC converter is required to operate all panels in their MPP and to feed power of all panels into the string at any shading condition with a constant bus voltage U_{Bus}. This is due to fact that a shaded panel is still receiving a fraction of the

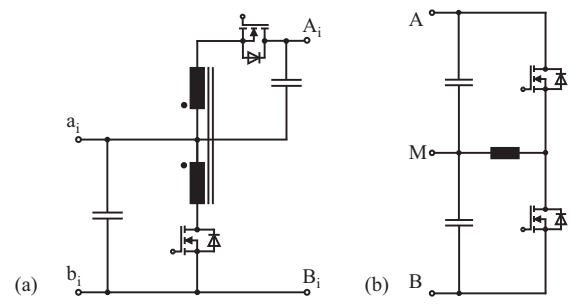

Fig. 6: Partial power concepts: (a) S-PPC based on a bidirectional flyback converter (snubber not shown) and (b) P-PPC based on a bidirectional buck-boost converter.

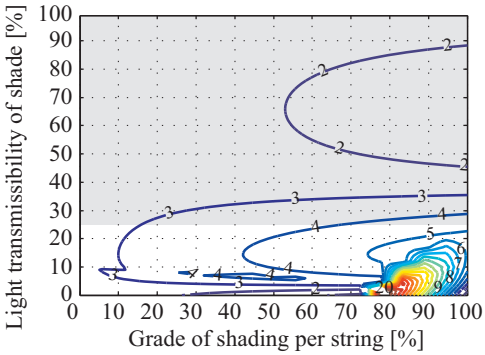

Fig. 7: Power loss for buck-boost full power converters with a maximum voltage conversion ratio of 4:1. The contour lines characterize the amount of power which cannot be harvested (in percent of nominal system power). The gray shaded area shows possible shading scenarios when only the direct irradiation component of the light is blocked.

light (i.e. diffuse irradiance and reflected irradiance) which is at least one quarter to one third of the global irradiance. The possible shading scenarios are shown by the gray shaded area in **Fig. 7**. This plot shows how much power in percent of the nominal system power is lost in a given shading scenario. For example, if 40% of the panels in string are shaded and receive only half of the irradiation of unshaded panels (i.e. "Light transmissibility of the cloud" = 50%), between 2-3% of the nominal system power is lost. Any power losses which are outside of the gray area have no relevance in practice. For the partial power converter, the voltage ratio of 4:1 would require that 3/4 of the panel power is processed by the partial power converter, thereby requiring similar sized components (switches, inductor, capacitor ratings etc.) as the full power converter and overriding any benefits of the partial power concept. Since the partial power concept requires an electrical isolation the disadvantages overweigh the advantages and the concept is unsuitable for the application as module integrated DC-DC converter and will not be considered in this paper any further.

The P-PPC concept (**Fig. 3(c)**) is well known from battery management systems where the currents of the battery cells are equalized [4]. With such a technique the share of string current which is greater than the MPP current of a panel is bypassed around the shaded panel and all panels can operate in their MPP despite of different MPP currents. For this concept the buck-boost topology (**Fig. 6(b)**) as well as other topologies ([4]-[6]) can be used. Again, like with all partial power converters, the efficiency of the converter is only influencing the total efficiency by the share of power that is processed by the converter in comparison to the total system power. However, opposed to the full power converters or the S-PPC, this concept cannot adjust the voltage of the string to a desired value and requires an additional DC-DC converter stage for this adaption. This additional adjustment of the bus voltage is beneficial for the overall system efficiency since the grid

inverters have a peak efficiency at a certain DC-bus voltage [3]. However, said additional DC-DC converter has also losses and typically a peak efficiency of 98%. So the overall efficiency is a multiplication of the P-PPC converter efficiency and the efficiency of the DC-DC stage. Therefore, aiming for the most efficient MIC concept, the P-PPC will not be considered in this paper further.

III. Converter Dimensioning

As a result of the evaluation process of section II the buck-boost converter concept [c.f. **Fig. 4(c)**] was chosen as most promising concept for a high efficiency MIC for series connected PV panels due to its high flexibility in the number of panels per string. Such a converter topology can either be a 4-switch (**Fig. 4(c)** upper drawing) or a 2-switch (**Fig. 4(c)** lower drawing) topology. Fundamental considerations show that the voltage stress across the switches is higher for the 2-switch buck-boost converter ($U_{\text{in}} + U_{\text{out}}$) than for the 4-switch buck-boost converter (U_{in} resp. U_{out}), which leads to higher switching losses. In addition, since the on-state resistance $R_{\text{ds,on}}$ of MOSFETs is proportional to the breakdown voltage of the switches (valid for superjunction MOSFETs) also higher conduction losses will occur. Therefore the 4-switch buck-boost converter is selected for the dimensioning.

A. Full Power 4-Switch Buck-Boost Converter

In this subsection a guideline for the design of a high efficiency module integrated buck-boost converter according to the specification in **Tab. II** is given. This includes the identification of the main sources of converter losses:

- Switching losses of MOSFETs (including gate drives).
- Copper and core losses of the inductor.
- Conduction losses of the PCB and the on-state resistance of the MOSFETs.
- Constant losses (i.e. auxiliary supply for DSP, current and voltage sensors and other peripheral electronics).

The choice of the input switches is based on their required blocking voltage and is defined by the maximum panel voltage ($U_{\text{in,max}}$) which occurs at full irradiation at low temperatures (T_{min}). In order to avoid avalanche conditions only switches with a voltage rating of 60 V are considered for selection. Furthermore, in order to account for the specification to withstand

TABLE II: Specifications of module integrated DC-DC converters. (STC: Standard Test Conditions)

Parameter	Variable	Value
Nominal converter power	P_{conv}	250 W
Panel voltage in MPP at STC	U_{MPP}	25 V
Max. input voltage	$U_{\text{in,max}}$	40 V
Panel current in MPP at STC	I_{MPP}	10 A
Max. converter output voltage	U_{out}	100 V
Max. converter output current	I_{out}	20 A
Min. ambient temperature	T_{min}	$-20°$C
Max. ambient temperature	T_{max}	$100°$C
Bus voltage	U_{Bus}	400 V

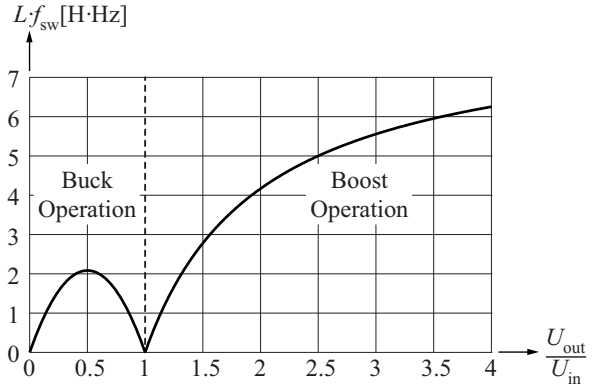

Fig. 8: Normalized inductance value in dependence of the output to input voltage ratio for a given input voltage U_{in} and a maximum current ripple of $I_{\text{MPP}} = 30\%$.

ambient temperatures of $T_{\text{max}} = 100°$C only switches with a chip size that allows to have an efficiency high enough to keep the junction temperature within the specification of the data sheet are considered. The same approach is used for the selection of the output side switches where MOSFETs with a break-down voltage of 150 V are chosen. The contribution of the semiconductor losses to the total losses of the converter is mainly determined by the choice of the output side switches. In buck operation the current through the output switches is causing conduction losses while in boost operation the switching losses of the output switches are dominant. Based on switching loss measurements the MOSFET IPB072N15N3 / Infineon was selected for the output switches and the MOSFET BSB028N06NN3 / Infineon in the low profile CanPak package was chosen as input switches.

The converter is designed to work in Continuous Conduction Mode (CCM) and thus has a DC current with superimposed switching frequency dependent current ripple. The value of the inductor is chosen by the condition to limit the peak to peak current ripple to a maximum of 30% of the MPP current I_{MPP} which is equal to 3 A. As shown in **Fig. 8** the worst case requirement to maintain this limit is given by the highest boost ratio operating point, i.e. $U_{\text{out}} = 100V$.

The core losses of the inductor have been calculated based on the improved generalized Steinmetz Equation (iGSE), where $P_{\text{V,core}}$ is the power loss per unit volume

$$P_{\text{V,core}} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{3}$$

with ΔB being the peak-to-peak flux density and

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{4}$$

where α, β and k are material parameters. According to [7] equations (3) and (4) can be simplified for the case of piecewise linear waveforms as present in the converter. Since the MIC is operating attached to the back of a PV panel where elevated temperature levels can be expected, the

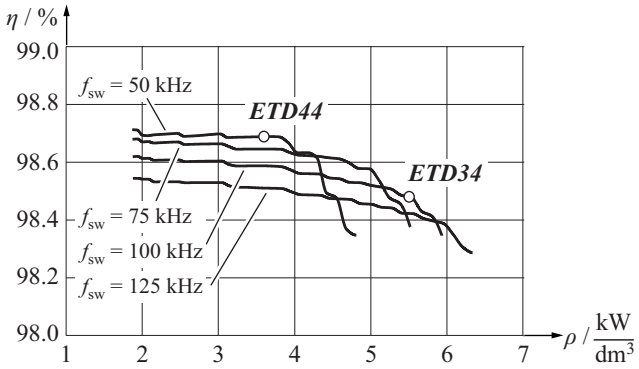

Fig. 9: η-ρ-Pareto-front of 4-switch buck-boost converter with two selected converter designs as prototypes ($U_{in} = 25\,V$, $U_{out} = 23\,V$, $P_{out} = 250\,W$).

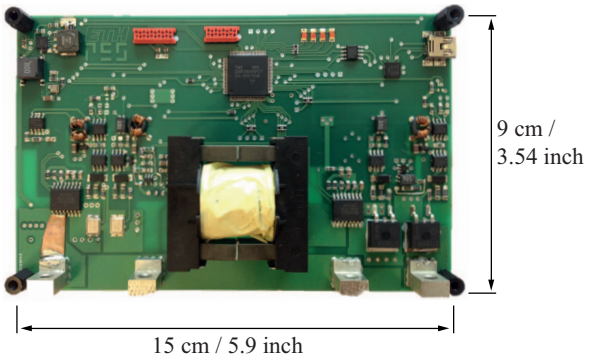

Fig. 10: Converter prototype with ETD34 core.

Siferrite material N87 / Epcos was chosen as core material which shows minimum losses at 100°C. As an alternative the material N51 / Epcos could be used with minimum losses at 50°C. The skin effect and the proximity effect contribute to the AC winding losses in the inductor and have been determined by FEM simulations for all considered designs.

As the value of the inductance is inversely proportional to the switching frequency, a trade-off has to be made between the power density of the converter and its efficiency. Based on the above mentioned loss factors, a Pareto-front (**Fig. 9**) has been calculated which visualizes the best possible trade-off between the power density and efficiency. Two different converter designs have been selected on the Pareto-front for the realization as prototypes. The first design comprises an ETD34 core with an inductance of 31 µH and operates at 100 kHz. The second design comprises an ETD44 core with 62 µH and 50 kHz switching frequency thus yielding a higher efficiency but lower power density compared to the first design selection.

In [11] it was shown, that the voltage ripple at the PV panel should be kept below 8.5% of the MPP voltage in order to extract 98% of available panel power. This statement mainly focuses on MPP trackers which periodically changes the converter input voltage in order to track the MPP of the PV panel. The voltage ripple which is caused by the switching transients should be kept to a minimum in order to not influence the MPP tracker. Thus, the maximum peak-to-peak voltage ripple was set to 2% of the MPP voltage, yielding a capacitance value of 15 times 4.7 µF (70.5 µF in total) for the input capacitors and 9 times 4.7 µF (42.3 µF in total) for the output capacitors. As a material the X7R dielectric was chosen since it offers a comparably low variation of the capacitance value over the required temperature range. The ESR of the capacitors hardly contribute to the total losses and were thus neglected in the loss calculations.

IV. Experimental Results

Based on aforementioned design considerations a prototype (**Fig. 10**) has been built with a swappable main inductor for testing of the two different designs.

As micro controller unit (MCU) the TMS320F20869 / TI floating point unit was chosen and downclocked to 20 MHz for additional power savings. The PCB is a four layer board with increased copper thickness (70 µm) of the inner layers for reduced conduction losses.

A. *Efficiency measurement setup*

For highly accurate efficiency measurements a special measurement setup has to be created since the losses are in the lower Watt range. In general, there are basically three possibilities how efficiency measurements can be performed:

- Using a power analyzer.
- Separate measurements of input and output voltages and currents.
- Calorimetric measurements.

The option of using a power analyzer is the most convenient way of such a measurement and therefore usually the first choice. However, measurements of a DC-DC converter in a typical operating point of solar module integrated converters with a power anaylzer such as the WT3000 / Yokogawa lead to an accuracy of only ± 0.18%. This would mean, that a measurement result of e.g. 98.5% would only indicate that the real value would be within the span of 98.32% and 98.68%. With calorimetric methods the efficiency of any converter is determined by measuring the dissipated heat. This method is more suited for power losses in the range of 10 to 200 W [12] and thus not suitable for the measurement of MICs.

Consequently, the efficiency measurements were performed by separately measuring input and output voltages and currents as shown in **Fig. 11**. The setup consists of a Solar Array Simulator (E4360 / Agilent) as the power source, two calibrated

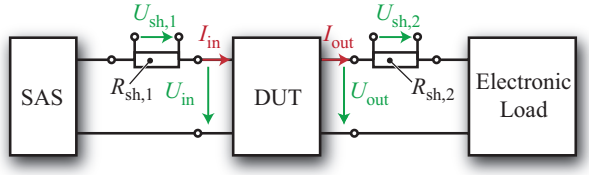

Fig. 11: Efficiency measurement setup with solar array simulator (SAS), device under testing (DUT), electronic load and shunts for current measurements.

measurement shunts (1282 / burster) and four high precision multimeters (34410A / Agilent) for the voltage measurements of the converter input and output voltage and the voltage across the shunts for precise current measurements and an electronic load (63202 / Chroma). The multimeters are triggered by a function generator (33220A / Agilent) in order to measure all values at the same instance. All devices are centrally controlled by a computer via MATLAB. The efficiency of the described setup can be calculated as

$$\eta_{\text{Conv}} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{U_{\text{out}} I_{\text{out}}}{U_{\text{in}} I_{\text{in}}} = \frac{U_{\text{out}} \frac{U_{\text{sh,2}}}{R_{\text{sh,2}}}}{U_{\text{in}} \frac{U_{\text{sh,1}}}{R_{\text{sh,1}}}} \tag{5}$$

The accuracy of this method for a typical operating point is $\pm$ 0.05%, i.e. more than three times more accurate than the method of using a power analyzer.

B. Measurement results

The efficiency of the prototype with ETD34 core and 100 kHz switching frequency was measured for different operating points, always with a fixed input voltage of 30 V. The results for buck operation in dependency of the input power for different voltage levels are shown in **Fig. 12**. For the case where the output voltage is equal to the input voltage, the upper switches were constantly switched on thus having no switching losses and reaching a peak efficiency of 99%. The efficiency is decreasing with decreasing output voltage due to the increasing current in the converter which leads to higher conduction losses.

The results for operation in boost mode with 30 V input voltage are shown in **Fig. 13**. The switching losses of the output switches increase with increasing output voltage and therefore lead to a lower efficiency.

The loss distribution of the converter operating at an output voltage of 40 V with 30 V input voltage and 200 W input power reveals that the main source of losses are the switches (**Fig. 14**). In contrast, the loss distribution for the same power level and input voltage in buck operation with 25 V output voltage shows that here the main source of losses are the conduction losses (**Fig. 15**).

The second design selection of the Pareto-front was tested on the same prototype but with a different inductor (ETD44) and lower switching frequency (50 kHz). The comparison of the efficiency between the two different designs is shown in **Fig. 16** for an input power of 200 W for an input voltage of 30 V in dependency of the output voltage.

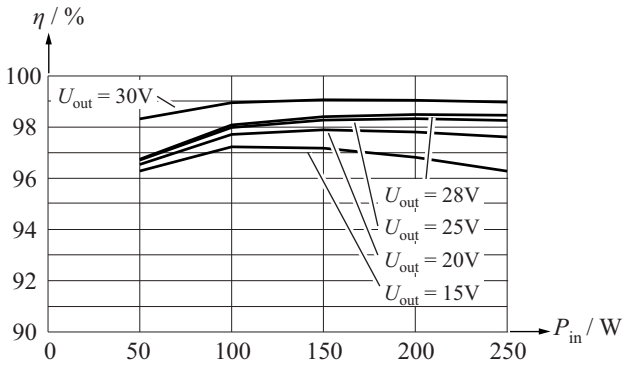

Fig. 12: Efficiency measurement results of prototype (ETD34 core, 100 kHz switching frequency) in buck operation at 30 V input voltage for different output voltage levels in dependency of the input power.

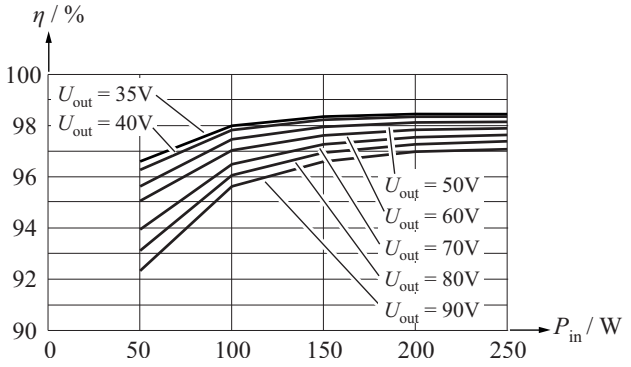

Fig. 13: Efficiency measurement results of prototype (ETD34 core, 100 kHz switching frequency) in boost operation at 30 V input voltage for different output voltage levels in dependency of the input power.

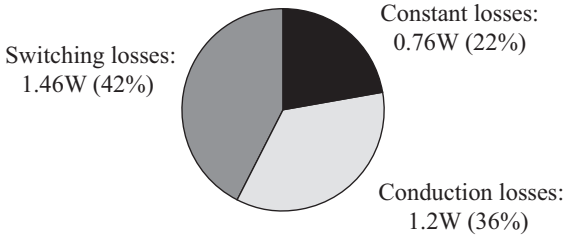

Fig. 14: Loss distribution of prototype (ETD34 core, 100 kHz switching frequency) in boost operation at 30 V input voltage and 40 V output voltage and 200 W input power with constant losses (DSP etc.), conduction losses of PCB and MOSFETs and losses related to the switching operations.

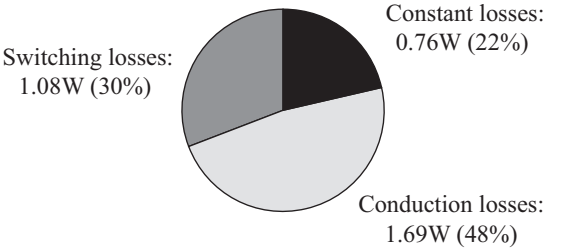

Fig. 15: Loss distribution of prototype (ETD34 core, 100 kHz switching frequency) in buck operation at 30 V input voltage and 25 V output voltage and 200 W input power with constant losses (DSP etc.), conduction losses of PCB and MOSFETs and losses related to the switching operations.

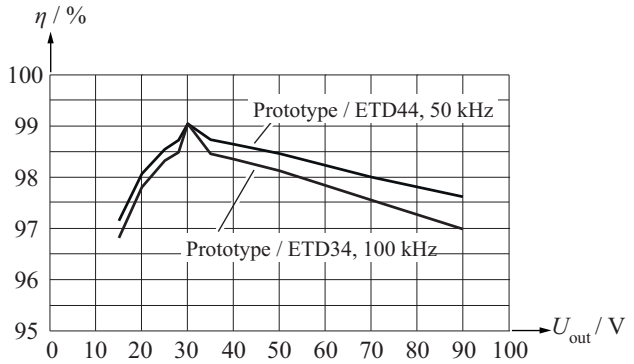

Fig. 16: Achievable efficiency improvement of the prototype with increased inductor volume (ETD44 core instead of ETD34 core) and decreased switching frequency (50 kHz instead of 100 kHz) at 30 V input voltage in dependency of the output voltage.

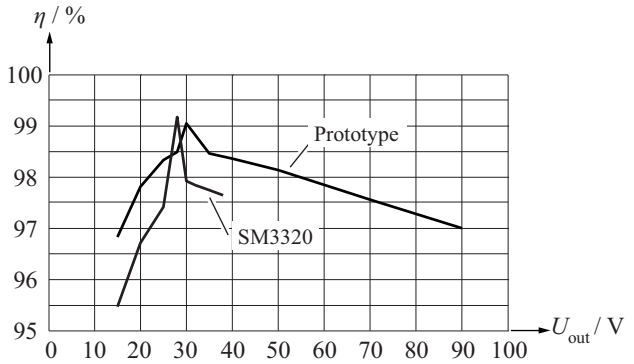

Fig. 17: Comparison of efficiency measurement results between prototype (ETD34 core, 100 kHz switching frequency) and SM3320 / National Semiconductor for 200 W input power at 30 V input voltage in dependency of output voltage.

TABLE III: Specifications of the prototype in comparison to the SM3320 by National Semiconductor.

Parameter	ETH Prototype	SM3320-1A1
Max. input MPP voltage	40 V	40 V
Max. converter output voltage	100 V	43 V
Max. converter output current	20 A	12.5 A
Physical dimensions	15 cm x 9 cm	12.7 cm x 8.8 cm

C. Comparison to commercial MIC

The evaluation board of the module integrated converter SM3320 / National Semiconductor was used as a benchmark system for the prototype. The specifications of both converters are compared in **Tab. III**. It has to be noted that the prototype has a higher rating of both the output voltage and output current thus providing a higher flexibility in the number of PV panels per string than the SM3320. Furthermore, with the extended operating range the prototype can adapt to a wider variety of different shading situations.

The efficiency curves in dependency of the output voltage have been plotted for different power levels. The result for 200 W input power is shown in **Fig. 17**. The SM3320 converter has a pass-through mode where a fifth switch directly connects input and output to reduce the losses when output and input voltage are equal. Even though the ETH prototype has an extend range of operation, it shows a higher efficiency in all operating points of about 1 percentage point except for the pass through mode where they reach equal results.

In literature [8]-[10] other prototypes of such a converter can be found with peak efficiencies in the range of 95% to 98% with special pass-through mode [10].

V. Conclusion

In this paper an overview of the possible topologies for module integrated DC-DC converters is given. They can be divided into full power and partial power converters both with subcategories of series and parallel connection. The full power buck-boost converter is identified as the most promising concept for series connected PV panels due to the great flexibility it provides regarding the number of panels per PV string with fixed DC bus voltage. A prototype of this concept was presented in detail with efficiencies up to 98.5% in switched mode operation and 99% in pass through operation. Furthermore the possibility of further efficiency improvement up to 98.7% with the use of larger inductor is shown.
Finally the prototype was compared to a commercial module integrated DC-DC converter and even though the operation range of the prototype is much wider than the one of the commercial converter, its efficiency is one percentage point higher at 200 W.

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