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***Abstract*—This paper introduces the methodology and the results of a comprehensive comparison of a direct matrix converter (MC), an indirect MC, and a voltage dc-link back-to-back converter for a 15-kW permanent magnet synchronous motor drive. The comparison involves the investigation of the passive components, including the EMI input filter, the required silicon chip area for a defined maximum admissible thermal loading of the power semiconductors, the total losses and/or achievable efficiency, a prediction of the resulting volume and weight of the passive components, and, finally, a tradeoff study between the efficiency, volume, and weight of the converters. Different performance indicators that ultimately allow a systematic determination of the application area of each converter topology are provided with this comparative evaluation.**

***Index Terms*—Comparative evaluation, matrix converter (MC), voltage dc-link back-to-back converter (V-BBC).**

I. Introduction

In ACADEMIA, matrix converters (MCs) have been considered for more than three decades as a main future concept for a wide range of industrial applications and, more recently, also for "more electric aircraft" applications. However, despite intensive research, MCs have, until now, only achieved a low market penetration. The most widely used bidirectional low-voltage ac-ac converter topology in industry remains the two-level voltage dc-link back-to-back converter (V-BBC). The proponents of the MC technology argue that the direct ac-ac power converters without intermediate energy storage elements would not only permit a more compact implementation but would also considerably increase the system lifetime due to the absence of the dc-link capacitor. On the contrary, critics claim that MCs would not provide significant advantages that would compensate for their limitations, such as, for example, the lack of voltage step-up capability and/or the limited maximum output voltage, and thus would not justify the higher implementation effort that they assume in comparison to V-BBCs.

Despite the broad spectrum of partially very detailed and in-depth investigations, research work performing a comprehensive comparison of direct ac-ac converter topologies for drive applications is comparatively rare. Most of the investigations focus on a performance comparison based on semiconductor loss calculations or measurements. In [1]–[3], the semiconductor losses and the design of the CMC and VSBBC are compared to identify the potential benefits and risks of the MC technology. Reference [3] suggests an electrothermal simulation-based approach to analyze the thermal stress of the power semiconductors of the CMC and V-BBC. A rather novel approach in academia is comparisons based on power cycling tests of the semiconductors [4], considering the amplitude of the cyclic changes of the power semiconductor junction temperatures which can be related to the semiconductor lifetime and thus also to the converter system lifetime. However, other converter features such as the volume of passive components or EMI, which have an important impact on the overall converter performance, are often neglected. A systematic and more complete converter topology evaluation is presented in [5] on ac-dc-ac converter systems for applications on aircraft.

The main objective of this paper is to show the methodology and criteria required for a systematic and comprehensive ac-ac converter system evaluation and to perform a comprehensive comparison of the conventional (direct) MC [CMC; cf., Fig. 1(a)], the indirect MC [IMC; cf., Fig. 1(b)], and the V-BBC [cf., Fig. 1(c)] for low-voltage and low-power applications ($\leq$ 100 kW) based on a 15-kW permanent magnet synchronous motor (PMSM) drive system.

Section II first gives an overview of the main properties of the MC and V-BBC and highlights the similarities and differences between the two converter concepts. Then, a brief overview of the modulation schemes considered and the main converter control loops is given. Section III is dedicated to the passive components and derives the basic relations between the volume, weight, and losses of capacitors and inductors. In Section IV, the essential considerations for a volume-optimized design of the passive components, including the EMI input filter, are demonstrated for all three converter topologies. Section V summarizes the main properties of the selected power

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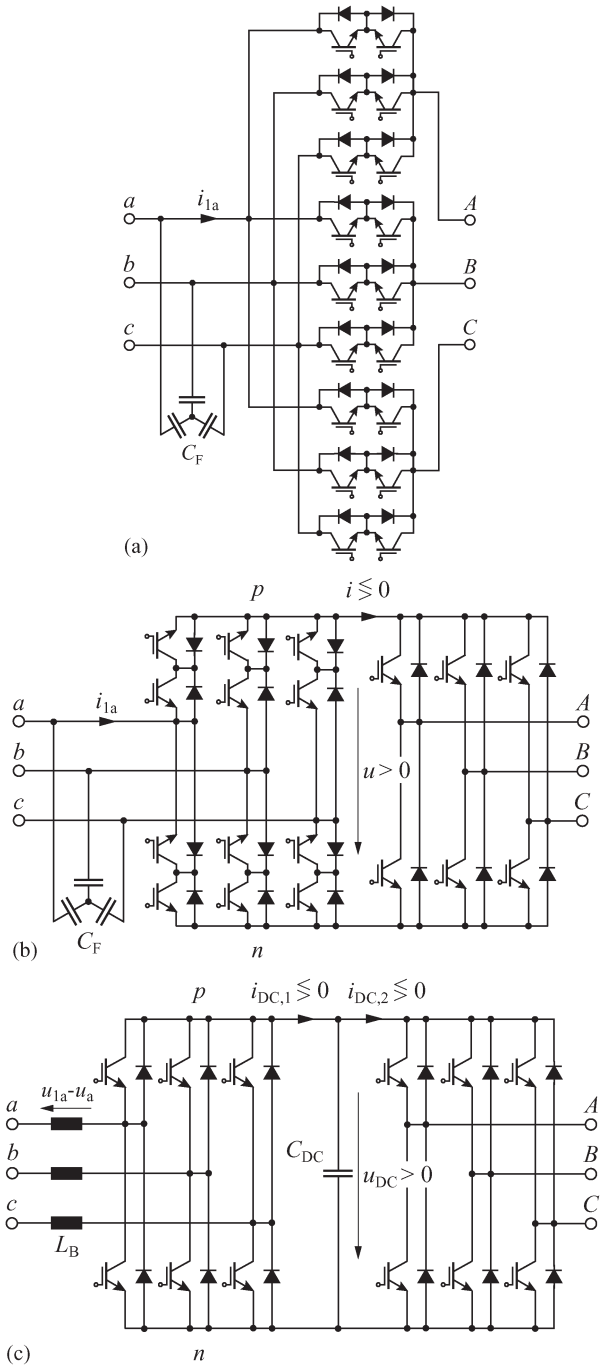

Fig. 1. Considered converter topologies (only the first stage of the EMI input filter, which is required for the basic operation, is shown). (a) CMC. (b) IMC. (c) V-BBC.

semiconductor devices and then discusses the design relevant operating points and their impact on the semiconductor losses and stress considering the mission profile of the drive system. Next, the motivation and procedure for a semiconductor-area-based comparison are described, and the thermal design of the semiconductors and the cooling system is defined. Section VI summarizes the assumptions and models of the auxiliary components such as the control and measurement hardware. Based on the criteria, models, and methods of comparison identified and derived in the previous sections, ultimately, in Section VII, the actual comparative evaluation of the CMC, IMC, and

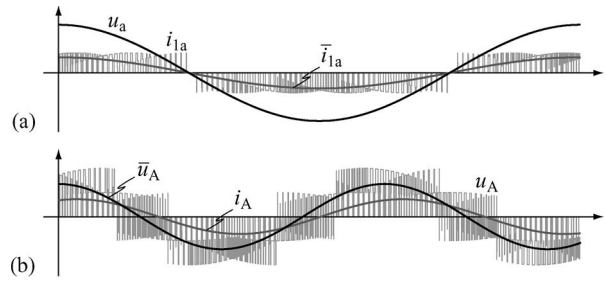

Fig. 2. Characteristic waveforms of the CMC for $\Phi_1 \approx 0$ and $\Phi_2 = \pi/9$ (inductive load). (a) Input line voltage i_{1a}, input current i_{1a}, and input current $\bar{i}_{1a}$ averaged over T_P. (b) Output line voltage u_A, output line voltage $\bar{u}_A$ averaged over T_P, and output line current i_A.

V-BBC is performed. Finally, in Section VIII, a compilation of the key findings is provided, including a decision-guidance using nine different performance indicators for the selection of an adequate converter topology with respect to an intended application. This paper concludes with a discussion of suitable application areas for MCs in the field of low-voltage drive systems.

II. Key Converter Properties

Forced commutated ac-ac converter topologies without any intermediate energy storage are referred to as MCs [6]. They can provide simultaneous amplitude and frequency transformation of three-phase voltage–current systems. Their operating principle is based on the constant power flow in a symmetrical three-phase voltage–current system. The CMC performs the voltage and current conversion in one stage. As an alternative, the IMC features a two-stage (indirect) power conversion. The CMC and IMC topologies are equivalent regarding their basic functionality. Their different physical implementation merely results in a different loading of the semiconductors and a different commutation scheme. Compared to the (two-level) V-BBC, MCs are inherently "quasi three-level" converters as all three instantaneous (but obviously not constant) line-to-line input voltages can be applied to the converter output terminals (cf., [6, Figs. 13 and 21]). The V-BBC is a two-stage topology that is formed by a back-to-back connection of a voltage-source-type input and an output stage, which are decoupled by the dc-link capacitor C_{DC}. The (boost) inductors L_B enable power factor correction at the input under the restriction of boost operation of the input stage $(U_{\mathrm{DC}} > \sqrt{6}U_1)$.

In summary, MCs require impressed voltages at the input (input capacitors C_F) and impressed currents at the output (inductive load). In contrary, V-BBCs have impressed currents at the input (boost inductors L_B) and output (inductive load). Figs. 2–4 show the characteristic waveforms of the CMC, IMC, and V-BBC when supplying a three-phase ohmic-inductive load.

A. Voltage Step-Up Capability

Output voltage step-up capability (boost operation) is a desirable feature of converter systems for drive applications as it enables a less conservative motor design and ultimately a

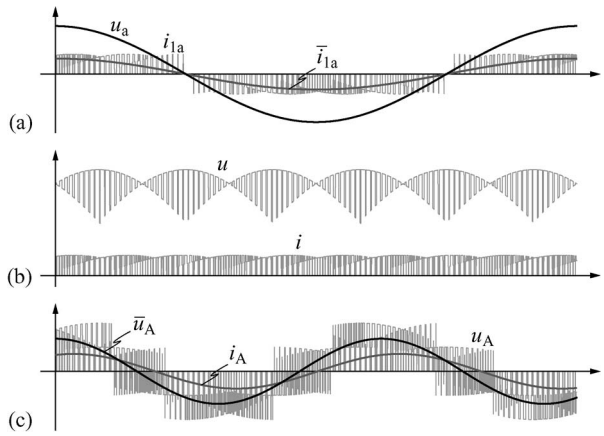

Fig. 3. Characteristic waveforms of the IMC for $\Phi_1 \approx 0$ and $\Phi_2 = \pi/9$ (inductive load). (a) Input line voltage u_{1a}, input current u_{1a}, and input current $\bar{i}_{1a}$ averaged over T_P. (b) Link voltage u and link current i. (c) Output line voltage u_A, output line voltage $\bar{u}_A$ averaged over T_P, and output line current i_A.

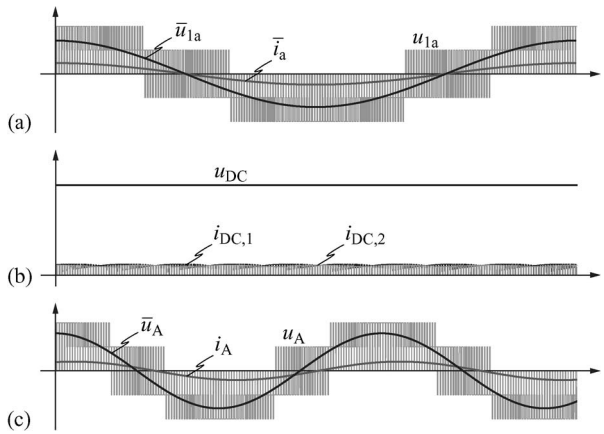

Fig. 4. Characteristic waveforms of the V-BBC for $\Phi_1 \approx 0$ and $\Phi_2 = \pi/9$ (inductive load). (a) Input voltage u_{1a}, input voltage $\bar{u}_{1a}$ averaged over T_P, and input line current i_a. (b) DC-link voltage u_{DC}, dc-link currents $i_{DC,1}$, and $i_{DC,2}$. (c) Output line voltage u_A, output line voltage $\bar{u}_A$ averaged over T_P, and output line current i_A.

better usage of the motor. The maximum output voltage of MCs is limited to $\sqrt{3}/2 \approx 86\%$ of the input voltage for sinusoidal modulation, and hence, the control can only compensate input voltage sags as long as the maximum voltage transfer ratio is not reached. As opposed to MCs, V-BBCs inherently provide voltage step-up (boost) functionality and thus are able to maintain the nominal output voltage also at reduced input voltages.

B. Considered Modulation Schemes

The basic functionality, the electrical properties, and the semiconductor losses of ac-ac converters are significantly determined by the implemented modulation schemes. In this comparison, for all three converter topologies, discontinuous space vector modulation schemes with loss optimal clamping are considered, as described in [6] and [7], which provide two active and one zero state per pulse period T_P.

A modulation scheme is used for the IMC (cf., [6, Fig. 14]), which enables zero-current switching (ZCS) of the input stage in which, for a complete switching sequence of the input stage, the switching sequence of the output stage is repeated for two different link voltage levels u. The advantage of this modulation scheme is that the switching state of the input stage can be changed during the freewheeling state of the output stage, when no current flows in the link $(i = 0)$, and thus, no special commutation strategy is required for the IMC. No switching losses occur in the input stage apart from losses due to component parasitics. An alternative modulation scheme that enables zero-voltage switching of the output stage is described in [6]–[9], but it is not further considered as it requires a voltage/current-dependent commutation and leads to a lower efficiency at part load. The CMC requires a multistep commutation strategy to guarantee safe commutation. In this paper, a conventional four-step commutation sequence (cf., [6, Fig. 22]), based on the measured input voltages and the measured output currents, is selected. The selected modulation scheme for the input and output of the V-BBC [cf., [6, Fig. 5(b)]] is synchronized to minimize the current ripple of the dc-link capacitor.

A more detailed description of the modulation and commutation scheme considered is provided in [6]. The modulation schemes selected have in common that, in total, six relative turn-on times need to be calculated per pulse period for all converter topologies. In terms of commutation safety, the CMC represents the most critical solution, followed by the IMC and the V-BBC.

C. Control

The main control properties of the individual converter topologies for a basic feedback control scheme of a motor drive are briefly discussed. There is no significant difference between the CMC and IMC from a point of view of control. Hence, it is sufficient to restrict the considerations to MCs in general.

The motor control of the MC and V-BBC is basically identical and typically consists of an outer speed control loop and two inner current control loops for the d- and q-axis stator currents. The motor control is actually the whole feedback control required for a simple MC-based drive system [buck-type control equivalent; cf., [6, Fig. 36(c) and (d)]]. The V-BBC requires another three control loops for its input stage [boost-buck-type control equivalent; cf., [6, Fig. 36(a)]]: one outer control loop for the dc-link voltage and two inner loops for the d- and q-axis input currents that are impressed in the boost inductors. As opposed to V-BBCs, MCs do not allow for feedback control of the input currents independent of the load currents, which affects the input current quality and leads to a typical input current THD of 5% for standard switching frequencies (e.g., 8 kHz) of low-voltage variable-speed drives. More advanced control schemes such as direct torque control or model predictive control can also obviously be applied to MC and have been investigated in detail [10], [11].

D. Reactive Power Compensation

Another preferable characteristic of three-phase ac-ac converters is the capability to supply or absorb reactive input power in order to compensate the capacitive currents drawn by the input filter or to perform power factor correction or

active damping. Assuming a proper design, the reactive power compensation capability of V-BBCs is limited primarily by the component ratings, whereas for MCs, there are different restrictions imposed by the topology. The formation of real input power P_1 and reactive input power Q_1 can be quantified by the subsequent equations, for standard modulation schemes of MCs, whereby the converter losses are neglected

$$P_1 = \frac{3\sqrt{3}}{4} M_{12} \hat{U}_1 \hat{I}_2 \cos\left(\Phi_1^*\right) \cos(\Phi_2) \tag{1}$$

$$Q_1 = \frac{3\sqrt{3}}{4} M_{12} \hat{U}_1 \hat{I}_2 \cos\left(\Phi_1^*\right) \sin(\Phi_2) \tag{2}$$

$$M_{12} = \frac{2}{\sqrt{3}} \frac{\hat{U}_2}{\hat{U}_1} \frac{1}{\cos\left(\Phi_1^*\right)} = [0 \ldots 1] \tag{3}$$

where $\hat{U}_1$ represents the amplitude of the input line voltage, $\hat{I}_2$ is the amplitude of the output line current, M_{12} is the modulation index [voltage transfer ratio; cf., [6, eqs. (12)–(19)]], Φ_1^* is the desired (reference) current-to-voltage displacement angle at the converter input, and Φ_2 is the current-to-voltage displacement angle at the converter output. Thus, it appears that the formation of reactive input power is only possible if the real power flow is different from zero and that the maximum reactive input power decreases with an increasing displacement angle Φ_2. The maximum output voltage achievable depends on the desired current-to-voltage displacement angle at the input, which is represented by the definition of the modulation index M_{12} in (3).

Special hybrid modulation schemes, suggested in [12] and [13], allow for decoupling the real power transfer from the reactive power transfer and, hence, also enable, for example, the formation of reactive input power for a purely reactive load ($\Phi_2 = \pm\pi/2$). However, if the instantaneous output currents of the MC are equal to zero (zero apparent output power, $S_2 = 0$), in principle, no reactive input power can be provided, neither with standard nor with extended hybrid modulation schemes. On the contrary to the MC, the V-BBC does not have such a restriction due to its intermediate energy storage and can provide reactive power at the input also at zero output current.

The input power factor control is implemented for both the MC and the V-BBC by adding an offset to the reference displacement angle Φ_1^* at the converter input.

E. Specifications

The considered specifications for the CMC, IMC, and V-BBC, including the motor and the assumed mission (load) profile, are shown in Table I. If not specified otherwise, they are valid throughout this paper.

TABLE I
CONVERTER DESIGN, MOTOR, AND LOAD SPECIFICATIONS

Quantity	Parameters
Line-to-line input voltage	$U_{ll,\mathrm{nom}} = 3 \times 400\,\mathrm{V}$ (rms)
Input frequency (mains)	$f_1 = 50\,\mathrm{Hz}$
Rated output power	$S_2 = 15\,\mathrm{kVA}$, $\Phi_2 = 0 \ldots 2\pi$
Switching frequency	$f_{\mathrm{sw}} = \{8\,\mathrm{kHz}, 32\,\mathrm{kHz}\}$
Load	Motor drive
DC-link voltage for V-BBC	$U_{\mathrm{DC}} = 700\,\mathrm{V}$
Max. ambient temperature	$T_{A,\max} = 50^\circ\mathrm{C}$
Max. sink temperature	$T_{S,\max} = 95^\circ\mathrm{C}$
Assumed mission profile	Continuous operation (S1)
Nominal operating points	$P_{2,\mathrm{nom}} = \pm 15\,\mathrm{kW}$, $\Phi_2 \approx 0/\pi$ $U_{2,\mathrm{nom}} = 0.9 \cdot U_{2,\max}$ at $f_{2,\mathrm{nom}} = \pm 140\,\mathrm{Hz}$
Required system lifetime	$\geq 10\,\mathrm{a}$ ($\approx 87\,600\,\mathrm{h}$)
Modulation	Discontinuous SVM
Number of gate signals	CMC: 18, IMC: 12, V-BBC: 12
Number of gate drivers	CMC: 18, IMC: 12, V-BBC: 12
Motor type	PMSM, 3 pole pairs
MC: Nominal motor voltage	$U_{M,\mathrm{nom,MC}} = 303\,\mathrm{V}$ (rms)
Nominal motor current	$I_{M,\mathrm{nom,MC}} = 28.6\,\mathrm{A}$ (rms)
Stator inductance	$L_{S,\mathrm{MC}} = 1.04\,\mathrm{mH}$
V-BBC: Nominal motor voltage	$U_{M,\mathrm{nom,V\text{-}BBC}} = 443\,\mathrm{V}$ (rms)
Nominal motor current	$I_{M,\mathrm{nom,V\text{-}BBC}} = 19.6\,\mathrm{A}$ (rms)
Stator inductance	$L_{S,\mathrm{V\text{-}BBC}} = 1.5\,\mathrm{mH}$
Rated electrical power	$P_{M,\mathrm{el}} = 15\,\mathrm{kW}$
Rated mechanical power	$P_{M,\mathrm{mech}} = 14.4\,\mathrm{kW} \approx 20\,\mathrm{hp}$
Nominal speed	$n_{\mathrm{nom}} = 2\,800\,\mathrm{rpm}$ at $140\,\mathrm{Hz}$

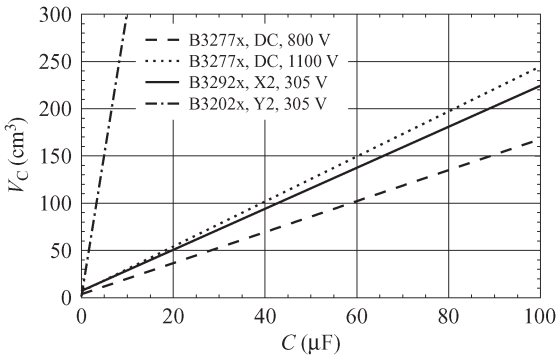

Fig. 5. Volume V_C versus capacitance C of polypropylene dc, X2, and Y2 capacitors (B320xx-, B3277x-, and B3292x-series; EPCOS) for an operating temperature of 85 °C.

III. PASSIVE COMPONENTS

Passive components have a significant impact on the overall converter losses, volume, weight, and lifetime due to their physical properties and must therefore be considered when comparing different converter concepts.

A. Capacitors

The following considerations are restricted to polypropylene foil capacitors which allow for a long enough lifetime. Two characteristic foil capacitor types are utilized for ac-ac converters: dc-link and EMI suppression capacitors. The component characteristics and ratings of different manufacturers are very similar. EPCOS is the reference manufacturer selected.

Fig. 5 shows the scaling of the boxed volume of the foil capacitors selected. The corresponding model parameters, including the ranges of validity, are summarized in Table II.

TABLE II
DC-LINK AND X2 CAPACITOR MODEL PARAMETERS

Quantity	Parameters and Ranges of Validity
$V_{C_{\mathrm{DC}}}$	$k_{1,V,C_{\mathrm{DC}}} = 1.64 \cdot 10^6\,\mathrm{cm^3/F}$
	$k_{2,V,C_{\mathrm{DC}}} = 3.72\,\mathrm{cm^3}$
$ESR_{C_{\mathrm{DC}}}$	$k_{1,\mathrm{ESR},C_{\mathrm{DC}}} = 2.29 \cdot 10^{-4}\,\Omega$
(at 10 kHz)	$k_{2,\mathrm{ESR},C_{\mathrm{DC}}} = -2.76 \cdot 10^{-1}$
$I_{C_{\mathrm{DC}},\mathrm{rms}}$	$k_{1,I_C,\mathrm{rms}} = 3.92 \cdot 10^5\,\mathrm{A/F}$
(at 10 kHz)	$k_{1,I_C,\mathrm{rms}} = 4.87\,\mathrm{A}$
Constraints	$U_{\mathrm{DC}} = 800\,\mathrm{V},\ C_{\mathrm{DC}} = 5\,\mu\mathrm{F} \ldots 500\,\mu\mathrm{F}$
	$T_{C_{\mathrm{DC}}} = 85°\mathrm{C}$
V_{X2}	$k_{1,V,C_{\mathrm{X2}}} = 2.17 \cdot 10^6\,\mathrm{cm^3/F}$
	$k_{2,V,C_{\mathrm{X2}}} = 7.25\,\mathrm{cm^3}$
$R_{S,C_{\mathrm{X2}}}$	$k_{1,R,C_{\mathrm{X2}}} = 1.97 \cdot 10^{-4}\,\Omega$
	$k_{2,R,C_{\mathrm{X2}}} = -3.69 \cdot 10^{-1}$
Constraints	$U_{\mathrm{X2,rms,max}} = 305\,\mathrm{V},\ C_{\mathrm{X2}} = 1\,\mu\mathrm{F} \ldots 100\,\mu\mathrm{F}$
	$T_{C_{\mathrm{X2}}} = 85°\mathrm{C}$
m_C	$\rho_C \approx 1.3\,\mathrm{g/cm^3}$

1) DC-Link Capacitors: The volume per capacitance scales with the rated voltage U_C and the surge voltage capability. If the relation between volume and capacitance (for a given voltage class) is evaluated, for instance, for the dc-link capacitors (B3277x-series; EPCOS), it is found that the volume scales, for a given rated voltage, linearly with the capacitance and, for a given capacitance, approximately with the square of the rated voltage, which is proportional to the stored energy

$$V_C|_{U_C} \propto C \quad \text{and} \ \propto U_C^2. \tag{4}$$

DC-link capacitors (800 V) are selected for the V-BBC due to the specified dc-link voltage of 700 V and for providing a margin of 100 V for transient voltage variations. The resulting scaling between the boxed volume $V_{C_{\mathrm{DC}}}$ of the dc-link capacitors and the capacitance, evaluated for an operating temperature $T_{C_{\mathrm{DC}}} = 85\ °\mathrm{C}$, yields to

$$V_{C_{\mathrm{DC}}}|_{U_{\mathrm{DC}}} = k_{1,V,C_{\mathrm{DC}}} \cdot C_{\mathrm{DC}} + k_{2,V,C_{\mathrm{DC}}}. \tag{5}$$

The capacitor losses scale with the volume of the dielectric material and, thus, with the capacitance and the resulting current ripple. The resulting total losses can be modeled with an equivalent series resistance (ESR). The ESR represents the dielectric and the ohmic (skin effect) losses of the metallic contacts for the considered polypropylene capacitor technology. Evaluated for a current ripple frequency of 10 kHz (the frequency dependence of the ESR is neglected), the ESR of the selected dc-link capacitors can be expressed as

$$ESR_{C_{\mathrm{DC}}}|_{U_{\mathrm{DC}}} = k_{1,\mathrm{ESR},C_{\mathrm{DC}}} \cdot \left(\frac{C_{\mathrm{DC}}}{\mathrm{F}}\right)^{k_{2,\mathrm{ESR},C_{\mathrm{DC}}}}. \tag{6}$$

In order to meet the lifetime requirements (e.g., $\geq 100\,000$ h) of the dc-link capacitors, the rms current ripple of the dc-link capacitors needs to be limited. The maximum tolerable current ripple, determined for a current ripple frequency of 10 kHz and an operating temperature of 85 °C, is then given by

$$I_{C_{\mathrm{DC}},\mathrm{rms}}|_{U_{\mathrm{DC}}} = k_{1,I_C,\mathrm{rms}} \cdot C_{\mathrm{DC}} + k_{2,I_C,\mathrm{rms}}. \tag{7}$$

2) EMI Suppression Capacitors: In this comparison, X2 and Y2 capacitors, both rated for a continuous rms voltage of 305 V, are considered for EMI suppression. The X-type capacitors are used for differential mode (DM) filtering, and the Y-type capacitors are used for common mode (CM) filtering.

The boxed volume of the considered X2 capacitors for a given operating voltage and an operating temperature of $T_{C_{X2}} = 85\ °\mathrm{C}$ can be written as

$$V_{C_{X2}}|_{U_{X2}} = k_{1,V,C_{X2}} \cdot C_{X2} + k_{2,V,C_{X2}}. \tag{8}$$

The resulting losses of polypropylene X2 EMI suppression capacitors are typically significantly lower than that for an equally sized dc-link capacitor in a V-BBC as the current ripple injected into the input filter capacitors is low for typical voltage-source-type input stages. The losses are accordingly determined mainly by the reactive currents generated by the mains voltage and are uncritical for 50/60-Hz applications. Exceptions are the input filter capacitors C_F of MCs (and, in general, for current-source-type converters) as they absorb the switched (rectangular-shaped) line currents. The series resistance of the considered X2 capacitors is approximately two to three times larger than that for the selected dc-link capacitors of equal capacitance as an assembly structure with a higher pulse peak voltage capability is required for mains application. The resulting ESR of the X2 capacitors can be approximated by

$$ESR_{C_{X2}}|_{U_{X2}} = k_{1,R_{S,X2}} \cdot \left(\frac{C_{X_2}}{\mathrm{F}}\right)^{k_{2,R_{S,X2}}}. \tag{9}$$

An additional important constraint for the X2 capacitors is given by the maximum admissible voltage rise and fall time, which, however, is not modeled for this investigation.

The Y2 capacitors have a marginal impact on the filter volume and the losses as the maximum allowable capacitance is limited by the specified current in the protective earth (PE) conductor and is small compared to the required DM input capacitors. The maximum CM capacitance value, assuming a maximum tolerable PE current of $I_{\mathrm{CM},Y,\mathrm{max}} = 3.5\,\mathrm{mA}$ for a 400-V/50-Hz mains system, is then limited to

$$C_{\mathrm{CM,max}} \leq \frac{I_{\mathrm{CM},Y,\mathrm{max}}}{2\pi U_1 f_1} = 48.4\ \mathrm{nF}. \tag{10}$$

By inspection of the curves in Fig. 5, it can be seen that the Y2 capacitance value hardly contributes to the overall filter volume and is accounted for with a default volume of 10 $\mathrm{cm^3}$.

The resulting mass of the capacitors can be calculated by utilizing the average density of foil capacitors ρ_C

$$m_C|_{U_C} = \rho_C \cdot V_C. \tag{11}$$

B. Inductors

1) DM Inductors: DM inductors are required to implement the boost inductors of the V-BBC and the DM filter inductors of all topologies. In this comparison, toroidal powder core inductors are considered. They provide a good compromise between the achievable inductance per volume and ac and dc

TABLE III
HIGH FLUX 60 CORE MATERIAL AND INDUCTOR PARAMETERS

Quantity	Parameters
Manufacturer	Magnetics
Core shape	Toroidal
Saturation flux density	1.5 T
Density	$7.6\,\mathrm{g/cm^3}$
Relative core losses:	
$\hat{B} = 0.1\,\mathrm{T}, f = 10\,\mathrm{kHz}$	$60\,\mathrm{mW/cm^3}$
$\hat{B} = 0.1\,\mathrm{T}, f = 50\,\mathrm{kHz}$	$0.52\,\mathrm{W/cm^3}$
Application	Boost and DM inductors
Frequency range	$< 50\,\mathrm{kHz}$
Conductor	Single-wire
Winding structure	Single-layer

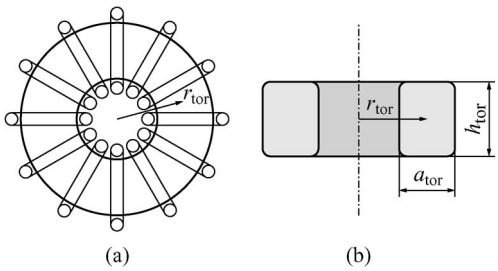

Fig. 6. (a) Top view of the considered toroidal DM inductor. (b) Core cross section with core dimensions.

magnetization properties. In order to minimize the parasitic winding capacitance, only single-layer designs are considered. The material selected is the powder core alloy High Flux HF 60, manufactured by Magnetics. A summary of the core material data is given in Table III.

The main inductor parameters are the inductance at zero current $L_{\mathrm{DM},0}$, the inductance at the peak current value L_{DM}, and the rms inductor current $I_{L,\mathrm{rms}}$ at a given frequency and temperature. Based on these quantities, the inductors are designed such that the desired DM inductance L_{DM} is provided at the peak inductor current $\hat{I}_L = \sqrt{2} I_{L,\mathrm{rms}}$ and that the inductance value drops at the peak current to $\gamma_\mu = 80\%$ of its initial value at zero current. The peak inductor current, which corresponds to the nominal converter input current, is equal to $\hat{I}_{\mathrm{DM}} = 32.5$ A for an estimated converter efficiency $\eta_{\mathrm{est}} = 95\%$. The core data are extracted from the manufacturer data. The core dimensions (cf., Fig. 6) are optimized to minimize the boxed volume of the DM inductors. The width a_{tor} and the height h_{tor} of the core are expressed as a function of the radius r_{tor} of the toroidal core for that purpose and the aforementioned constraints

$$a_{\mathrm{tor}}(r_{\mathrm{tor}}) = 2r_{\mathrm{tor}} - \frac{d_{w,\mathrm{tot}}(\hat{I}_L + 2H_{\max} r_{\mathrm{tor}} \gamma_{\mathrm{tt}})}{\hat{I}_L} \quad (12)$$

$$h_{\mathrm{tor}}(a_{\mathrm{tor}}, r_{\mathrm{tor}}) = \frac{\hat{I}_L^2 L_{\mathrm{DM}}}{2\pi\mu_0\mu_r\gamma_\mu H_{\max}^2 a_{\mathrm{tor}} r_{\mathrm{tor}}}. \quad (13)$$

The total wire diameter $d_{w,\mathrm{tot}}$ is selected such that a maximum rms current density $J_{w,\max}$ of 6 A/mm^2 results, providing a good compromise between the resulting volume and losses for the selected core material and inductor design. An insulation coating thickness of $d_{\mathrm{ct}}/2 = 0.05$ mm is assumed. The resultant boxed volume of the DM inductors can then be calculated as a function of the core radius r_{tor}

$$V_{L,\mathrm{box}} = 4\left(r_{\mathrm{tor}} + \frac{a_{\mathrm{tor}} + 3d_{w,\mathrm{tot}}}{2}\right)^2 (h_{\mathrm{tor}} + 3d_{w,\mathrm{tot}}). \quad (14)$$

The minimum inductor volume and, thus, the optimal radius of the toroidal core $r_{\mathrm{tor,opt}}$ are found by minimizing (14)

$$V_{L_{\mathrm{DM}}}|_{I_L}(r_{\mathrm{tor,opt}}) = \min\left(V_{L,\mathrm{box}}|_{\hat{I}_L}(r_{\mathrm{tor}})\right) \quad (15)$$

as shown in Fig. 7.

In analogy to the capacitors, the inductor volume scales, for a given peak current, approximately linearly with the inductance and, for a given inductance, approximately with the square of the peak current, which again corresponds to the stored energy

$$V_{L_{\mathrm{DM}}}|_{I_L} \propto L \text{ and } \propto \hat{I}_L^2. \quad (16)$$

The resulting relation between the boxed volume of the DM inductor and the inductance is shown in Fig. 8 for different peak inductor currents and may be written as

$$V_{L_{\mathrm{DM}}}|_{I_L} = k_{1,V,L_{\mathrm{DM}}} \cdot L_{\mathrm{DM}} + k_{2,V,L_{\mathrm{DM}}}. \quad (17)$$

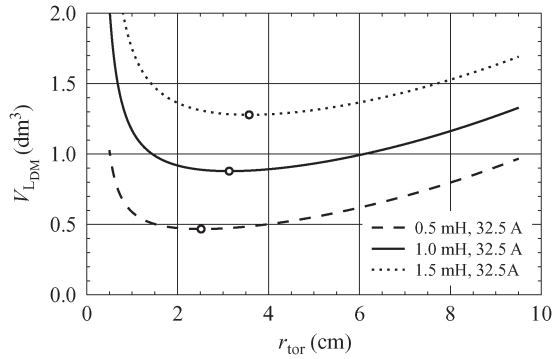

Fig. 7. Resulting boxed volume of the designed DM inductors using High Flux 60 powder core material (Magnetics) for the nominal peak inductor current $\hat{I}_L = 32.5$ A and different inductance as a function of r_{tor}. The minimum achievable core volumes are marked with circles. The resulting optimal core dimensions are, for example, $a_{\mathrm{tor,opt}} = 3.1$ cm, $h_{\mathrm{tor,opt}} = 8.0$ cm, and $r_{\mathrm{tor,opt}} = 3.1$ cm for $\hat{I}_L = 32.5$ A and $L_{\mathrm{DM}} = 1.0$ mH.

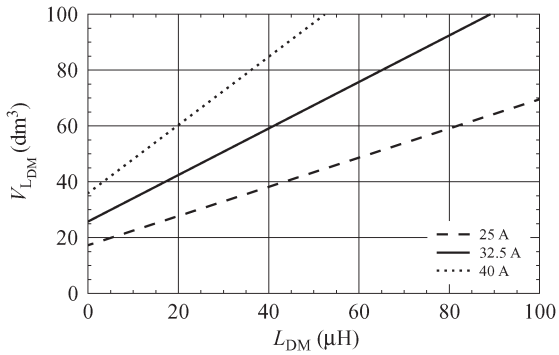

Fig. 8. Boxed volume $V_{L_{\mathrm{DM}}}$ versus inductance L_{DM} of the designed single-layer toroidal DM inductors for different peak DM inductor currents using High Flux 60 powder core material (Magnetics). The top view and cross section are shown in Fig. 6.

TABLE IV
DM INDUCTOR MODEL PARAMETERS

Quantity	Parameters and Ranges of Validity
$V_{L_{\rm DM}}$	$k_{1,V,L_{\rm DM}} = 8.33 \cdot 10^5\,{\rm cm}^3/{\rm H}$
	$k_{2,V,L_{\rm DM}} = 2.58 \cdot 10^1\,{\rm cm}^3$
$m_{L_{\rm DM}}$	$k_{1,m,L_{\rm DM}} = 3.94 \cdot 10^3\,{\rm kg/H}$
	$k_{2,m,L_{\rm DM}} = 3.82 \cdot 10^{-2}{\rm kg}$
$R_{{\rm DC},L_{\rm DM}}$	$k_{1,R,L_{\rm DM}} = 4.06\,\Omega$
	$k_{2,R,L_{\rm DM}} = 6.39 \cdot 10^{-1}$
$P_{{\rm core,HF},L_{\rm DM}}$	$\alpha = 2.22,\ \beta = 1.32,\ k = 492$
Constraints	$I_{L_{\rm DM}} = 23.0\,{\rm A},\ \hat{I}_{L_{\rm DM}} = 32.5\,{\rm A}$
	$L_{\rm DM} = 5\,\mu{\rm H} \ldots 3\,{\rm mH}$
	$H_{\max} = 5990\,{\rm A/m}\ J_{\rm Cu} = 6\,{\rm A/mm}^2$
	$T_{w_{\rm Cu}} = 85°{\rm C},\ \gamma_\mu = 0.8,\ \mu_r = 60$

The ratio between the mass of the core material and the copper wire within the boxed inductor volume is not constant. The mass of the inductor thus has to be estimated by

$$m_{L_{\rm DM}}|_{I_L} \approx k_{1,m,L_{\rm DM}} \cdot L_{\rm DM} + k_{2,m,L_{\rm DM}} \tag{18}$$

for a given inductor current I_L.

The dc wire resistance of the DM inductors can be calculated by

$$R_{{\rm DC},L_{\rm DM}}|_{I_L} = k_{1,R,L_{\rm DM}} \cdot \left(\frac{L_{\rm DM}}{H}\right)^{k_{2,R,L_{\rm DM}}}. \tag{19}$$

If not specified otherwise, the wire temperature is assumed as $T_{w_{\rm Cu}} = 85$ °C. The DM inductor parameters are compiled in Table IV.

The major loop core losses at the mains frequency, referred to as low-frequency (LF, i.e., 50 Hz) core losses, are modeled with the standard Steinmetz equation. If the Steinmetz parameters were known as a function of the dc bias of the core, the HF core losses could be determined by a calculation approach based on the modified Steinmetz equation according to [14]. The pragmatic approach chosen here is to perform core loss measurements on sample inductors with a square-wave voltage that is generated with a switched bridge-leg. The measurement results prove that, for the selected DM inductor design, the core losses hardly depend on the resulting dc bias of the minor loop and that the HF core losses can be approximated by the maximum amplitude $\hat{B}_{\Delta i,\max}$ of the resulting flux density of the current ripple in the inductor

$$P_{{\rm core,HF},L_{\rm DM}} \approx k \cdot \left(\frac{\hat{B}_{\Delta i,\max}}{T}\right)^{\alpha} \cdot \left(\frac{f_{\rm sw}}{\rm Hz}\right)^{\beta}. \tag{20}$$

This quasi-linear loss behavior results from the selected core material and the applied inductor design, limiting the variation of the relative permeability in operation to $\gamma_\mu = 80\%$ of its initial value $\mu_{r,{\rm ini}}$.

2) Three-Phase CM Inductors: Toroidal cores from Vacuumschmelze (VAC) are considered for the three-phase CM filter inductors with a tape-wound nanocrystalline core, which is fabricated of Vitroperm 500 F core material. The main design parameters of a CM inductor are the impedance $|\underline{Z}_{\rm CM}|$ (insertion loss) provided at a certain frequency, the CM saturation current and/or the corresponding voltage-time area product, and the inductor current. In order to minimize the parasitics, again a single-layer winding design is assumed with a winding sector angle of 100° each.

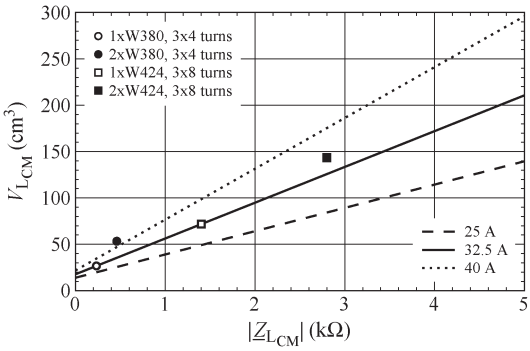

Fig. 9. Boxed volume $V_{L_{\rm CM}}$ versus the absolute value of the impedance $|\underline{Z}_{L_{\rm CM}}|$ of the three-phase toroidal CM inductors for different peak DM inductor currents using Vitroperm 500 F nanocrystalline tape-wound core material (Vacuumschmelze).

TABLE V
CM INDUCTOR MODEL PARAMETERS

Quantity	Parameters and Ranges of Validity
$V_{L_{\rm CM}}$	$k_{1,V,L_{\rm CM}} = 3.86 \cdot 10^{-2}\,{\rm cm}^3/{\rm k\Omega}$
	$k_{2,V,L_{\rm CM}} = 1.77 \cdot 10^1\,{\rm cm}^3$
$L_{{\rm lk},L_{\rm CM}}$	$k_{1,{\rm lk},L_{\rm CM}} = 3.34$
	$k_{2,{\rm lk},L_{\rm CM}} = 9.20 \cdot 10^{-8}\,{\rm H}$
$R_{{\rm S},L_{\rm CM}}$	$k_{1,R_{\rm S},L_{\rm CM}} = 7.16 \cdot 10^5\,\Omega/{\rm H}$
	$k_{2,R_{\rm S},L_{\rm CM}} = 0.62 \cdot 10^{-8}\,\Omega$
$m_{L_{\rm CM}}$	$k_{1,m,L_{\rm CM}} = 7.40 \cdot 10^{-2}\,{\rm g/k\Omega}$
	$k_{2,m,L_{\rm CM}} = 1.85 \cdot 10^1\,{\rm g}$
$R_{{\rm DC},L_{\rm CM}}$	$k_{1,R_{\rm DC},L_{\rm CM}} = 9.27 \cdot 10^{-7}$
	$k_{2,R_{\rm DC},L_{\rm CM}} = 7.12 \cdot 10^{-4}\,\Omega$
Constraints	$I_{L_{\rm DM}} = 23\,{\rm A},\ \hat{I}_{L_{\rm DM}} = 32.5\,{\rm A}$
	$\lvert\underline{Z}_{\rm CM}\rvert = 0.2\,{\rm k\Omega} \ldots 5\,{\rm k\Omega}$
	$T_{w_{\rm Cu}} = 85°{\rm C},\ J_{\rm Cu} = 8\,{\rm A/mm}^2$

As opposed to the DM inductors, the CM inductor model is based on standard core sizes (VAC W409, W380, and W424) and substantiated by inductor impedance measurements as the selected core material features strongly nonlinear characteristics to enable simple scaling of the core geometry. The scaling law for the boxed volume of the CM inductor volume, evaluated at 100 kHz, is modeled with

$$V_{L_{CM}}|_{I_{L_{\rm DM}}} = k_{1,V,L_{\rm CM}} \cdot |\underline{Z}_{\rm CM}| + k_{2,V,L_{\rm CM}}. \tag{21}$$

The impedance of the CM inductor at $f_{Z_{\rm CM}} = 100$ kHz and the equivalent (small-signal) resistance are then given by

$$|\underline{Z}_{\rm CM}||_{I_{L_{\rm DM}}} = \sqrt{\left(2\pi f_{Z_{\rm CM}} \cdot L_{\rm CM}\right)^2 + R_{S,Z,L_{\rm CM}}^2} \tag{22}$$

$$R_{S,Z,L_{\rm CM}}|_{I_{L_{\rm DM}}} = k_{1,R_S,L_{\rm CM}} \cdot L_{\rm CM} + k_{2,R_S,L_{\rm CM}}. \tag{23}$$

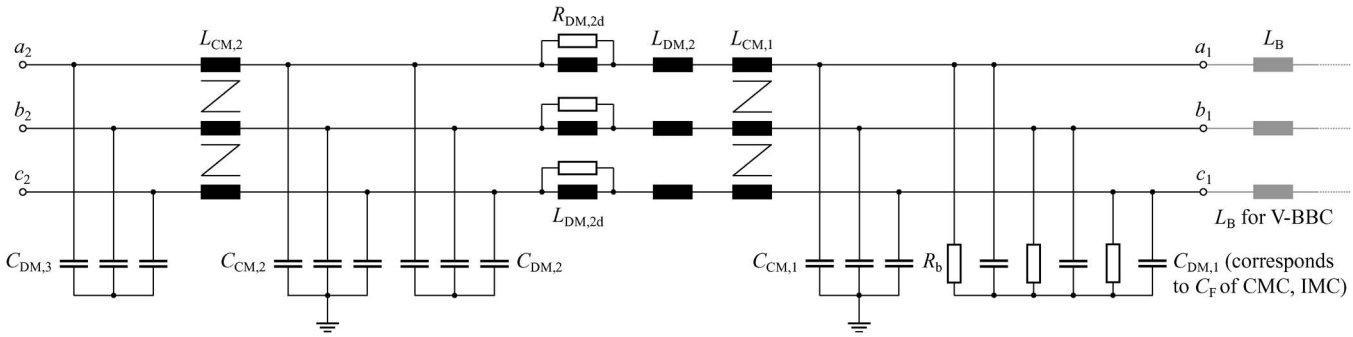

Fig. 10. EMI input filter topology considered. $C_{\mathrm{DM},1}$ corresponds to the input capacitors C_F of the MCs. The boost inductors L_B of the V-BBC, colored in gray, are connected to the terminals a_1, b_1, and c_1 and represent the DM filter inductors $L_{\mathrm{DM},1}$ of the input filter. Over-voltage protection devices such as varistors or components for inrush current control or precharging of the dc-link capacitor in case of the V-BBC are not shown.

Finally, the leakage inductance can be approximated by

$$L_{\mathrm{lk},L_{\mathrm{CM}}}|_{I_{L_{\mathrm{DM}}}} \approx k_{1,\mathrm{lk},L_{\mathrm{CM}}} \cdot L_{\mathrm{CM}} + k_{2,\mathrm{lk},L_{\mathrm{CM}}}. \tag{24}$$

The relationship between the boxed volume of the CM inductors and the impedance is shown in Fig. 9, and the inductor model parameters are summarized in Table V.

The mass of the CM inductor is modeled with

$$m_{L_{\mathrm{CM}}}|_{I_{L_{\mathrm{DM}}}} \approx k_{1,m,L_{\mathrm{CM}}} \cdot |\underline{Z}_{\mathrm{CM}}| + k_{2,m,L_{\mathrm{CM}}} \tag{25}$$

in a similar manner as that for the DM inductors.

An rms current density of 8 A/mm^2 is assumed for the CM inductors, leading to a dc wire resistance of

$$R_{\mathrm{DC},L_{\mathrm{CM}}}|_{I_{L_{\mathrm{DM}}}} = k_{1,R_{\mathrm{DC}},L_{\mathrm{CM}}} \cdot |\underline{Z}_{\mathrm{CM}}| + k_{2,R_{\mathrm{DC}},L_{\mathrm{CM}}}. \tag{26}$$

CM inductors generate core losses similar to any other magnetic component. However, for the filter topology (cf., Fig. 10) and switching frequency range considered, the losses of the CM inductors are dominated by the copper losses, and hence, the core losses can be neglected.

IV. Passive Component and EMI Filter Design

The EMI input filter should allow for a highly efficient power transfer at the mains frequency with a minimal voltage-to-current phase lag and should meet the specified conducted emission (CE) EMI levels (cf., Table VI) and power quality standards. Additionally, in order to avoid oscillations that could occur at resonance frequencies of the input filter above the converter input current control bandwidth and/or around the switching frequency, passive damping has to be provided. In the frequency range of the input current control bandwidth, filter resonances should be avoided.

A. LISN and Load

A detailed description of the CE measurement chain can be found in [15] and [16]. It consists of the following main components: the line impedance stabilizing network (LISN), the EMI test receiver, the power converter, and the load (motor). The LISN for the required three-phase converters is modeled with three single-phase 50-Ω/50-μH LISNs.

TABLE VI
CE Limits at the Mains Terminals for Class B Equipment According to CISPR 11

Frequency Range	*Class B Limit*	
	Quasi-peak	Average
150 . . . 500 kHz	56 . . . 46[a] dB/μV	6 dB/μV
0.5 . . . 5 MHz	56 dB/μV	46 dB/μV
5 . . . 30 MHz	60 dB/μV	50 dB/μV

[a]Linearly decreasing with logarithm of frequency

The impact of the PMSM on the DM input current can be neglected for the DM filter design. However, for the CM filter design, a second-order equivalent circuit of the CM impedance $\underline{Z}_{M,\mathrm{CM,HF}}$ of the load is used. The impedance is parameterized based on measurement results of a PMSM (LST-series, LTi Drives), including a 3-m-long motor cable

$$\underline{Z}_{M,\mathrm{CM,HF}} = \frac{1}{j2\pi C_{M,\mathrm{CM}}} + j2\pi f L_{M,\mathrm{CM}} + R_{M,\mathrm{CM}}$$
$$C_{M,\mathrm{CM}} = 2\ \mathrm{nF} \quad L_{M,\mathrm{CM}} = 435\ \mathrm{nH} \quad R_{M,\mathrm{CM}} = 2.1\ \Omega. \tag{27}$$

The impedance parameters are valid within the frequency range of 100 kHz to 5 MHz, which is sufficient for the CM filter design. In order to ensure that the CM inductors do not saturate in the frequency range of the electrical input and output frequency of the converter, the low-frequency CM impedance of the load $\underline{Z}_{M,\mathrm{CM,LF}}$ has to be determined, which, for the sake of brevity, is not shown.

The parasitic capacitance of the semiconductors to the heat sink per unit area can be approximated by $C'_{\mathrm{SM,PE}} \approx 20$ pF/cm^2. The omission of $C_{\mathrm{SM,PE}}$ in the derived DM and CM equivalents (cf., Fig. 12) is justifiable to determine the filter volume as the capacitance of the load $\underline{Z}_{M,\mathrm{CM,HF}}$ is approximately ten times larger than the expected maximum value of $C_{\mathrm{SM,PE}}$.

The DM noise of the CMC and IMC is virtually identical within the considered EMI measurement range from 150 kHz to 30 MHz for the selected modulation schemes, and the CM noise spectrum differs mainly in the low-frequency range at multiples of the input and output frequencies. Thus, it is sufficient to consider in the following paragraphs the EMI filter requirements for MCs in general.

B. Filter Topology

Although different advanced filtering concepts have been introduced for ac-ac converters, as, for instance, in [17] for the CMC, in this comparison, a conventional multistage LC filter topology is applied in order to enable comparability with typical EMI filters of ac-ac converters. The filter topology considered is shown in Fig. 10. $C_{\mathrm{DM},1}$ corresponds to the input filter capacitors C_F of the CMC and IMC. The boost inductors L_B of the V-BBC are connected to the terminals a_1, b_1, and c_1 and represent the DM filter inductors $L_{\mathrm{DM},1}$ of the first filter stage.

The main attenuation is achieved with the first two DM and CM stages. The third capacitor stage $C_{\mathrm{DM},3}$ together with the DM leakage inductance $L_{\mathrm{lk,CM},2}$ of $L_{\mathrm{CM},2}$ is used to suppress the HF noise typically above 5 MHz and thus hardly contributes to the overall filter volume.

C. Filter Design Procedure

The suggested filter design procedure is demonstrated by the flowchart in Fig. 11. It is performed with a custom-developed automated filter design software that incorporates the filter transfer function, the second-order equivalents of the passive components, and the models of the CE measurement setup. In a first step, the considered EMI filter topology (cf., Fig. 10), the EMI standard for CE (i.e., CISPR 11, class B, and 150 kHz–30 MHz), and the load parameters have to be determined.

1) Reactive Power Limitation of the Input Filter: Special attention has to be given to the sizing of the DM input filter capacitors, particularly to the size of the input capacitors C_F of the MC, in order to meet the requirements for the input power factor. A reasonable measure is to restrict the total reactive power drawn by the input filter to 15% of the nominal converter output power $P_{2,\mathrm{nom}}$. In respect of [6, eq. (19)], the desired maximum current-to-voltage displacement angle $\Phi^*_{1,\max}$ at the input of the MC can be varied for a practical implementation within -25° to 25° in order to limit the corresponding reduction of the output voltage to 90% of the maximum output voltage. The suggested design guideline enables the provision of a unity input power factor down to a minimum output power $P_{2,\Phi_1=1,\min}$ of one third of the nominal output power

$$P_{2,\Phi_1=1,\min} = \frac{0.15 P_{2,\mathrm{nom}} \eta_{\mathrm{est}}}{\tan\left(\Phi^*_{1,\max}\right)} \approx 0.31 \cdot P_{2,\mathrm{nom}} \tag{28}$$

and an estimated converter efficiency of $\eta_{\mathrm{est}} = 95\%$. This leads to a maximum DM capacitance per input phase of

$$C_{\mathrm{DM,max}} = 45\ \mu\mathrm{F} \tag{29}$$

for a line-to-line voltage of 400 V (rms), a mains frequency of 50 Hz, and a nominal converter output power $P_{2,\mathrm{nom}} = 15$ kW.

2) Constraints for CM Design: The selected CM filter strategy is to provide most of the required CM attenuation between 150 kHz and 1 MHz with the first CM stage implemented by $C_{\mathrm{CM},1}$ and $L_{\mathrm{CM},1}$ and, in the case of the V-BBC, also with the boost inductors, and the attenuation above 1 MHz with the second stage, given by $C_{\mathrm{CM},2}$ and $L_{\mathrm{CM},2}$. A VAC core

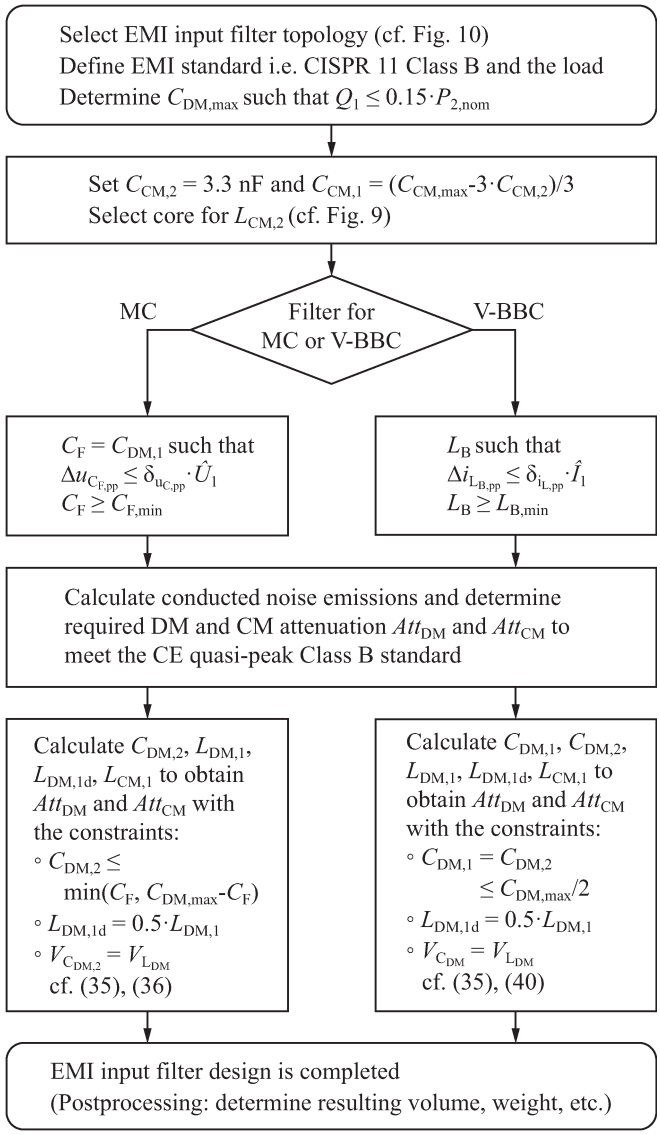

Fig. 11. Flowchart of the design procedure for the EMI input filter and the ac-side passive components at the converter input.

of the type W380 (3×5 turns, $\hat{I}_{L_{\mathrm{DM}}} = 32.5$ A; cf., Fig. 9) is selected for $L_{\mathrm{CM},2}$, and $C_{\mathrm{CM},1}$ is set to $C_{\mathrm{CM},1} = 3.3$ nF. The remaining CM capacitance $(C_{\mathrm{CM,max}} - 3 \cdot C_{\mathrm{CM},2})/3$ is equally distributed to $C_{\mathrm{CM},1} = 12.7$ nF. This approach is beneficial for the following two reasons: first, the size and, therewith, the impedance of $L_{\mathrm{CM},1}$ are significantly larger compared to $L_{\mathrm{CM},2}$, leading to a nonnegligible leakage (DM) inductance $L_{\mathrm{lk,CM},1}$ that can be used to partly implement $L_{\mathrm{DM},2}$. Second, due to the comparatively small size of $L_{\mathrm{CM},2}$, the component parasitics are low and thus still enable a high CM impedance above 5 MHz.

3) Input Capacitors C_F and Boost Inductors L_B: The input capacitors C_F have to be dimensioned for a maximum peak-to-peak voltage ripple $\Delta u_{C_F,\mathrm{pp,max}}$ as the measured capacitor voltage is required for the sector detection of the applied space vector modulation or may even determine the commutation sequence as in the case of the CMC. The maximum peak-to-peak voltage ripple across the input capacitors should be limited to $\delta_{u_{C,\mathrm{pp,max}}} = 20\%$ of the input voltage amplitude $\hat{U}_1$ based

on practical experience. In order to enable safe operation, in this paper, $\Delta u_{C_f,\mathrm{pp,max}}$ is limited to $\delta_{u_{C,\mathrm{pp,max}}} = 10\%$. The required capacitance can then be calculated by

$$C_F = C_{F,\Delta u} = \frac{\hat{I}_2}{4\hat{U}_1 f_{\mathrm{sw}} \delta_{u_{C,\mathrm{pp,max}}}}. \tag{30}$$

The switching frequency f_{sw} in the aforementioned equation refers to the switching frequency of the output stage when considering the IMC. The maximum voltage ripple across the input capacitors is obtained for $\Phi_2 = 0$ for the considered modulation schemes of the two MCs.

To meet the dynamic requirements that are imposed by the load and/or the control, for all of the converter concepts considered, a minimal internal energy storage is required, which, in the case of the MC, is mainly provided by the input capacitors C_F. It is hence reasonable from a control perspective to constrain the voltage drop Δu_{C_F} across the input capacitors during transient operation, leading to an additional control-based constraint for C_F. However, for the converter and load specifications considered (cf., Table I), the ripple-based design criterion according to (30) is more conservative than the control-based one. Accordingly, this is not further discussed here. The corresponding equations can be found in [18].

In analogy to the filter input capacitors C_F, the boost inductors L_B of the V-BBC are designed based on the current ripple at the switching frequency f_{sw} for a given input voltage amplitude $\hat{U}_1$ and a dc-link voltage U_{DC}. In this comparison, they are dimensioned for a maximum peak-to-peak current ripple $\Delta i_{L_{B,\mathrm{pp,max}}}$ of $\delta_{i_{L,\mathrm{pp,max}}} = 20\%$ of the fundamental input current amplitude $\hat{I}_1$. The inductance value of the boost inductors can be calculated as follows:

$$L_B = L_{B,\Delta i} = \frac{1}{\hat{I}_1 f_{\mathrm{sw}} \delta_{i_{L,\mathrm{pp,max}}}} \left(\hat{U}_1 - \frac{3\hat{U}_1^2}{2U_{\mathrm{DC}}} \right). \tag{31}$$

Attention has to be paid to converter stability when reducing the boost inductance with increasing switching frequencies. The theory and methodology for investigating the ac system stability are described in [19] and [20]. A practical rule of thumb is that the minimum boost inductance $L_{B,\min}$ should be at least eight to ten times larger than the inner mains inductance L_N for switching frequencies below 100 kHz

$$L_{B,\min} = 400\ \mu\mathrm{H} \approx 8 \ldots 10 \cdot L_N \quad L_{N,\mathrm{typ}} = 50\ \mu\mathrm{H}. \tag{32}$$

4) DM and CM Filter Equivalent Circuits: The filters are designed for nominal converter operation to meet the CISPR 11 class B quasi-peak standard for CE levels (150 kHz–30 MHz) that is compiled in Table VI. The used DM and CM equivalent circuits are shown in Fig. 12. A detailed description of the derivation of the equivalent circuits can be found in [7]. The required DM and CM input filter attenuations Att_{DM} and Att_{CM} of the MC and V-BBC to meet the specified EMI standard are shown in Fig. 13 for a switching frequency of 8 and 32 kHz. The attenuation values presented refer to the (additional) attenuation that has to be provided by the input filter without the attenuation that is already given by the input

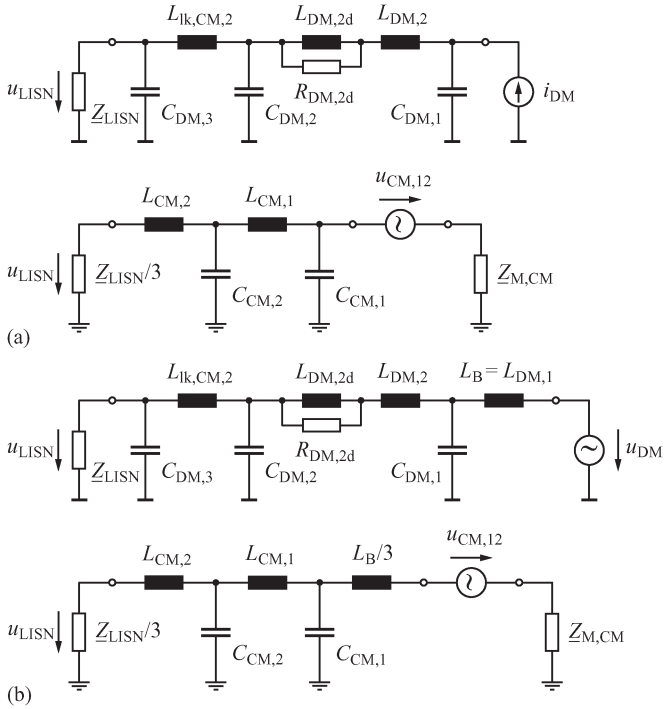

Fig. 12. Simplified DM and CM conducted EMI emission equivalent circuits for (a) MC and (b) V-BBC.

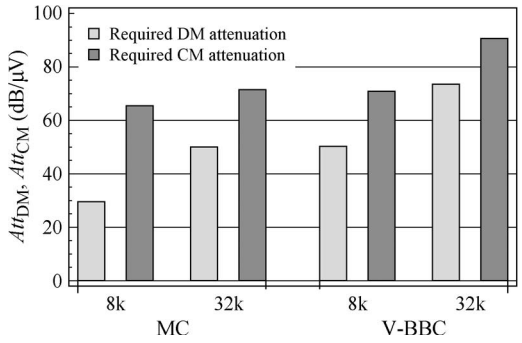

Fig. 13. Required DM and CM attenuations Att_{DM} and Att_{CM} for the MC and V-BBC at $f_{\mathrm{sw}} = 8$ kHz and a switching frequency $f_{\mathrm{sw}} = 32$ kHz.

capacitors C_F of the MC or the boost inductors L_B of the V-BBC.

5) Completion of Filter Design: Finally, the remaining filter components are designed using algorithms that minimize the overall filter volume. It should be noted again that $C_{\mathrm{DM,3}}$ is used to provide attenuation above 5 MHz, which requires small capacitance values and therefore hardly contributes to the filter volume. Its design is mainly determined by the parasitics of the other components, which are not shown here for the sake of brevity.

The capacitance range for the MC of $C_{\mathrm{DM,2}}$ is defined by

$$C_{\mathrm{DM,2}} \leq \min(C_F, C_{\mathrm{DM,max}} - C_F). \tag{33}$$

This constraint ensures that the reactive power drawn by the filter is limited as desired, and the larger DM capacitor of C_F and $C_{\mathrm{DM,2}}$ (if they are not equal) is always placed closest to the converter input stage. In consequence, the input filter always

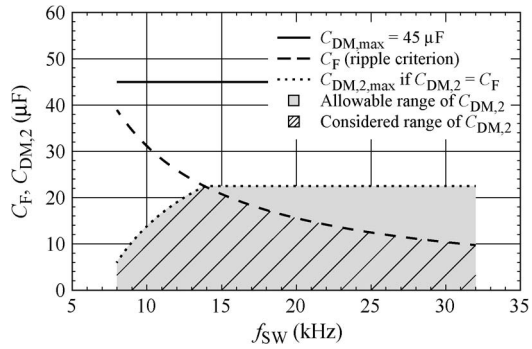

Fig. 14. $C_F = C_{\mathrm{DM},1}$ and $C_{\mathrm{DM},2}$ capacitance values versus the switching frequency for the considered EMI input filter design for MCs.

provides the lowest filter output impedance at terminals a_1, b_1, and c_1 for the given component values. The DM damping inductors $L_{\mathrm{DM},2d}$ are designed depending on $L_{\mathrm{DM},2}$

$$L_{\mathrm{DM},2d} = n \cdot L_{\mathrm{DM},2}, \qquad n = 0.5 \tag{34}$$

leading to a good compromise between damping performance and additional volume with respect to $L_{\mathrm{DM},2}$. The inductors $L_{\mathrm{DM},2d}$ and resistors $R_{\mathrm{DM},2d}$ are used to damp oscillations that may occur between $C_{\mathrm{DM},1}$, $C_{\mathrm{DM},2}$, and $L_{\mathrm{DM},2}$. $R_{\mathrm{DM},2d}$ is determined in respect of [21] to ensure an optimally damped filter stage, which means to minimize the peak output impedance of the input filter. The resistance $R_{\mathrm{DM},2d}$ that provides optimal damping for a given choice of $L_{\mathrm{DM},2d}$ can be calculated as

$$R_{\mathrm{DM},2d} = \sqrt{\frac{L_{\mathrm{DM},2,\mathrm{tot}}}{C_{\mathrm{DM},1}}} \sqrt{\frac{n(3+4n)(1+2n)}{2(1+4n)}}. \tag{35}$$

Ultimately, the values of $C_{\mathrm{DM},2}$ and $L_{\mathrm{DM},2}$ are determined such that

$$V_{C_{\mathrm{DM},2}} = V_{L_{\mathrm{DM},2}} + V_{L_{\mathrm{DM},2d}} \tag{36}$$

and (33) as well as (34) are fulfilled. This algorithm always leads to the smallest resultant total volume of $C_{\mathrm{DM},2}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{DM},2d}$ independent on the volumetric scaling of the DM capacitors and inductors (cf., [7] and [22]) under the constraint that $C_{\mathrm{DM},2} \leq C_F$ and the capacitive reactive power of the filter is minimized. Thereby, the value of the filter capacitance $C_F = C_{F,\Delta u}$ is designed based on the voltage ripple criterion given in (30). However, for the filter topology selected and switching frequencies above 35 kHz (cf., Fig. 25), a lower passive component volume can be obtained if

$$C_{\mathrm{DM},2} = C_F \geq C_{F,\Delta u}. \tag{37}$$

The voltage-ripple-based design criterion for C_F and the allowable design spaces considered for $C_{\mathrm{DM},2}$ are shown in Fig. 14 depending on the switching frequency.

Slightly different DM filter design algorithms are applied for the V-BBC as the reactive power caused by the input filter can be compensated independent of the output power of the V-BBC and is not a key design criterion for the filter. Therefore, the constraint in (33) can be weakened

$$C_{\mathrm{DM},2} = C_{\mathrm{DM},1} \leq \frac{C_{\mathrm{DM,max}}}{2} \tag{38}$$

and the capacitances of $C_{\mathrm{DM},1}$ and $C_{\mathrm{DM},2}$ are selected to be equal for simplicity. The rest of the DM filter design algorithm does not vary compared to the MC. The design equation that is used to obtain the component values of $C_{\mathrm{DM},2}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{DM},2d}$ under the condition of a minimum filter component volume may then be written as

$$V_{C_{\mathrm{DM},1}} + V_{C_{\mathrm{DM},2}} = V_{L_{\mathrm{DM},2}} + V_{L_{\mathrm{DM},2d}}. \tag{39}$$

Next, the impedance of $L_{\mathrm{CM},1}$ is calculated to meet the CM attenuation requirements. Finally, the resulting filter transfer function is analyzed to avoid any occurrence of resonances at critical frequencies such as the switching frequency or the beginning of the CE measurement range at 150 kHz.

D. DC-Link Capacitor

In a similar manner as that for the input capacitors C_F of the MC, a minimum dc-link capacitance needs to be determined to meet the dynamic requirements and to enable safe operation. The worst case considered for the V-BBC occurs for a step change from nominal motor operation to no load, which is initiated by the load and therefore cannot be precontrolled (prevented) by the converter control. This load change is more severe than a change from motor to generator operation as, in such a case, the power reversal of the input and output stage would be coordinated to minimize the transient dc-link voltage variation. In order to limit the relative overshoot of the dc-link voltage $\delta_{u_{\mathrm{DC}}} = \Delta u_{\mathrm{DC}}/U_{\mathrm{DC}}$, a minimal dc-link capacitance is required, which can be calculated, based on [18] (cf., Section III-B), by

$$C_{\mathrm{DC,ctrl}} \geq \frac{P_2}{18 U_{\mathrm{DC}} \delta_{u_{\mathrm{DC}}} \eta_{\mathrm{est}}^2} \cdot \left(\frac{\sqrt{3} L_B P_2}{U_1^2 \left(\sqrt{2} U_1 + \frac{U_{\mathrm{DC}}}{\sqrt{3}} \right)} + \frac{36 \eta_{\mathrm{est}}}{U_{\mathrm{DC}} f_{\mathrm{sw}}} \right) \tag{40}$$

assuming regular sampling and a maximum dead time of two pulse periods ($2T_P = 2 f_{\mathrm{sw}}^{-1}$).

The minimum dc-link capacitance may also be determined by an energy-based dimensioning guideline as an extension to the control-based design. Energy-based criteria are applied to ensure a certain ride-through capability and robustness or can be considered as a simplification of (40) when the dc-link voltage and the switching frequency vary only within a small range. Typical values for compact low-voltage drive trains reported in [22] are within 5 to 10 μF/kVA. Thus, for the case at hand, the minimum dc-link capacitance to enable robust operation is assumed with

$$C_{\mathrm{DC,rob}} \geq 7.5 \frac{\mu\mathrm{F}}{\mathrm{kVA}} \cdot S_{2,\mathrm{nom}} = 110\ \mu\mathrm{F} \tag{41}$$

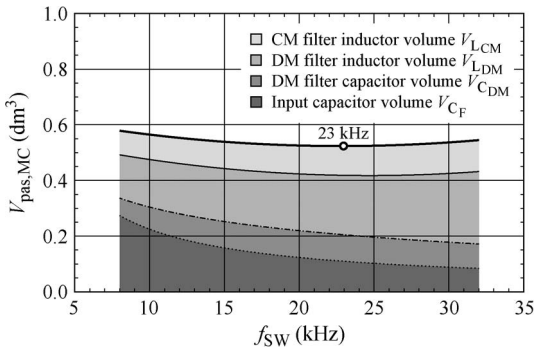

Fig. 15. Volume of the passive components of the MC $V_{\mathrm{pas,MC}}$ versus switching frequency f_{sw}.

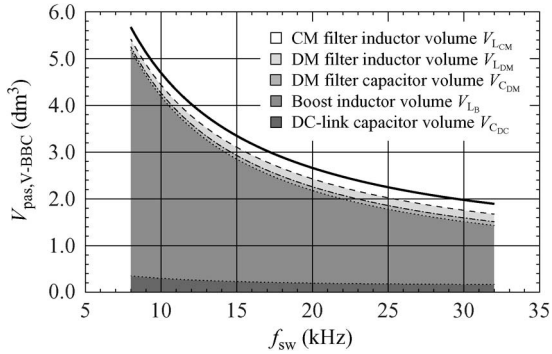

Fig. 16. Volume of the passive components of the V-BBC $V_{\mathrm{pas,V-BBC}}$ versus switching frequency f_{sw}.

and the required dc-link capacitance is then selected according to

$$C_{\mathrm{DC}} = \max(C_{\mathrm{DC,ctrl}}, C_{\mathrm{DC,rob}}). \tag{42}$$

An additional design criterion for the dc-link capacitance is to limit the voltage variation with twice the mains frequency for two-phase operation; however, this is not considered here.

E. Volume of Passive Components

Finally, the passive components and the EMI input filters of the MC and the V-BBC are designed with the dimensioning guidelines derived in Sections IV-A–D. Figs. 15 and 16 show the total boxed volume of the passive components for the MC and V-BBC, including the contribution of the individual component volumes in the dependence of the switching frequency from 8 to 32 kHz. It can be seen that, for the MC, the share of the individual component volumes is balanced, whereas for the V-BBC, the volume of the passive component is dominated by the boost inductors under the applied constraint of a small dc-link capacitance.

V. Semiconductor Design and Losses

A. Semiconductor Selection

The power semiconductors considered are fourth-generation Trench and Field-Stop T&FS 1200 V silicon IGBT4 devices and emitter controlled EmCon4 diodes from Infineon due to their performance and the variety of available devices and semiconductor modules. Both devices are rated for a maximum junction temperature of 175 °C. Although it is known that CMCs are often implemented with reverse-blocking IGBTs (RB-IGBTs), in this comparison, conventional IGBTs are used as only a few manufacturers of RB-IGBTs exist and also higher switching frequencies are considered.

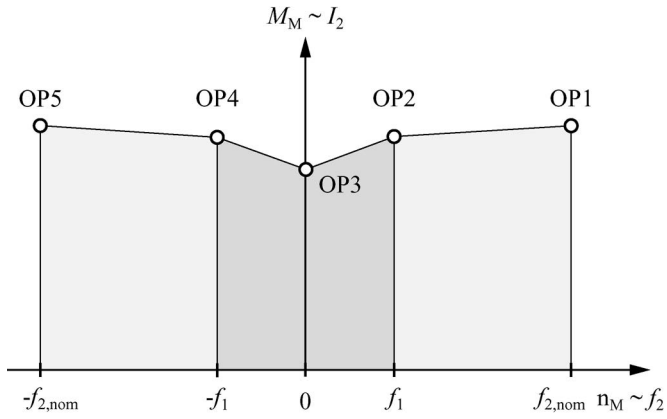

Fig. 17. Characteristic operating points of a bidirectional drive system, shown in two quadrants of the torque-speed $(M-n)$ plane.

B. Design-Relevant Operating Points

In this comparison, it is assumed that the mission profile requires continuous duty (S1 operation) mainly for nominal motor and generator operation (cf., Table I). It is hence essential to identify adequate operating points for the dimensioning of the power semiconductors and for the semiconductor loss calculation. A method to determine the required operating points is to consider the operating range of the drive system in the torque-speed plane. The semiconductor losses of three-phase ac-ac converters are modulated with the electrical input frequency f_1 and/or output frequency f_2 of the converter. This means that, the lower the resulting frequency that modulates the semiconductor losses is, the more is the modulation (pulsation) of the losses, resulting in a variation of the semiconductor junction temperature T_J for a given thermal impedance of the semiconductor chip. In order to ensure a minimum semiconductor lifetime, the amplitude of the cyclic junction temperature variation $\Delta T_{J,\max}$ and the maximum junction $T_{J,\max}$ have to be limited for the main operating range of the mission profile.

Fig. 17 shows the design-relevant operating points for continuous operation that have been identified in the torque-speed plane based on the aforementioned considerations. It is sufficient to consider only two instead of four quadrants for reasons of symmetry.

1) **OP1/OP5**: motor/generator operation at nominal motor speed (nominal electrical output frequency $f_2 = \pm f_{2,\mathrm{nom}}, |f_2| > |f_1|$) and nominal motor torque $M_{M,\mathrm{nom}}$.
2) **OP2/OP4**: motor/generator operation at reduced motor speed (the electrical output frequency is equal to the input frequency $f_2 = \pm f_1$).
3) **OP3**: motor operation at electrical standstill (the electrical output frequency is equal to zero $f_2 = 0$ Hz) and

at standstill torque $M_{M,0}$. At this operating point, it is assumed that the output voltage is equal to 2% of the topology-dependent maximum output voltage level (ohmic voltage drop of cable and motor).

The operating points at nominal operation (OP1 and OP5) and at standstill (OP3) are relevant for all three ac-ac converter topologies from the point of view of an application.

C. Required Semiconductor Chip Area

Semiconductor-related comparisons of power converters are frequently applied. A commonly used method is to compare different converter topologies by determining the losses using the same semiconductors for all topologies, as shown in [23]–[26]. In this approach, the semiconductors have to be selected such that they fulfill the ratings of all of the converter topologies compared, and thus, they are not necessarily matched to the individual topologies.

In order to enable a comparative evaluation with semiconductors matched to each converter topology, a semiconductor-chip-area-based converter comparison (SABC) is introduced [27]. The basic idea is that, if the same transistor and diode chip configuration is implemented in different converter topologies and is analyzed regarding losses and thermal stress, it is most likely that, for one topology, the transistor chip is overdimensioned and the diode chip is underdimensioned, whereas for an another topology, the opposite is true. That is exactly where the SABC provides benefits. The implemented algorithm allows the calculation of the minimum required semiconductor area for the individual transistor and diode chips for a given converter topology, operating point, and semiconductor module assembly such that the maximum junction temperature $T_{J,\max}$, the average junction temperature $T_{J,\mathrm{avg}}$, or the maximum junction temperature variation $\Delta T_{J,\max}$ of the individual transistor and diode chips are equal or less than a predefined maximum value. This method does not only guarantee optimal chip area partitioning and semiconductor material usage but also provides a common basis for converter topology comparisons: the required total semiconductor chip area. The chip area data can then be directly used to determine the semiconductor costs. Another advantage seen in the SABC is that, with the junction temperature variation, the average junction temperature, and the respective energy loss, the reliability of the semiconductors can also be predicted [28].

The transistor and diode current rating is proportional to the active chip area $A_{\mathrm{chip,act}}$, whereas the resulting thermal impedance between the junction and the heat sink $Z_{\mathrm{th,JS}}$ depends on the total chip area $A_{\mathrm{chip}} > A_{\mathrm{chip,act}}$, the semiconductor module assembly (shown in Fig. 21), and the cooling system. The electrical equivalent circuit of the thermal impedance is modeled with an RC network and can be written as a complex transfer function $\underline{G}_{\mathrm{th,JS}}(\omega)$. The resulting time behavior of the junction temperature $T_J(t)$ can be calculated using the heat sink temperature $T_S(t)$ according to

$$T_J(t) = T_S(t) + \mathcal{F}^{-1}\left\{\underline{G}_{\mathrm{th,JS}}(\omega) \cdot P_{\mathrm{chip}}(\omega)\right\} \tag{43}$$

with reference to [18, Sec. 5.1.1].

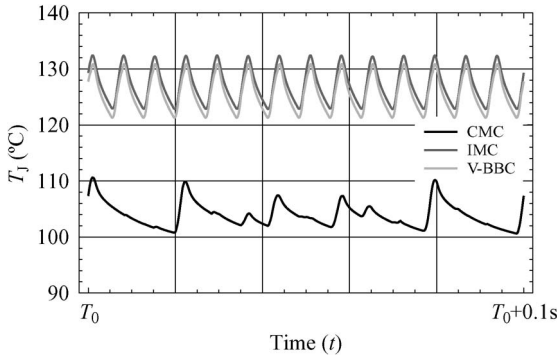

Fig. 18. Typical progression of the junction temperature $T_J(t)$ over time for the CMC, IMC, and V-BBC at $f_{2,\mathrm{nom}} = 140$ Hz, showing the different characteristic patterns of the (periodic) junction temperature variation.

Fig. 18 shows typical waveforms of the junction temperature T_J for the CMC, IMC, and V-BBC at OP1. The junction temperature of the IMC/V-BBC is modulated with the output frequency, whereas in case of the CMC, the progression of the junction temperature depends on the input and output frequencies and on the phase-angle between the current–voltage systems at the input and output. The impact of these properties on the performance of the CMC is discussed in Section VII.

In this comparison, the semiconductors of CMC, IMC, and V-BBC are designed for continuous nominal motor and generator operation (OP1 and OP5) with the algorithm shown in Fig. 19 for the SABC to determine the minimum required semiconductor chip area. The additional operating points are then investigated to further characterize the performance of the three converter systems. The relevant design constraints can be summarized as follows.

1) The minimum chip areas of the individual transistors and diodes are determined such that all three converter systems can supply/absorb the nominal electrical output power $P_{2,\mathrm{nom}} = \pm 15$ kW at the nominal output frequency $|f_2| = 140$ Hz such that the required lifetime of 10 a (cf., Table I) can be achieved. For that purpose, the maximum cyclic junction temperature variation is limited to $\Delta T_{J,\max} = 10$ K, and the maximum junction temperature is limited to $T_{J,\max} = 140$ °C for nominal operation (OP1/OP5) at 90% of the corresponding maximum converter output voltage and a heat sink temperature beneath the semiconductor module of $T_S = 95$ °C in respect of the reliability data provided by the manufacturer [29], [30].
2) Custom designs for the PMSMs with nominal motor voltages $U_{M,\mathrm{nom,MC}}$ and $U_{M,\mathrm{nom,V-BBC}}$ and stator inductances $L_{S,\mathrm{MC}}$ and $L_{S,\mathrm{V-BBC}}$ matched to the converter output voltage ranges of the MC and V-BBC are assumed (cf., Table I).
3) The switching frequency applied to the motor is identical for all three converter topologies and is selected to be equal for the input and output stages of the V-BBC (Fig. 20).

The margin between $T_{J,\max} = 140$ °C and the maximum specified junction temperature of 175 °C is required to enable

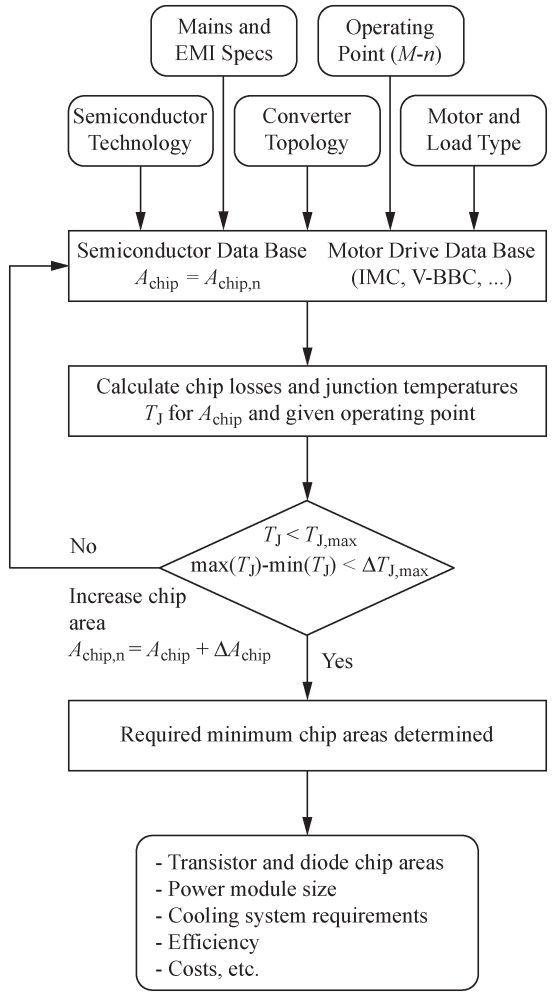

Fig. 19. Simplified flowchart of the SABC.

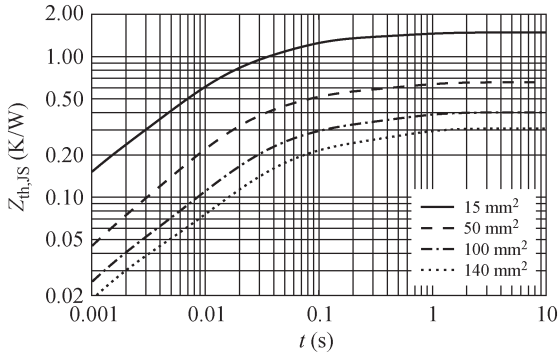

Fig. 20. Transient thermal impedance $Z_{\mathrm{th,JS}}$ for various chip areas and a CSPI of 11 $\mathrm{W/(Kdm^3)}$, calculated with the semiconductor module model.

safe shutdown, when an over-current limit at 200% of the respective nominal converter output current is assumed.

D. Semiconductor Models

The required semiconductor loss and chip size data of the IGBT4 devices and EmCon4 diodes are determined based on a statistical analysis of power module data sheets and manufacturer data. The extracted data are related to a set of voltage-, current-, chip-area-, and temperature-dependent semiconductor loss equations (cf., [18, Sec. 4]).

1) Conduction Losses: The instantaneous transistor and diode conduction losses $p_{\mathrm{cond},S/D}$ are modeled with an active chip area $A_{S/D,\mathrm{chip,act}}$ and junction temperature T_J dependent forward voltage drop $U_{S/D,F}$ and a differential forward resistance $r_{S/D,F}$, leading to

$$p_{S/D,\mathrm{cond}} = U_{S/D,F}(A_{S/D,\mathrm{chip,act}}, T_J) \cdot i_{S/D} + r_{S/D,F}(A_{S/D,\mathrm{chip,act}}, T_J) \cdot i_{S/D}^2 \quad (44)$$

where $i_{S/D}$ denotes the instantaneous transistor or diode current.

2) Switching Losses: The instantaneous transistor or diode switching losses $p_{S/D,\mathrm{sw}}$ are calculated based on switching loss energy functions of the transistor or diode $w_{S/D,\mathrm{tot}}$. These switching loss energy functions model the loss energies of an entire switching cycle (turn-on and turn-off) depending on the active chip area $A_{S/D,\mathrm{chip,act}}$, the switched current $i_{S/D}$, the switched voltage $u_{S/D}$, and the junction temperature T_J. For the transistors, the turn-on and turn-off losses are considered, whereas for the diodes, only the reverse-recovery (turn-off) losses are modeled

$$p_{S/D,\mathrm{sw}} = f_{\mathrm{sw}} \cdot w_{S/D,\mathrm{tot}}(A_{S/D,\mathrm{chip,act}}, i_{S/D}, u_{S/D}, T_J). \quad (45)$$

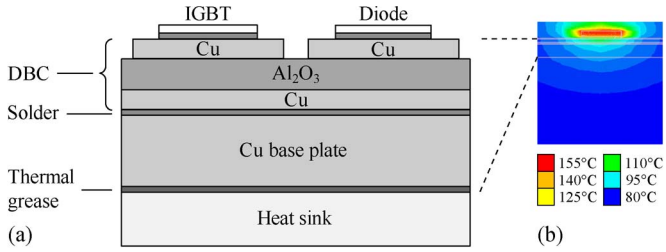

Fig. 21. (a) Cross section of the semiconductor module assembly considered. (b) Typical thermal FEM simulation result of a single chip for the module assembly at the left, showing the heat spreading.

E. Semiconductor Module

1) Module Assembly: In order to determine the thermal impedance between the semiconductor junction and the heat sink, a well-defined thermal interface between the chip and the heat sink and/or power the power semiconductor module construction is required. A model of a semiconductor module is developed for that purpose, inspired by the EconoPACK3 from Infineon. The cross section of the selected module assembly is shown in Fig. 21.

2) Thermal Impedance: The dependence of the thermal impedance $Z_{\mathrm{th,JS}}$ between the semiconductor junction and the heat sink on the total chip area is determined by transient thermal simulations with the simulation software ICEPAK. It is shown in [31] that, for an optimized custom-made aluminum heat sink with forced air-cooling, a cooling system performance index (CSPI) between 10 and 12 $\mathrm{W/(Kdm^3)}$ can be implemented with a justifiable manufacturing expenditure. Assuming an average CSPI of 11 $\mathrm{W/(Kdm^3)}$, the specific thermal power

TABLE VII
SEMICONDUCTOR MODULE AND GATE DRIVER MODEL PARAMETERS

Quantity	Parameters and Ranges of Validity
Height of the power module	$h_{\mathrm{SM}} = 15\,\mathrm{mm}$
Density of the power module	$\rho_{\mathrm{SM}} = 2.4\,\mathrm{g/cm^3}$
Ratio of chip-to-base-plate area	$\xi_{\mathrm{A_{chip\text{-}SM}}} = 0.15$
Volume of a gate driver	$V_{\mathrm{drv}} = 8\,\mathrm{cm^3}$
Mass of a gate driver	$m_{\mathrm{drv}} = 20\,\mathrm{g}$
Constraints	$A_{S,\mathrm{chip,act}} = 2\,\mathrm{mm^2} \ldots 150\,\mathrm{mm^2}$
	$f_{\mathrm{sw}} = 1\,\mathrm{kHz} \ldots 300\,\mathrm{kHz}$

flow through the heat sink cooling surface can be calculated and is then used to define the boundary conditions required for the thermal simulations. The resulting thermal impedance curves, shown in Fig. 20, are approximated with fourth-order RC foster networks and interpolated with chip-area-dependent functions as the thermal impedance is inversely proportional to the total chip area. The functions for $R_{1\ldots4,\mathrm{th,JS}}$ and $\tau_{1\ldots4,\mathrm{th,JS}}$, the step response, i.e., the transient thermal impedance between the junction and the heat sink, can be expressed as a function of the chip area by solving the differential equation resulting from the RC network and substitution

$$Z_{\mathrm{th,JS}}(A_{\mathrm{chip}}, t) = \sum_{i=1}^{4} R_{i,\mathrm{th,JS}} \left(1 - e^{\frac{-t}{\tau_{i,\mathrm{th,JS}}}}\right). \tag{46}$$

3) Volume and Mass: The total required semiconductor chip area of a power electronic converter can be used to determine the volume of its semiconductor module. The ratio $\xi_{A_{\mathrm{chip-SM}}}$ between the total implemented chip area of a semiconductor module $A_{\mathrm{chip,SM}}$ and the area of the base plate A_{SM} needs to be determined for that purpose. Considering commercial power modules, a realistic value for $\xi_{A_{\mathrm{chip-SM}}}$ is found to be 15%. Assuming a constant height of the semiconductor module of $h_{\mathrm{SM}} = 15$ mm, the volume of the module can then be calculated by

$$V_{\mathrm{SM}} = \frac{A_{\mathrm{chip,SM}}}{\xi_{A_{\mathrm{chip-SM}}}} \cdot h_{\mathrm{SM}}. \tag{47}$$

Finally, the mass of the semiconductor module can be estimated by the average density ρ_{SM} found for commercial power modules

$$m_{\mathrm{SM}} = V_{\mathrm{SM}} \cdot \rho_{\mathrm{SM}} = \frac{A_{\mathrm{chip,SM}}}{\xi_{A_{\mathrm{chip-SM}}}} \cdot h_{\mathrm{SM}} \cdot \rho_{\mathrm{SM}}. \tag{48}$$

The main semiconductor module model parameters are compiled in Table VII.

F. Gate Driver

The SABC also enables the estimation of the losses of the gate driver as the active transistor chip area $A_{S,\mathrm{chip,act}}$ is proportional to the gate charge. With a difference between the maximum and minimum gate–emitter $U_{\mathrm{GE/S,max}} = +15$ V and $U_{\mathrm{GE/S,min}} = -3$ V and a switching frequency f_{sw}, for a given gate charge Q_G, the losses generated in the gate resistor can be calculated by

$$P_G = Q_G(U_{\mathrm{GE/S,max}} - U_{\mathrm{GE/S,min}}) f_{\mathrm{sw}} \tag{49}$$

$$Q_G = 6.5\ \frac{\mathrm{nC}}{\mathrm{mm^2}} A_{S,\mathrm{chip,act}} + 4.5\ \mathrm{nC}. \tag{50}$$

The losses in the gate resistor can be utilized to estimate the resulting gate driver losses P_{drv}. A model of a gate driver circuit is developed for that purpose, comprising an H-bridge oscillator and a transformer for the galvanically isolated gate driver power supply, a magnetic coupler for the gate signal isolation, and a gate driver IC with a half-bridge MOSFET output stage. The power consumption of the driver IC is derived from the IXDN4xx gate driver series from IXYS and is verified with the results of gate driver power consumption measurements. The overall power consumption of a gate driver may then be approximated by the empirical equation

$$P_{\mathrm{drv}} \approx \frac{P_G}{0.053 \ln\left(\frac{1}{\mathrm{Hz}} f_{\mathrm{sw}}\right) + 0.074} + 0.1\ \mathrm{W} \tag{51}$$

derived in [18] and thus can be expressed with (49) as a function of the active chip area and the switching frequency (the constant term of 0.1 W accounts for the standby losses of the gate driver).

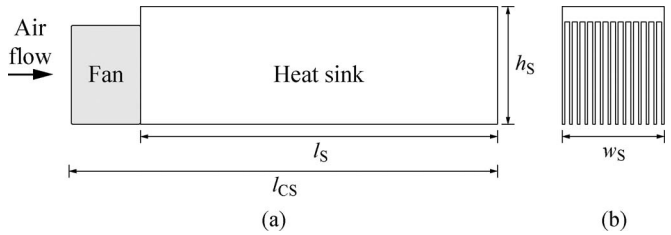

Fig. 22. (a) Schematic profile and (b) cross section of a heat sink element, showing the dimensions and the direction of the air flow.

G. Cooling System

1) Heat Sink Profile: The cooling system design aims for a simple and compact construction with an average CSPI of 11 $\mathrm{W/(Kdm^3)}$ as assumed for the simulation of the semiconductor module (cf., Section V-E). The demanded characteristics can be achieved with a forced air-cooled optimized aluminum heat sink as suggested in [32]. The schematic profile and the cross section of a single heat sink element are shown in Fig. 22.

Such a heat sink element consists of a high-performance 12-V dc fan from Sanyo Denki (SanAce 40, GA-series) and a custom-made aluminum heat sink with a variable length l_S, a width $w_S = 40$ mm, and a height $h_S = 46$ mm. Depending on the cooling requirements and the base plate area of the semiconductor module, n_S heat sink elements are arranged in parallel, thus forming a heat sink to obtain the required thermal resistance of the cooling system. The components and dimensions of the designed cooling system are summarized in Table VIII.

2) Thermal Resistance: The thermal resistance of the cooling system between the heat sink and the ambient air $R_{\mathrm{th,CS}}$ is

TABLE VIII
COOLING SYSTEM MODEL PARAMETERS

Quantity	Parameters
Thermal resistance $R_{\mathrm{th,CS}}$	$k_{1,R_{\mathrm{CS}}} = 1.50 \cdot 10^{-4}\,\mathrm{K/(W\,mm)}$
	$k_{2,R_{\mathrm{CS}}} = -8.86 \cdot 10^{-2}\,\mathrm{K/W}$
	$k_{3,R_{\mathrm{CS}}} = 21.01\,\mathrm{K\,mm/W}$
Volume V_{CS}	$k_{1,V_{\mathrm{CS}}} = 4.60 \cdot 10^{-2}\,\mathrm{cm^3/mm^2}$
	$k_{2,V_{\mathrm{CS}}} = -1.68 \cdot 10^{-1}\,\mathrm{cm^3/mm}$
Mass m_{CS}	$k_{1,m_{\mathrm{CS}}} = 5.33 \cdot 10^{-2}\,\mathrm{g/mm^2}$
	$k_{2,m_{\mathrm{CS}}} = -3.20 \cdot 10^{-1}\,\mathrm{g/mm}$
	$k_{3,m_{\mathrm{CS}}} = 18.4\,\mathrm{g}$
Fan power consumption	$P_{\mathrm{CS}} = 5.9\,\mathrm{W} \cdot n_{\mathrm{S}}$
Constraints	$l_{\mathrm{CS}} = 100\,\mathrm{mm} \ldots 280\,\mathrm{mm}$
	$n_S = 1 \ldots 7$

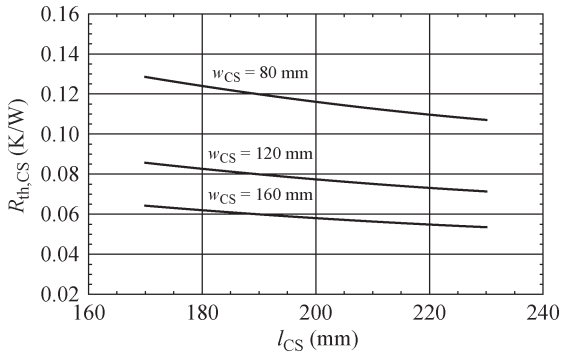

Fig. 23. Thermal resistance $R_{\mathrm{th,CS}}$ of the cooling system depending on its length l_{CS} and width w_{CS}.

determined according to [32, eqs. (11)–(14)]. The heat sink (cf., Fig. 22) is modeled by the thermal resistance of the base plate, the fins, and the interface between the fin surface and the air flow through the heat sink. The resulting thermal resistance of the cooling system $R_{\mathrm{th,CS}}$ can then be represented as a function of the length l_{CS} and width w_{CS} of the cooling system. In Fig. 23, the thermal resistance of the designed cooling system is plotted as a function of its length

$$R_{\mathrm{th,CS}} = \left(k_{1,R_{\mathrm{CS}}} l_{\mathrm{CS}}^2 + k_{2,R_{\mathrm{CS}}} l_{\mathrm{CS}} + k_{3,R_{\mathrm{CS}}}\right) \cdot \frac{1}{w_{\mathrm{CS}}}. \quad (52)$$

3) Volume and Mass: The volume of the cooling system V_{CS} is the boxed volume of the heat sink and the fans and is modeled using the length l_{CS} and width w_{CS} of the cooling system

$$V_{\mathrm{CS}} = \left(k_{1,V_{\mathrm{CS}}} l_{\mathrm{CS}} + k_{2,V_{\mathrm{CS}}}\right) \cdot n_S\, w_S. \quad (53)$$

Using the density of aluminum and the mass of a fan, the total mass of the cooling system m_{CS} can be calculated with the length l_{CS} and width w_{CS} of the cooling system

$$m_{\mathrm{CS}} = \left(k_{1,m_{\mathrm{CS}}} l_{\mathrm{CS}} + k_{2,m_{\mathrm{CS}}}\right) \cdot n_S w_S + k_{3,m_{\mathrm{CS}}}. \quad (54)$$

H. Protection Concepts and Semiconductor Requirements

All converters should enable a controlled emergency stop of the drive, even in case of mains phase loss. In order to meet this requirement, the V-BBC has to be implemented with a brake chopper connected across the dc-link capacitor. Additional protection circuitry, ideally integrated with the auxiliary supply, is necessary for the CMC and IMC. Thereby, it is assumed that the auxiliary supply is implemented with a three-phase diode rectifier that is connected to the input phases and thus provides a dc-bus voltage of approximately $U_{\mathrm{aux}} = \sqrt{6}U_1$. In order to provide a path for the motor currents during mains phase loss, for the CMC, an additional three-phase diode rectifier needs to be connected between the output phases and the dc input U_{aux} of the auxiliary supply [33], [34]. The IMC requires only two additional power diodes that are connecting the rails of the intermediate link to the dc input of the auxiliary supply [35]. In order to provide a similar protection capability for the CMC and IMC, the three-phase diode rectifiers at the input and output of the CMC are implemented by utilizing the same total chip area as is required for the freewheeling diodes of the output stage of the IMC. The two protection diodes of the IMC are dimensioned for the resultant nominal link current. A brake chopper [33], [36] is connected across the dc-bus of the auxiliary supply in a similar manner as that for the V-BBC. The chopper IGBTs of all converter topologies are dimensioned for a continuous current that is equal to the peak output current.

TABLE IX
PARAMETER OVERVIEW OF THE AUXILIARY COMPONENTS

Quantity	Parameters
Power of the control hardware	$P_{\mathrm{ctrl}} = 8\,\mathrm{W}$
Volume of the control hardware	$V_{\mathrm{ctrl}} = 50\,\mathrm{cm^3}$
Mass of the control hardware	$m_{\mathrm{ctrl}} = 100\,\mathrm{g}$
Efficiency of the auxiliary supply	$\eta_{\mathrm{aux}} = 80\%$
Volume of the auxiliary supply	$V_{\mathrm{aux}} = 200\,\mathrm{cm^3}$
Mass of the auxiliary supply	$m_{\mathrm{aux}} = 150\,\mathrm{g}$

VI. AUXILIARY COMPONENTS

A. Control and Measurement

The control and measurement hardware includes a DSP, a FPGA, and analog and digital circuitries. The main system quantities that need to be measured are the following:

1) for the CMC/IMC, the input voltages u_a, u_b, and u_c; the dc input voltage of the auxiliary supply u_{aux}; and the output currents i_A, i_B, and i_C;
2) for the V-BBC, the three input voltages u_a, u_b, and u_c; the dc-link voltage u_{DC}; the input currents i_a, i_b, and i_c; and the output currents i_A, i_B, and i_C.

Additionally, for all topologies, the motor speed is sensed, and the base plate temperature of the semiconductor module, the motor temperature, and the operating state of the auxiliary supply and the fans are monitored. The data of the power consumption, the boxed volume, and the weight are acquired from the implemented hardware prototypes [7], [35], [36] with a TMS320F2808 DSP (Texas Instruments), a MachXO FPGA (Lattice), and magnetoresistive current sensors (CDS4000-series, Sensitec) and are compiled in Table IX.

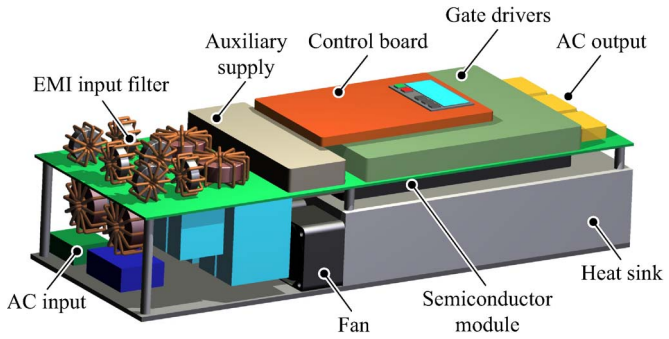

Fig. 24. Three-dimensional conceptual drawing of an IMC, showing the components modeled and the layout considered.

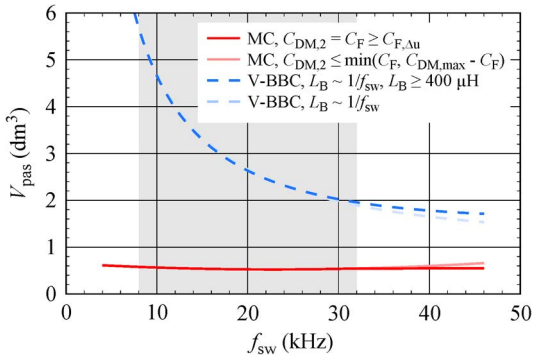

Fig. 25. Volume of the passive components (without heat sink) $V_{\rm pas}$ versus the switching frequency $f_{\rm sw}$ of the MC (CMC/IMC) and V-BBC for different filter designs (cf., Section IV). The gray shaded area indicates the switching frequency range considered from $f_{\rm sw} = 8$–32 kHz.

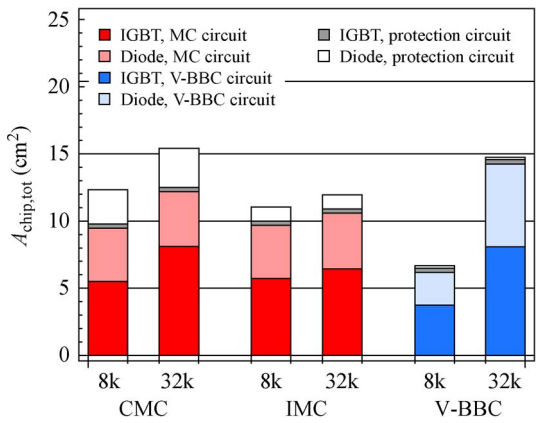

Fig. 26. Required total semiconductor chip area $A_{\rm chip,tot}$ of the CMC, IMC, and V-BBC for $T_{J,\max} \leq 140$ °C, $\Delta T_{J,\rm nom} \leq 10$ K, $T_S = 95$ °C, and $f_{\rm sw} = \{8, 32\ \text{kHz}\}$.

B. Auxiliary Supply

An isolated auxiliary supply with a wide input voltage range (e.g., 200–900 V) is considered to provide the voltage for the fans of the cooling system, the gate drivers, and the control board. The required input power can be calculated by

$$P_{\rm aux} = (P_{\rm CS} + P_{\rm drv,tot} + P_{\rm ctrl})\frac{1}{\eta_{\rm aux}} \tag{55}$$

and is supplied via a three-phase diode rectifier that is connected to the DM capacitors $C_{\rm DM,1} = C_F$ of the input filter. The key data can be found in Table IX.

VII. Comparative Evaluation

In this section, the results of the comparative evaluation of the CMC, IMC, and V-BBC for a 15-kVA drive system with a PMSM for switching frequencies of 8 and 32 kHz are introduced by applying the models, the design equations, and the optimization concepts derived in the previous sections. The results of this comparison are used subsequently to provide a comprehensive and unbiased evaluation of the three converter concepts for low-voltage and low-power applications (≤ 100 kW), which is supported by various experimental results [18], [35], [37]. Fig. 24 shows, as an example, the construction considered and the components modeled for an IMC.

A. Volume of Passive Components

In a first step, the boxed volumes of the passive components for the MC and the V-BBC are compared in Fig. 25 as a function of the switching frequency for the passive component introduced and EMI input filter design guidelines from Section IV to meet the CE noise levels for CISPR 11 class B. Two options are shown for both converter concepts. The input filter of the MC is designed by using the maximum amount of DM capacitance $C_{\rm DM,2} = C_F = C_{\rm DM,max}/2$ (cf., gray shaded area in Fig. 14) or just the amount required by the voltage ripple criterion to minimize the reactive current drawn by the filter with $C_{\rm DM,2} = C_F \leq C_{\rm DM,max}/2$ (cf., hatched area in Fig. 14). Correspondingly, the input filter for the V-BBC is calculated with and without restricting the boost inductance to a minimum value $L_{B,\min}$. Within the switching frequency range of 8 to 32 kHz, the two design methods considered hardly affect the total volume of the passive components, and thus, the DM filter capacitors of the MC can be designed according to the voltage ripple criterion to reduce the reactive power.

In conclusion, the boxed volume of the passive components with or without the cooling system of the MC (CMC or IMC) is approximately ten times smaller at $f_{\rm sw} = 8$ kHz and approximately 3.5 times smaller at $f_{\rm sw} = 32$ kHz compared to the V-BBC. It is important to note that increasing the switching frequency for the MC leads to a reduction of the filter volume only up to $f_{\rm sw} \approx 23$ kHz, which occurs mainly as a result of the limitation of the maximum DM capacitance per phase of $C_{\rm DM,max} = 45\ \mu$F. Contrary to the MC, the total volume of the passive components of the V-BBC steadily decreases for increasing switching frequencies over the whole switching frequency range considered as the total volume is mainly dominated by the volume of the boost inductors, which scales with the inverse of the switching frequency due to the applied current ripple criterion.

B. Semiconductor Chip Area

Fig. 26 shows the required semiconductor chip area, split into the chip area used for the main power circuit and protection, such that the maximum junction temperature does not exceed

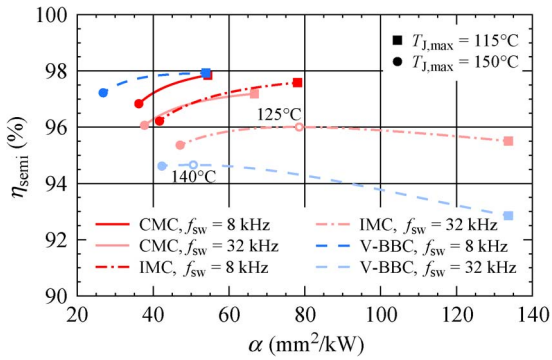

Fig. 27. Achievable efficiency considering only the semiconductor losses η_{semi} versus the chip area per output power α evaluated for $T_{J,\max} = 115\ ^\circ\text{C}{-}150\ ^\circ\text{C}$, $T_S = 95\ ^\circ\text{C}$, and $f_{\text{sw}} = \{8, 32\ \text{kHz}\}$.

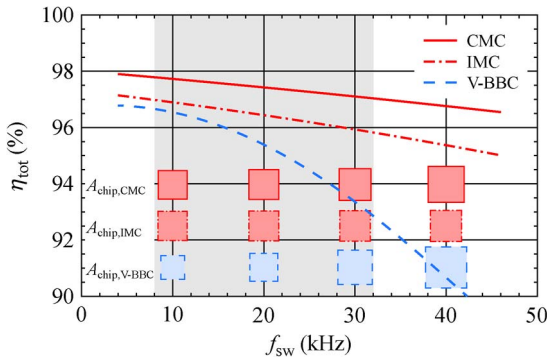

Fig. 28. Total converter efficiency versus switching frequency for $T_{J,\max} \leq 140\ ^\circ\text{C}$, $\Delta T_{J,\text{nom}} \leq 10$ K, and $T_S = 95\ ^\circ\text{C}$. The required chip areas without protection hardware are shown at $f_{\text{sw}} = \{10, 20, 30, 40\ \text{kHz}\}$.

$T_{J,\max} \leq 140\ ^\circ\text{C}$ and the maximum cyclic junction temperature variation is limited to $\Delta T_{J,\max} \leq 10$ K for both nominal motor operation (OP1) and nominal generator operation (OP5) at $f_{\text{sw}} = 8$ kHz and $f_{\text{sw}} = 32$ kHz (cf., considerations regarding the semiconductor lifetime in Section V). The CMC as well as the IMC requires a total Si chip area of $A_{\text{chip,tot}} = 11{-}15\ \text{cm}^2$ for $f_{\text{sw}} = 8{-}32$ kHz, whereby the CMC uses typically 15% more chip area compared to the IMC. On the contrary to the MCs, the V-BBC requires a total Si chip area of only $A_{\text{chip,tot}} = 7\ \text{cm}^2$ at 8 kHz but $A_{\text{chip,tot}} = 15\ \text{cm}^2$ at $f_{\text{sw}} = 32$ kHz similar to the MCs. In consequence, at low switching frequencies, the V-BBC is the most advantageous topology with regard to the semiconductor expenditure and, in general, has the best ratio of the installed chip area in the power circuit with respect to the chip area required for the protection circuitry, followed by the IMC and the CMC.

C. Efficiency Versus Chip Area per Output Power

The dependence of the resulting efficiency, considering only the semiconductor losses on the chip area per output power α, is shown in Fig. 27, evaluated at a sink temperature beneath the power module of $T_S = 95\ ^\circ\text{C}$ and switching frequencies of $f_{\text{sw}} = 8$ kHz and $f_{\text{sw}} = 32$ kHz when the maximum junction temperature is varied between $T_{J,\max} = 115\ ^\circ\text{C}{-}150\ ^\circ\text{C}$. $T_{J,\max}$ is controlled by changing the chip areas of the individual semiconductors without restricting $\Delta T_{J,\max}$.

Two key results can be extracted: the V-BBC enables the lowest chip area per output power α at $f_{\text{sw}} = 8$ kHz and is comparable to the CMC at $f_{\text{sw}} = 32$ kHz. Both the IMC and the V-BBC (topologies with two-level voltage source input and/or output stage) show a decrease in the efficiency at $f_{\text{sw}} = 32$ kHz when the junction temperature is reduced, and thus, the chip area is increased. This is due to the fact that the reduction in conduction losses is overcompensated by the contribution of the capacitive switching losses due to the large chip area.

D. Total Efficiency Versus Switching Frequency

Next, the total efficiency, including the losses of the semiconductors, all passive components, the fans, the gate drivers, the control and measurement hardware, and the auxiliary supply, is evaluated as a function of the switching frequency. The semiconductor chip areas are again designed such that the maximum junction temperature is limited to $T_{J,\max} \leq 140\ ^\circ\text{C}$ and/or the maximum junction temperature variation at $f_{2,\text{nom}}$ is limited to $\Delta T_{J,\max} \leq 10$ K for both nominal motor operation (OP1) and generator operation (OP5). The calculated efficiency curves are shown in Fig. 28, and the resultant efficiency values evaluated at $f_{\text{sw}} = 8$ kHz and $f_{\text{sw}} = 32$ kHz are summarized in Table X.

TABLE X
TOTAL EFFICIENCIES FOR NOMINAL MOTOR OPERATION (OP1) AT $T_{J,\max} \leq 140\ ^\circ\text{C}$, $\Delta T_{J,\max} \leq 10$ K, AND $T_S = 95\ ^\circ\text{C}$

Converter Topology	η_{nom} at 8 kHz	η_{nom} at 32 kHz
CMC	97.8%	97.0%
IMC	97.0%	95.8%
V-BBC	96.7%	92.9%

At $f_{\text{sw}} = 8$ kHz, the IMC as well as the V-BBC allows for approximately the same total efficiency $\eta_{\text{tot,CMC}} \approx \eta_{\text{tot,V-BBC}} \approx 97\%$. The achievable efficiency with the CMC is higher compared to the IMC or V-BBC within the considered switching frequency range; at $f_{\text{sw}} = 8$ kHz, the CMC reaches 97.8% compared with 97.0% of the IMC and 96.7% of the V-BBC, and at $f_{\text{sw}} = 32$ kHz, the CMC reaches 97.0% compared with 95.8% of the IMC and 92.9% of the V-BBC. The lower efficiency of the IMC compared to the CMC mainly results from its higher conduction losses as, in the IMC topology, always three semiconductor devices are in the current paths between the input and output terminals compared to only two in the CMC topology.

The higher efficiency of the CMC and IMC compared to the V-BBC (particularly at higher switching frequencies) is enabled by the lower commutation voltage of the MCs, which is approximately two thirds of the commutation voltage of the V-BBC for the selected dc-link voltage of $U_{\text{DC}} = 700$ V, and the ZCS strategy of the input stage of the IMC. The efficiency of the V-BBC for switching frequencies below 10 kHz is limited primarily by the copper losses of the boost inductors. Thus, by using boost inductors with a lower rms current density value than 6 A/mm^2, the V-BBC can reach almost the same efficiency as the CMC at 4 kHz and a higher efficiency than the IMC below 10 kHz.

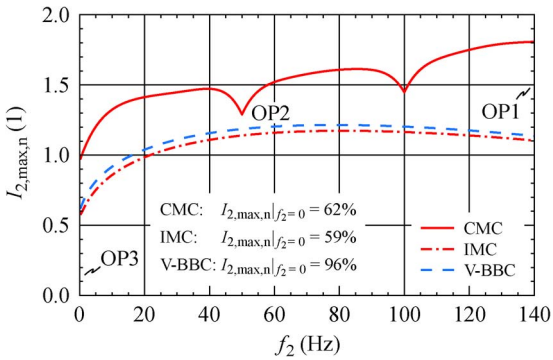

Fig. 29. Normalized output current versus electrical output frequency such that $T_{J,\max} = 140$ °C and $T_S = 95$ °C $\Rightarrow \Delta T_{J,\max} \leq 45$ K, and $f_{\rm sw} = 8$ kHz. The considered chip areas can be found in Fig. 26.

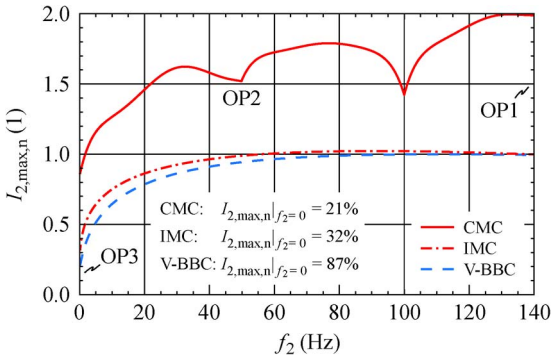

Fig. 30. Normalized output current versus the electrical output frequency such that $T_{J,\max} = 140$ °C, $T_S = 95$ °C $\Rightarrow \Delta T_{J,\max} \leq 45$ K, and $f_{\rm sw} = 32$ kHz. The considered chip areas can be found in Fig. 26.

E. Output Current Versus Output Frequency

The available output current I_2 for a given output frequency f_2 under the specified thermal constraints of the junction temperature is of particular importance for the characterization of ac-ac converters for drive applications. The normalized maximum output current for that purpose

$$I_{2,\max,n} = \frac{I_{2,\max}}{I_{2,\rm nom}} \tag{56}$$

which is proportional to the motor torque, is shown in Figs. 29 and 30 versus the output frequency for $f_{\rm sw} = 8$ kHz and $f_{\rm sw} = 32$ kHz such that $T_{J,\max} \leq 140$ °C and $T_S = 95$ °C. This means that the peak-to-peak junction temperature variation due to the modulation of the semiconductor losses with the electrical input and/or output frequency is limited to $\Delta T_{J,\max} \leq 45$ K. The semiconductor chip areas are again designed as previously specified and visualized in Fig. 26 for nominal operation at $f_{2,\rm nom} = \pm 140$ Hz.

The modulation index of the converter system is reduced in proportion to the output frequency for the PMSM load being considered from 90% at 140 Hz to 2% at standstill. When the output frequency is lowered, the modulation frequency of the semiconductor losses is also decreased (or changes), whereas the thermal time constant of the semiconductor chips remains obviously invariant. This leads to a higher $\Delta T_{J,\max}$, and thus, the output current has to be decreased to maintain the specified thermal constraints. The IMC and V-BBC feature a similar derating of the output current for $f_{\rm sw} = 8$ kHz and $f_{\rm sw} = 32$ kHz when the output frequency is decreased to zero as both topologies have the same output stage topology and generate conduction and switching losses in the output stage (for the selected discontinuous modulation schemes, cf., Section II and [6]). The maximum available output current of the IMC and V-BBC slightly exceeds the nominal output current above 30 Hz, while the thermal constraints of the semiconductors are still fulfilled. This is due to the variation of the modulation index which leads to a different loading of the transistors and diodes compared to OP1 and OP5 and the margin of the peak junction temperature to $T_{J,\max} = 140$ °C (cf., Fig. 18) and thus allows for an output current above the nominal current level (cf., Figs. 29 and 30).

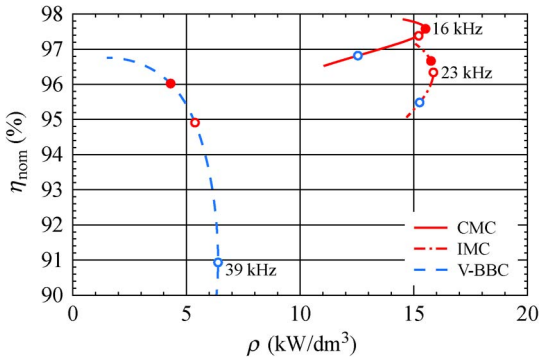

Fig. 31. Total converter efficiency for nominal motor operation (OP1) $\eta_{\rm nom}$ versus power density ρ for $T_{J,\max} \leq 140$ °C, $\Delta T_{J,\rm nom} \leq 10$ K, $T_S = 95$ °C, and $f_{\rm sw} = 4-46$ kHz.

The semiconductor losses of the CMC are modulated with the input frequency f_1 and the output frequency f_2, and the phase angle between the input and output currents due to the missing dc-link. Thus, the CMC shows a significantly different derating curve compared to the IMC and V-BBC, with dips in the available output current at 50 and 100 Hz. If $f_1 \approx f_2$, the loading of the individual semiconductors is modulated with $|f_1| - |f_2| \approx 0$ (beating effect). The most critical operating points (OP2/OP4) occur at $f_2 = \pm f_1$, which may be considered as equivalent to the electrical standstill condition of a V-BBC for the semiconductor losses of the CMC. In particular, for drive systems that are mainly operated at $f_2 \approx f_1$, a careful thermal design of the semiconductors is mandatory in order not to limit the semiconductor lifetime of the CMC. The CMC can provide the highest available output current (torque) particularly at $f_2 = 0$ Hz (OP3) as the semiconductor losses are modulated with $|f_1| - |f_2| = f_1$, and thus, it prevents a strong loading of single semiconductors compared with the output stage of the IMC and V-BBC but requires also the largest semiconductor chip area for the switching frequency range of interest from 8 to 32 kHz.

F. Efficiency, Power Density, and Power-to-Mass Ratio

In Figs. 31–33, the tradeoff between the total efficiency at nominal motor operation (OP1) $\eta_{\rm nom}$, the achievable power density ρ, and the resultant power-to-mass ratio γ are shown

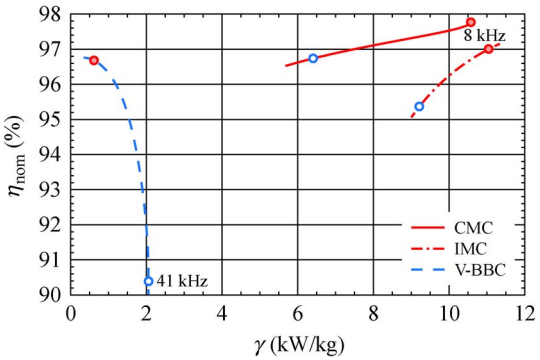

Fig. 32. Total converter efficiency for nominal motor operation (OP1) $\eta_{\rm nom}$ versus power-to-mass ratio γ for $T_{J,\max} \leq 140\,^{\circ}$C, $\Delta T_{J,\rm nom} \leq 10$ K, $T_S = 95\,^{\circ}$C, and $f_{\rm sw} = 4{-}46$ kHz.

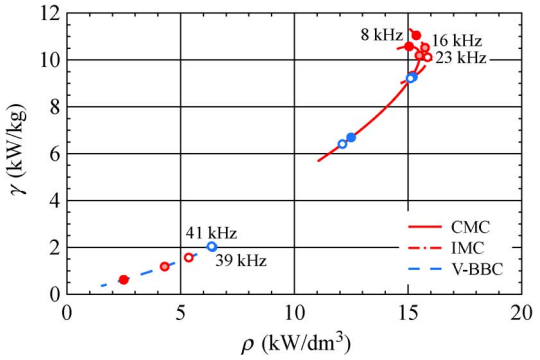

Fig. 33. Power-to-mass ratio γ versus power density ρ for $T_{J,\max} \leq 140\,^{\circ}$C, $\Delta T_{J,\rm nom} \leq 10$ K, $T_S = 95\,^{\circ}$C, and $f_{\rm sw} = 4{-}46$ kHz, indicating all optima as a function of the switching frequency.

for the considered design guidelines. The switching frequency range is within 4 and 46 kHz.

The CMC and IMC enable a 2.5 times higher maximum power density at a nominal efficiency of 97.6% at $f_{\rm sw} \approx 16$ kHz for the CMC and 96.3% at $f_{\rm sw} \approx 23$ kHz for the IMC compared to 90.9% at $f_{\rm sw} = 39$ kHz for the V-BBC. The achievable power density decreases for the CMC and IMC for lower switching frequencies, as shown in Fig. 31. This occurs mainly due to the limitation of $C_{\rm DM,max}$, which leads to a relative increase of the input filter volume compared to the required attenuation as a larger amount of DM inductance with a higher volumetric scaling than that for the DM capacitors (cf., Figs. 5 and 7) is required. A similar result is obtained when comparing the maximum power-to-mass ratio in Fig. 32, which is five times higher for the CMC and IMC than that for the V-BBC at a difference of the nominal efficiency of approximately 97.8% for the CMC and 97.2% for the IMC compared to 90.4% for the V-BBC. The optimal power-to-mass ratio for the MCs occurs at low switching frequencies, whereas for the V-BBC, it is found at $f_{\rm sw} = 41$ kHz as a result of the reduction in boost inductance with increasing switching frequency and, therewith, a reduction of the mass of the inductors.

G. Overview of Performance Indicators

Finally, the resultant main properties of the CMC, IMC, and V-BBC are shown in Figs. 34 and 35 with nine characteristic

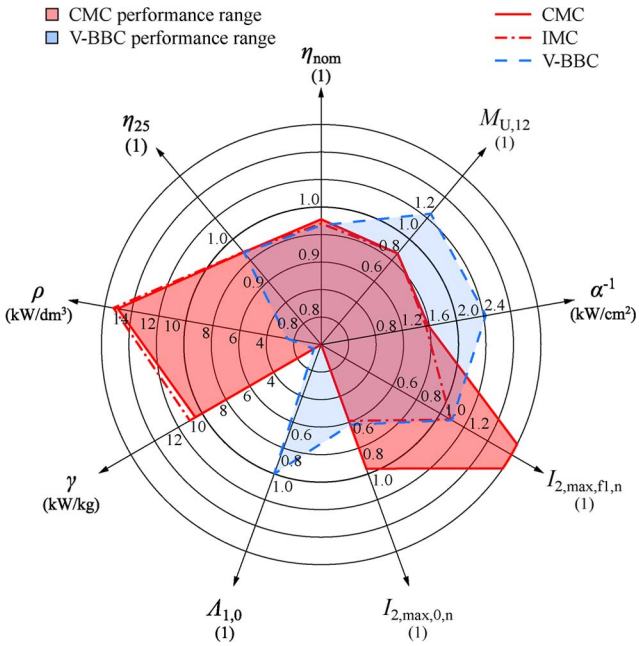

Fig. 34. Comparison of the CMC, IMC, and V-BBC with performance indicators for $T_{J,\max} \leq 140\,^{\circ}$C, $\Delta T_{J,\max} \leq 10$ K, $T_S = 95\,^{\circ}$C, and $f_{\rm sw} = 8$ kHz.

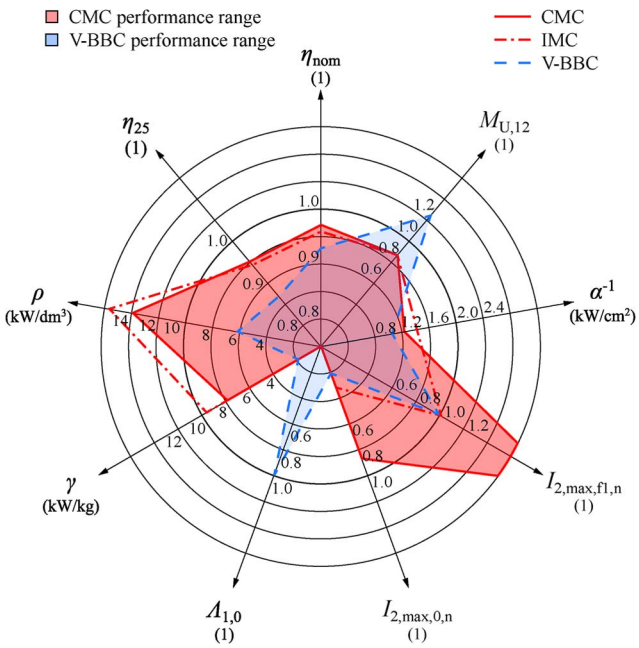

Fig. 35. Comparison of the CMC, IMC, and V-BBC with performance indicators for $T_{J,\max} \leq 140\,^{\circ}$C, $\Delta T_{J,\max} \leq 10$ K, $T_S = 95\,^{\circ}$C, and $f_{\rm sw} = 32$ kHz.

performance indicators for a switching frequency of 8 and 32 kHz. The following measures are defined for that purpose.

1) Voltage Transfer Ratio:

$$M_{U,12} = \frac{U_{2,\max}}{U_1}. \tag{57}$$

The dc-link voltage of the V-BBC is assumed with $U_{\rm DC} = 700$ V. U_1 and U_2 denote the rms value of the input and output line voltages.

2) Nominal Efficiency at OP1:

$$\eta_{\rm nom} = \frac{P_{2,\rm nom}}{P_{2,\rm nom} + P_{\rm loss,nom}} \tag{58}$$

at a modulation index for the MCs of $M_{12} = 0.9$ and a modulation index for the output stage of the V-BBC of $M_2 = U_2\sqrt{6}/U_{\rm DC} = 0.9$.

3) Efficiency at 25% of the Nominal Output Power for Motor Operation:

$$\eta_{25} = \frac{P_{2,25}}{P_{2,25} + P_{\rm loss,25}} \quad I_{2,25} = \frac{1}{2} \cdot I_{2,\rm nom} \tag{59}$$

at half of the nominal output current $I_{2,25}$, a modulation index for the MCs of $M_{12} = 0.45$, and a modulation index for the output stage of the V-BBC of $M_2 = 0.45$.

4) Power Density:

$$\rho = \frac{P_{2,\rm nom}}{V_{\rm tot}}. \tag{60}$$

$V_{\rm tot}$ accounts for the total boxed volume of the passive components, the cooling system, the semiconductor module, the gate drivers, the control and measurement hardware, and the auxiliary supply (cf., Fig. 24).

5) Power-to-Mass Ratio:

$$\gamma = \frac{P_{2,\rm nom}}{m_{\rm tot}}. \tag{61}$$

$m_{\rm tot}$ is equal to the total mass of the passive components, the cooling system, the semiconductor module, the gate drivers, the control and measurement hardware, and the auxiliary supply.

6) Reactive Input Power Compensation Capability at Zero Apparent Output Power:

$$\Lambda_{1,0} = \left.\frac{S_1}{P_{2,\rm nom}}\right|_{S_2=0}. \tag{62}$$

S_1 and S_2 refer to the apparent input and output powers of the converter.

7) Nominal Output Power per Si Chip Area:

$$\frac{P_{2,\rm nom}}{A_{\rm chip,tot}}. \tag{63}$$

8) Maximum Output Current When the Output Frequency Is Equal to the Input Frequency:

$$I_{2,\max,f_1,n} = \left.\frac{I_{2,\max}}{I_{2,\rm nom}}\right|_{f_2=f_1}. \tag{64}$$

9) Maximum Output Current When the Output Frequency Is Equal to Zero:

$$I_{2,\max,0,n} = \left.\frac{I_{2,\max}}{I_{2,\rm nom}}\right|_{f_2=0} \tag{65}$$

such that the maximum junction temperature does not exceed $T_{J,\max} = 140$ °C at a sink temperature $T_S = 95$ °C (beneath the power module), leading to a limitation of the maximum junction temperature variation of $\Delta T_{J,\max} = 45$ K.

The performance spaces where the MC is superior to the V-BBC technology and vice versa are highlighted with the corresponding colors in the aforementioned diagrams. The area spanned by the polygon curves can be considered as a relative measure for comparison. The better the converter performance is, the larger is the area.

VIII. Conclusion

A. Main Results

In this paper, a systematic methodology and the main component models required for a holistic comparison of three-phase ac-ac converter systems have been presented and applied to perform a comparative evaluation of CMC, IMC, and V-BBC for a 15-kW PMSM drive.

All three converter systems are designed to operate on a balanced three-phase 50-Hz mains system with a nominal line-to-line voltage of 3 × 400 V (rms) and to meet the CISPR 11 (class B) EMC standard for CE and are investigated for a switching frequency range of 4–46 kHz. The converters are controlled to provide sinusoidal input currents and unity power factor at the input. The dc-link voltage $U_{\rm DC}$ of the V-BBC is assumed to be 700 V. In order to enable a fair comparison, the rated voltages of the PMSMs are matched to the respective output voltage ranges of the MC and V-BBC such that, at 90% of the maximum output voltage of the converter and at equal electrical nominal output frequency of 140 Hz, all motors deliver the same mechanical shaft power (i.e., 14.4 kW ≈ 20 hp). Si Trench and Field-Stop IGBT4 devices (1200 V) and EmCon4 diodes (Infineon) are utilized. The semiconductor chip areas are designed such that, at nominal motor/generator operation, the maximum cyclic junction temperature variation is limited to 10 K and the maximum junction temperature does not exceed 140 °C.

Within the considered switching frequency range of 4–46 kHz, the MC topologies enable a 2.5 times higher maximum power density and a five times higher maximum power-to-mass ratio at a higher efficiency of 97.6% at 16 kHz for the CMC and 96.3% at 23 kHz for the IMC compared to the V-BBC that allows for an efficiency of 90.9% at the point of maximum power density at 39 kHz (cf., Fig. 31) and an efficiency of 90.4% at the point of maximum power-to-mass ratio at 41 kHz (cf., Fig. 32). At 4 kHz, the IMC and V-BBC feature a similar nominal efficiency of approximately 97%, whereby below 10 kHz, the efficiency of the V-BBC is mainly determined by the copper losses of the boost inductors, which could be reduced. The CMC allows for the highest efficiency in the considered switching frequency range. The V-BBC requires a significantly smaller semiconductor chip area compared to the CMC and IMC for switching frequencies below 30 kHz, e.g., at 8 kHz, only 7 cm^2 compared to 12 cm^2 for the CMC and 11 cm^2 for the IMC under the considered thermal constraints, whereas above 30 kHz, the V-BBC requires the largest total chip area, followed by the CMC and the IMC.

Unfortunately, the higher achievable power density and power-to-mass ratio of MCs compared to the V-BBC within the considered switching frequency range is outweighed by the lack of desirable basic converter properties such as output voltage step-up capability, unconstrained reactive input power compensation, simple feedback control of the input currents independent of the output currents, and the possibility for single-phase operation. Consequently, the MC is not the appropriate topology for a general-purpose, flexibly configurable, bidirectional, low-voltage, and low-power ac-ac converter system. The V-BBC clearly is the preferred choice for such requirements.

B. Application Areas of MCs

Suitable application areas for the MC technology for low-voltage and low-power ($\leq$ 100 kW) systems can be identified by analyzing the performance indicators shown in Figs. 34 and 35. The MC represents a converter concept that aims at minimizing the internal energy storage. This key converter system property should be considered as an assessment criteria on whether the MC well matches its intended application. This means that, for ac-ac converter applications that require internal energy storage due to high load dynamics, single-phase operation capability, extended ride-through capability, or unconstrained reactive power compensation, the MC is not the appropriate converter concept. In addition, there should be a certain degree of freedom on the system design level to adapt the overall drive system to the MC, i.e., the nominal voltage of the motor, in order to fully exploit its benefits without restricting the performance of the drive due to the limited voltage transfer ratio of 86.6% for sinusoidal modulation.

Ideal loads for MCs require low dynamic performance and are mainly operated between 30% and 100% of their rated power level. This enables the reactive currents drawn by the filter to be compensated at a limited reduction of the available nominal output voltage ($\leq 10\%$) and/or to maintain unity power factor $\cos\Phi_1 \approx 1$ [cf., (28)] over the whole load (mission) profile of the drive. The MC enables, particularly at higher switching frequencies, better performance than the V-BBC as can be immediately seen by comparing Figs. 34 and 35 and requires, e.g., at 32 kHz, approximately the same semiconductor chip area as the V-BBC. Suitable application areas for the MC technology based on the aforementioned performance indicators are therefore the following:

1) compressors (e.g., for air conditioners and vacuum dryers);
2) fans (blowers);
3) mixers;
4) general pumps or heat pumps;
5) escalator drive systems

for 50/60-Hz mains application, where a switching frequency above the audible range (>20 kHz) is desirable.

Although MCs are often suggested as an alternative topology to the V-BBC for more electric aircraft applications with a variable frequency mains system (360–800 Hz), despite its unquestionable advantage of a high power density and power-to-mass ratio, the properties of the MCs do not provide an optimal matching with the stringent requirements of this application area. The high mains frequency and the capacitive input filter result in a high reactive input power, which can only be compensated within limits and typically at the expense of a reduction of the available output voltage. In addition, simple feedback control of the input currents independent of the load currents as with the V-BBC is not possible with the MC. A voltage-source-based converter system from this perspective, possibly with a three-level PFC input stage, is a more appropriate solution for an aircraft drive system [38], [39]. This finding is confirmed by the investigation performed in [5], where different converter topologies have been analyzed regarding their suitability for a lightweight aircraft ac-dc-ac converter system.

C. CMC Versus IMC

Most of the properties of the CMC and IMC are identical or can at least be achieved by adequate modulation and control. The major difference is found in the three-phase symmetry of the power circuit of the CMC compared to the IMC, which inherently leads to an equal average loading of all semiconductors of the CMC and thus allows for a lower semiconductor area in the power circuit (without the power semiconductors required for protection) than for the IMC. It can hence be stated that the simple commutation of the IMC due to its two-stage structure is achieved at the expense of more power devices in the current path, which results in a higher semiconductor effort and typically a lower achievable efficiency compared with the CMC.

A sort of electrical standstill condition for the CMC occurs when the output frequency is equal to the input frequency $f_2 = \pm f_1$ (OP2/OP4; cf., Fig. 17) or to a multiple of the input frequency, and thus, only a few devices conduct the load current for a comparatively long time. The available output current has to be reduced for this operating condition for a given maximum junction temperature variation $\Delta T_{J,\max}$, or a larger semiconductor chip area has to be provided (cf., Figs. 29 and 30). However, compared with the worst case of the IMC, which occurs at $f_2 = 0$, the operating conditions at $f_2 = \pm f_1$ for the CMC are less severe as the conduction intervals of the more heavily loaded power devices are still cyclically changing with the input/output frequency.

In view of the dependence between the available output current and the output frequency, the CMC should be selected for applications with a mission profile that mainly requires operation at low output frequencies (<10 Hz), ideally with a maximum output frequency of 85% of the input frequency. Correspondingly, the IMC should be applied for drives that are operated above 10 Hz. The efficiency of the IMC at part load for modulation indices below typically $M_{12} = 0.5$ is higher compared to the CMC as the output stage is then comparatively long in the freewheeling state which reduces the conduction interval and the losses of the input stage.

The IMC should be considered for part load operation or high switching frequency applications when advanced (more expensive) semiconductor devices are indispensable. Such a high-performance IMC could be built with Si IGBT and diodes in the input stage that are optimized for low conduction losses

to fully benefit from the ZCS strategy of the input stage. The six switches and diodes of the output stage could be implemented, for instance, with only six normally-on SiC JFETs (Infineon/SiCED) as they provide an integral antiparallel diode. The IMC then requires 30 power semiconductor chips (or 18 chips if RC-IGBTs are used) and has a normally-off device in all current paths between the inputs and the outputs. If the same performance should be achieved with a CMC, 18 high-speed IGBTs and 18 SiC diodes (36 chips) [40] or 18 SiC JFETs would be required.

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