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***Abstract*—An advanced synergetic charge-based mains current control (ASC) for three-phase power factor correction (PFC) buck-boost current DC-link AC/DC converters, which integrate a front-end buck-type current DC-link PFC rectifier and a DC/DC boost converter output stage, is proposed. The charge control is embedded in the synergetic (coordinated) control of the two converter stages, retaining all advantageous features such as only a minimum number of switches operating at any given time and a seamless transition between buck- and boost-mode. Compared to conventional synergetic current control (CSC) with synchronous sampling or oversampling, the ASC achieves an reduction of the AC-side current harmonics (simulated total harmonic distortion lower by up to 30 %) for operation over a wide output voltage range from 200 to 1000 V without increased implementation complexity or hardware cost. Furthermore, the ASC improves the light-load efficiency by inherently enabling a smooth transition into discontinuous conduction mode (DCM) without additional modifications of the control structure. Finally, the proposed ASC can control a system featuring significantly higher DC-link current ripples without a degradation of the grid current quality, which facilitates more compact DC-link inductor and hence converter realizations.**

***Index Terms*—Three-Phase Buck-Boost Current DC-Link PFC Rectifier System, Three-Phase Buck-Type Current Source Rectifier, Synergetic DC-Link Current Control, Charge Control, Two-Third Pulse-Width Modulation, Discontinuous Conduction Mode.**

I. Introduction

Buck-boost capability has become an essential requirement for advanced three-phase (3-Φ) AC/DC converters as a significantly increasing number of applications operate with wide input/output voltage ranges [1], [2]. As a typical example, battery charger systems for electric vehicles (EVs) must handle charging voltages from 150 V up to 1 kV as proposed in the latest CHAdeMO protocol [3]. For galvanic isolation of the charger output, a highly efficient series resonant DC/DC converter is an attractive solution but can provide only limited voltage regulation capability. Also, an isolation stage might not be present in future non-isolated EV charging systems at all [4]. In both cases, the AC/DC power factor correction (PFC) rectifier front-end must thus cover the required output voltage range. Considering the vehicle-to-grid (V2G) trend, bidirectional power flow capability is needed for EVs to serve as distributed energy storage elements supporting the grid operation [5], [6].

In recent years, extensive research has been carried out to investigate current DC-link systems [7]–[13]. In this paper, a 3-Φ bidirectional buck-boost (bB) current DC-link PFC rectifier system (see **Section III**), formed by a 3-Φ buck-type current source rectifier (CSR) stage and a subsequent boost-type DC/DC-stage, is analyzed and implemented, which offers several advantages compared to a conventional boost-type PFC rectifier approach, i.e., a reduced number of magnetic components, direct start-up capability without pre-charging of capacitor banks, and reduced losses enabled by 2/3-PWM [14], [15]. Furthermore, upcoming monolithic bidirectional power semiconductor devices will further decrease the implementation complexity [16]. A synergetic control structure for this 3-Φ bidirectional buck-boost (bB) current DC-link PFC rectifier system has been proposed in [17], [18], which achieves minimum total losses over the wide output voltage range, i.e., covering buck-mode ($\frac{3}{2}\hat{V}_{\mathrm{in}} > V_{\mathrm{out}}$), and boost-mode ($\sqrt{3}\hat{V}_{\mathrm{in}} < V_{\mathrm{out}}$) operation, by always clamping either one phase of the CSR-stage or clamping the DC/DC-stage. According to this conventional synergetic control (CSC) structure, the 3-Φ input currents are not directly regulated. Instead, the CSR-stage regulates the DC-link current in the buck-mode, ensuring a tight tracking of the DC-link current reference but still allowing 3-Φ input current distortions. In the boost-mode, the synergetic control shifts the DC link regulation task to the DC/DC-stage, i.e., from the viewpoint of the CSR-stage, it is externally impressed, resulting in lower mains current distortions even without direct mains current regulation. However, standards such as [19] impose strict limitations on the harmonic spectrum of the 3-Φ input currents regardless of the operating point.

This motivates a detailed analysis and comparison of current control strategies for current source rectifiers, specifically PWM-based DC [14] or AC [20] current control methods as well as charge-based AC current control [21]. Due to its low implementation cost, superior tracking performance and high current ripple tolerance demonstrated in various applications such as [22], charge control [23] (or so-called one-cycle control [24]) appears attractive. We propose its integration into the CSC structure, resulting in advanced synergetic current control (ASC), which directly improves the 3-Φ input current quality in the buck-mode. Advantageously, a higher gain of the DC-link current controller can be employed, as in the CSC approach the minimum stability margin of the DC-link current controller (which in ASC remains only active in the boost-mode) occurs in the buck-mode [25], and the controller design is simplified. The ASC also conveniently enables a discontinuous conduction mode (DCM) operation in the buck-mode without additional special modulation schemes as used in [26], [27].

This paper first summarizes different current control strate-

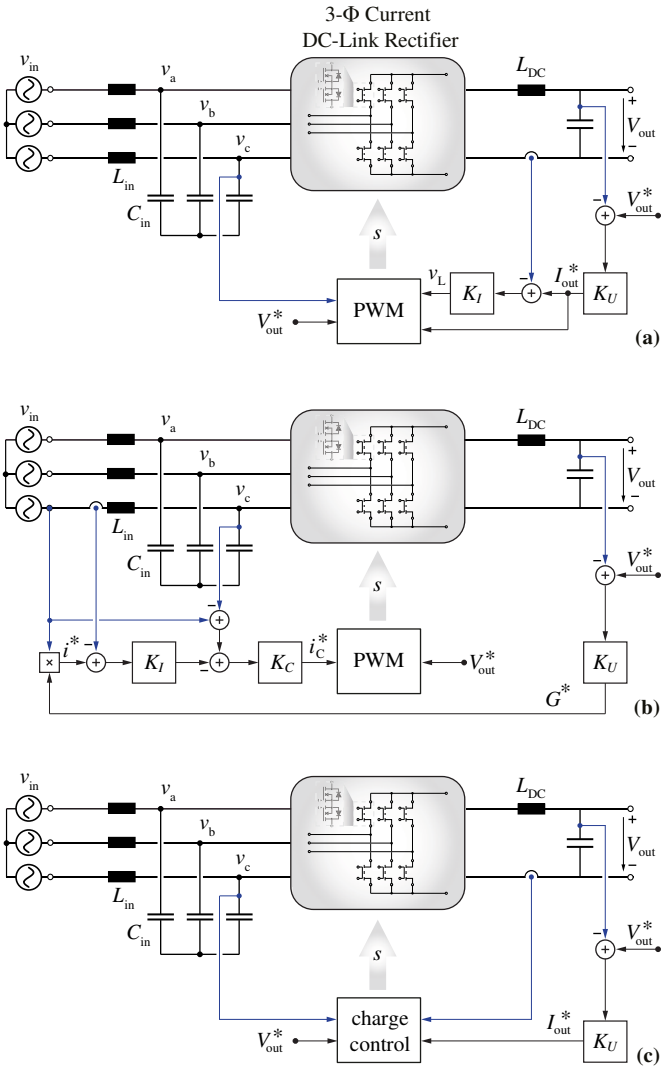

Fig. 1: Summary of different current control strategies for a 3-Φ current DC-link PFC rectifier, assuming a cascaded structure with an outer output voltage control loop. **(a)** Inner DC-link current control [14] and **(b)** inner AC current control [20] are the state-of-the-art solutions. **(c)** Charge-based inner AC current control was proposed in [21]. It features direct control of the AC currents with a reduced number of current sensors (i.e., only one DC-link current measurement instead of at least two out of 3-Φ AC current measurements), and achieves very low AC current distortions.

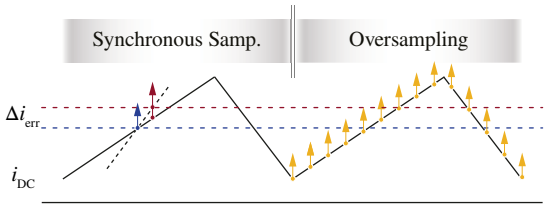

Fig. 2: Comparison between synchronous sampling **(left)** and oversampling **(right)** of the DC-link current i_{DC} to extract its local average value. Synchronous sampling could lead to a significant error Δi_{err} due to measurement misalignments/delays, especially in case of steep current rising/falling slopes.

gies and sampling schemes for current DC-link rectifiers in **Section II**, which also explains the charge control method based on a DC/DC buck converter in detail. In **Section III**, charge control is then integrated into a synergetic control structure with a regulation capability over a wide output voltage range. In **Section IV**, detailed circuit simulations including a realistic discrete digital controller implementation of the CSCs (with synchronous sampling and oversampling) and the ASC verify the 3-Φ input current quality improvement. Furthermore, DCM operation in buck-mode based on the proposed ACS is demonstrated. ASC allows for a higher DC-link inductor current ripple, and thus ultimately enables a more compact realizations which is verified using a DC-link inductor Pareto optimization. Finally, **Section V** summarizes and concludes this paper.

II. Review of Current Control Strategies

Three commonly applied current control strategies for 3-Φ current DC-link AC/DC PFC rectifiers are shown in **Fig. 1**, including **(a)** PWM-based DC-link current control, **(b)** PWM-based AC current control, and **(c)** charge-based AC current control. A cascaded control structure employing an outer output voltage control loop is present in all cases. This outer output voltage control loop defines the input power reference and thus ultimately the required grid currents.

A. PWM-Based DC-Link Current Control

In the PWM-based DC-link current control (see **Fig. 1(a)**), the AC currents are not directly controlled. Instead, the DC-link current is measured and compared with its reference (output of the voltage controller). The current error serves as the controller input and leads to a DC-link inductor voltage reference v_{L}^{*}. The modulation of the rectifier stage is adjusted accordingly to achieve a direct tracking of the DC-link current reference. Note that the 3-Φ input currents thus result from the PWM in an open-loop manner [17]. This state-of-the-art method is implemented in the inner current loop of CSC (see **Section III-A**).

The presence of a high-frequency ripple in the DC-link inductor current complicates the required measurement of its local average value. Typically, synchronous sampling techniques are employed, which sample the instantaneous current once or twice (single/double update mode) per switching period at those instances when it (theoretically) equals its local average value, as shown in **Fig. 2**. However, a misalignment between this intended and the *actual* sampling instant could occur due to hardware imperfections, e.g., calculation delays, gate driver delays, and current sensor delays, and lead to a current measurement error Δi_{err}. This error especially increases for steeper rising/falling current slopes, i.e., a higher current ripple that advantageously would allow smaller DC-link inductors, and could ultimately destabilize the control loop. To overcome this issue and to take advantage of available high-speed ADCs and FPGAs, oversampling, i.e., sampling of the instantaneous current in a free-running mode with a very high sampling rate (several Msps) can be employed. The local average value is obtained as the mean value of all samples taken during the last switching period.

B. PWM-Based AC Current Control

Direct tracking of the 3-Φ input currents can be realized with the PWM-based AC current control scheme (see **Fig. 1(b)**), where the input current references are calculated from the input conductance reference G^{*} and the measured mains voltages. These input current references are tightly tracked by a two-loop cascaded control structure with an outer AC inductor current control loop and an inner AC capacitor voltage control loop. Thus, because a high-order system needs to be controlled, the current loop bandwidth

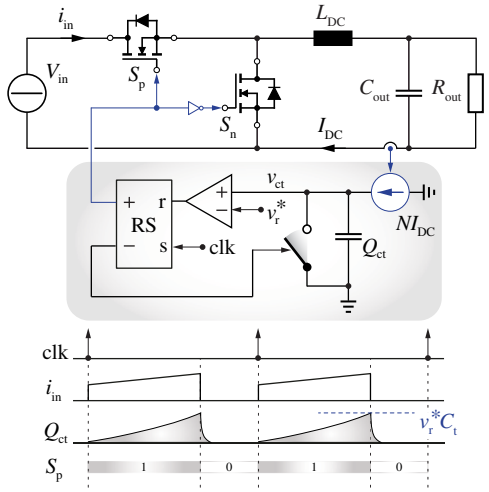

Fig. 3: Charge control of the DC/DC buck converter. Considering the scaling factor N, the inductor current I_{DC} is measured to charge an integrating capacitor C_t, whose voltage v_{ct} is used to compare with **the input current reference** $v_r^* \propto i_{in}^*$ through a comparator. The comparator output serves as the input of an RS flip-flop, which drives the buck converter switches and the discharging switch of the integrating capacitor.

has to be well below the input filter resonance frequency and additional active or passive damping might be required [28]. Moreover, three cascaded loops render the controller design relatively complex. At least two current sensors and two more grid voltage sensors are needed, which contributes to increased hardware costs. On the other hand, the method can achieve actual unity power factor operation at the grid interface, i.e., the reactive power consumed by input inductors and capacitors is compensated.

C. Charge-Based AC Current Control

Charge control [23], or so-called current-mode one-cycle control [24], has been introduced in the 1990s as a large-signal nonlinear control strategy that can ensure faster dynamic response and better perturbation rejection capability than linear feedback control. Before discussing its application in current DC-link rectifiers, we describe the basic operating principle of charge control on the example of a DC/DC buck converter whose input current i_{in} (with a local average value of I_{in}) should be controlled (see **Fig. 3**). In such a current-mode control scheme, the duty cycle D (with $D \cdot T_{sw}$ denoting the on-time of the switch S_p) could be calculated as $D = I_{in}^*/I_{DC}$, i.e., in the same way as the duty cycle in a voltage-mode control is derived to synthesize a desired reference voltage. However, this approach does not directly *control* the input current, as disturbances, ripple components etc. in i_{DC} directly affect the input current quality. Instead, a local average input current reference I_{in}^* can be translated into a required amount of charge transfer during the corresponding switching period, i.e., $Q^* = I_{in}^* \cdot T_{on}$. With T_{on} denoting the on-time of the switch S_p, the transferred charge during a switching period becomes

$$Q = \int_0^{T_{on}} I_{DC}(t)\, dt. \tag{1}$$

It is thus possible to control the local average value of the input current via an *integral* quantity, i.e., the charge Q. By ensuring $Q = Q^*$ also $I_{in} = I_{in}^*$ is achieved—regardless of the *effective* shape of i_{DC} (i.e., taking into account its ripple and potential disturbances from the input/output voltage sources).

Fig. 3 shows a practical implementation, in which the control system employs a capacitor C_t to integrate the measured (and scaled by factor N) current i_{DC} and thus obtain a voltage signal $v_{ct} \propto Q$. In digital implementations an accumulator emulates the integrating behavior of the capacitor. At the beginning of each switching period, the clock signal sets the RS flip-flop, which turns on S_p. This switching state is maintained until v_{ct} increases from zero to $v_{ct} > v_r^*$, at which point the RS flip-flop is reset. Correspondingly, S_p is turned off (S_n is turned on) and the capacitor C_t is discharged (the accumulator is reset). The voltage v_r^* represents the charge reference Q^* (and hence the local input current reference I_{in}^*) and can be calculated as

$$v_r^* = \frac{N}{C_t} Q^* = \frac{N}{C_t} T_{sw} I_{in}^*. \tag{2}$$

In this way, the required amount of charge within one switching period is exactly delivered without steady-state error. Moreover, any dynamic error is considerably limited by the one-cycle control concept [24], i.e., the discrepancy between a new reference current value and the actual average current can be corrected in only one switching period. In contrast, for a conventional PI controller, a correction is only possible after the error signal deviates from zero and hence the transient normally lasts several switching periods with ringing or overshoot, depending on the controller bandwidth. Further, charge control shows reinforced perturbation rejection capability because an *integral* quantity is controlled, i.e., high-frequency current disturbances introduced by, e.g., measurement or switching behavior are taken into account by the integration of the current i_{dc}.

Charge control can be employed in current DC-link rectifiers to improve the 3-Φ input current quality without an increase in the controller implementation complexity or the hardware cost. Therefore, charge-based AC current control (see **Fig. 1(c)**) for three-phase buck-type rectifiers was first proposed in [21]. In the following, we propose its integration into an advanced synergetic control structure for current DC-link buck-boost rectifier systems.

III. Proposed Synergetic Control Structure with Direct Charge-Based AC Current Control

In this section, first the conventional synergetic control (CSC) employing a PWM-based DC-link current control and different optimal operating modes of the analyzed converter (see **Fig. 4(a)** and key waveforms in **Fig. 5**) is introduced. Then, a charge-based AC current control is successfully integrated to form a new advanced synergetic control (ASC) concept featuring direct feedback control of the 3-Φ mains currents.

A. Conventional Synergetic Control (CSC)

The state-of-the-art synergetic control structure [17] comprises an *output voltage control* unit (see **Fig. 4(b.i)**) which generates a converter input conductance reference G^*. The *DC-link current reference generation* block (see **Fig. 4(b.ii)**) uses G^* to obtain the 3-Φ mains current references i_a^*, i_b^*, and i_c^* that are proportional to the corresponding 3-Φ input voltages v_a, v_b, and v_c, i.e., ensure pure ohmic operation. The

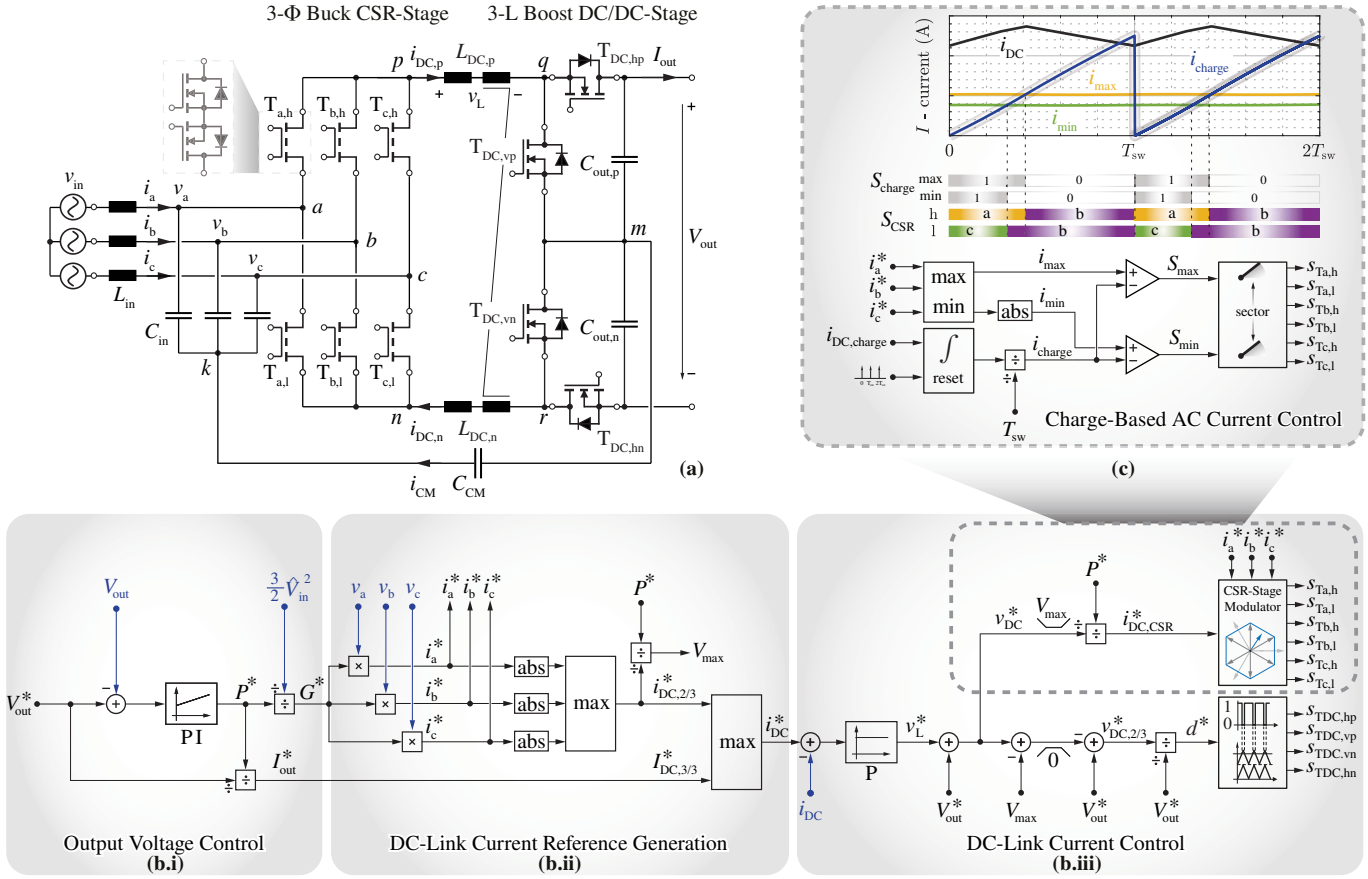

Fig. 4: (a) Circuit schematic of the three-phase (3-Φ) buck-boost (bB) current DC-link PFC rectifier system employing a three-level (3-L) boost DC/DC-stage. **(b)** Block diagram of the conventional synergetic control (CSC) [17] with its three main functional units, i.e., the *Output Voltage Control*, the *DC-Link Current Reference Generation*, and the *DC-Link Current Control*, which enable the synergetic operation of the 3-Φ CSR-stage and of the boost-type DC/DC-stage, and seamless transitions between the buck and boost modes needed to cover the wide output voltage range. **(c)** Proposed integration of a charge-based advanced synergetic current control strategy (ASC) that replaces the DC-link current control by the CSR-stage in the buck-mode, and replaces the rectifier-stage space vector modulator in all operating modes. In each sector of the output current period, the two active states' gate signals $S_{\max}$ and $S_{\min}$ are obtained by comparing the integral of the measured DC-link current i_{DC} with the 3-Φ input current references. They are then assigned to the corresponding power transistors according to the sector information. Importantly, $i_{\mathrm{DC,charge}} = (d^* \geq 1) \cdot i_{\mathrm{DC}} + (d^* < 1) \cdot i^*_{\mathrm{DC}}$ is applied to avoid interaction between the AC current and DC-link current controllers in the boost-mode. The controller behavior is exemplarily shown for the sector where $i^*_{\mathrm{a}} > 0 > i^*_{\mathrm{b}} > i^*_{\mathrm{c}}$.

upper envelope of the absolute 3-Φ mains current references defines the varying DC-link current reference $i^*_{\mathrm{DC,2/3}}$ for 2/3-PWM operation (in boost-mode, where the DC/DC stage regulates the DC-link current accordingly). The DC-link current reference $i^*_{\mathrm{DC,3/3}}$ for 3/3-PWM operation is simply equal to the output current reference I^*_{out}, as in the buck-mode the DC/DC-stage is clamped ($\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ are permanently conducting, see **Fig. 5(c)**). Finally, the DC-link current reference, $i^*_{\mathrm{DC}} = \max\{i^*_{\mathrm{DC,2/3}}, I^*_{\mathrm{DC,3/3}}\}$, is the input of the inner current control loop. In the boost-mode, the DC/DC-stage regulates the output voltage and controls the DC-link current into the six-pulse shape needed for the CSR-stage to operate with 2/3-PWM. The CSR-stage ensures a sinusoidal shape of the 3-Φ mains currents by essentially acting as a modulator. Importantly, during this 2/3-PWM operation, a well-regulated (by the DC/DC-stage) DC-link current leads to tightly-tracked 3-Φ mains currents resulting from modulation of the CSR-stage, which is limited to the switching between two phases (2/3-PWM) without using zero states (**Fig. 5(b)**).

If $V^*_{\mathrm{out}} < V_{\max} = P^*/i^*_{\mathrm{DC,2/3}}$, the system operates in buck-mode with 3/3-PWM, i.e., the CSR-stage provides sinusoidal 3-Φ currents at the mains interface and tracks the output voltage reference by controlling the DC-link current, while the DC/DC-stage operates in a pass-through mode without regulation capability, i.e., always gating $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ on. Note that the DC-link current controller (via v^*_{L}) ultimately modifies the duty cycles of the CSR-stage's active states to track the DC-link current. I.e., the accordingly modified current reference $i^*_{\mathrm{DC,CSR}}$ used in the SVPWM of CSR-stage does not necessarily equal the reference DC-link current i^*_{DC} nor the actual DC-link current i_{DC}, even if a perfect tracking of the DC-link current reference is assumed, because of the control output v^*_{L}. For example, in case of $i^*_{\mathrm{DC}} > i_{\mathrm{DC}}$, the resulting positive v^*_{L} leads to $i^*_{\mathrm{DC,CSR}} < i_{\mathrm{DC}}$ and hence the duty cycles of the active vectors calculated based on $i^*_{\mathrm{DC,CSR}}$ are prolonged to produce a larger voltage-time area across L_{DC}, which finally brings i_{DC} closer to i^*_{DC}. It is thus the DC-link current that is directly regulated at the expense of allowing larger harmonic distortions in the 3-Φ mains currents (due to the modified duty cycles). This is in contrast to the boost-mode, where the CSR-stage modulates an *externally* impressed (regulated) DC-link current into the desired phase currents.

B. Advanced Synergetic Control (ASC)

To improve the 3-Φ input current tracking performance, we here propose an integration of a charge-based con-

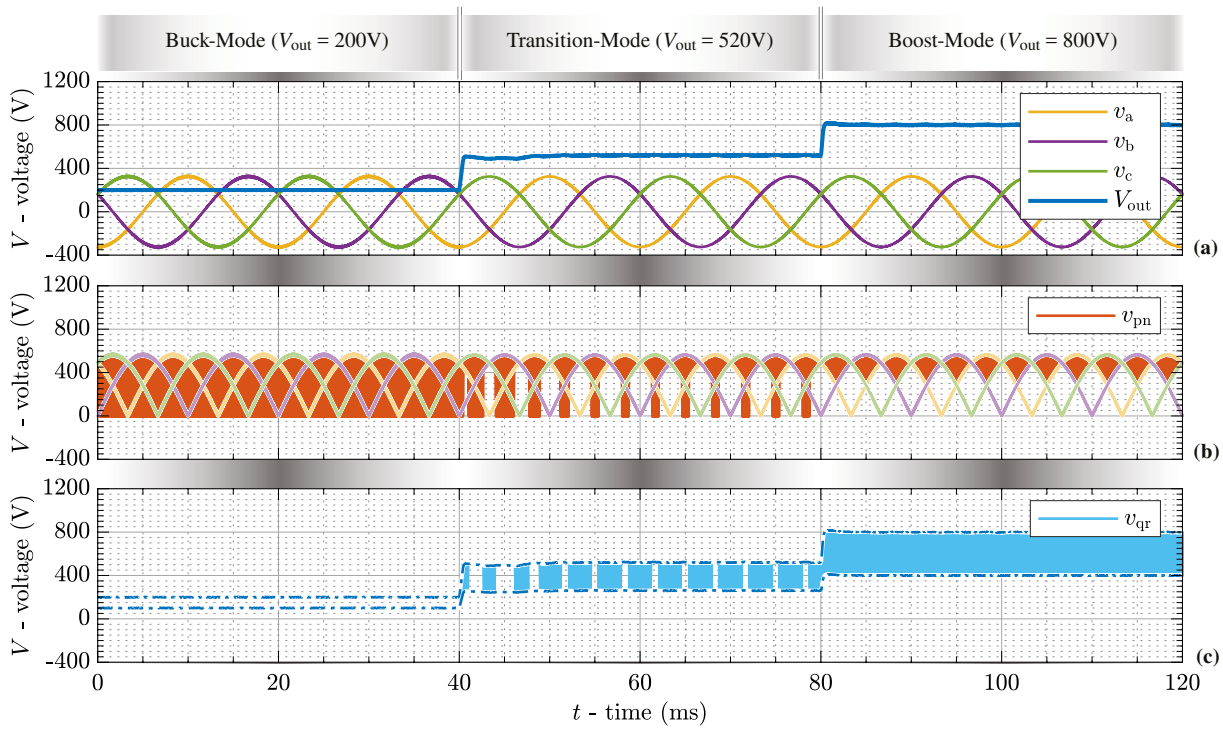

Fig. 5: Simulated voltage waveforms of the analyzed converter with the ASC for three different operating modes. **(a)** 3-Φ mains voltages v_a, v_b, v_c and output voltage V_{out}; **(b)** output voltage of the CSR-stage v_{pn} alternately assuming the absolute values of the line-to-line voltages during the active states and 0 V during the zero state; **(c)** input voltage of the DC/DC-stage v_{qr} switching between 0 V and $\frac{1}{2}V_{out}$ or $\frac{1}{2}V_{out}$ and V_{out}.

troller/modulator (see **Section II-C** and [21]) in the CSC discussed above. As shown in **Fig. 4(c)**, the 3-Φ input current references i_a^*, i_b^*, and i_c^*, and the measured DC-link current i_{DC} serve as the inputs of the AC current charge control block. The maximum i_{max} and the minimum i_{min} phase currents are first selected and forwarded to the comparators, e.g., in the sector where $i_a^* > 0 > i_b^* > i_c^*$, $i_{max} = i_a^*$ and $i_{min} = -i_c^*$. In a digital controller implementation, i_{DC} is measured with a Hall-effect-based current sensor and a high-speed ADC, and a discrete integrator programmed in an FPGA emulates the functionality of the integrating capacitor. Its output i_{charge} is reset at the start of each switching period. The two characteristic switching signals, S_{max} and S_{min}, are calculated from the comparisons of i_{charge} with i_{max} and i_{min}, respectively. They are then assigned to the actual gate signals according to the sector information. Considering the example shown in the figure, when i_{max} $(i_{min}) > i_{charge}$, its characteristic switching signal S_{max} (S_{min}) is on, and the corresponding phase a (phase c) of the upper (lower) commutation cell conducts the DC-link current; otherwise, if i_{max} $(i_{min}) < i_{charge}$, the phase with the minimum current amplitude, e.g., phase b of the upper (lower) commutation cell, is connected to the current DC-link. Different from the DC-link current control employed in the CSC, the 3-Φ mains currents are now always tightly tracked in the buck-mode, i.e., direct AC current feedback control is achieved by regulating the amount of charge injected into the phases over one switching period. Note that this is possible even without directly measuring the 3-Φ mains currents (only one DC-link current sensor is necessary instead of at least two for 3-Φ AC current measurement) [21]. The DC-link current is not directly controlled and can thus contain harmonic distortions, which, however, are of no concern for the grid current quality.

In boost-mode operation, the DC/DC-stage takes over the control of the DC-link current (as in CSC). Note that since i_{DC} is controlled by the DC/DC-stage, a corresponding ripple would occur in the output current instead of in the input currents. Therefore, the charge control block shown in **Fig. 4(c)** only behaves as a modulator which is achieved by using i_{DC}^* instead of i_{DC} as the input of the integrator. Defining $i_{DC,charge} = (d^* \geq 1) \cdot i_{DC} + (d^* < 1) \cdot i_{DC}^*$ ensures a smooth transition between buck and boost operating modes. Note that because in ASC the DC-link current controller is only needed in the boost-mode, its gain can be increased (as the stability margin in buck-mode is smaller, see [25]). The thus improved DC-link current tracking directly translates into an improved mains current quality in boost-mode, as always one out of three phase currents (absolute value) equals that DC-link current. Therefore, the proposed ASC guarantees high-quality 3-Φ mains currents while operating over a wide output voltage range, i.e., in buck- and boost-mode.

IV. Simulation Results

In this section, the closed-loop operation of the proposed ASC is validated by circuit simulations of the converter shown in **Fig. 4(a)** with the specifications listed in **Tab. I** [29], and its performance is compared with the CSC (using either synchronous sampling or oversampling). The simulation environment is set to emulate a real digital control system: the measurement skew is included by passing the measured DC-link current through a low-pass transfer function obtained from the datasheet of the applied current sensor (*ACS732KLATR-40AB-T*) with a high measurement bandwidth of 1 MHz. Furthermore, the analog data is discretized by an ADC (*LTC2325-14*) with a sampling rate of 5 Msps/Ch, and the AC current charge controller is imple-

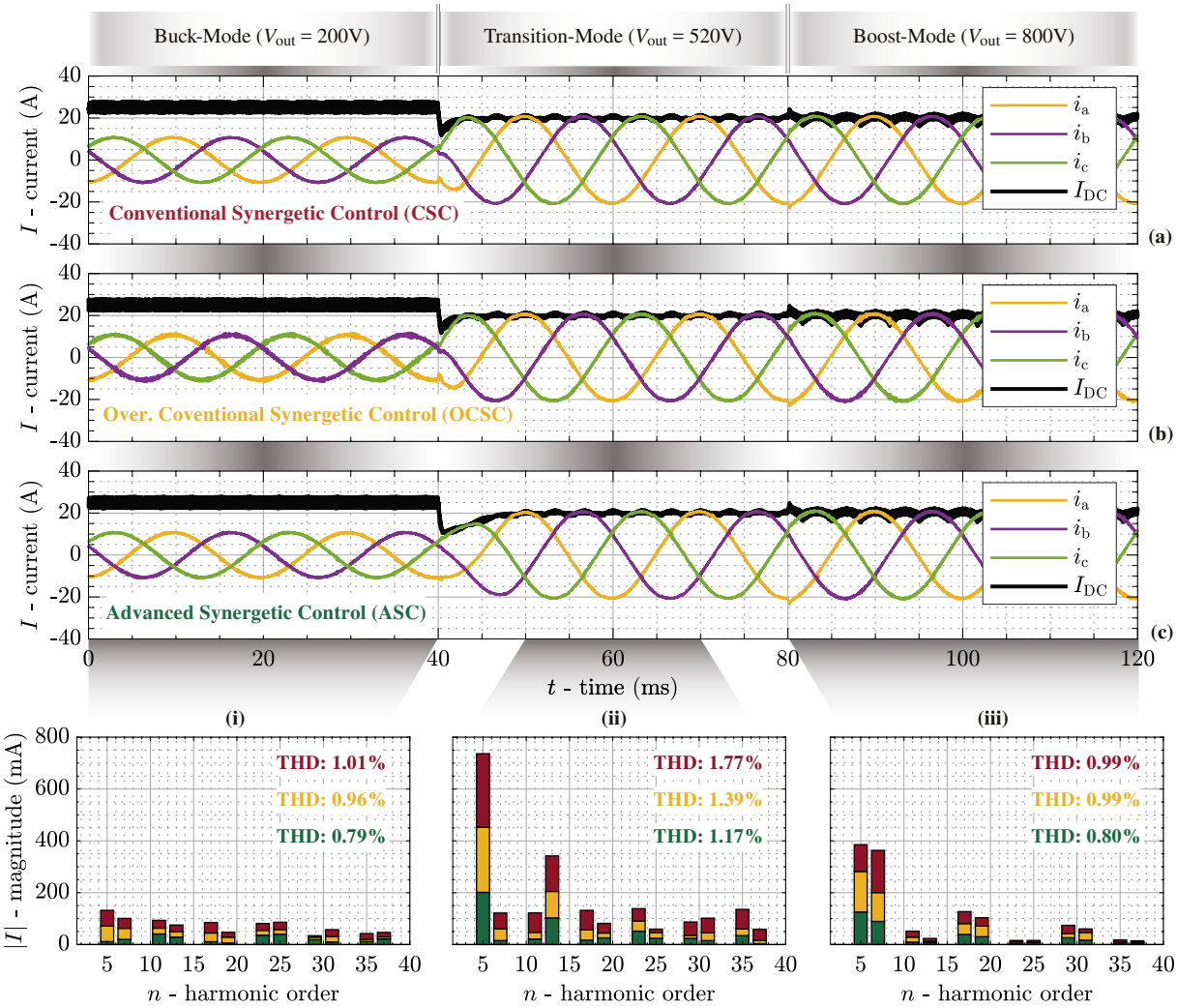

Fig. 6: Simulated current waveforms, i.e., 3-Φ mains currents i_a, i_b, i_c and DC-link current i_{DC}, of the analyzed converter for three different operating modes, when employing different synergetic control strategies, i.e., conventional synergetic control (CSC) with synchronous sampling, oversampled conventional synergetic control (OCSC), and advanced synergetic control (ASC). The steady-state current harmonics are shown together with their Total Harmonic Distortion (THD), considering harmonics up to the 40th. Over the whole operating range, ASC shows superior mains current quality due to the direct feedback control of the 3-Φ mains currents in the buck-mode and a higher DC-link current controller gain in the boost-mode.

TABLE I: System specifications and simulation parameters.

	Description	Value		
V_{in}	AC-bus RMS phase voltage	230 V		
$\cos(\phi)$	power factor	1.0		
f_{in}	AC-bus frequency	50 Hz		
f_{sw}	switching frequency	100 kHz (both stages)		
C_{in}	input capacitance	3 × 6 µF		
$L_{DC,DM}$	DM DC-link inductance	250 µH		
C_{out}	output capacitance	2 × 10 µF		
V_{out}	DC output voltage	200 V	400 V	1000 V
I_{out}	output current	25 A	25 A	10 A
P_{out}	output power	5 kW	10 kW	10 kW

mented considering an FPGA clock frequency of 100 MHz, which could be ach ieved with state-of-the-art system-on-chips such as the Xilinx Zynq 7000.

A. Grid Current Quality Improvement

Fig. 5 shows the characteristic voltage waveforms of the three different operating modes, i.e., the 3-Φ mains voltages v_a, v_b, v_c, the switched output voltage of the CSR-stage v_{pn}, and the switched input voltage of the DC/DC-stage v_{qr}, when applying the proposed ASC. The results highlight the seamless transitions between different operating modes as well as the optimal clamping of bridge-legs to minimize the switching losses.

Fig. 6 presents the 3-Φ mains currents i_a, i_b, i_c and the DC-link current i_{DC} when applying the CSC (using DC-link current control in buck- and in boost-mode) with synchronous sampling **(a)** and with oversampling **(b)**, and the proposed ASC **(c)** that employs AC current charge control when operating in the buck-mode. The CSC with oversampling achieves a better current tracking performance than the CSC with synchronous sampling. The proposed ASC performs best over the full wide output voltage range, i.e., in all three modes. In the buck-mode, a clear improvement of the 3-Φ input current quality (lower amplitudes of the low-frequency harmonics and accordingly lower Total Harmonic Distortion (THD)) results from the direct feedback control of the 3-Φ input currents. Moreover, as now the DC-link current control is only needed/activated in the boost-mode, a larger controller gain is possible according to the worst-case stability control

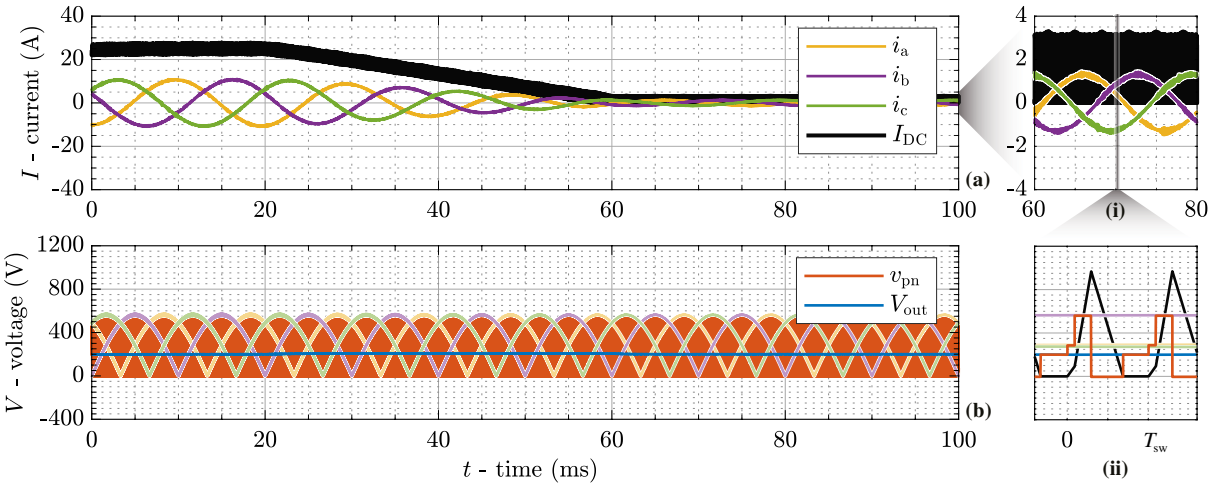

Fig. 7: Simulated waveforms of the analyzed converter regulated by the proposed ASC showing the transition to discontinuous conduction mode (DCM) in the buck operating region. Specifically, **(a)** 3-Φ mains currents i_a, i_b, i_c and DC-link current i_{DC} with a vertically zoomed view of one mains period, and **(b)** output voltage V_{out} and output switched voltage of the CSR-stage v_{pn} with a zoomed view of the switching pattern during one switching period, which demonstrates DCM operation at light load. The simulation starts from the nominal load, i.e., V_{out} = 200 V and P_{out} = 5 kW, and ends up with light-load operation, i.e., V_{out} = 200 V and P_{out} = 0.2 kW.

margin analysis in [25], which explains the observed THD improvement in the boost-mode operation.

B. Discontinuous Conduction Mode (DCM) Operation

Current DC-link rectifiers enter the discontinuous conduction mode (DCM) under light-load conditions [26], [27] due to a reduced average value of the DC-link inductor current at low output power (i.e., when the average value becomes lower than the DC-link current ripple amplitude). Thus, DCM operating capability is significant in extending the operating region for conventional buck-type rectifiers. Even though in the analyzed system the DC-link current value reference is independent of the output power because of its buck-boost functionality, DCM operating capability increases the light-load efficiency in buck-mode (as the DC/DC-stage can remain clamped). This is important for EV charger applications because of an extended constant voltage (CV) charging period [30]. Furthermore, DCM operating capability allows a higher DC-link current ripple without the need to correspondingly increase the minimum allowable DC-link current average value (to prevent entering DCM), which facilitates a more compact DC-link inductor realization.

In DCM operation, a continuous DC-link current should be ensured during the active states so that the injected phase charge (equivalent to the phase current local average value) is well-regulated [26], [27]. Advantageously, this is intrinsically fulfilled by the charge control strategy as each switching period always starts with active switching states that lead to an increasing (from zero in DCM) DC-link current (see v_{pn} in **Fig. 7(ii)**). Note that in DCM the bidirectional CSR-stage (see **Fig. 4(a)**) is operated in a unidirectional mode to prevent negative DC-link currents that would interfere with the multi-step commutation sequences. Thus, transistors capable of conducting negative DC-link current are permanently off, i.e., act as diodes only.

The simulation results from **Fig. 7** demonstrate how the proposed ASC inherently enables a smooth transition to DCM operation once the operating point changes from nominal load (V_{out} = 200 V and P_{out} = 5 kW) to light load (V_{out} = 200 V and P_{out} = 0.2 kW). Note that also in DCM the 3-Φ input currents are sinusoidal and a regulated constant output voltage V_{out} is provided.

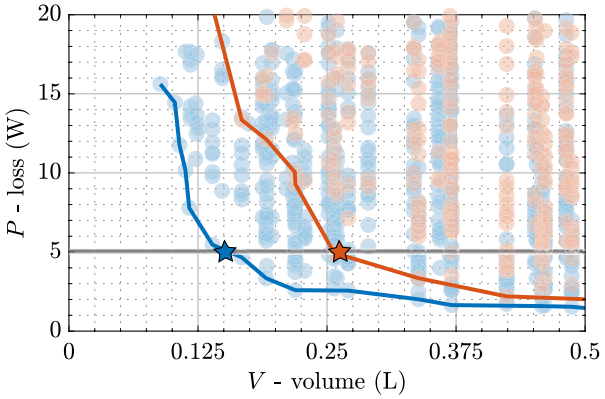

Fig. 8: Comparison of DC-link inductor design space with 25% (orange) and 40% (blue) peak-to-peak current ripple limitation. With an increased DC-link current ripple, only half of the volume is needed while keeping the same inductor losses, e.g., 5 W.

C. Impact of Higher DC-Link Current Ripple

Sensing errors introduced by synchronous sampling of a current with high ripple and/or the minimum local average DC-link current needed to provide a certain minimum output power without entering DCM determine the maximum allowed DC-link current ripple. Thus, an increased DC-link current ripple is allowed by taking advantage of either CSC with oversampling to mitigate sensing errors, or the proposed ASC. Furthermore, the ASC inherently facilitates DCM operation in buck-mode, which further eases the DC-link inductor current ripple limit by eliminating the local average DC-link current limitation in the buck-mode, where DCM enables arbitrarily low local average DC-link currents (note that with CSC, the critical DCM boundary, i.e., the largest voltage-time area across the DC-link inductor, which defines the critical inductance design point, occurs in the buck-mode [31]). Thus, increasing the current ripple allows

for reducing the DC-link inductor volume, which is verified by an inductor Pareto optimization (see **Fig. 8**). Increasing the peak-to-peak current ripple from 25% (orange) to 40% (blue) reduces the inductor's boxed volume to about half the original value.

To verify the converter operation considering a worst case with an even larger DC-link current ripple, a $100\,\mu\text{H}$ (40% of nominal value) DC-link inductance is employed in the circuit simulation. When CSC with synchronous sampling is employed, the system becomes unstable due to a considerable sampling error. In contrast, systems regulated by CSC with oversampling or by the proposed ASC operate appropriately without a degradation of the grid-current THD, i.e., in the buck-mode operation ($V_{\text{out}} = 200\,\text{V}$), ASC (CSC with oversampling) realizes 3-Φ mains currents with a THD of 0.75% (0.96%).

V. Conclusion

In this paper, we propose an improved and advanced synergetic control (ASC) structure for a three-phase bidirectional buck-boost current DC-link PFC rectifier system, formed by a 3-Φ buck-type CSR-stage and a subsequent boost-type DC/DC-stage. The proposed scheme employs the charge control concept to regulate the AC-side currents in buck-mode operation directly and facilitates a seamless transition to the boost-mode, i.e., retains this essential feature of conventional synergetic control (CSC). In the boost-mode, still, the DC/DC-stage regulates the DC-link current but can do so with a higher control gain. Detailed simulation results confirm a clearly reduced (by up to $30\,\%$) total harmonic distortion of the AC-side currents for operation over the entire output voltage range (from 200 to $1000\,\text{V}$). The proposed ASC successfully enables operation with higher DC-link current ripples (smaller DC-link inductors, e.g., half the original size) without degradation of the grid current THD, and ultimately a smooth transition to the discontinuous conduction mode (DCM) for light-load operation.

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