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Duty-Cycle Dependent Phase Shift Modulation of Dual Three-Phase Active Bridge Four-Port AC–DC/DC–AC Converter Eliminating Low Frequency Power Pulsations

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ABSTRACT A recently introduced Dual Three-Phase Active Bridge Converter (D3ABC) provides two three-phase ac ports (ac_1 and ac_2), two dc ports (dc_1 and dc_2), and galvanic isolation between the ports ac_1, dc_1 (primary side) and ac_2, dc_2 (secondary side). Previously documented studies confirm that the D3ABC is generally capable of transferring power between all four ports. However, it has been found challenging to operate the converter if ac voltages with different line frequencies, $f_1 \neq f_2$, are present at the ports ac_1 and ac_2. Such operation causes Low-Frequency (LF) power pulsations in the converter's dc links, leading to fluctuating dc link voltages and distorted phase currents. In this paper, a new duty-cycle dependent phase shift modulation scheme is proposed that eliminates such LF power pulsations and substantially increases the theoretical maximum transmittable power between primary and secondary sides compared to previous work. The new modulation scheme is developed on the basis of analytical considerations, which are supported by the results of numerical calculations, and verified by means of circuit simulations and experimental results. A hardware demonstrator originally designed for a rated power of 8 kW when operated from ac_1 to dc_2 at the European low-voltage ac mains ($V_{ac,1} = 230$ V line-to-neutral rms, $V_{dc,1} = 800$ V, $V_{dc,2} = 400$ V) is used for experimental verification. Since the operation with $f_1 \neq f_2$ leads to an increase of the currents in the converter, the experimental verification is conducted at half voltages and for a reduced power of 2 kW that is transferred from ac_1 to ac_2 at substantially different primary-side and secondary-side line frequencies of $f_1 = 50$ Hz and $f_2 = 77$ Hz. The measured results agree well with the simulated results. In particular, the dc link voltages show almost constant waveforms, which confirms the correct operation of the proposed modulation scheme.

INDEX TERMS Ac-dc power converters, dc-ac power converters, ac-ac converters, Dual Three-Phase Active Bridge Converter (D3ABC) topology, Dual Active Bridge (DAB) converter, four-port ac-dc/dc-ac converter.

I. INTRODUCTION

As part of a successful evolution from the current ac distribution grid to the smart grid of the future, the development and integration of dc and ac microgrids, i.e., the interconnections of local power generators and consumers, into the smart grid are expected to play key roles [1], [2]. In this context, the connection of a microgrid to the smart grid is achieved by a suitable bidirectional power converter [3]. Preferrably, this bidirectional converter should feature an integrated galvanic isolation, to allow the realization of a suitable grounding concept and thus achieve an increased reliability of the system, as discussed in [4]. In addition, converter systems with multiple power ports increase the flexibility in terms of controlling power transfers between the ports and enable the implementation of innovative concepts, such as the Energy Internet described in [5]. A four-port ac–dc/dc–ac converter system that provides two three-phase ac ports, two dc ports, and galvanic isolation between the

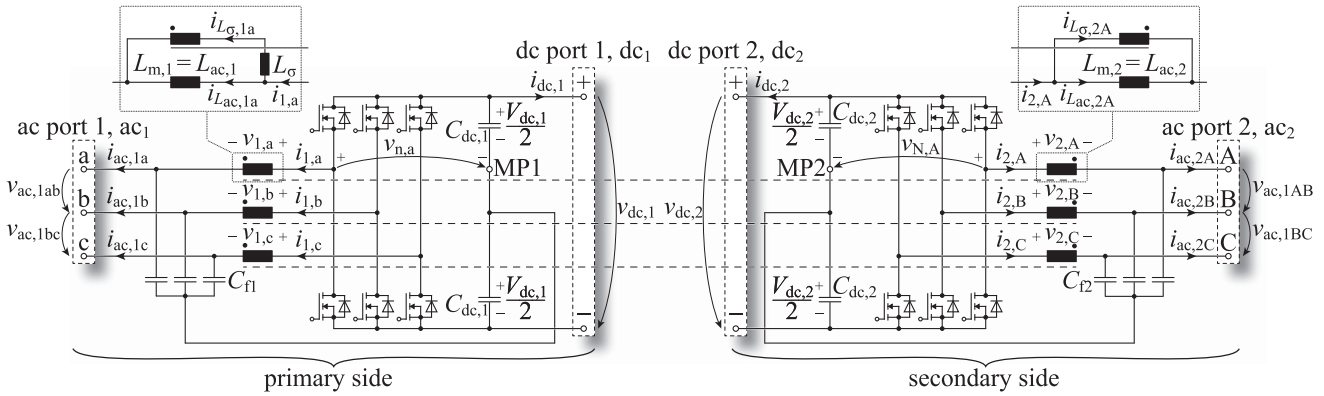

FIGURE 1. Dual Three-Phase Active Bridge Converter (D3ABC) with primary-side ac and dc ports (ac_1, dc_1) and galvanically isolated secondary-side ac and dc ports (ac_2, dc_2).

primary- and secondary-side ac and dc ports can meet these requirements.

Conventionally, such a four-port ac–dc/dc–ac converter system can be realized by means of a series connection of a primary-side three-phase rectifier, a dc/dc converter with galvanic isolation, and a secondary-side three-phase inverter. However, rectifier and inverter circuits with a voltage dc link must be used, since otherwise no dc voltage ports would be available [6]. Most related publications describe the realization of a conventional ac–dc/dc converter structure, i.e., the series connection of a primary-side three-phase rectifier and a dc/dc converter with galvanic isolation, which can be immediately extended to an ac–dc/dc–ac structure. Documented examples include the series connection of a two-level six-switch rectifier and single-phase Dual Active Bridge (DAB) converter [7] or full-bridge dc/dc converter [8]; the combination of a three-level T-type rectifier and full-bridge dc/dc converter [9] or of a three-level Neutral Point Clamped (NPC) rectifier and three-phase DAB converter [10].

In the context of improving the efficiency and/or volume requirements of power electronic circuits, the integration of several converter stages into a single converter stage is of particular importance. Examples of documented rectifiers with integrated galvanic isolation are the current-fed rectifiers with integrated LLC resonant converter described in [11] or with a DAB converter presented in [12], the rectifier with integrated full-bridge dc/dc converter presented in [13], the rectifier with integrated three-phase DAB converter explained in [14], or the nine-switch converter with integrated three-phase resonant converter described in [15]. These topologies are complemented by further rectifier topologies with integrated galvanic isolation, but without a primary-side dc voltage port, such as matrix-type converters [16], [17] and Swiss-type converters [18], [19].

If the four-port converter system would be realized with one of the topologies described in [11], [12], [13], [14], [15], a secondary-side inverter would still be needed. However, fully integrated circuits also exist for the examined four-port operation [20], [21], although the description in [20] is limited to four-port operation with one ac port and three dc ports, and the one in [21] to rectifier operation with galvanic isolation. Nevertheless, after minor adjustments, a four-port operation with two ac ports and two dc ports can be achieved with both systems. Due to the significantly higher circuit complexity of the converter analyzed in [20] (e.g., 24 semiconductor switches), the focus of this paper is on the further investigation of the D3ABC introduced in [21], which is shown in Fig. 1. Table 1 lists the nominal voltages and frequency as well as the maximum power of the considered D3ABC. This topology can be understood as the integration of two three-phase VSCs and three DAB converters.

TABLE 1. Main specifications of the considered Dual Three-Phase Active Bridge Converter (D3ABC).

ac_1 voltage (line-to-neutral, nominal rms)	$V_{ac,1} = 230\,\mathrm{V}$
ac_1 nominal line frequency	$f_1 = 50\,\mathrm{Hz}$
dc_1 voltage	$V_{dc,1} = 800\,\mathrm{V}$
ac_2 voltage (line-to-neutral, nominal rms)	$V_{ac,2} = 115\,\mathrm{V}$
dc_2 voltage	$V_{dc,2} = 400\,\mathrm{V}$
Maximal output power	$P_{out} = 8\,\mathrm{kW}$

The integration of several converter stages into a single converter stage is achieved by using the switching nodes of the half-bridges for multiple purposes. As a result, certain degrees of freedom are lost, which leads to various limitations. In case of the D3ABC it turns out that the operation with non-synchronous input and output voltage waveforms, e.g., with different line frequencies, $f_1 \neq f_2$, may cause LF power pulsations between the two dc links. This LF power pulsation is not sinusoidal but has a spectrum with a fundamental frequency component at $|f_1 - f_2|$.

If, for example, the grid frequency is $f_1 = 50.0\,\mathrm{Hz}$ at port ac_1 and $f_2 = 50.1\,\mathrm{Hz}$ at port ac_2, power pulsation with fundamental $|f_1 - f_2| = 0.1\,\mathrm{Hz}$ can occur in the primary-side and secondary-side dc links. These can lead to unacceptable fluctuations of the dc link voltages. Usually, these voltage fluctuations are counteracted by suitably adjusting the dc link capacitances [22], improving the utilizations of the dc link capacitors by using power pulsation buffers [23], or by involving

an alternative means of energy storage, such as the kinetic energy stored in an electric machine [24]. Alternatively, large filter capacitances connected to the ac ports could absorb the power pulsation. These filter capacitances could also be implemented as solid-state variable capacitors, as, e.g., shown in [25] and [26] for single-phase systems. However, since the minimum required storage capacities are inversely proportional to the frequency of the pulsation [27] and the frequency of the power pulsation can take on very small frequencies down to zero (0.1 Hz in the example described above), the issue actually cannot be solved in this way. Alternatively, the pulsating power could be supplied to the grid. However, a related study concludes that LF power pulsations can be subject to very restrictive limits, especially in the context of flicker [28], which rules out this option. Accordingly, the only remaining option is to adapt the modulation scheme such that pulsating power is suppressed in the dc links.

A previous study [29] describes the four-port operation of the D3ABC under the simplifying condition that the individual DAB converter parts of the D3ABC are operated at constant power in steady state. This leads to a major reduction of the maximum transferrable power. In this paper, a new duty-cycle dependent phase shift modulation scheme is developed which considerably increases the transferrable power. First, Section II explains the multiport operation of the D3ABC. Subsequently, the new modulation scheme for elimination of LF power pulsation is derived in Section III. Finally, Section IV verifies the derived modulation scheme through circuit simulations and measurements on a hardware prototype.

II. MULTI-PORT OPERATION OF THE D3ABC

The systematic description of the operation of the D3ABC with different line frequencies at the ports ac_1 and ac_2 and the consequences of this kind of operation of the D3ABC, is divided into the three steps listed below.

1) Summary of the general operating principle of the D3ABC in Section II-A.
2) Investigation of the known operation with synchronized three-phase ac voltages at the ports ac_1 and ac_2 (same line frequencies and no phase shift) in Section II-B.
3) Operation with three-phase ac voltages with different line frequencies at ac_1 and ac_2 in Section II-C.

A. OPERATING PRINCIPLE OF THE D3ABC

In this paper, symmetric three-phase systems are considered at the primary-side and secondary-side ac ports. Accordingly, three sinusoidal voltages are present at ac_1 and ac_2, respectively,

$$v_{\mathrm{ac},1,\mathrm{a,b,c}}(t) = \sqrt{2}V_{\mathrm{ac},1}\sin\left(2\pi f_1 t + \theta_{\mathrm{a,b,c}}\right), \quad (1)$$

$$v_{\mathrm{ac},2,\mathrm{A,B,C}}(t) = \sqrt{2}V_{\mathrm{ac},2}\sin\left(2\pi f_2 t + \theta_{\mathrm{A,B,C}} + \Theta\right). \quad (2)$$

Here, $V_{\mathrm{ac},1}$ and $V_{\mathrm{ac},2}$ denote the rms values of the phase voltages, f_1 and f_2 denote the line frequencies, $\theta_{\mathrm{a,b,c}} \in \{0°, 120°, 240°\}$ and $\theta_{\mathrm{A,B,C}} \in \{0°, 120°, 240°\}$ the phase shifts between the primary-side and secondary-side phase voltages, respectively, and Θ an initial phase shift between the primary-side and secondary-side phase voltages at time $t = 0$.

TABLE 2. Parameters for the three operating scenarios considered. The given values for the ac voltages are the rms values of the line-to-neutral voltages.

Parameter	Var.	S1	S2	S3	S4
ac_1 voltage	$V_{\mathrm{ac},1}$	230 V	230 V	230 V	115 V
ac_1 line frequency	f_1	50 Hz	50 Hz	50 Hz	50 Hz
dc_1 voltage	$V_{\mathrm{dc},1}$	800 V	800 V	800 V	400 V
ac_2 voltage	$V_{\mathrm{ac},2}$	115 V	115 V	115 V	57.5 V
ac_2 line frequency	f_2	50 Hz	77 Hz	77 Hz	77 Hz
dc_2 voltage	$V_{\mathrm{dc},2}$	400 V	400 V	400 V	200 V
Power at port ac_1	$P_{\mathrm{ac},1}$	−7 kW	−7 kW	−8 kW	−2 kW
Power at port dc_1	$P_{\mathrm{dc},1}$	−1 kW	−1 kW	0	0
Power at port ac_2	$P_{\mathrm{ac},2}$	6 kW	6 kW	8 kW	2 kW
Power at port dc_2	$P_{\mathrm{dc},2}$	2 kW	2 kW	0	0

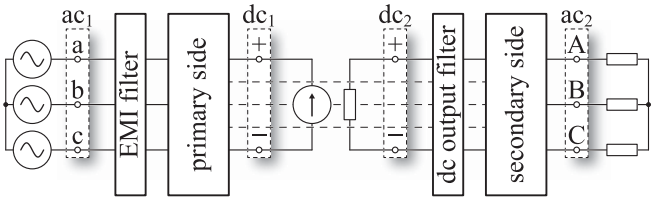

FIGURE 2. Considered configuration of sources and loads for all circuit simulations and all measurements performed on the hardware demonstrator. The exact structure and component values of the Electromagnetic Interference (EMI) filter and the dc output filter can be found in [30]. Since the hardware demonstrator was built for a rectifier operation between ports ac_1 and dc_2, ports dc_1 and ac_2 have no additional input/output filters.

Further, this paper consideres three different operating scenarios, S1 to S4: S1 refers to multi-port operation with synchronized line voltages, S2 to multi-port operation with different line frequencies, S3 to ac–ac operation with different line frequencies, and S4 to ac–ac operation with different line frequencies and reduced voltages as used for the hardware demonstrator. Table 2 lists the parameters for S1 to S4. In this context, it is noted that the sign of the power is defined in the generator reference system, as seen by the D3ABC. Accordingly, a power flow directed from the D3ABC to an external component (e.g., a resistor) has a positive sign. A negative power is present if the power flow at the port under consideration is directed into the converter system. In the context of the bidirectional conversion capability of the D3ABC, this careful definition serves to unambiguously define the operating condition present at each port. Fig. 2 shows the considered configuration of sources and loads, both for the circuit simulations and for the measurements performed on the hardware demonstrator. The resistor values are chosen so that the powers listed in Table 2 result. For scenarios S3 and S4, the current source at dc_1 and the resistor at dc_2 are removed.

For reasons of compactness, a description of the operating principle of the D3ABC is omitted here, since this has been described in detail in [21], [29] (for completeness, a summary

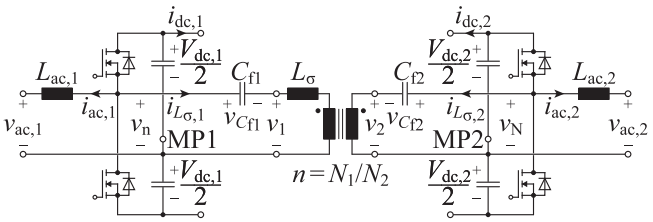

FIGURE 3. Single-phase equivalent system with primary-side and secondary-side boost inductances, $L_{ac,1}$ and $L_{ac,2}$, stray inductance, L_σ, and isolating High-Frequency (HF) transformer with turns ratio n. A detailed derivation of this equivalent circuit can be found in [30].

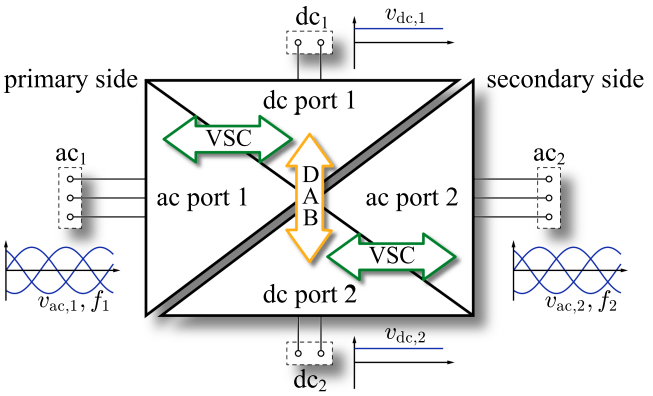

FIGURE 4. The power transfer between the four ports of the D3ABC can be separated into ac_1–dc_1 and ac_2–dc_2 operation w/o galvanic isolation and dc_1–dc_2 operation w/ galvanic isolation. For ac_1–dc_1 and ac_2–dc_2 the corresponding Voltage Source Converters (VSCs) are operated according to (5) and (6) to achieve PFC functionality. The power transfer dc_1–dc_2 is utilizing the DAB functionality, cf. (7).

of this is given in Appendix A of this paper). The following paragraphs summarize the most important aspects.

The D3ABC can be divided into three independent converter systems, i.e., one converter system per phase. Fig. 3 depicts the equivalent circuit of such a single-phase converter system. The primary-side dc link circuits of the three single-phase converter systems are combined in parallel connection and the secondary-side dc link circuits are also connected in parallel.

The energy exchange between ac_1 and the dc link capacitor connected to dc_1 is accomplished in analogy to a Power Factor Correction (PFC) rectifier. Based on the assumption that the mains-side filter inductors have low impedance at the mains frequency, the local average value of the switched voltage generated by a half-bridge (e.g., $v_{n,a}$ in Fig. 1)[1] is approximately equal to the waveform of the mains voltage of this phase. Therefore, taking the example of phases a and A, the result is

$$\langle v_{n,a}\rangle_{T_s} = \left(D_{1a} - \frac{1}{2}\right) V_{dc,1} \approx v_{ac,1a}, \tag{3}$$

$$\langle v_{N,A}\rangle_{T_s} = \left(D_{2A} - \frac{1}{2}\right) V_{dc,2} \approx v_{ac,2A}, \tag{4}$$

where D_{1a} and D_2A denote the relative turn-on times of the low-side transistors of phase a of the primary-side inverter and phase A of the secondary-side inverter, respectively. These expressions can be modified in terms of the phases b, B and c, C, leading to the relations

$$D_{1,a,b,c}(t) \approx \frac{1}{2}\left[1 + m_1 \sin\left(2\pi f_1 t + \theta_{a,b,c}\right)\right], \tag{5}$$

$$D_{2,A,B,C}(t) \approx \frac{1}{2}\left[1 + m_2 \sin\left(2\pi f_2 t + \theta_{A,B,C} + \Theta\right)\right], \tag{6}$$

for the duty cycles of the six half-bridges. The method to control the power transfer between the ports ac_1 and dc_1 depends on what ac_1 is connected to. If ac_1 is connected to a three-phase resistive load, it is sufficient to set the three-phase ac voltages using the duty cycles calculated according to (5). If ac_1 is connected to a three-phase grid, a closed-loop control, e.g., the indirect current control described in [31], is used.

[1]The local average of a considered variable is equal to the average value of this variable calculated over a switching period, T_s.

This controller slightly adjusts $D_{1,a,b,c}(t)$ in order to shape the mains-side phase currents according to the given requirements (e.g., sinusoidal with defined amplitude and in phase to the corresponding phase voltage). However, since the modulation scheme described in this paper is related to the operation of the DAB part of the D3ABC, it is irrelevant whether the duty cycles are determined by open- or closed-loop control. The same applies to the ports ac_2 and dc_2, whereas the power transfer between these two ports is controlled by slightly adjusting $D_{2,A,B,C}$. The energy exchange between the dc link capacitors connected to dc_1 and dc_2 is achieved in analogy to a DAB converter, i.e., the square-wave voltage (e.g. $v_{n,a}$) at the switching node of a primary-side half-bridge is shifted by a certain HF phase with respect to the square-wave voltage (e.g. $v_{N,A}$) at the switching node of the secondary-side half-bridge of the same converter phase. This leads to the formation of the typical transformer current of a DAB converter. The associated power flow between the primary-side and secondary-side dc link capacitors can be described using the local average value of the instantaneous power. For example,

$$\begin{aligned}\langle p_{aA}\rangle_{T_s}(t) = \langle p_{aA}\rangle(t) &= \frac{1}{T_s}\int_0^{T_s} p_{aA}(t+\tau)\,\mathrm{d}\tau \\ &= \frac{1}{T_s}\int_0^{T_s} v_{1a}(t+\tau)\, i_{L\sigma,1a}(t+\tau)\,\mathrm{d}\tau \end{aligned} \tag{7}$$

applies to phase a. Thereby the half-bridges on the primary and secondary sides are switched with the same switching frequency. Fig. 4 illustrates the considered power transfers by means of a diagram.

Fig. 5(a) exemplarily depicts the waveform of the primary-side transformer current in phase a, for operation according to S1 in Table 2 and over two mains periods. Since the switching frequency is much higher than the mains frequency, the

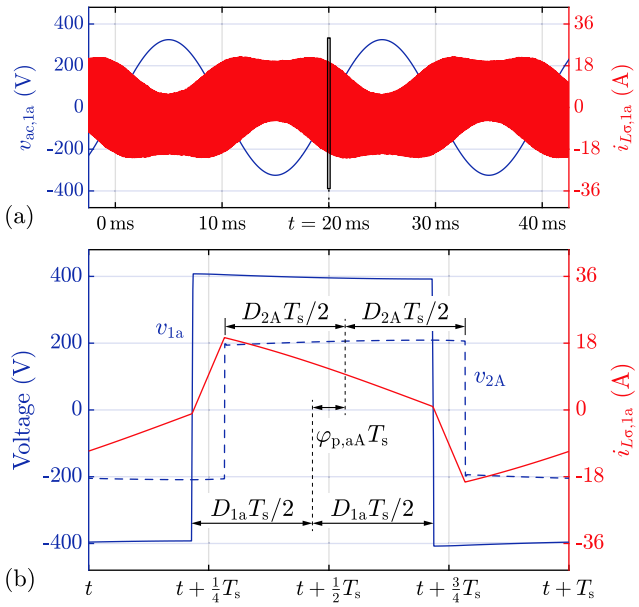

FIGURE 5. Simulated voltage and current waveforms of phase a for operation according to S1 in Table 2. (a) Sinusoidal input voltage, $v_{ac,1a}$, and primary-side transformer current, $i_{L\sigma,1a}$. (b) Transformer current, $i_{L\sigma,1a}$, together with the primary-side and secondary-side transformer voltages, v_{1a} and v_2 A, during one switching period, T_s, at $t \approx 20$ ms. Subfigure (b) reveals the definitions of the duty cycles, D_{1a} and D_2 A, and the HF phase shift $\varphi_{p,aA}$. Parameters as listed in Table 3.

transformer current waveform, $i_{L\sigma,1a}(t)$, appears as a continuous band.[2] Fig. 5(b) therefore shows a magnified view of a switching period in the region of the zero crossing of the line current ($t = 20$ ms), which reveals the characteristic waveform of the transformer current. It is worth noting that Fig. 5(b) is additionally used to define the duty cycles D_{1a} and D_2 A and the HF phase shift $\varphi_{p,aA}$. The same picture results for phases b and c, except for a time displacement of $\pm 20\,\text{ms}/3 = \pm 6.67$ ms.

B. SYNCHRONIZED LINE VOLTAGES AT AC_1 AND AC_2

Fig. 6 presents the results of a circuit simulation for operation according to S1 in Table 2 and with synchronized line voltages at ac_1 and ac_2. In this context, Fig. 6(a) and (b) show the waveforms of the phase voltages and phase currents present at ac_1 and ac_2 as well as the dc voltages and dc currents present at dc_1 and dc_2.

Fig. 6(c) depicts the waveforms of the duty cycles $D_{1a}(t)$ and $D_{2A}(t)$ as well as the HF phase shift $\varphi_{p,aA}$. Direct comparison of $v_{ac,1a}$ in Fig. 6(a) and $D_{1a}(t)$ in Fig. 6(c) reveals that, due to the relationship described by (3), $D_{1a}(t) - 0.5$ is practically proportional to $v_{ac,1a}$ (the same is true for $D_{2A}(t) - 0.5$ and $v_{ac,2A}$). Moreover, the modulation scheme described in [21] applies a constant HF phase shift, $\varphi_{p,aA}$, in the steady state.

Fig. 6(d) shows the instantaneous powers at the four ports of the D3ABC, which agree with the values for S1 listed in Table 2. It is well known that rectifier or inverter operation in the balanced three-phase system (e.g., power conversion between ac_1 and dc_1) results in a constant local average value of the power at the dc link. This explains the waveforms of $p_{ac,1}(t)$ and $p_{ac,2}(t)$ in this figure, which are practically constant except for switching-frequency fluctuations.

Fig. 6(e) reveals the waveforms of the local average values of the powers of the three DAB converter stages, $\langle p_{aA}\rangle$, $\langle p_{bB}\rangle$, and $\langle p_{cC}\rangle$, which, for the investigated mode of operation, are sinusoidal and phase-shifted with respect to each other by $\pm 120°$. Accordingly, the total power of the DAB part of the D3ABC,

$$\langle p_\Sigma\rangle = \langle p_{aA}\rangle + \langle p_{bB}\rangle + \langle p_{cC}\rangle, \tag{8}$$

is constant. For this reason, no power pulsations with frequencies in the range of the line frequencies occur at the dc link capacitors, which allows the realization of the converter with comparably small dc link capacitors.

C. OPERATION WITH DIFFERENT LINE FREQUENCIES AT AC_1 AND AC_2

Fig. 7 presents the results of a circuit simulation for operation according to S2 in Table 2, i.e., for a line frequency of $f_2 = 77$ Hz at ac_2. Accordingly, the voltages of corresponding phases of the three-phase system of the primary side [Fig. 7(a)] and the secondary side [Fig. 7(b)] are not synchronous anymore. According to (3) and (4), this leads to unequal duty cycles in corresponding converter phases (e.g., primary-side phase a and secondary-side phase A), as shown in the example of phases a and A in Fig. 7(c).

The sum of the powers in the three DAB converter stages, $\langle p_\Sigma\rangle$, shown in Fig. 7(e) contains pronounced LF components, in contrast to the simulation with $f_1 = f_2$ shown in Fig. 6(e). The pronounced LF components in $\langle p_\Sigma\rangle$ lead to variations in the dc-link voltages and distortions in the phase currents. Since the phase current controller (implemented as described in [31]) keeps the voltage on the primary-side dc link almost constant, a major part of the power pulsation is transferred to ac_1 and thus to the grid. However, the dc link voltage on the secondary side is not controlled (HF phase shift is kept constant) and therefore the power pulsation is split between the ports dc_2 and ac_2. This explains the non-constant power waveforms for the three ports ac_1, dc_2, and ac_2 shown in Fig. 7(d).

The non-sinusoidal total power, $\langle p_\Sigma\rangle$, plotted in Fig. 7(e) reveals spectral components at $f_2 - f_1 = 27$ Hz and $2(f_2 - f_1) = 54$ Hz in addition to the dc component with a power of ≈ 8 kW, as shown in Fig. 8. As described in the introduction, especially the component at $f_2 - f_1$ is a challenge for filtering and should therefore be eliminated by using a suitable modulation scheme.

[2]The presumable phase shift of 180° between $v_{ac,1a}$ and $i_{L\sigma,1a}$ in Fig. 5(a) is not present in reality. Instead, the shape of the current band is a result of different positive and negative current peak values of $i_{L\sigma,1a}(t)$ due to the DAB converter operation during a mains period. For more details, the reader is referred to Section II in [21].

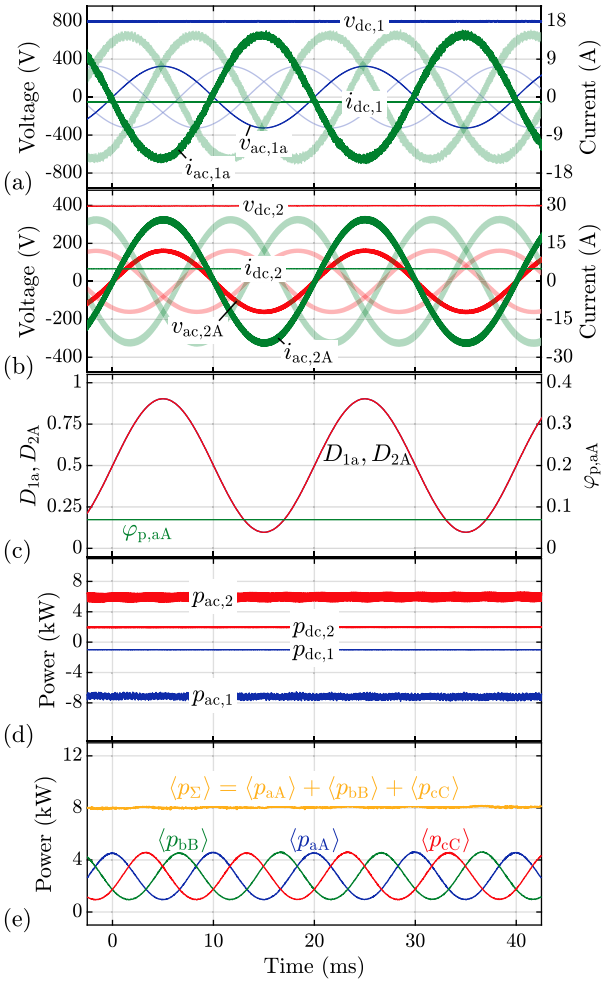

FIGURE 6. Simulation results for the operation of the D3ABC with synchronized line voltages at the ports ac_1 and ac_2 (S1 in Table 2) using the parameters given in Table 3: (a) primary-side voltages and currents, (b) secondary-side voltages and currents, (c) duty cycles and the HF phase shift at phase a, (d) power levels at the four ports, and (e) local average values of the powers of the three DAB converter stages and the resulting total power, $\langle p_\Sigma \rangle$. Apart from switching-frequency fluctuations, the powers at the four ports and the total power of the DAB part show practically constant waveforms, i.e., no LF components are present.

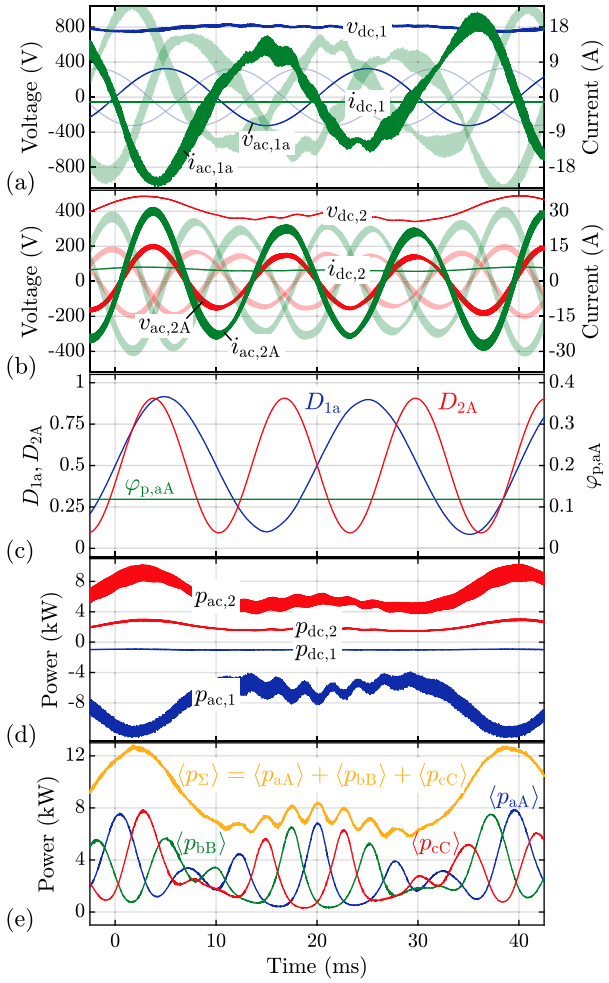

FIGURE 7. Simulation results for converter operation according to S2 in Table 2, i.e., for a line frequency of $f_2 = 77$ Hz at ac_2: (a) primary-side voltages and currents, (b) secondary-side voltages and currents, (c) duty cycles and the HF phase shift at phase a, (d) power levels at the four ports, and (e) local average values of the powers of the three DAB converter stages and the resulting total power, $\langle p_\Sigma \rangle$. The pronounced LF components in $\langle p_\Sigma \rangle$ lead to fluctuating dc link voltages and distorted phase currents. As a result, the powers at the dc and ac ports are no longer constant.

III. ELIMINATION OF LF POWER PULSATION

Based on the consideration that symmetric three-phase systems are present at the primary-side and secondary-side ac ports, the LF components in $\langle p_\Sigma \rangle$ exclusively occur in the DAB part of the D3ABC, as discovered in Section II-C. Furthermore, according to (5) and (6), the waveforms of the three-phase line voltages at ac_1 and ac_2 already specify the waveforms of the primary-side and secondary-side duty cycles. Hence, only the HF phase shifts, $\varphi_{p,aA}$, $\varphi_{p,bB}$, and $\varphi_{p,cC}$, remain as degrees of freedom. This also implies that the power flow between the ports ac_1 and dc_1 or between ac_2 and dc_2 has no influence on LF components in the currents of the dc link capacitors. Consequently, the powers at dc_1 and dc_2 can be set to zero without limiting the generality.

A. CONSIDERED CONSTRAINTS

In a first step, three constraints are defined for the functions of the power waveforms of the three DAB converter phases,

$$\langle p_\Sigma \rangle (t) = \langle p_{aA} \rangle (t) + \langle p_{bB} \rangle (t) + \langle p_{cC} \rangle (t) \stackrel{!}{=} P_\Sigma = \text{const.}, \tag{9}$$

$$\langle p_{aA} \rangle (t) \stackrel{!}{=} \langle p_{bB} \rangle (t - T/3) \stackrel{!}{=} \langle p_{cC} \rangle (t + T/3), \tag{10}$$

$$\left| \langle p_{aA,bB,cC} \rangle (t) \right| \leq P_{max}(D_{1,a,b,c}(t), D_{2,A,B,C}(t)). \tag{11}$$

The first constraint, (9), formulates the suppression of the LF components in the total power, $\langle p_\Sigma \rangle (t)$. Constraint (10) enforces that the waveforms of $\langle p_{aA,bB,cC} \rangle$ have the same shape except that they are phase-shifted with respect to each other by 120°. There, T denotes the effective period of $\langle p_{aA,bB,cC} \rangle$. The aim of (10) is to achieve even loading of the phases.

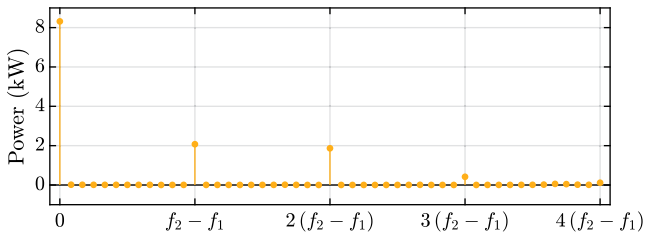

FIGURE 8. The total power in the DAB part of the D3ABC, $\langle p_\Sigma \rangle$, as shown in Fig. 7(e), in the frequency domain. In addition to the dc component with a power of ≈ 8 kW, spectral components at $f_2 - f_1 = 27$ Hz and $2(f_2 - f_1) = 54$ Hz are clearly visible.

Finally, the third constraint, (11), ensures that the power in each phase never exceeds the maximum possible power, $P_{\max}(D_{1,\mathrm{a,b,c}}(t), D_{2,\mathrm{A,B,C}}(t))$, of the corresponding converter phase. This third constraint also leads to a limit for the total power,

$$-P_{\Sigma,\max} \le P_\Sigma \le P_{\Sigma,\max}. \tag{12}$$

The achievable value for $P_{\Sigma,\max}$ is determined in this Section as part of the development of the modulation scheme.

A simple approach which fulfills (9), (10), and (11) is presented in [29]. There, constant and equal power is used in all three phases, $\langle p_{\mathrm{aA}} \rangle = \langle p_{\mathrm{bB}} \rangle = \langle p_{\mathrm{cC}} \rangle = \text{const.} = P_\Sigma/3$. However, this approach results in a maximum power of only $P_{\Sigma,\max} = 2.9\,\mathrm{kW}$, which is significantly less than the rated power of 8 kW that is available for operation from ac_1 to dc_2, which the converter was designed for [21]. This is, because a single phase of the D3ABC can transfer only comparably low power between the primary and the secondary side if the duty cycles of the same phase have values close to zero or one. Consequently, the development of an improved modulation scheme is based on the idea that the power shortfall of those DAB converter stages, which are operated at a given time with duty cycles close to zero or one, is compensated by an increased power of the remaining converter stages.

In the new approach, the power in each phase is adjusted based on a polynomial function that depends on the primary-side and secondary-side duty cycles,

$$\begin{aligned}\langle p \rangle(t) = P_0 \big[\, & a_0 + a_1 \tilde{D}_1(t) + a_2 \tilde{D}_1(t)^2 + a_4 \tilde{D}_1(t)^4 \\ & + b_1 \tilde{D}_2(t) + b_2 \tilde{D}_2(t)^2 + b_4 \tilde{D}_2(t)^4 \,\big] \\ \tilde{D}_1(t) = D_1(t) - \frac{1}{2},\ & \tilde{D}_2(t) = D_2(t) - \frac{1}{2}.\end{aligned} \tag{13}$$

The scaling factor P_0 in (13) was determined in the course of the analysis of the operating modes of the DAB presented in [29] and contains all hardware-specific values,

$$P_0 = \frac{n\, T_\mathrm{s}\, V_{\mathrm{dc1}}\, V_{\mathrm{dc2}}}{2 L_\sigma}. \tag{14}$$

It is to be noted that the indices denoting the converter phases are omitted in (13) to provide a more comprehensible description of the subsequent derivations. Accordingly, the variables p, D_1, and D_2 are to be replaced by the variables of the DAB converter part to be evaluated, e.g., by p_{aA}, $D_{1,\mathrm{a}}$, and $D_{2,\mathrm{A}}$ in case of converter phases a-A. As shown in Appendix A, (13) is conceived in such a way that a significant increase of P_Σ is achieved (compared to the previous approach presented in [29]) and that the constraints (9) and (10) are met for sinusoidal duty cycles according to (5) and (6), regardless of the values of the seven coefficients, $a_0 \ldots b_4$. Thus, the coefficients must be selected such that the third constraint (11) is also fulfilled, which is described in the following Subsection.

B. DERIVATION OF THE MODULATION SCHEME

In this Subsection, first, the power transfer characteristic of a single DAB converter phase is investigated to gain a better understanding of the constraints associated with the transferable power. Thereafter, different considerations on possible simplifications are made. The findings obtained in this context reveal that only two coefficients of (13) remain. The expressions for these remaining coefficients are derived in a subsequent step.

The maximum power that can be transferred by each phase, $P_{\max}(D_1, D_2)$, is calculated with the expressions derived in [29] and summarized in Appendix A. The contour plot presented in Fig. 9(a) illustrates the characteristic of $P_{\max}(D_1, D_2)/P_0$ for $D_1, D_2 \in [0, 1]$. In order to fulfill (11), $\langle p \rangle$ must be less than $P_{\max}(D_1, D_2)$ in the complete range of D_1 and D_2,

$$\frac{1 - m_{\max}}{2} = D_{1,\min} \le D_1 \le D_{1,\max} = \frac{1 + m_{\max}}{2}, \tag{15}$$

$$\frac{1 - m_{\max}}{2} = D_{2,\min} \le D_2 \le D_{2,\max} = \frac{1 + m_{\max}}{2}, \tag{16}$$

where, for simplicity, same maximum modulation indices are considered on the primary and secondary sides,

$$0 \le m_1 \le m_{\max}, \quad 0 \le m_2 \le m_{\max}. \tag{17}$$

The dotted blue rectangle in Fig. 9(a) illustrates the boundary of the area defined with (15) and (16) for $m_{\max} = 0.81$, that results for operation according to Table 2. It should be noted that all four considered scenarios, S1 to S4, result in the same $m_{\max} = 0.81$. It is apparent from Fig. 9(a) that $P_{\max}(D_1, D_2)$ decreases if the duty cycles differ from 0.5 and reaches zero for duty cycles equal to 0 or 1.

Within the dotted blue rectangle, the lowest achievable power is present at the corners. To have a more detailed view of the corners, a cross-sectional drawing is shown in Fig. 9(b) for the dash-dotted diagonal intersection line shown in Fig. 9(a). The dashed orange line refers to the characteristic of the normalized maximum power of a DAB converter phase, $P_{\max}/P_0$, for $D_2 = 1 - D_1$. In view of this characteristic, it may be reasonable to assume that the power at the corners of the duty-cycle ranges defined with (15) and (16),

$$P_\mathrm{c} = \langle p \rangle (D_{1,\min}, D_{2,\max}) = \langle p \rangle (D_{1,\max}, D_{2,\min}), \tag{18}$$

has to be considered to determine the coefficients of (13), to ensure that the D3ABC never exceeds the maximum feasible power. However, at this operating point also the polynomial (13) returns the lowest value within the considered

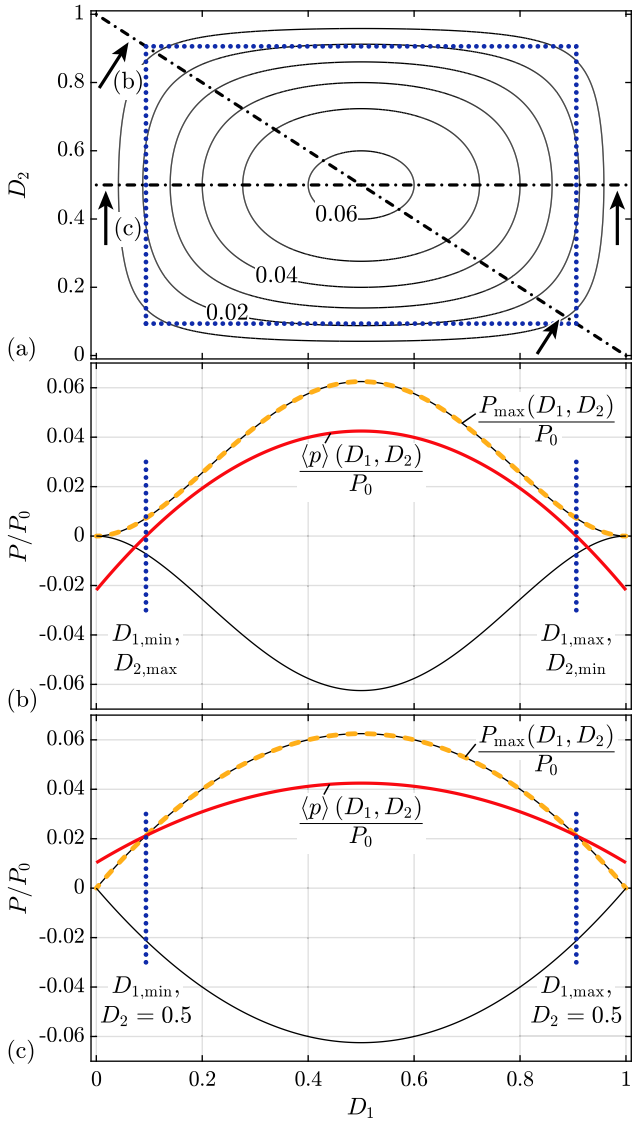

FIGURE 9. (a) Contour plot of the maximum normalized power in a single DAB converter phase with respect to D_1 and D_2. The dotted blue rectangle refers the boundary of operation defined with (15) and (16). (b), (c) Cross sections through (a) projected onto the D_1-(P/P_0)-plane, which result for the cut edges defined by $D_2 = 1 - D_1$ and $D_2 = 0.5$, respectively. The red line anticipates the maximum power that can be achieved with the described method in the DAB converter part of one phase, which within the operating range is always below the maximum power (dashed orange line).

ranges of D_1 and D_2 [in anticipation of the result, the shape of $\langle p \rangle$ is plotted as solid red line in Fig. 9(b)]. Since (13) is conceived such that the sum over the three phase powers is constant, i.e., the remaining converter phases compensate for the missing power, the operating point at the corner is not necessarily the most critical. Instead, it is found in the course of the derivation of useful expressions for the coefficients of $\langle p \rangle$ that the operating conditions $D_1 = 0.5$, $D_2 = D_{2,\min,\max}$ and $D_2 = 0.5$, $D_1 = D_{1,\min,\max}$ are of major importance. Therefore, Fig. 9(c) shows a corresponding cross-sectional drawing for $D_2 = 0.5$, i.e., for the dash-dotted horizontal intersection line marked in Fig. 9(a). The power at the edge of the operating range, e.g., $D_1 = D_{1,\min}$ and $D_2 = 0.5$, is denoted by P_e,[3]

$$P_e = \langle p \rangle (D_{1,\min}, D_2 = 0.5) = \langle p \rangle (D_{1,\max}, D_2 = 0.5). \tag{19}$$

Based on these observations, the number of required coefficients can be reduced and the remaining coefficients determined. With (17) and due to the symmetry of the D3ABC (i.e., the primary and secondary sides can be swapped without changing the circuit), $a_1 = b_1$, $a_2 = b_2$, and $a_4 = b_4$ must hold true. Furthermore, the function of $\langle p \rangle$ is intended to be symmetric around the operating point $D_1 = D_2 = 0.5$, since maximum power can be transferred there, which leads to $a_1 = b_1 = 0$. Finally, to further simplify the problem, only a quadratic polynomial is considered in a first approach, i.e., $a_4 = b_4 = 0$ applies. With these considerations and simplifications, solely the coefficients a_0 and a_2 need to be determined such that (11) is fulfilled.

In the last step, a connection is made between the maximum transferrable power and the remaining coefficients, a_0 and a_2, to obtain the final expressions for a_0 and a_2. In this context, it is recalled that (13) is designed such that (10) is fulfilled. As a consequence, the global average values of the powers of the three phase, i.e., evaluated over $-\infty \leq t \leq +\infty$, are equal to one third of the total power. As a side note, it is worth noting that the average value of a sum term can be calculated by adding the average values of the individual terms,

$$\begin{aligned} \frac{1}{T}\int_0^T [y_1(t) + y_2(t)]\mathrm{d}t &= \frac{1}{T}\int_0^T y_1(t)\mathrm{d}t + \frac{1}{T}\int_0^T y_2(t)\mathrm{d}t \\ &= \frac{1}{T_1}\int_0^{T_1} y_1(t)\mathrm{d}t + \frac{1}{T_2}\int_0^{T_2} y_2(t)\mathrm{d}t, \end{aligned} \tag{20}$$

where T, T_1, and T_2 refer to the periods of $y_1(t) + y_2(t)$, $y_1(t)$, and $y_2(t)$, respectively. In this regard (20) is applied to (13) to establish a relation between P_Σ, a_0, and a_2,

$$\frac{P_\Sigma}{3} = P_0 \left[a_0 + \frac{a_2 \, {m_{\max}}^2}{4} \right]. \tag{21}$$

Furthermore, a_0 and a_2 can be expressed as functions of P_c and P_e,

$$a_0 = \frac{1}{P_0}(2P_e - P_c), \; a_2 = \frac{4}{P_0 \, {m_{\max}}^2}(P_c - P_e), \tag{22}$$

by evaluating (13) at the operating points defined by (18) and (19) and subsequently solving for a_0 and a_2. If (22) is substituted into (21),

$$\frac{P_\Sigma}{3} = P_e \tag{23}$$

results, i.e., only P_e defines the average power. Accordingly, P_c remains as a degree of freedom. A numerical inspection of (11) shows that any value of P_c that satisfies $|P_c| \leq$

[3]Due to the definition (17), the same value for P_e results for $D_1 = 0.5$ and $D_2 = D_{2,\min}$ as well as $D_1 = 0.5$ and $D_2 = D_{2,\max}$.

$P_{\max}(D_{1,\max}, D_{2,\max})$ also satisfies (11). However, minimum rms values of the transformer currents result if P_e is set equal to the respective maximum power and P_c is set to zero,

$$P_e = P_{\max}(D_{1,\min}, D_2 = 0.5) = \frac{P_0}{16}\left(1 - {m_{\max}}^2\right), \quad (24)$$

$$P_c = P_{\max}(D_{1,\min}, D_{2,\max}) = 0. \quad (25)$$

With this, the final result is obtained,

$$a_{0,\max} = \frac{1}{8}\left(1 - {m_{\max}}^2\right), a_{2,\max} = \frac{1}{4}\left(1 - \frac{1}{{m_{\max}}^2}\right). \quad (26)$$

The solid red curves shown in Fig. 9(b) and (c) depict the results for (13), i.e., $\langle p \rangle (D_1, D_2)$, if (26) is applied. The results of a numerical analysis presented in Appendix B reveal that the obtained function for $\langle p \rangle (D_1, D_2)$ is less than or equal to the maximum phase power, $P_{\max}$, (dashed orange line) in the entire range defined by (15) and (16).

Finally, with (24) substituted into (23) the maximum total power,

$$P_{\Sigma,\max} = \frac{3}{16} P_0 \left(1 - {m_{\max}}^2\right) \quad (27)$$

is obtained. Note that $P_{\Sigma,\max}$ represents the maximum power that can be transmitted between primary side and secondary side through the three DAB converter stages of the D3ABC, using (13) (with $a_4 = b_4 = 0$) and the maximum modulation indices at the two ac ports as defined in (17). Thereby it is irrelevant whether the power transmitted over the galvanic isolation is supplied by the ac or dc port (e.g., of the primary side) or whether the load being supplied is connected to the ac or dc port (e.g., of the secondary side). The limitation of $P_{\Sigma,\max}$ is rooted in the power limitation known from DAB converters, due to which the transmitted power above a certain HF phase shift φ_p does not increase further but decreases as shown in Fig. 5 in [21]. If, for example, $P_{\Sigma,\max}$ is to be increased for a given converter, either $m_{\max}$ must be decreased or P_0 increased. A decrease of $m_{\max}$ results in a reduction of the maximum possible ac voltages at the ac ports. An increase of P_0 is achieved, e.g., by decreasing the leakage inductance L_σ or the switching frequency f_s.

Inserting the values listed for S1, S2, or S3 in Table 2 and Table 3 into (14) and (27) gives a maximum power of $P_{\Sigma,\max} = 8.5\,\text{kW}$, what is substantially higher than the maximum power of $P_{\Sigma,\max} = 2.9\,\text{kW}$ achieved with the simple approach described in [29]. This value, $P_{\Sigma,\max} = 8.5\,\text{kW}$, therefore represents the maximum theoretical total power for a specific hardware with given transformer parameters (L_σ, n) and given operating conditions ($V_{dc,1}$, $V_{dc,2}$, f_s). In this context, it is important to emphasize that $P_{\Sigma,\max}$ represents a theoretical limit and must not be mistaken for the maximum permissible operating power of the converter, which is determined on the basis of the maximum permissible stresses of the designed or selected converter components. Consequently, the component stresses must be considered separately, which is done in Appendix B using a numerical analysis.

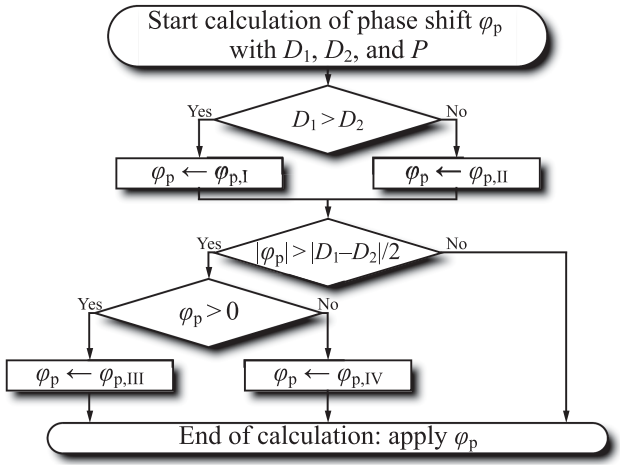

FIGURE 10. Algorithm used to determine the current operating mode of the DAB and to calculate the HF phase shift φ_p, as given in Appendix A.

It is noted that the functions for a_0 and a_2 derived in this Section can be directly used to operate the D3ABC with modulation indices smaller than $m_{\max}$. In this regard, the possible total power, $P_{\Sigma,\max}$, increases for smaller modulation indices. The expressions (26) are valid for operation at maximum power. However, the results of a numerical analysis show that the power in the DAB part of the D3ABC can be adjusted by scaling both coefficients at the ratio $r_p = P_\Sigma / P_{\Sigma,\max}$,

$$a_0 = a_{0,\max}\, r_p,\ a_2 = a_{2,\max}\, r_p. \quad (28)$$

With this, currents with nearly minimal rms values result into the switching nodes on primary and secondary side, $I_{1,\text{rms}}$ and $I_{2,\text{rms}}$, of the D3ABC, as described in Appendix B.

The functions for calculating the HF phase shifts $\varphi_{p,aA}(t)$, $\varphi_{p,bB}(t)$, and $\varphi_{p,cC}(t)$ that correspond to the phase powers, $\langle p_{aA} \rangle (t)$, $\langle p_{bB} \rangle (t)$, and $\langle p_{cC} \rangle (t)$, determined with (13) are provided in Appendix A and in [29]. Fig. 10 illustrates the flow chart of the algorithm used to determine the current operating mode of the DAB and to calculate the corresponding HF phase shift φ_p (described in Appendix A). Table 4 in Appendix A lists the expressions used for $\varphi_{p,I}$, $\varphi_{p,II}$, $\varphi_{p,III}$, and $\varphi_{p,IV}$. Fig. 11 shows a pseudocode for a runtime-optimized implementation of the algorithm implemented on the hardware demonstrator's Digital Signal Processor (DSP). The expression for the intermediate variable e_1 used in this implementation has been derived based on (13) together with the coefficients (28). The constant $m_q = m_{\max}^2$ defines the maximum modulation index that occurs during operation. The variables $D_1[1..3]$ and $D_2[1..3]$ denote the primary-side and secondary-side duty cycles present in each phase due to the line voltages, and the variables d_{11}, d_{12}, d_{22}, d_{21}, c_1, c_2, e_1, e_2, and e_3 serve as intermediate variables for calculating φ_p. Note: e_1 to e_3 correspond to the intermediate variables used in Table 4. The variable r_p denotes the scaling factor for the transferred power and has a value range of $-1 \le r_p \le 1$ ($r_p = 1$ corresponds to a power transferred from the primary

```
const m_q = 0.82 * 0.82                    // m_max * m_max
sub φ_p = calcPhi(D_1, D_2, r_p)
   for i = 1 to 3                          // 3 phases
      d_11 = D_1[i] * (1 - D_1[i])
      d_12 = D_1[i] * (1 - D_2[i])
      d_22 = D_2[i] * (1 - D_2[i])
      d_21 = D_2[i] * (1 - D_1[i])
      e_1 = d_11 + d_22 - (1 - m_q) / 2
      e_1 = e_1 * (1 - m_q) * r_p / 4 / m_q
      if D_1[i] > D_2[i]
         c_1 = 2 * d_21                    // Mode I
         c_2 = (D_1[i] - D_2[i]) / 2
      else
         c_1 = 2 * d_12                    // Mode II
         c_2 = (D_2[i] - D_1[i]) / 2
      end if
      if abs(e_1) > (c_1 * c_2)
         e_2 = d_11 * d_22
         e_3 = (d_12 + d_21) / 2
         if e_1 > 0
            φ_p = e_3 - sqrt(e_2 - e_1)    // Mode III
         else
            φ_p = sqrt(e_2 + e_1) - e_3    // Mode IV
         end if
      else
         φ_p = e_1 / c_1
      end if
   end for
end sub
```

FIGURE 11. Pseudocode of the algorithm implemented on the DSP of the hardware demonstrator for real-time calculation of the HF phase shift φ_p. The three lines highlighted in gray (two square roots and the division by a variable) indicate the most time-consuming calculations for the DSP used.

to the secondary side equal to $P_{\Sigma,\max}$, moreover, if $r_p < 0$, the power is transferred from the secondary to the primary side). The calculation is performed three times within a for-loop, once for each phase. The three lines highlighted in gray (two square roots and the division by a variable) indicate the most time-consuming calculations for the DSP used. The remaining calculations, i.e., additions, subtractions, multiplications, and divisions by constants have a comparatively short computing time due to the existing Floating-Point Unit (FPU). Using single-precision floating-point variables, the used DSP (TMS320F28335) can achieve a total calculation time that is less than one switching period. Consequently, the HF phase shifts of each phase, $\varphi_{p,aA}(t)$, $\varphi_{p,bB}(t)$, and $\varphi_{p,cC}(t)$, are updated once per switching period.

For completeness, also solutions with $a_4 = b_4 \neq 0$, i.e., based on a fourth-order polynomial according to (13), have been considered. The numerical results presented in Appendix B reveal that this enables a further increase of the theoretical power limit, $P_{\Sigma,\max}$, from 8.5 kW to 9.8 kW.[4] Apart from this, however, the solution with fourth-order polynomial does not show substantial advantages over the quadratic solution. For this reason and because of the significantly higher complexity of the fourth-order solution, this paper focuses on the quadratic solution.

[4]A specification of the dc link capacitances in per unit values would facilitate understanding whether a present power pulsation necessitates a large or small dc link capacitance. However, such normalization is not possible here, because the only reasonable characteristic frequency, which is required for such a normalization, is the fundamental frequency of the power pulsation, i.e., the difference frequency $|f_1 - f_2|$. This frequency depends on the operating conditions and is therefore not defined.

TABLE 3. Switching frequency and main component values of the hardware demonstrator. All circuit simulations in this paper use the same parameters.

Switching frequency	$f_s = 35\,\text{kHz}$
Primary-side dc link capacitors[4]	$C_{dc1} = 12\,\mu\text{F}$
Secondary-side dc link capacitors[4]	$C_{dc2} = 37\,\mu\text{F}$
Primary-side filter capacitors	$C_{f1} = 10\,\mu\text{F}$
Secondary-side filter capacitors	$C_{f2} = 21.5\,\mu\text{F}$
Primary-side ac inductances	$L_{ac,1} = 231\,\mu\text{H}$
Secondary-side ac inductances	$L_{ac,2} = 34\,\mu\text{H}$
Stray inductances	$L_\sigma = 89\,\mu\text{H}$
Transformers' turns ratio	$n = 2.6$

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

In this Section, the modulation scheme derived above for suppressing LF components in $\langle p_\Sigma \rangle$ when operating with $f_1 \neq f_2$ is verified using circuit simulations and hardware experiments. According to the explanation given at the beginning of Section III, the power flow between the ports ac_1 and dc_1 or between ac_2 and dc_2 has no effect on the LF components in the currents of the dc link capacitors. Therefore, to simplify the setup, no power is fed into or drawn from the terminals dc_1 and dc_2. Instead, plain ac–ac operation with power flowing from ac_1 to ac_2 is considered, with a three-phase voltage source, which provides sinusoidal voltages according to (1) (with $\theta_{a,b,c} \in \{0°, 120°, 240°\}$), connected to ac_1 and a three-phase load connected to ac_2.The three-phase load is formed by the star connection of three 5 Ω resistors. Simulation and experiment both use the same converter components, according to Table 3, to allow for a direct comparison of the results.

The implemented control scheme is the same as described in Section II-C, except that instead of the HF phase shift the variable r_p is constant.

A. SIMULATION RESULTS

Fig. 12 depicts the result of the circuit simulation for converter operation according to S3 in Table 2, showing the primary-side voltages and currents in Fig. 12(a) and those of the secondary side in Fig. 12(b). Fig. 12(d) presents the waveforms of the instantaneous powers at the four ports of the D3ABC. The local average values of the instantaneous powers at the ports of the D3ABC are approximately constant, except for minor residual LF components. The phase powers of the DAB part, shown in Fig. 12(e), are shaped such that the sum of the three phase powers is almost constant, $\langle p_\Sigma \rangle = 8\,\text{kW}$. The remaining fluctuations in the power $\langle p_\Sigma \rangle$ are due to simplifications in the power calculation (e.g., piecewise linear currents in the inductors are assumed, thus neglecting the feedback effects of the voltages across the filter capacitances C_{f1} and C_{f2}), voltage distortions due to dead-time effects, and time delays caused by the signal processing and the PWM units. Due to these influences, the effective DAB power in the three phases deviates from the calculated power, which results in the small fluctuations of the total power $\langle p_\Sigma \rangle$. It is further apparent that the waveforms of $\langle p_{aA} \rangle$, $\langle p_{bB} \rangle$, and $\langle p_{cC} \rangle$ are similar except for a time shift, indicating that condition (10) is also satisfied.

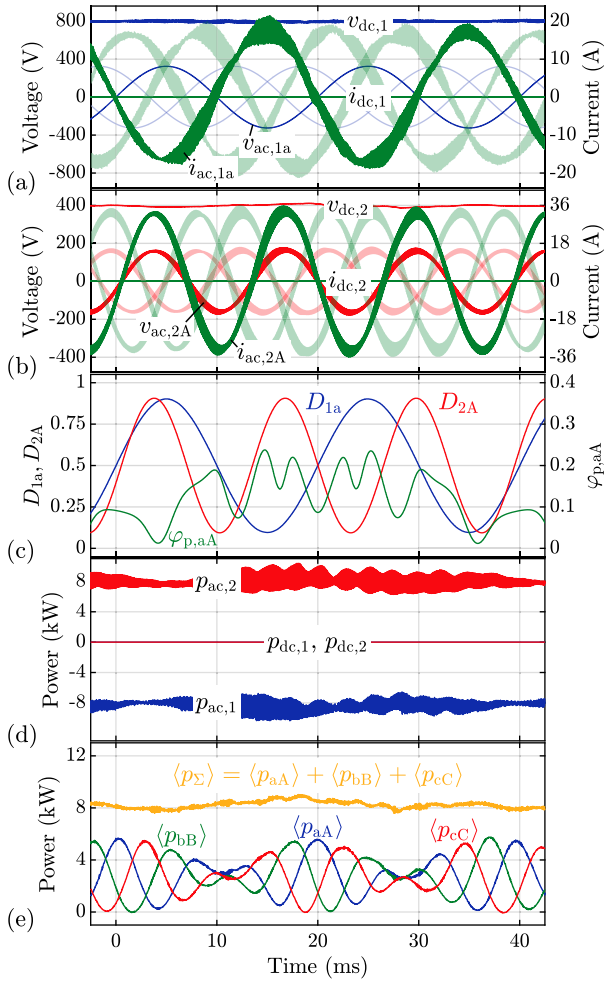

FIGURE 12. Simulation results for converter operation according to S3 in Table 2, using the proposed modulation scheme: (a) primary-side voltages and currents, (b) secondary-side voltages and currents, (c) duty cycles and HF phase shift at phase a, (d) power levels at the four ports, and (e) local average values of the powers of the three DAB converter stages and the resulting total power, $\langle p_\Sigma \rangle$. Compared to Fig. 7, the developed modulation scheme nearly eliminates the LF components in $\langle p_\Sigma \rangle$.

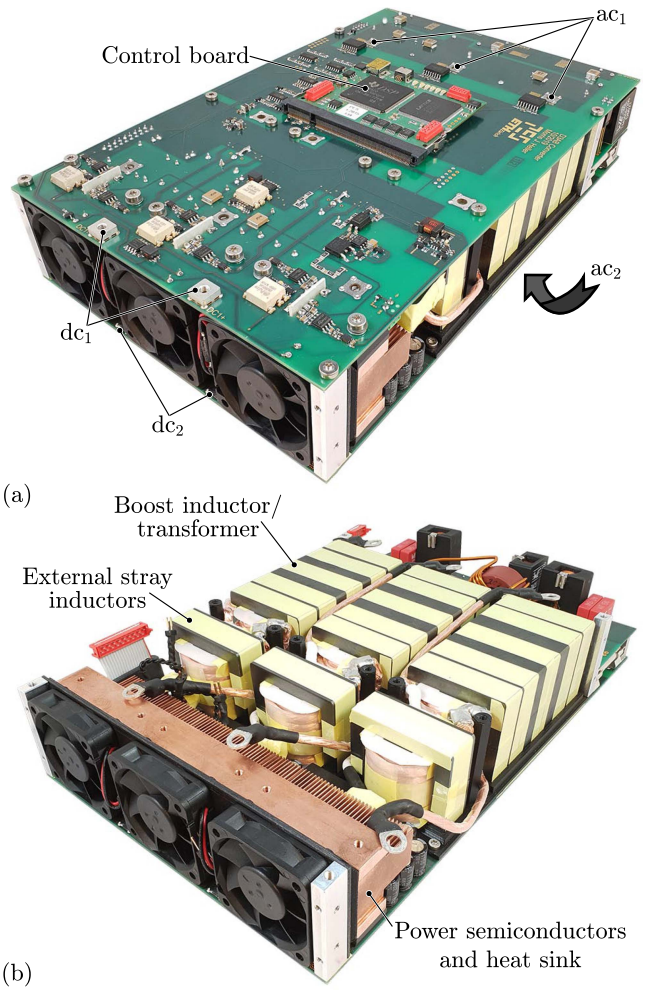

FIGURE 13. (a) Hardware demonstrator of the D3ABC featuring an output power of 8 kW for rectifier operation with galvanic isolation, i.e., from ac_1 to dc_2. The port ac_2 is located at the bottom of the converter and is therefore not visible on this picture. The overall dimensions are 150 *mm* × 240 *mm* × 54 *mm* = 5.91 *in* × 9.45 *in* × 2.13 *in* (width × depth × height). (b) Picture without top PCB revealing heat sink, three coupled boost inductors, and three external stray inductors, which are used to increase the stray inductances of the coupled boost inductors according to the needs of the D3ABC. The labeled magnetic components are those of phase a.

Fig. 12(c) shows the waveforms of the duty cycles and the HF phase shift, which the waveform of p_{aA} is based on. This figure reveals the highly dynamic changes of the HF phase shifts that are required to meet the constraints (9), (10), and (11) defined at the beginning of Section III-A.

B. EXPERIMENTAL VERIFICATION

Fig. 13 shows the hardware demonstrator of the D3ABC and reveals three of the four ports (port ac_2 is at the bottom of the hardware and therefore not visible on this picture). The demonstrator has been originally designed for operation from ac_1 to dc_2 (isolated rectifier operation) considering $f_1 = f_2$ as described in [21]. The maximum peak current in the leakage inductance for this operation with $f_1 = f_2$ is calculated to be $I_{L\sigma,1,\text{peak}} \approx 20\,A$, which is approximately half of the value that is calculated for operation with $f_1 \neq f_2$ as shown in Fig. 20. To avoid saturation of the leakage inductance when operating with $f_1 \neq f_2$, all voltages are reduced by a factor of 1/2 as listed for S4 in Table 2. The reduction of the dc link voltages by 1/2 results according to (14) in a reduction of the power by a factor of 1/4, which leads to $P_\Sigma = 2\,\text{kW}$.

To make the measurements obtained with the hardware demonstrator directly comparable with the simulation results, the two simulations in Figs. 7 and 12 are repeated with reduced power according to S4 in Table 2. Accordingly, Figs. 14 and 15(c) present both the simulation results and the measurement results in the same way, such that a direct comparison is possible. The simulation results shown in Fig. 14(a) and (b) are obtained when operating with constant HF phase shift, i.e., without the derived modulation scheme. The power in

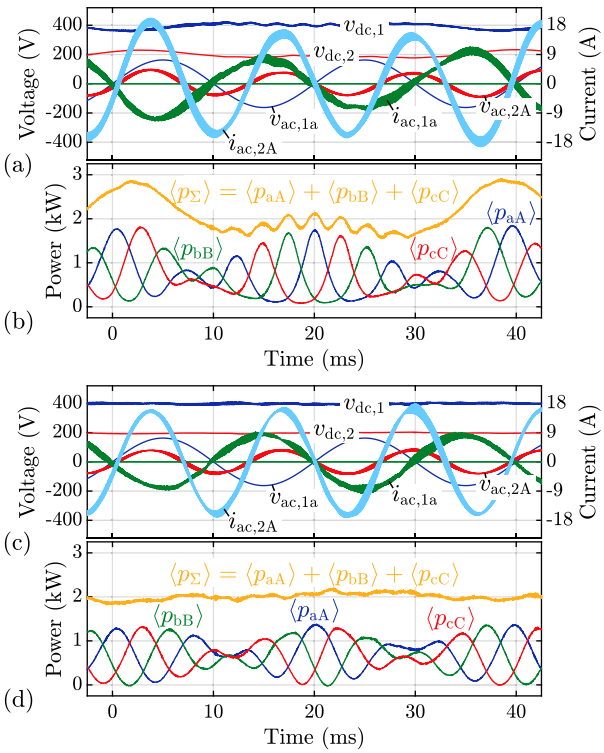

FIGURE 14. Two simulation results for converter operation according to S4 in Table 2, w/o (a,b) and w/ (c,d) the proposed modulation scheme: (a) and (c) Dc link voltages, phase voltages, and phase currents of phases a/A on primary and secondary side. (b) and (d) Local average values of the powers of the three DAB converter stages and the resulting total power $\langle p_\Sigma \rangle$.

the DAB part of the D3ABC, $\langle p_\Sigma \rangle$, plotted in Fig. 14(b), shows pronounced LF components that, as Fig. 14(a) illustrates, lead to variations in the dc-link voltages and distortions in the phase currents. The simulation results obtained with the derived modulation scheme depicted in Fig. 14(c) and (d) show that the LF components in $\langle p_\Sigma \rangle$ almost disappear and therefore the fluctuations of the dc-link voltages are much smaller.

Fig. 15 depicts the measured waveforms during a time span of 50 ms. Fig. 15(a) shows the primary-side dc link voltage, phase voltages, and phase currents and Fig. 15(b) depicts secondary-side dc link voltage, phase voltages, and phase currents. Fig. 15(c) shows the dc link voltages, the phase voltages, and the phase currents of phases a/A, i.e., both the primary side and secondary side. Fig. 15(a) reveals a phase shift of 180° between the phase voltages and the phase currents, indicating rectifier operation at ac_1. The waveforms in Fig. 15(b) of the output-side phase voltages, measured from the terminals to the star point of the load, are sinusoidal with a frequency of $f_2 = 77$ Hz and in phase with the currents, indicating inverter operation at ac_2. The measurement shown in Fig. 15(c) agree well with the simulation results in Fig. 14(c). Specifically, the dc link voltages, $v_{dc,1}$ and $v_{dc,2}$, show almost constant waveforms, indicating that the LF power pulsations are eliminated by the modulation

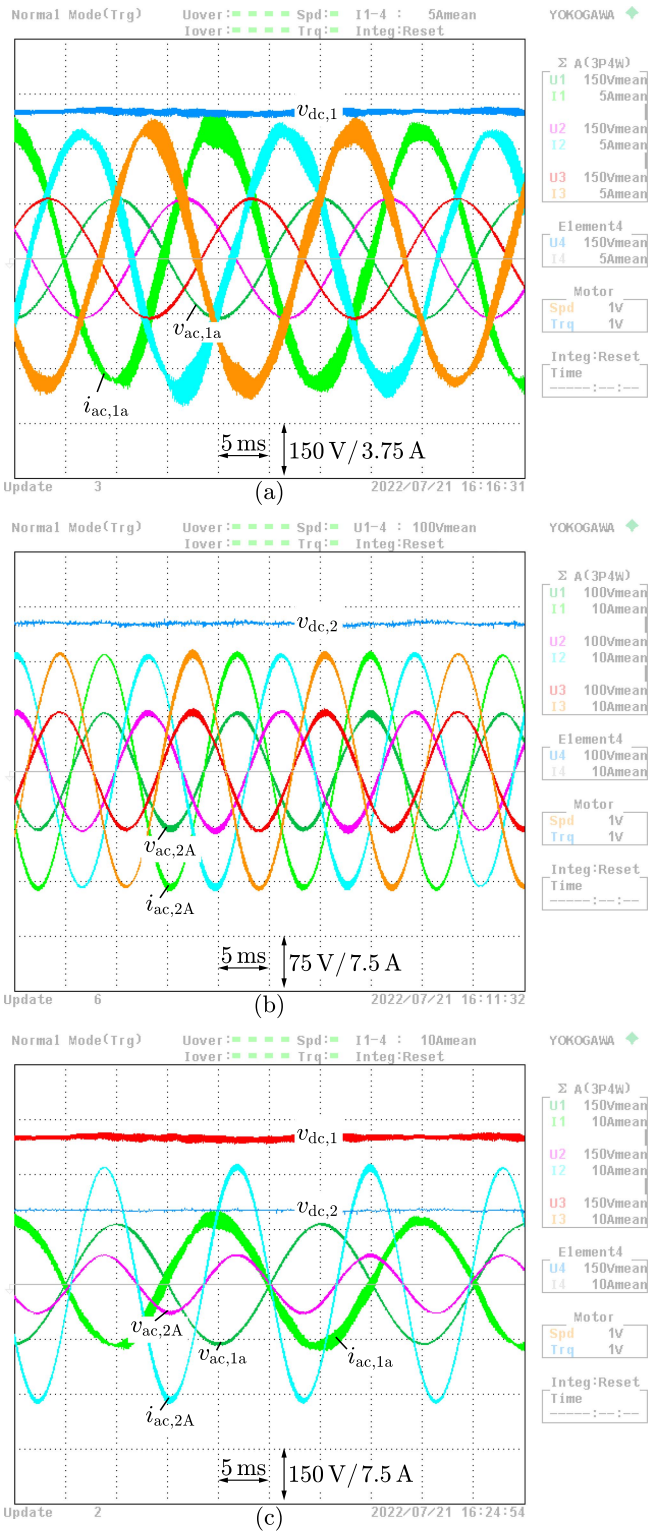

FIGURE 15. Measurement results for converter operation according to S4 in Table 2. (a) primary-side voltages and currents, (b) secondary-side voltages and currents, and (c) dc link voltages, phase voltages, and phase currents of phases a/A on primary and secondary side. The waveforms in (c) agree well with the simulation results in Fig. 14(c). Specifically, the dc link voltages, $v_{dc,1}$ and $v_{dc,2}$, show almost constant waveforms, indicating that the LF power pulsations are eliminated by the modulation scheme.

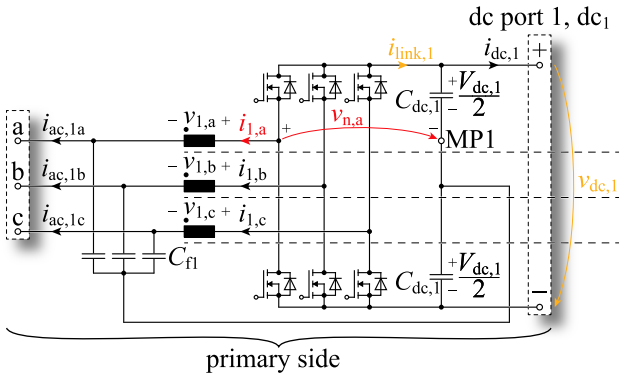

FIGURE 16. Section of the D3ABC from Fig. 1 highlighting the voltages and currents that need to be measured to determine the power in the DAB part, $\langle p_\Sigma \rangle$. Either the dc link voltage and the current in the dc link are measured, $v_{\mathbf{dc,1}}$ and $i_{\mathbf{link,1}}$, or the voltages and currents of the three switching nodes (see $v_{\mathbf{n,a}}$ and $i_{\mathbf{1,a}}$ highlighted for phase a).

scheme. A direct measurement of the power in the DAB part of the D3ABC, $\langle p_\Sigma \rangle$, would show the elimination of LF power pulsations even better. However, the power $\langle p_\Sigma \rangle$ is difficult to measure. Fig. 16 shows two possible measurement methods to determine $\langle p_\Sigma \rangle$. The first method requires the dc link voltage and the current in the dc link, $v_{\mathrm{dc},1}$ and $i_{\mathrm{link},1}$. These measured values, multiplied and averaged over a switching period as in (7), result in $\langle p_\Sigma \rangle + p_{\mathrm{ac},1}$. Based on this measurement result, the waveform of $\langle p_\Sigma \rangle$ can be determined if the waveform of $p_{\mathrm{ac},1}$ is measured with, for example, a power analyzer. However, $i_{\mathrm{link},1}$ is not accessible, because this current is distributed over a planar conductor configuration, which realizes the connection between the dc-link capacitance and the semiconductors to keep the commutation loop inductance as small as possible. The second method requires the voltages and the currents at the three switching nodes (e.g., $v_{\mathrm{n,a}}$ and $i_{1,\mathrm{a}}$ marked in Fig. 16 in case of phase a). These measured values, multiplied for each phase, averaged over one switching period, and summed up over all three phases, also give $\langle p_\Sigma \rangle + p_{\mathrm{ac},1}$. These voltages and currents are accessible, but both contain main switching frequency components. For this reason, the measurements of the powers at the switching nodes are not feasible with the available measurement equipment, e.g., the available power analyzer.

In a second experiment, the capability of the presented modulation scheme is further assessed by generating a three-phase voltage with time-changing frequency, f_2, and modulation index, m_2, at the port ac_2. An application scenario could be an asynchronous machine with V/F control, i.e., the voltage of the motor is increased proportionally to the frequency, ramping up the asynchronous machine at port ac_2 from standstill. In this context, the voltage sources at port ac_1 remain unchanged. At port ac_2, the asynchronous machine is emulated by inductors, which are connected in parallel to the load resistors.

Fig. 17 depicts the measured waveforms of $v_{\mathrm{ac,1a}}$, $i_{\mathrm{ac,1a}}$, $v_{\mathrm{ac,2A}}$, $i_{\mathrm{ac,2A}}$, $v_{\mathrm{dc},1}$, and $v_{\mathrm{dc},2}$ during a time span of 1 s.

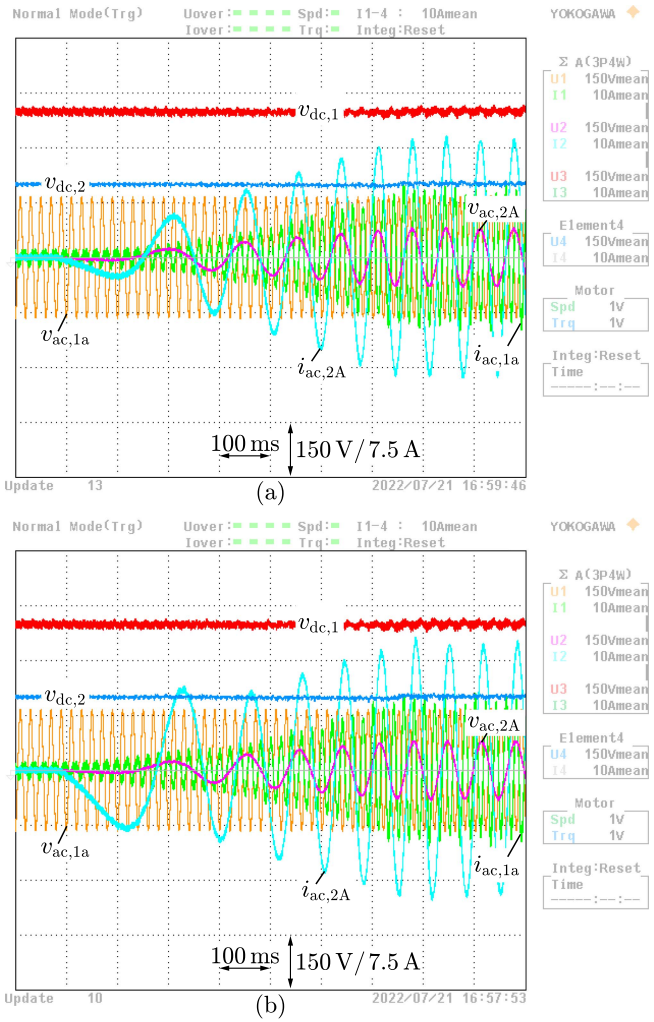

FIGURE 17. (a) Measurement results for an example scenario where the modulation index and frequency are varied on the secondary side. The current in the primary-side phase a, $i_{\mathbf{ac,1a}}$, increases as the voltage across the resistive load, $v_{\mathbf{ac,2}}$ A, increases. During this process, the primary- and secondary-side dc link voltages, $v_{\mathbf{dc,1}}$ and $v_{\mathbf{dc,2}}$, remain constant. (b) The same setup as (a) but with a resistive-inductive load.

Fig. 17(a) is measured with a pure resistive and Fig. 17(b) with a resistive-inductive load connected to ac_2. During the first 100 ms of the measurement, $v_{\mathrm{ac,2\,A}} = i_{\mathrm{ac,2\,A}} = 0$ apply. Accordingly, a small amplitude results for the primary-side phase current, $i_{\mathrm{ac,1a}}$, since the power drawn from the voltage sources only has to cover the losses of the converter and the reactive power demand of the input filter. After $t = 5$ ms, the line frequency, f_2, and the modulation index at port ac_2 are increased at constant rates of 20 Hz/s and 1.07 s^{-1}, respectively. At the same time, the amplitude of the phase current of the primary-side phase a, $i_{\mathrm{ac,1a}}$, increases proportionally to the output power, which increases quadratically over time. At $t \approx 750$ ms, the D3ABC reaches the final output frequency and amplitude of 15 Hz and 80 V, respectively. During the entire process, the primary- and secondary-side dc link voltages, $v_{\mathrm{dc},1}$ and $v_{\mathrm{dc},2}$, remain constant.

V. CONCLUSION

This paper proposes a duty-cycle dependent phase shift modulation scheme to prevent LF power pulsations in the D3ABC. Such LF power pulsations occur, e.g., if the D3ABC is operated with different line frequencies, $f_1 \neq f_2$, at its primary-side and secondary-side ac ports. Compared to a previous study [29], the new approach increases the transmittable power of the DAB part by a factor of 2.9, i.e., from 2.7 kW to 8.5 kW.

The effectiveness of the developed modulation scheme is verified by means of circuit simulations and experimental evaluations. The circuit simulations are conducted for an output power of 8 kW, which is delivered to a three-phase resistive load at the secondary-side three-phase port ac_2. The rms values of the primary-side and secondary-side phase voltages are $V_{\mathrm{ac},1} = 230\,\mathrm{V}$ and $V_{\mathrm{ac},2} = 115\,\mathrm{V}$, respectively, and the line frequencies are $f_1 = 50\,\mathrm{Hz}$ and $f_2 = 77\,\mathrm{Hz}$, respectively. The simulation results confirm constant power in the DAB part, resulting in approximately constant dc link voltages

The experimental verification conducted for $f_1 = 50\,\mathrm{Hz}$ and $f_2 = 77\,\mathrm{Hz}$ confirms the proper operation of the proposed modulation scheme, as well. Since the realized converter was designed for a power transfer between the ports ac_1 and dc_2, and power transfer between the ports ac_1 and ac_2 leads to higher currents in the power stage of the D3ABC, the experimental verification has been conducted for a reduced power of 2 kW and the voltages have been halved. The measured voltages and currents agree well with the simulation results.

In a second experiment, the operation with time-varying rms values and frequencies of the voltages at port ac_2 is investigated. A possible application of this is the V/F control of an asynchronous machine. In this operating scenario, the dc link voltages also exhibit constant characteristics. This indicates that the described modulation scheme remains effective even in the case of time-varying modulation indices and/or line frequencies.

APPENDIX

A. OPERATING MODES OF THE DAB CONVERTER PART

Since the three converter phases of the D3ABC can be considered separately, only the DAB part of one converter phase is examined in this Section. Accordingly, simplified designations for the voltages at the switching nodes and the current in the DAB converter inductance can be used. For example, if phase a is considered,

$$v_1 = v_{1\mathrm{a}}, \qquad v_2' = \frac{v_{2\mathrm{A}}}{n}, \qquad i_1 = i_{L\sigma,1\mathrm{a}} \tag{29}$$

applies.

According to (7), the power transferred in a DAB converter phase depends on the characteristics of v_1, v_2', and i_1. Accordingly, the duty cycles D_1 and D_2 and the HF phase shift φ_p that are present during a switching period have an impact on the power transferred in a DAB converter phase.

For the evaluation of (7), it is assumed that the inductor current waveform, $i_1(t)$, can be approximated by a piecewise linear function, as shown in Fig. 18. Thus, the integral in (7) is separated into time intervals with constant values for v_1 and v_2, i.e., intervals during which $i_1(t)$ changes linearly, and the determined subexpressions are summed up.

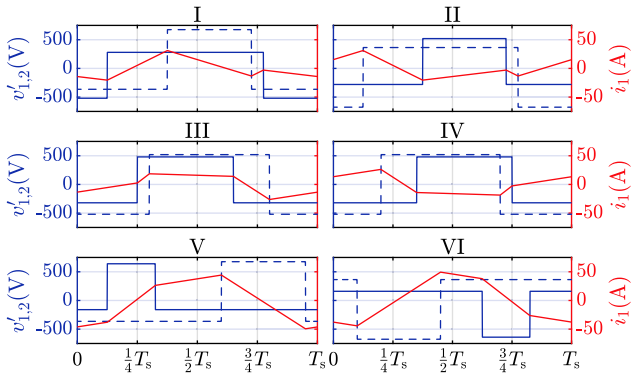

FIGURE 18. Illustration of the six operating modes of the DAB part of the D3ABC, showing calculated waveforms of v_1, v_2', and i_1 over one switching period, T_s; $2\pi f_s L_\sigma \approx 19.6\,\Omega$, $n = 2.6$, $V_{\mathrm{dc1}} = 800\,\mathrm{V}$, and $V_{\mathrm{dc2}} = 400\,\mathrm{V}$.

TABLE 4. Conditions for Operating Modes i to IV and Solutions for the HF Phase Shift, φ_p, for Each Operating Mode That Sets the Power Level of a Single DAB Converter Phase Equal to the Reference Power, P

Mode	Conditions	φ_p
I	$\lvert\varphi_\mathrm{p}\rvert < \frac{D_1-D_2}{2} \wedge D_1 > D_2$	$\varphi_{\mathrm{p,I}} = \frac{e_1}{2D_2(1-D_1)}$
II	$\lvert\varphi_\mathrm{p}\rvert < \frac{D_2-D_1}{2} \wedge D_1 < D_2$	$\varphi_{\mathrm{p,II}} = \frac{e_1}{2D_1(1-D_2)}$
III	$\varphi_\mathrm{p} > \frac{\lvert D_1-D_2\rvert}{2} \wedge \varphi_\mathrm{p} < \frac{D_1+D_2}{2}$	$\varphi_{\mathrm{p,III}} = e_3 - \sqrt{e_2 - e_1}$
IV	$\varphi_\mathrm{p} < -\frac{\lvert D_1-D_2\rvert}{2} \wedge \varphi_\mathrm{p} > -\frac{D_1+D_2}{2}$	$\varphi_{\mathrm{p,IV}} = -e_3 + \sqrt{e_2 + e_1}$
	$e_1 = P/P_0$	
	$e_2 = D_1\,(1-D_1)\,D_2\,(1-D_2)$	
	$e_3 = \frac{1}{2}\,[D_1\,(1-D_2) + D_2\,(1-D_1)]$	

The operation with different input and output frequencies, $f_1 \neq f_2$, leads to different functions for the duty cycles on the primary and the secondary sides, $D_1(t) \neq D_2(t)$, cf. (5) and (6). As a consequence, it turns out in the course of the evaluation of (7) that a distinction must be made between a total of six different operating modes, which are illustrated in Fig. 18. However, it is found that the operating modes V and VI are redundant with respect to the transferable power, but lead to transformer currents with increased rms values. Therefore, the presented modulation scheme only uses the operating modes I to IV. Furthermore, maximum positive power is achieved with mode III and minimum negative power with mode IV.

Table 4 lists the conditions which must apply for a certain operating mode to be present, as well as the resulting expressions for the HF phase shifts for the various operating modes. Table 5 presents the power limits depending on the considered operating mode. Further details, e.g., the description of an algorithm used to determine the current operating mode, are described in [29].

B. RESULTS OF THE NUMERICAL ANALYSIS

This section describes the implementation of the procedure used for numerical verification of the results in Appendix B1 and discusses the obtained results in Appendix B2.

TABLE 5. Expressions for the Minimum and Maximum Power Levels, P_{min} and P_{max}, That are Feasible in Each Operating Mode

	φ_P	Power
I	$\frac{D_1-D_2}{2}$	$P_{\mathrm{I,max}} = P_0\left[D_2\left(1-D_1\right)\left(D_1-D_2\right)\right]$
	$\frac{D_2-D_1}{2}$	$P_{\mathrm{I,min}} = P_0\left[-D_2\left(1-D_1\right)\left(D_1-D_2\right)\right]$
II	$\frac{D_2-D_1}{2}$	$P_{\mathrm{II,max}} = P_0\left[D_1\left(1-D_2\right)\left(D_2-D_1\right)\right]$
	$\frac{D_1-D_2}{2}$	$P_{\mathrm{II,min}} = P_0\left[-D_1\left(1-D_2\right)\left(D_2-D_1\right)\right]$
III	$\frac{D_1(1-D_2)+D_2(1-D_1)}{2}$	$P_{\mathrm{III,max}} = P_0\left[D_1\left(1-D_1\right)D_2\left(1-D_2\right)\right]$
	–	$P_{\mathrm{III,min}} = \begin{cases} P_{\mathrm{I,max}}, D_1 > D_2 \\ P_{\mathrm{II,max}}, D_1 < D_2 \end{cases}$
IV	–	$P_{\mathrm{IV,max}} = \begin{cases} P_{\mathrm{I,min}}, D_1 > D_2 \\ P_{\mathrm{II,min}}, D_1 < D_2 \end{cases}$
	$-\frac{D_1(1-D_2)+D_2(1-D_1)}{2}$	$P_{\mathrm{IV,min}} = P_0\left[-D_1\left(1-D_1\right)D_2\left(1-D_2\right)\right]$

1) NUMERICAL DERIVATION OF THE MODULATION SCHEME

The numerical procedure is used to numerically determine valid values for the coefficients a_0, $a_1 = b_1$, $a_2 = b_2$, and $a_4 = b_4$, i.e., values that satisfy condition (11). Regarding the studied operating point, the voltages given for S3 in Table 2 are considered, leading to $m_1 = m_2 = 0.81$. The component values considered are listed in Table 3. Loads on the dc ports are omitted, i.e., solely ac–ac operation is considered.

In a first step, $\langle p\rangle(t)$ is examined without fourth-order terms, i.e., for $a_4 = 0$. Initially, 200 uniformly distributed values in the range between -10 and $+10$ are considered for each coefficient, e.g., for a_0: $a_0 \in \{-10.0, -9.9, -9.8, \ldots, 9.9, 10.0\}$. There, the limits -10 and 10 are chosen sufficiently large to ensure that optimal solutions are not missed; e.g., $a_2 = 10$ leads to $\langle p\rangle > 40P_{\mathrm{max}}$ for $D_1 = D_2 = 0.5$.

In the subsequent computational run, compliance with (11) is checked for each of the $200 \times 200 \times 200$ combinations of coefficients. For this purpose, $n_{\mathrm{D}} = 100$ evenly distributed values are calculated for each duty cycle, D_1 and D_2, within the ranges defined by (15) and (16), e.g., $D_1 \in \{0.095, 0.103, 0.111, \ldots, 0.905\}$. For each of the $n_{\mathrm{D}} \times n_{\mathrm{D}}$ combinations of duty cycles, $C_{\mathrm{D}} \in \{(0.095, 0.095), (0.103, 0.095), (0.111, 0.095), \ldots, (0.905, 0.905)\}$, the value of $\langle p\rangle$ that results for the currently considered coefficients is calculated according to (13). This value must be in between the minimum and the maximum power of the D3ABC for each duty-cycle combination of C_{D} ($P_{\mathrm{IV,min}}$ and $P_{\mathrm{III,max}}$, respectively, in Table 5). If the power is outside these limits, the corresponding set of coefficients is marked as invalid.

After this computational run, the ranges of invalid coefficients are examined in order to enable a refinement of the resolution of the coefficients. For example, if the results for the boundary regions of $a_0 \in \{-10.0, -9.9, -9.8\}$ and $a_0 \in \{9.8, 9.9, 10\}$ are marked as invalid for any combinations of a_1 and a_2, the following calculation run is performed for $-9.8 \leq a_0 \leq 9.8$, again for 200 uniformly distributed values. These boundaries are checked and adjusted individually for each coefficient. The above described computational run is repeated until the boundaries do not change between two runs. Table 6 lists the resulting boundaries. For $a_4 \neq 0$ the analysis is the same as for $a_4 = 0$. However, since it turned out during the investigation that $a_1 = 0$ leads to most valid solutions (an indication of this is also the narrowly defined range for a_1 in Table 6), the analysis for $a_4 \neq 0$ was performed for $a_1 = 0$. The boundaries for $a_4 \neq 0$ are also given in Table 6.

TABLE 6. Numerically determined boundaries for a_0, a_1, a_2, and a_4 for quadratic and fourth-order polynomials for $\langle p\rangle$, cf. (13).

	a_0	a_1	a_2	a_4
Quadratic polynomial $\langle p\rangle$	± 0.048	± 0.0092	± 0.16	0
Fourth-order polynomial $\langle p\rangle$	± 0.0496	0	± 0.05488	± 0.64

Three different criteria are used to further assess suitable values for the coefficients a_0, a_2, and a_4. The first criterion is the square of the rms value of the current into the switching node of a primary-side half-bridge (e.g. $i_{1,\mathrm{a}}$ in case of phase a, cf. Fig. 1), since this is a measure for the conduction losses in the converter.[5] The second criterion is the peak value of the current in L_σ, which is proportional to the peak value of the magnetic flux in the core of L_σ and is thus a measure for the size of the inductor's magnetic core.[6] The third criterion is the switching losses of the primary-side and secondary-side semiconductors, which are calculated based on the measured losses published in [32] and [33], respectively.

Due to the ac–ac operation of the inverter, the voltages and currents in each phase of the D3ABC change continuously. Therefore, the global time average values of the above evaluation criteria are calculated in a final step, i.e., the average values that result for a duration that approaches infinity, $T \to \infty$. Provided that the ratio between the two ac frequencies, f_1/f_2, is an irrational number,[7] this average value of $x(\tilde{D}_1, \tilde{D}_2)$ can be calculated according to

$$\langle x\rangle_{T\to\infty} = \frac{1}{\pi^2}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} x(\tilde{D}_1, \tilde{D}_2)\Big|_{\substack{\tilde{D}_1=\frac{1}{2}m_1\sin(\alpha)\\ \tilde{D}_2=\frac{1}{2}m_2\sin(\beta)}} \mathrm{d}\alpha\mathrm{d}\beta. \tag{30}$$

Using the substitution rule, the double integral from (30) can be rewritten into a double integral with respect to D_1 and D_2,

$$\langle x\rangle_{T\to\infty} = \int_{D_{2,\mathrm{min}}}^{D_{2,\mathrm{max}}}\int_{D_{1,\mathrm{min}}}^{D_{1,\mathrm{max}}} F_{D_1}F_{D_2}x(D_1, D_2)\,\mathrm{d}D_1\mathrm{d}D_2, \tag{31}$$

[5]The rms value of the current into the switching node of a secondary-side half-bridge shows a similar characteristic and is therefore not explicitly shown.

[6]At a given total power, the peak currents in the primary-side and secondary-side filter coils, $I_{Lac,1,peak}$ and $I_{Lac,2,peak}$, are practically independent of the investigated coefficients and were therefore disregarded.

[7]The effective period of the superposition of two sinusoidal signals with different frequencies approaches infinity, $T \to \infty$, if the ratio of the two frequencies is irrational. This guarantees that each duty-cycle combination occurs once within the range defined by (15) and (16). For the case considered in this paper, i.e., $f_1 = 50\,\mathrm{Hz}$ and $f_2 = 77\,\mathrm{Hz}$, the effective period is 1 s and thus, considerably higher than the periods of the two line frequencies. Accordingly, (30) approximates the mean values very well for this case.

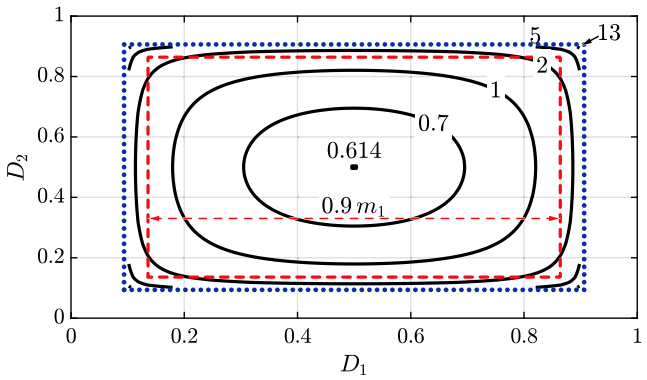

FIGURE 19. Contour plot of the product $F_{D_1}F_{D_2}$ with the functions defined in (32) with $m_1 = m_2 = m_{\max} = 0.81$. The dotted blue rectangle refers to the boundary of operation defined with (15) and (16). The value at each point within this boundary can be understood as the joint probability density function of the duty-cycle combination (D_1, D_2). At the corners of the boundary the value of $F_{D_1}F_{D_2}$ approaches infinity. The integral over the area enclosed by the boundary is equal to 1. The red dashed rectangle with edge length $m_1 \sin(\pi/\sqrt{8}) \approx 0.9\,m_1$ corresponds to a median of the joint probability density function.

$$F_{D_1} = \frac{2}{\pi m_1 \sqrt{1 - \frac{(2D_1-1)^2}{m_1{}^2}}}, F_{D_2} = \frac{2}{\pi m_2 \sqrt{1 - \frac{(2D_2-1)^2}{m_2{}^2}}}. \tag{32}$$

Here, $F_{D_1}(D_1)$ and $F_{D_2}(D_2)$ can be considered as density functions and the product $F_{D_1}F_{D_2}$, shown in Fig. 19, can be understood as the joint probability density function of the occurrence of the duty-cycle combination (D_1, D_2).

2) DISCUSSION OF CALCULATED COMPONENT STRESSES

Fig. 20 presents the results for the global average values of $I^2_{1,\mathrm{rms}}$, $P_{\mathrm{sw},1}$, and $P_{\mathrm{sw},2}$ and the global maximum value of $I_{L\sigma,1,\mathrm{peak}}$ in a converter phase with respect to the total power of the D3ABC.

The green areas represent the results calculated by numerical analysis, which are obtained by choosing a quadratic polynomial for $\langle p \rangle$, i.e., $a_4 = b_4 = 0$. The red dashed curves show the results that are obtained if the coefficients are calculated according to (28). A direct comparison of these two results indicates that the analytically calculated coefficients can be used to achieve practically the minimum rms currents. In addition, near-optimal peak currents in L_σ and switching losses are obtained. The maximum transmissible power is $P_{\Sigma,\max,\mathrm{D}^2} = 8.5\,\mathrm{kW}$ which, apart from a slight deviation of $20\,W$ (corresponding to 0.2 %), agrees well with the power calculated in Section III-B.

The blue areas represent the additional solutions that can be obtained if a fourth-order polynomial is chosen for $\langle p \rangle$. It is mainly noticeable that the maximum transmittable power can then be increased to $P_{\Sigma,\max,\mathrm{D}^4} = 9.8\,\mathrm{kW}$. Apart from this, small reductions of as much as $-3\,\%$ in peak current values in L_σ can be achieved. However, a detailed analysis shows that this comes at the cost of an increase in the current rms values $I_{1,\mathrm{rms}}$ and $I_{2,\mathrm{rms}}$, e.g., at $P_\Sigma = 8\,\mathrm{kW}$ both

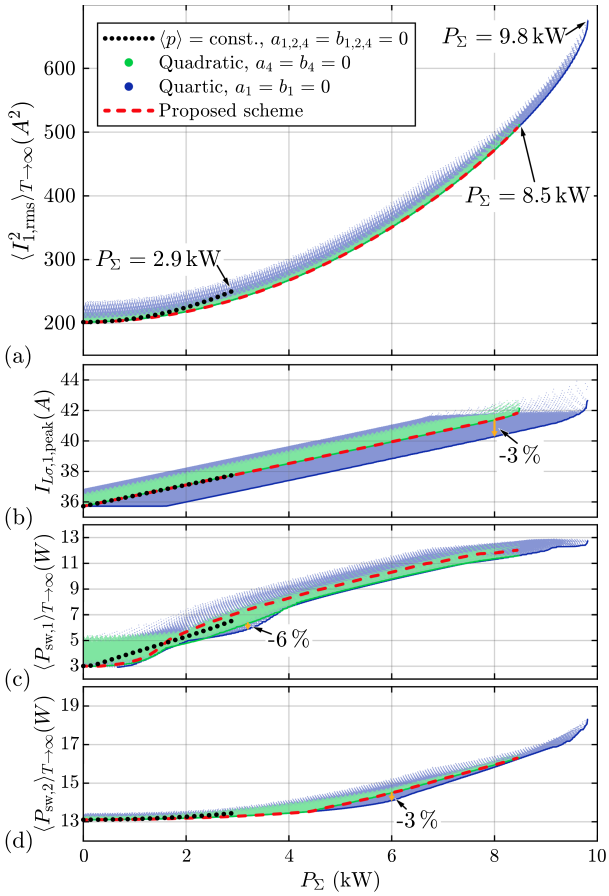

FIGURE 20. Selected component stresses of a phase versus total power transmitted over the DAB part of the D3ABC, P_Σ, determined with a numerical analysis for quadratic and fourth-order polynomials of $\langle p \rangle$. Each point on the area corresponds to a combination of coefficient values which fulfill (11). The voltage and component values used are listed in Table 2 and Table 3, respectively and $f_1 \neq f_2$ is assumed. (a) Global time average value of the square of the rms current into a switching node on the primary side. (b) Global maximum value for the peak current in the leakage inductor. (c), (d) Global time average switching losses for a half-bridge on the primary and secondary side, respectively. The black dotted line corresponds to the resulting component stresses for the modulation scheme presented in [29]. The red dashed line corresponds to the values obtained with the modulation scheme presented in this paper. The presented results have been determined for pure ac–ac operation, from ac_1 to ac_2. Since the converter is considered lossless, P_Σ is equal to the power transferred from ac_1 to ac_2.

$\langle I^2_{1,\mathrm{rms}} \rangle_{T\to\infty}$ and $\langle I^2_{2,\mathrm{rms}} \rangle_{T\to\infty}$ increase by 2 % respectively. Similarly, the switching losses depicted in Fig. 20(c) and (d), can be reduced by 6 % (for $P_\Sigma = 3.2\,\mathrm{kW}$) and 3 % (for $P_\Sigma = 5.2\,\mathrm{kW}$). However, this improvement is associated with an increase in $\langle I^2_{1,\mathrm{rms}} \rangle_{T\to\infty}$ and $\langle I^2_{2,\mathrm{rms}} \rangle_{T\to\infty}$ by 4 % and 2 %, respectively. Due to the limited advantages and the substantially higher effort required to analyze and implement the approach using the fourth-order polynomial for $\langle p \rangle$, it is not considered further in this paper.

The black dotted lines in Fig. 20 refer to the results obtained with the approach proposed in [29], i.e., for $\langle p \rangle = P_\Sigma/3 =$ constant, which is equivalent to $a_{1,2,4} = b_{1,2,4} = 0$. Accordingly, the solutions calculated with this approach represent

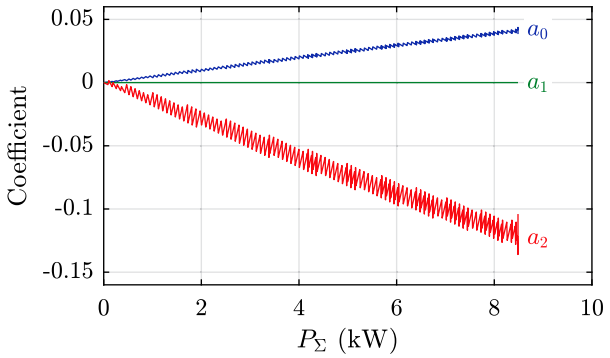

FIGURE 21. Values of the coefficients for all points on the green area in Fig. 20(a) that lead to minimum values for $\langle I^2_{1,\mathrm{rms}}\rangle_{T\to\infty}$ at given power, P, i.e., the points located at the bottom edge of the green area. As can be seen, the values of the coefficients are approximately proportional to the power. Based on these results, the linear scaling of the coefficients is proposed according to (28).

a subset of the solutions discussed in this section. Direct comparison shows that even this very simple approach leads to near-optimal results for the chosen criteria. However, this choice of coefficients has the disadvantage of a comparatively low value for the maximum power of $P_{\Sigma,\max,\mathrm{D}^0} = 2.9\,\mathrm{kW}$. Finally, Fig. 21 depicts the values of those coefficients that lead to minimum current rms values for the quadratic approach at given power P_Σ. In Fig. 20(a), these are the points located at the bottom edge of the green area. As can be seen from Fig. 21, the values of the coefficients are approximately proportional to the power P_Σ. In addition, the values of the coefficients at maximum power, $P_\Sigma = 8.5\,\mathrm{kW}$, agree with the values calculated with (26). Based on these results, the linear scaling of the coefficients is proposed according to (28).

REFERENCES

[1] H. Farhangi, "The path of the smart grid," *IEEE Power Energy Mag.*, vol. 8, no. 1, pp. 18–28, Jan./Feb. 2010.

[2] T. Dragicevic, J. C. Vasquez, J. M. Guerrero, and D. Skrlec, "Advanced LVDC electrical power architectures and microgrids: A step toward a new generation of power distribution networks," *IEEE Electrific. Mag.*, vol. 2, no. 1, pp. 54–65, Mar. 2014.

[3] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical control of droop-controlled AC and DC microgrids–A general approach toward standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, Jan. 2011.

[4] J. Mohammadi, F. B. Ajaei, and G. Stevens, "Grounding the DC microgrid," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 4490–4499, Sep./Oct. 2019.

[5] B. Liu et al., "An AC–DC hybrid multi-port energy router with coordinated control and energy management strategies," *IEEE Access*, vol. 7, pp. 109069–109082, 2019.

[6] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three-phase PWM AC-AC converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011.

[7] F. Feng, F. Wu, and H. B. Gooi, "Impedance shaping of isolated two-stage AC-DC-DC converter for stability improvement," *IEEE Access*, vol. 7, pp. 18601–18610, 2019.

[8] A. Mallik and A. Khaligh, "Intermediate DC-link capacitor reduction in a two-stage cascaded AC/DC converter for more electric aircrafts," *IEEE Trans. Veh. Technol.*, vol. 67, no. 2, pp. 935–947, Feb. 2018.

[9] R. Yamada, Y. Nemoto, S. Fujita, and Q. Wang, "A battery charger with 3-phase 3-level t-type PFC," in *Proc. IEEE Int. Telecommun. Energy Conf.*, Osaka, Japan, 2015, pp. 1–5.

[10] S. Madhusoodhanan et al., "Three-phase 4.16 kV medium voltage grid tied AC-DC converter based on 15 kV/40 A SiC IGBTs," in *Proc. IEEE Energy Convers, Congr. Expo.*, Montreal, QC, Canada, 2015, pp. 6675–6682.

[11] J. Song, W. Ding, D. Yang, H. Bai, C. Zhang, and B. Duan, "A novel three-phase single-stage isolated AC-DC converter with symmetrical structure for battery charger," in *Proc. Conf. Veh. Control Intell.*, Hefei, China, 2019, pp. 1–5.

[12] H. Kim, H. Belkamel, J. Park, R. M. Hakim, and S. Choi, "Modular three-phase single-stage isolated AC-DC converter for electrolytic capacitor-less EV DC charging," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, 2020, pp. 1573–1578.

[13] Y. Jang, M. M. Jovanovic, M. Kumar, Y. Chang, Y. W. Lin, and C. L. Liu, "A two-switch, isolated, three-phase AC-DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10874–10886, Nov. 2019.

[14] H. Jeong, J. Lee, T. Song, and S. Choi, "Three-phase single-stage bidirectional electrolytic capacitor-less AC-DC converter with minimum switch count," in *Proc. IEEE Energy Convers., Congr. Expo.*, Singapore, 2021, pp. 2011–2015.

[15] K. Ali, S. K. Dube, P. Das, J. C. -H. Peng, and D. J. Rogers, "Improvement of ZVS range and current quality of the nine-switch single-stage AC–DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4658–4668, May 2020.

[16] D. Das, N. D. Weise, K. Basu, R. Baranwal, and N. Mohan, "A bidirectional soft-switched DAB-based single-stage three-phase AC-DC converter for V2G application," *IEEE Trans. Transp. Electrific.*, vol. 5, no. 1, pp. 186–199, Mar. 2019.

[17] K. Shigeuchi, J. Xu, N. Shimosato, and Y. Sato, "A modulation method to realize sinusoidal line current for bidirectional isolated three-phase AC/DC dual-active-bridge converter based on matrix converter," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 6015–6029, May 2021.

[18] M. Silva, N. Hensgens, J. A. Oliver, P. Alou, O. Garcia, and J. A. Cobos, "Isolated Swiss-forward three-phase rectifier with resonant reset," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4795–4808, Jul. 2016.

[19] B. Zhang, S. Xie, Z. Li, P. Zhao, and J. Xu, "An optimized single-stage isolated Swiss-type AC/DC converter based on single full-bridge with midpoint-clamper," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11288–11297, Oct. 2021.

[20] A. U. Barbosa, B. R. de Almeida, D. d. S. Oliveira, P. P. Praca, and L. H. S. C. Barreto, "Multi-port bidirectional three-phase AC-DC converter with high frequency isolation," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1386–1391.

[21] F. Krismer, E. Hatipoglu, and J. W. Kolar, "Novel isolated bidirectional integrated dual three-phase active bridge (D3AB) PFC rectifier," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 3805–3812.

[22] Y. Shi, R. Li, Y. Xue, and H. Li, "High-frequency-link-based grid-tied PV system with small DC-link capacitor and low-frequency ripple-free maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 328–339, Jan. 2016.

[23] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308–1319, Mar. 2013.

[24] H.-S. Jung, S.-J. Chee, S.-K. Sul, Y.-J. Park, H.-S. Park, and W.-K. Kim, "Control of three-phase inverter for AC motor drive with small DC-link capacitor fed by single-phase AC source," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1074–1081, Mar. 2014.

[25] R. Chen, Y. Liu, and F. Z. Peng, "A solid state variable capacitor with minimum capacitor," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5035–5044, Jul. 2017.

[26] Y. Liu and F. Z. Peng, "DC capacitor-less solid-state variable capacitor," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3540–3550, Mar. 2021.

[27] A. Marcos-Pastor, E. Vidal-Idiarte, A. Cid-Pastor, and L. Martinez-Salamero, "Minimum DC-link capacitance for single-phase applications with power factor correction," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 5204–5208, Jun. 2020.

[28] J. Bohler, F. Krismer, and J. W. Kolar, "Analysis of low frequency grid current harmonics caused by load power pulsation in a 3-phase PFC rectifier," in *Proc. Int. Conf. Smart Grid Renewable Energy*, 2019, pp. 1–6.

[29] M. J. Heller, F. Krismer, and J. W. Kolar, "Quad-port AC–DC–DC–AC operation of isolated dual three-phase active bridge converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 1643–1650.
[30] M. J. Heller, F. Krismer, and J. W. Kolar, "EMI filter design for the integrated dual three-phase active bridge (D3AB) PFC rectifier," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14527–14546, Dec. 2022.
[31] J. Dixon and Boon-Teck Ooi, "Indirect current control of a unity power factor sinusoidal current boost type three-phase rectifier," *IEEE Trans. Ind. Electron.*, vol. 35, no. 4, pp. 508–515, Nov. 1988.
[32] D. Zhang, M. Guacci, M. Haider, D. Bortis, J. W. Kolar, and J. Everts, "Three-phase bidirectional buck-boost current DC-link EV battery charger featuring a wide output voltage range of 200 to 1000 V," in *Proc. IEEE Energy Convers., Congr. Expo.*, Detroit, MI, 2020, pp. 4555–4562.
[33] J. A. Anderson, C. Gammeter, L. Schrittwieser, and J. W. Kolar, "Accurate calorimetric switching loss measurement for 900 V 10 mΩ SiC mosfets," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 8963–8968, Dec. 2017.

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