Power Electronic Systems
Laboratory

Proceedings of the 10th ICPE International Conference on Power Electronics (ICPE 2019-ECCE Asia),
Bexco, Busan, Korea, May 27-30, 2019

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New 40 kV / 300 kVA Quasi-2-Level Operated 5-Level Flying Capacitor SiC "Super-Switch" IPM

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***Abstract*—Emerging applications, e.g., traction systems and utility scale renewable energy systems, demand for Medium Voltage (MV) power electronic switches with blocking capabilities above 20 kV, which cannot be provided with today's 10 kV or 15 kV SiC power semiconductors. Therefore, this work investigates different concepts for the realization of a MV half-bridge, i.e., a series connection of 10 kV SiC MOSFETs, a JFET Super Cascode arrangement, and Modular Multilevel Converter (MMCs) and Flying Capacitor Converter (FCCs) topologies. The FCC topology features several advantages such as reduced switching losses, reduced chip area, lower $\mathrm{d}v/\mathrm{d}t$ of the switching transitions, and robust voltage balancing. Moreover, the volume of the flying capacitors can be reduced with Quasi-2-Level (Q2L) operation of the half-bridge, where the intermediate voltage levels are only used during very short time intervals, i.e., during the switching transitions. This paper analyzes the design, the switching behavior, and the voltage balancing of the Q2L-FCC bridge-leg and confirms its suitability as a versatile MV switch. Finally, the integration of a complete bridge-leg, including gate drivers, isolated cooling interfaces, measurements, and Q2L control into a 300 kVA / 40 kV SiC Super-Switch Intelligent Power Module (SiC-SS-IPM) is presented.**

I. Introduction

At present, Solid-State Transformers (SSTs) for traction and smart-grid applications are intensively discussed [1]–[3]. However, despite the recent availability of 10 kV or 15 kV SiC MOSFET technology, the corresponding high ac input voltages, e.g., 15 kV or 25 kV for traction applications and 13.8 kV in case of a typical Medium Voltage (MV) mains in the USA [4], still represent a key challenge for converter realization. In this work, a 250 kW dc–dc step-down Dual Active Bridge (DAB) converter (cf. **Fig. 1(a)**) is considered, which is part of the SST of a future single-phase 15 kV / 16.7 Hz traction system, where two such DAB converters could deliver the power necessary to supply axle motors in a distributed traction chain.

According to the standard [5], the SST is subject to non-permanent maximum ac grid rms voltages of 18 kV for up to 5 minutes (peak voltage of 25.5 kV), which leads to a selected input-side dc-link voltage of $V_{\mathrm{dc}} = 28\,\mathrm{kV}$. Hence, the DAB converter's MV half-bridge requires power electronic switches which withstand blocking voltages that clearly exceed the rating of today's cutting-edge 10 kV or 15 kV SiC power semiconductors. Furthermore, the peak currents in the switches are 21.5 A and the apparent switching power is 300 kVA.

This paper considers the module integration of a complete half-bridge of the DAB converter, i.e., all power semiconductors, commutation capacitors, gate drivers, control and measurements, isolated gate driver power supplies, and isolated cooling surfaces, are accommodated in a *SiC Super-Switch Intelligent Power Module* (SiC-SS-IPM), cf. **Fig. 1(b)**. For this purpose, the following power semiconductor arrangements have been initially considered:

- The first and most straightforward concept is a direct series connection of SiC MOSFETs, as shown in **Fig. 2(a)** [6], [7]. However, due to mismatches in the semiconductor properties and gate drivers, special circuitry is needed to ensure equal transient and stationary blocking voltage sharing in order to prevent a destruction of the whole stack of switches [6]. Moreover, snubbers are needed and significantly increase the switching losses.
- The second concept is a Super Cascode arrangement with a series connection of SiC JFETs, cf. **Fig. 2(b)**, which is reported in [8], [9] for the realization of a 5 kV and a 6.5 kV power switch. This approach requires only a simple gate driver for each stack of switches, however, the operation with balanced blocking voltages requires a passive network that is adapted to the parasitic capacitances of the SiC JFETs to ensure proper operation. Furthermore, only few suppliers of MV SiC JFETs exist and SiC JFETs feature only blocking voltages well below 10 kV, which requires the series connection of many devices.

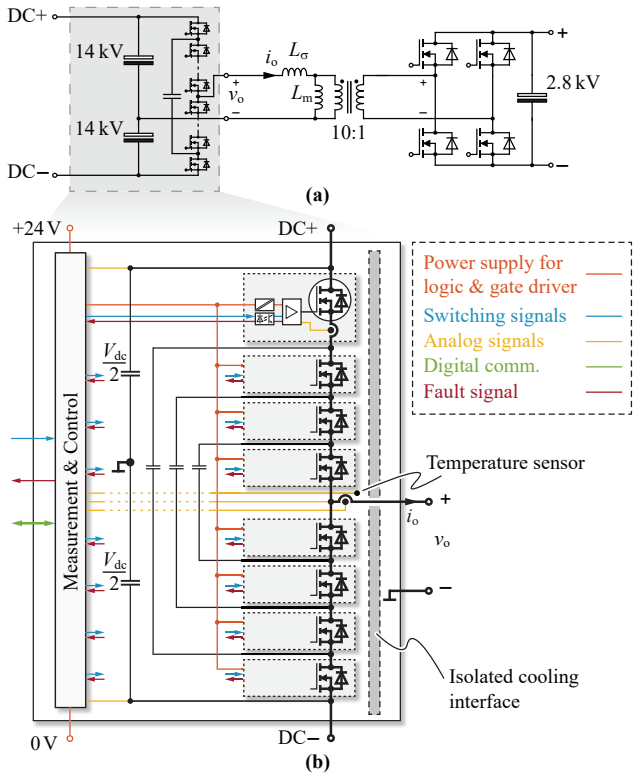

Fig. 1. (a) Considered 28 kV / 2.8 kV step-down 250 kW DAB converter and **(b)** block diagram of the proposed SiC Super-Switch Intelligent Power Module (SiC-SS-IPM) used to realize the MV half-bridge of a DAB converter. The half-bridge module is realized with a 5-Level Flying Capacitor Converter (FCC) operated with Quasi-2-Level (Q2L) modulation; power switches, gate drivers, flying capacitors, commutation capacitors, measurements, and control are integrated in the module such that the Q2L commutations can be triggered by a single optical signal.

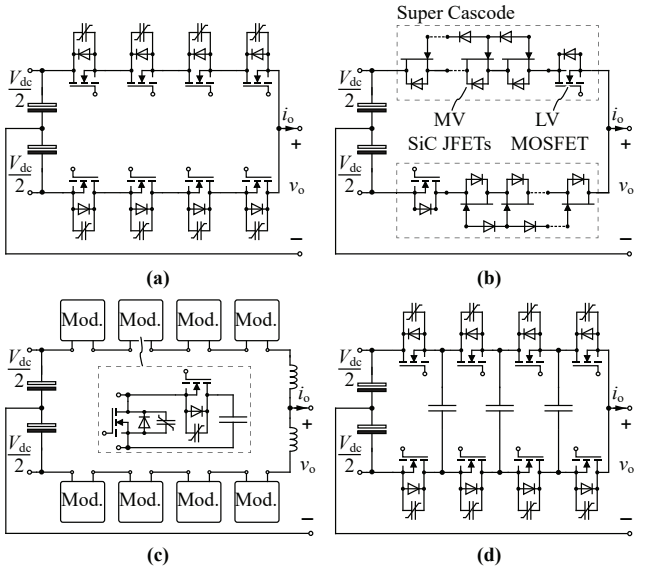

Fig. 2. Realization of a MV half-bridge using different semiconductor arrangements: **(a)** direct series connection of MV SiC MOSFETs, **(b)** Super Cascode (series connection of MV SiC JFETs with a low-voltage MOSFET), **(c)** 5-Level MMC, and **(d)** 5-Level FCC.

- The Modular Multilevel Converter (MMC) can be used for realizing MV bridge-legs, cf. **Fig. 2(c)** [10]–[12]. The main drawbacks of this topology are the increased chip area, the high number of gate drivers, the presence of leg inductors, and the large volume of the capacitors. Nevertheless, the MMC is highly modular and redundancy can easily be added.
- The Flying Capacitor Converter (FCC) type half-bridge can also be used for MV converters, cf. **Fig. 2(d)** [7], [13]–[15]. The FCC features several advantages such as reduced switching losses (snubberless) and robust voltage balancing without additional chip area and gate drivers. However, for conventional multilevel operation the total volume of the flying capacitors is relatively large.

The large capacitor volumes required for the MMC and FCC can be mitigated with a Quasi-2-Level modulation scheme (Q2L-MMC, Q2L-FCC), where the intermediate voltage levels are only used during the switching transitions, producing staggered output waveforms [11]–[13]. Additionally, the Q2L-MMC and Q2L-FCC topologies, cf. **Figs. 2(c), (d)**, feature lower $\mathrm{d}v/\mathrm{d}t$ during the switching transitions compared to the 2-Level converters shown in **Figs. 2(a), (b)**, which is beneficial for the electric insulation [16]–[18].

The focus of this paper is on a comprehensive analysis of the Q2L-FCC, due to the advantages of FCCs listed above and identified in [13]. **Section II** studies the Q2L-FCC operation, which to the knowledge of the authors has not been considered in the literature so far, during soft- and hard-switching transitions. Afterwards, in **Section III**, passive and active balancing schemes are proposed for the Q2L-FCC. The analysis shows that an adequate sharing of the semiconductors' blocking voltages can be achieved with very small capacitance values, which outweighs unfavorable scaling properties of the flying capacitors at high voltages. Thus, the Q2L-FCC is a highly promising candidate for the targeted SiC-SS-IPM, which is presented in **Section IV**. Finally, **Section V** evaluates the impact of Q2L-operation on the electrical insulation in comparison to a 2-Level bridge-leg realized with direct series connection of MOSFETs.

Tab. I. Specifications of the Q2L-FCC.

(a) SiC MOSFET package with 2 parallel dies		
$V_{\mathrm{ds,max}}$	10 kV	max. blocking voltage
$I_{\mathrm{ds,max}}$	2×18 A	max. drain current
$R_{\mathrm{ds,on}}$	550 mΩ / 2	on-state res. @ 125°C
$C_{\mathrm{oss,eq}}$	2×200 pF	charge eq. capacitance
(b) 3-Level Q2L-FCC specifications (20 kV / 150 kVA)		
n	2	devices in series
N	3	voltage levels
C_{FC}	21.5 nF	flying capacitors
V_{dc}	14 kV	dc-link voltage
$I_{\mathrm{o,max}}$	21.5 A	nominal output current
(c) 5-Level Q2L-FCC specifications (40 kV / 300 kVA)		
n	4	devices in series
N	5	voltage levels
C_{FC}	21.5 nF	flying capacitors
V_{dc}	28 kV	dc-link voltage
$I_{\mathrm{o,max}}$	21.5 A	nominal output current

II. Q2L-Operation of the FCC

This Section investigates the processes in the Q2L-FCC for Zero Voltage Switching (ZVS) and Hard Switching (HS) with turn-on losses, since HS transitions might occur during transients or at partial load in the considered DAB converter. In-depth understanding of the switching operations is required to determine the total charges provided to the flying capacitors and/or to enable the development of a robust Q2L-FCC.

The considered simulations are using MOSFET equivalent circuits that consist of a voltage controlled current source, the non-linear parasitic MOSFET capacitances, the antiparallel body diode, the reverse recovery charge, and package inductances, as presented in [19].

The switching operations are explained for a 3-Level FCC to enable a clear and comprehensive explanation of Q2L-operation. The specifications of the considered Q2L-FCCs are summarized in **Tabs. I (a), (b)**. The obtained findings also apply to FCCs with higher number of levels.

A. Zero Voltage Switching (ZVS)

Fig. 3(a) illustrates the different operating states for a falling edge of v_{o} and a positive output current i_{o}, which is assumed to be constant during the considered time interval, $t_0 < t < t_4$. **Fig. 3(b)** depicts the corresponding time intervals during the switching operations with negative slopes of v_{o}. Simulated waveforms of output current and voltage, i_{o} and v_{o}, flying capacitor current and voltage, i_{FC} and v_{FC}, and the MOSFETs' blocking voltages are shown.

During the first time interval, $t < t_0$, in **Fig. 3(a)**, $v_{\mathrm{o}} = +V_{\mathrm{dc}}/2$ applies, and both upper switches, $S_{1\mathrm{p}}$ and $S_{2\mathrm{p}}$, are turned on. The transition to voltage level $-V_{\mathrm{dc}}/2$ starts with turning off switch $S_{1\mathrm{p}}$ and during the corresponding interval $[t_0, t_1]$, complete charging and discharging of $C_{\mathrm{oss,1p}}$ and $C_{\mathrm{oss,1n}}$, i.e., ZVS, is achieved. Approximately half of the inductor current charges the flying capacitor during interval $[t_0, t_1]$, due to a capacitive current divider at node A ($C_{\mathrm{oss,1n}} \ll C_{\mathrm{FC}}$). After completion of the ZVS transition, the anti-parallel diode of $S_{1\mathrm{n}}$ conducts ($t \in [t_1, t_2]$), the output current charges the flying capacitor, and $v_{\mathrm{o}} = V_{\mathrm{dc}}/2 - v_{\mathrm{FC}} \approx 0\,\mathrm{V}$ applies. At this point, $S_{1\mathrm{n}}$ can be turned on and, in a second step, $S_{2\mathrm{p}}$ can be turned off, to initiate the second ZVS transition, of flying capacitor cell 2, and achieve $v_{\mathrm{o}} = -V_{\mathrm{dc}}/2$. These two events are independent of each other, however, for the sake of simplicity, the two transitions are performed simultaneously at $t = t_2$. The time interval between t_0 and t_2

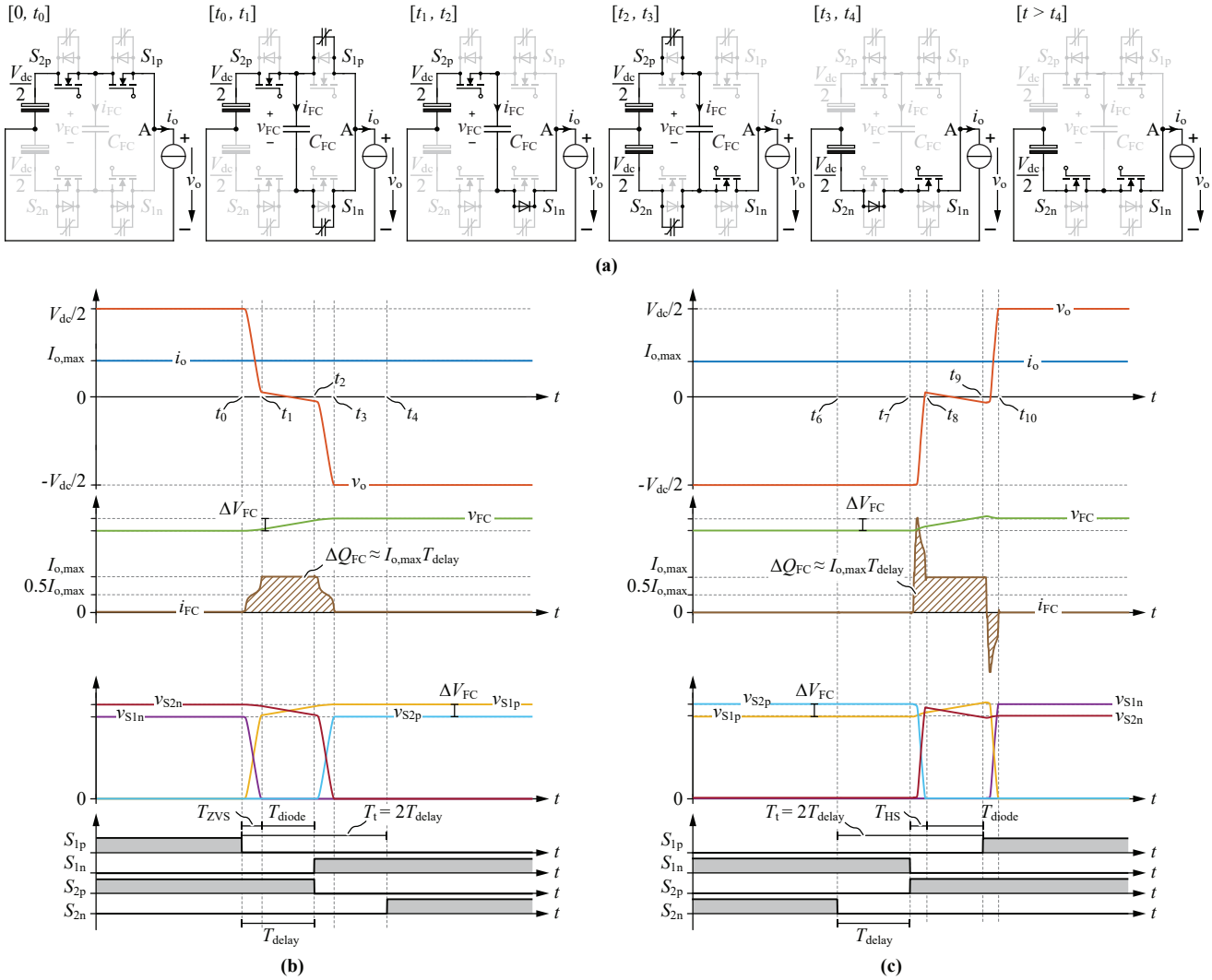

Fig. 3. Simulation results for Q2L-operation of the 3L-FCC: **(a)** operating states of a half-bridge with constant positive output current (i_o) during the switching operations with negative slopes of v_o, which result in a ZVS transition. **(b)** Corresponding time intervals and simulated waveforms of output current (i_o) and output voltage (v_o), flying capacitor current (i_{FC}) and capacitor voltage (v_{FC}), and MOSFET voltages and signals. **(c)** Time intervals and simulated waveforms for the HS case with positive slope of v_o and constant output current. A delay of $T_{delay} = 1\,\mu s$ is considered.

is defined as T_{delay}, and will be used in **Section III** for the balancing of the flying capacitor voltage, v_{FC}. The processes during the interval $[t_2, t_3]$ are similar to those of interval $[t_0, t_1]$, i.e., ZVS is achieved and half of the inductor current charges the flying capacitor. The anti-parallel body diode of S_{2n} starts to conduct at the end of interval $[t_2, t_3]$ and, at this instant, all charging or discharging processes of the flying capacitor and of all switches' effective output capacitances are completed. The transition is over when S_{2n} is switched on at t_4 after the dead time. The ZVS transition with a rising edge of v_o and a negative output current i_o produces similar waveforms, and, therefore, does not require a separate analysis.

B. Hard Switching (HS)

Fig. 3(c) shows simulated waveforms for switching operations with positive slopes of v_o and positive output current i_o. The transition starts with turning off the switch S_{2n} and during the corresponding interval $[t_6, t_7]$, the current keeps flowing through its anti-parallel diode. At $t = t_7$, S_{2p} turns on hard and generates turn-on losses. Furthermore, the flying capacitor is subject to the superposition of the output current i_o, the reverse recovery current of S_{2n}, and the current charging $C_{oss,2n}$ ($t \in [t_7, t_8]$). Once S_{2n} is in the blocking state, the output current charges the capacitor ($t \in [t_8, t_9]$). At $t = t_9$, S_{1p} turns on and the second switching transition starts. The processes during $t \in [t_9, t_{10}]$ are similar to those of interval $[t_7, t_8]$, i.e., HS of S_{1p} and reverse recovery of S_{1n} occur, however, in this case the reverse recovery current and the current charging $C_{oss,1n}$ discharge the flying capacitor with approximately the same charge as it was charged with, before. The transition is completed when switch S_{1n} is in the blocking state at t_{10}. The HS transition with a falling edge of v_o and a negative output current i_o is similar to the considered case and, therefore, not analyzed in detail.

C. Charge of the Flying Capacitor

According to **Figs. 3(b), (c)**, the duration of the complete transition of the Q2L 3L-FCC, is given by

$$T_t \approx 2T_{delay}. \tag{1}$$

Dimensioning of T_{delay} is explained in **Section III**. Furthermore, based on the assumption of constant current during

the switching transients, $i_o(t) = I_{o,max}$, the total change of charge provided to the flying capacitor is

$$\Delta Q_{FC} \approx T_{delay} I_{o,max}, \tag{2}$$

which is a general description of the charge increments in the flying capacitor for all switching cases, i.e., ZVS, partial ZVS, or HS. It is worth noting that the flying capacitors are active only during the switching transition and their transferred charges are independent of the switching frequency and the number of levels.

III. Modulation and Control of the Q2L-FCC

Modulation schemes and control of FCCs are widely known and have been thoroughly analyzed in the literature [15], [20], [21], however exclusively for classic multilevel and not for Q2L-operation. In this Section, a novel modulation concept guaranteeing natural balancing of the flying capacitors' voltages of Q2L-FCCs in steady-state is presented. Afterwards, a new active control method is proposed to ensure safe operation during the transients. Using the proposed active control method, the capacitance value of the flying capacitors can be significantly decreased. As in **Section II**, a 3-Level FCC is considered, cf. **Tabs. I(a),(b)**. However, the obtained results can be generalized to any number of levels.

A. Modulation with Passive FC Voltage Balancing

In case of constant output current, the flying capacitor is subject to the load current for a time interval T_{delay}, cf. (2). The sign of ΔQ_{FC} depends on the signs of the output current and the voltage slope, i_o and dv_o/dt, and the considered switching sequence,

$$SEQ_I = \{(S_{1p}, S_{1n}), (S_{2p}, S_{2n})\}, \tag{3}$$

$$SEQ_{II} = \{(S_{2p}, S_{2n}), (S_{1p}, S_{1n})\}. \tag{4}$$

Tab. II lists the corresponding sign of ΔQ_{FC}. For example, **Fig. 3(b)** presents SEQ_I for a negative slope of voltage v_o and positive value of i_o, which leads to a positive charge increment, whereas **Fig. 3(c)** shows SEQ_{II} for a positive slope of v_o and a positive value of i_o, which results in a positive charge increment. This degree of freedom can be used to balance the flying capacitor where two cases should be considered: symmetrical and asymmetrical output currents.

Fig. 3(a) shows the passive balancing scheme for symmetrical currents, e.g., a triangular inductive current with zero average value (ensuring the ZVS condition). At instant t_0, SEQ_{II} is selected to discharge the flying capacitor. In the next transition, at t_1, SEQ_I is applied to charge the capacitor. It can be noticed that for this operation of a half-bridge the alternating modulation of sequences $\{1,2,1,2,...\}$ occurs, since equal currents charge and discharge C_{FC} in each transition. In such operating mode, the maximum peak-to-peak ripple on the flying capacitor is

$$\Delta V_{FC} \approx \frac{T_{delay} \cdot I_{o,max}}{C_{FC}}. \tag{5}$$

For asymmetrical currents, the same sequence cannot be applied, since the flying capacitor would be charged and discharged with unequal currents and the capacitor's voltage would therefore diverge from the nominal value. This can be resolved by modifying the order of the modulation sequences to $\{1,1,2,2,1,1,...\}$, and hence charging and discharging C_{FC} with the sum of the minimum and maximum values of i_o. This case is shown in **Fig. 4(b)** for a triangular current with a dc offset (HS condition). It should be noted that, during the HS transition, the current through C_{FC} is further increased by the reverse recovery current of the complementary MOSFET (cf. **Fig. 3(c)**). Since the capacitor is balanced over two switching periods, this doubles the peak-to-peak voltage ripple,

$$\Delta V_{FC} \approx 2\frac{T_{delay} \cdot I_{o,max}}{C_{FC}}. \tag{6}$$

The presented balancing scheme, which is using the degree of freedom offered by the switching sequence, is robust in case of steady-state operation and does not

Tab. II. Modulation sequences depending on the slope of the output voltage v_o and the sign of the output current i_o and resulting effect on the flying capacitor: (+) charge, (-) discharge.

v_o	i_o	Sequence	ΔQ_{FC}
Falling	>0	SEQ_I	+
		SEQ_{II}	-
	<0	SEQ_I	-
		SEQ_{II}	+
Rising	>0	SEQ_I	-
		SEQ_{II}	+
	<0	SEQ_I	+
		SEQ_{II}	-

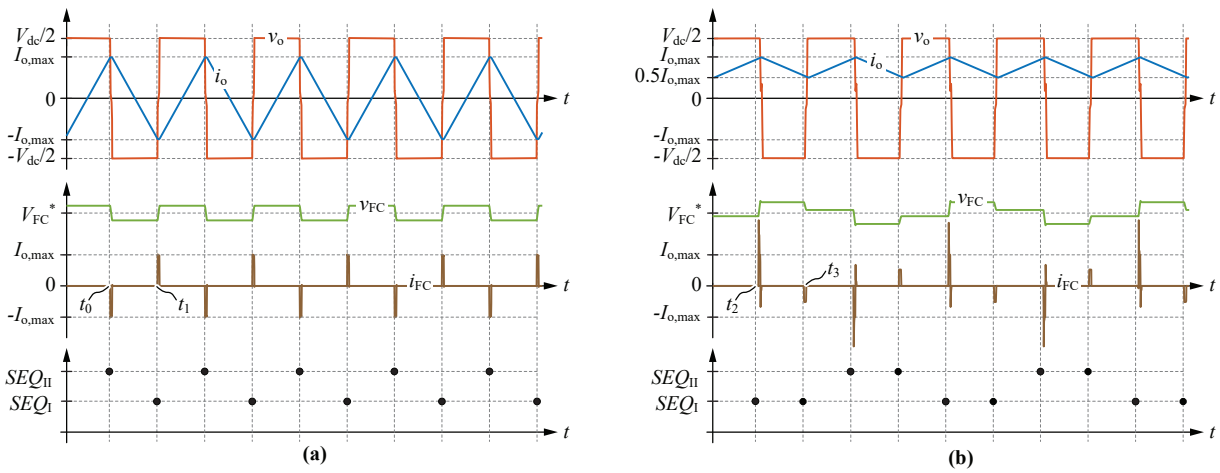

Fig. 4. Simulation results for the Q2L-FCC with passive balancing of the flying capacitor voltage. The proposed modulation scheme is shown: **(a)** sequences for symmetrical waveforms (ZVS) and **(b)** sequences for asymmetrical waveforms (HS). A delay $T_{delay} = 1\,\mu s$ is considered together with a switching frequency of $f_s = 20\,kHz$.

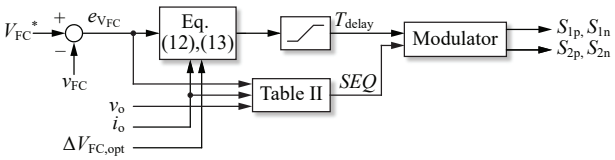

Fig. 5. Control structure for balancing the flying capacitor voltage of a Q2L-FCC with a minimal component stress while ensuring ZVS.

require the measurement of the flying capacitor voltage, but leads to high voltage ripples, which translate to additional voltage stress applied to the MOSFETs and/or to large flying capacitors. Therefore, in case of transients, e.g., resulting from high step changes of the load, the voltage ripple computed with (6) can be exceeded for a limited time. Thus, an active control of T_{delay} is discussed in the following for improving the voltage balancing.

B. Control with Active FC Voltage Balancing

The proposed active control scheme, depicted in **Fig. 5** is responsible for adapting the control variable T_{delay} in order to operate the converter with minimum component stress, i.e., minimum voltage fluctuation across C_{FC}, while ensuring ZVS.

In a first step, the optimal ripple of v_{FC} is determined such that ZVS can be achieved within the typical operating range. The ZVS switching transition duration can be estimated as

$$C_{oss,eq} = \frac{\int_0^{V_{DC}/2} C_{oss}(v)\,\mathrm{d}v}{V_{DC}/2}, \tag{7}$$

$$T_{ZVS}(i_o) = \frac{2C_{oss,eq}}{|i_o|}\frac{V_{DC}}{2}, \tag{8}$$

where $C_{oss,eq}$ represents the charge equivalent capacitance and a margin (k_m) is added, to ensure complete ZVS,

$$T_{ZVS,m}(i_o) = (1+k_m)\,T_{ZVS}(i_o). \tag{9}$$

Finally, from the computed time interval, the optimal peak-to-peak voltage ripple can be predicted as (cf. (2))

$$\Delta V_{FC,opt} = \frac{T_{ZVS,m}|i_o|}{C_{FC}} = (1+k_m)\frac{2C_{oss,eq}}{C_{FC}}\frac{V_{DC}}{2}. \tag{10}$$

It can be seen that $\Delta V_{FC,opt}$ is independent of i_o, and as a result, constant. With $\Delta V_{FC,opt}$ known, the voltage swing, $\Delta V_{FC,ctrl}$, required to meet the specified ripple, is computed,

$$e_{V_{FC}} = V_{FC}^* - v_{FC}, \tag{11}$$

$$\Delta V_{FC,ctrl} = \left|e_{V_{FC}}\right| + \frac{\Delta V_{FC,opt}}{2}, \tag{12}$$

where V_{FC}^* denotes the reference value of the flying capacitor voltage. Afterwards, the required optimized delay (T_{delay}) is computed with the help of the instantaneous switched current (i_o),

$$T_{delay}(i_o) = \frac{C_{FC}\Delta V_{FC,ctrl}}{|i_o|} = \frac{C_{FC}\left|e_{V_{FC}}\right|}{|i_o|} + \frac{T_{ZVS,m}(i_o)}{2}, \tag{13}$$

$$T_{delay}(i_o) \in [T_{min}, T_{max}], \tag{14}$$

where T_{min} and T_{max} are the boundaries on T_{delay}. The minimum boundary is limited by the system's physical limitations, since below a specified value, potential shoot-through could result. The maximum boundary is limited by the maximum allowable duration of the switching transition, given that increased commutation times decrease the output voltage-time product. Additionally, the switching sequence is chosen according to **Tab. II**. Finally, with the selected switching sequence and time delay, the modulator generates the gate signals.

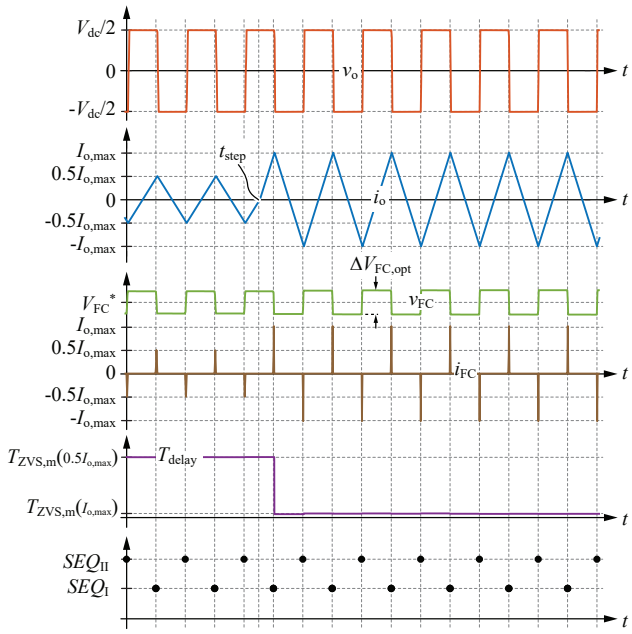

Fig. 6. Simulation results for Q2L-operation of a FCC test circuit (cf. **Fig. 3(a)**) after a step change from $0.5I_{o,max}$ to $I_{o,max}$, while employing the proposed active controller (cf. **Fig. 5**). A switching frequency of $f_s = 20\,\mathrm{kHz}$ is considered.

In case of low load conditions, where T_{delay} is limited to T_{max}, partial ZVS transitions and reduced values of ΔV_{FC} will occur. On the contrary, in case of extreme load conditions, where T_{delay} is limited to T_{min}, ΔV_{FC} will surpass its optimal value, hence increasing the stress across the flying capacitors and the adjacent MOSFETs.

Fig. 6 shows an inductive load step of the Q2L-FCC half-bridge from $0.5I_{o,max}$ to $I_{o,max}$ with the presented controller. It can be observed, that the voltage ripple of v_{FC} remains constant during the transient and, compared to the case of **Fig. 4**, decreases by a factor of 1/3. This is achieved by proper adaptation of T_{delay}.

C. Idle Mode/Reduced Output Current

For balancing in idle state, i.e., if the switching operation is ceased, additional passive balancers (resistors connected in parallel with the switches) should be used, similar to [15]. The values of the balancing resistors need to be selected considering the leakage currents of the MOSFETs and capacitors.

The balancing of the flying capacitors at low output currents is critical since the two presented (passive and active) balancing schemes rely on i_o. In such cases, the charges delivered by i_o to the flying capacitor during the switching transitions are not sufficient and other balancing schemes need to be considered. The control of the Q2L-FCC in this special case is subject to current research.

D. Measurements Required for Control

The presented active control method (cf. **Section III-B**) requires the measurements of v_{FC} and i_o. However, due to insulation requirements, the realization of multiple high voltage measurements (for each flying capacitor) constitutes a complex circuit featuring a substantial volume. Alternatively, the flying capacitor voltages can be estimated from the switching pattern and the output voltage since the flying capacitor voltage combined with the dc-link voltage appears in v_o during the Q2L transitions. This can be seen during $t \in [t_1, t_2]$ in **Figs. 3(a),(b)** and during $t \in [t_8, t_9]$ in **Fig. 3(c)**.

Tab. III. Flying capacitors and commutation dc-link capacitors of the 5-Level Q2L-FCC.

Capacitor (nF)		Operating voltage (kV)	Rated voltage (kV)	Capacitor realization	Volume (dm^3)	Total volume (dm^3)
C_{FC1}		7	8 (surge 12)	24 nF	0.03	
C_{FC2}	$1.1 \cdot 21.5 \approx 24$	14	15 (surge 22.5)	2 parallel 12 nF	0.06	0.30
C_{FC3}		21	24 (surge 36)	3 series 72 nF	0.20	
C_{dc}	12	28	30 (surge 45)	2 series 24 nF	0.13	0.13

IV. Design of the 5-Level Q2L-FCC

This Section provides an evaluation of the Q2L-FCC bridge-leg considering the semiconductors and the capacitor volumes. In addition, the integration of the Q2L-FCC half-bridge into the SiC-SS-IPM is shown. The proposed Q2L-FCC is part of a DAB converter as depicted in **Fig. 1**, with specifications as listed in **Tabs. I(a),(c)**.

A. Power Semiconductors

Each die of the used SiC MOSFETs (research samples from Wolfspeed) features a blocking voltage of 10 kV, an on-state resistance of $R_{ds,on} \approx 550\,m\Omega$ (at $T_j = 150°C$,) and a linearized charge equivalent capacitance of $C_{oss,eq} = 200\,pF$ [22]. Two parallel dies per switch are considered in order to reduce the conduction losses. With this, $280\,ns < T_{ZVS} < 1\,\mu s$ applies for $21.5\,A > i_o > 6\,A$. Thus, with $T_{delay} = 1\,\mu s$, ZVS is achieved in a wide load range and the total output voltage transition time remains reasonable: $T_t = n\,T_{delay} = 4\ \mu s$.

The 5-Level Q2L-FCC requires 8 MOSFETs and/or 16 dies. In this regard, a Q2L-MMC-based approach, the closest competitive design, would require 16 MOSFETs and a total of $16 + 8 = 24$ dies, since the switches connected in series to the dc-link capacitors, cf. **Fig. 2(c)**), are subject to low currents in case of Q2L-operation and could be realized with only one die. The higher number of MOSFETs employed in the MMC would be linked to a higher number of gate drivers and additional isolation requirements. In this regard, the redundancy featured by a Q2L-MMC-based half-bridge would come at the cost of a more expensive and complex system compared to the Q2L-FCC.

B. Capacitors

Based on (6), for $T_{delay} = 1\,\mu s$, a maximum instantaneous current during switching of $I_{o,max} = 21.5\,A$, and a specified peak-to-peak capacitor voltage ripple of $\Delta V_{FC} = 2\,kV$, the value of the flying capacitors are

$$C_{FC} = 2\frac{T_{delay} I_{o,max}}{\Delta V} = 21.5\,nF. \tag{15}$$

With $\Delta V_{FC} = 2\,kV$, the maximum voltage applied to a MOSFET is 8 kV ($V_{dc}/n + \Delta V_{FC}/2$). However, this voltage ripple only appears for passive balancing with asymmetric currents, cf. (6). For passive balancing with symmetrical currents, the maximum voltage is 7.5 kV, cf. (5). This value further decreases with the active control scheme presented in **Section III-B**.

Of particular interest is the investigation of the implications of the capacitor volumes on the converter's volume. For this analysis, high voltage film capacitors are found to be most suitable, due to their high voltage ratings, low losses, and highest volumetric capacitance density, in comparison to high voltage ceramic capacitors. An algorithm analyzing combinations of different capacitors, connected in series and / or parallel, has been implemented and used for selecting the combination which yields minimum total volume. According to the results of this optimization, *HA*-type capacitors manufactured by FTCAP GmbH [23], arranged as stated in **Tab. III**, are found to be optimal. However, the considered film capacitors are subject to capacitance reductions at elevated case temperatures, which is accounted for by over-dimensioning the nominal capacitance by 10%. It is found that the total boxed volume for all flying capacitors of the Q2L-FCC is only $0.30\,dm^3$. In comparison, a Q2L-MMC with similar rating would lead to a capacitor volume of $0.70\,dm^3$.

In addition to flying capacitors, also dc-link commutation capacitors are considered. For the discussed realization of a half-bridge-based Q2L-FCC, a configuration with a split dc-link is preferred. It enables the use of the mid-point as reference ground for voltage measurements to reduce the voltage stresses on the measurement circuits. Since the main, high energy dc-link has to be designed for a specific application and is located outside of the SiC-SS-IPM module, a reduced total capacitance of 12 nF is installed inside the module.

C. Realization of the SiC-SS-IPM

A 3–D model of the SiC-SS-IPM is presented in **Fig. 7**. The designed SiC-SS-IPM is enclosed in a polyamide housing, which is integrated with Aluminum Nitride (AlN) baseplates on top and bottom of the module to provide isolated thermal interfaces between the MOSFETs' baseplates and the external cooling system. The high voltage terminals are located on the sides of the module (labelled with "dc input" and "ac output"). The MOSFETs of the upper half-bridge arm are located on the top side and those of the lower half-bridge arm on the bottom side. This layout allows for the realization of low-inductance commutation loops that are arranged in the xy-plane. The control board implements isolated communication and isolated power supply of the module. The presented layout features a very compact design and consequently a low boxed volume of $2.9\,dm^3$, i.e., the presented 300 kVA / 40 kV SiC-SS-IPM features a power density of $102\,kVA/dm^3$. Furthermore, the SiC-SS-IPM enables scalability, e.g., a full-bridge topology could be built by stacking modules in y-axis direction, and interleaving them with a required cooling system (cold plates with heat pipes of water cooling or heat sinks).

V. Impact of Q2L on the Electrical Insulation

From the design of the Q2L-FCC, presented in the previous Section, it is clear that it offers a less complex, more compact, and cheaper design than the MMC-based counterpart. In the following, it is proven that the Q2L staggered switching also offers reduced dv/dt of the switching transitions compared to 2-Level topologies (cf. **Figs. 2(a), (b)**) and, thus, reduces the stress on the electrical insulation and the emitted EMI disturbances.

The fast voltage transients (up to 100 kV/µs [22]) with high repetition rates (up to 100 kHz [24]), generated by MV SiC switches, have negative effects on the electrical

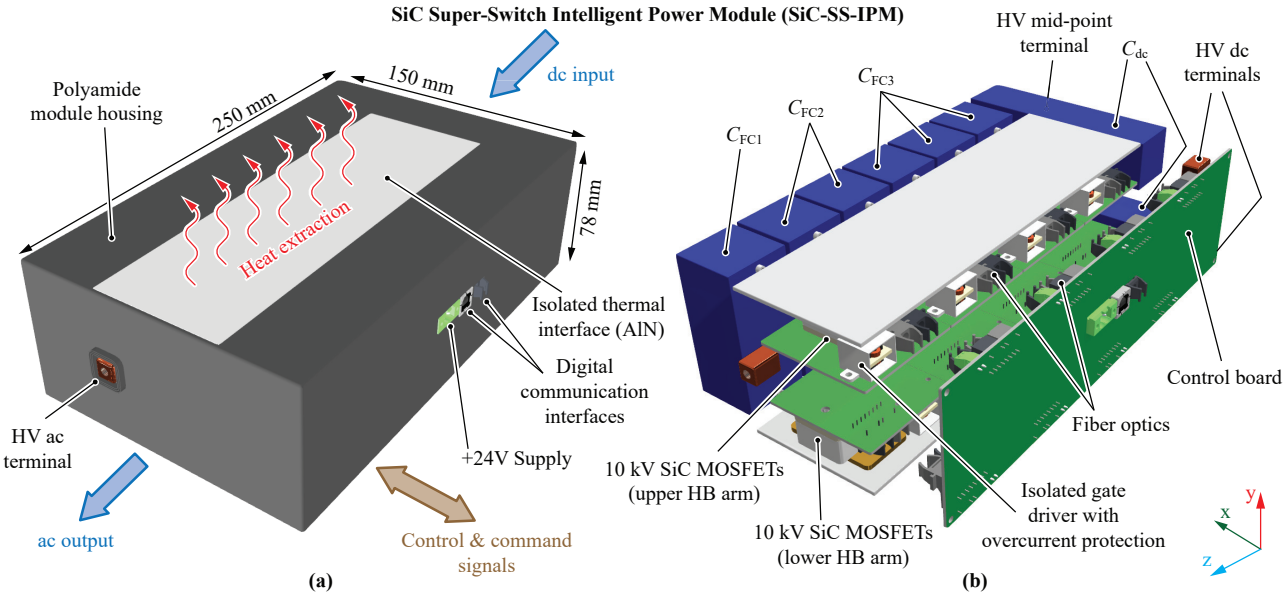

Fig. 7. 3–D rendering of the 300 kVA / 40 kV half-bridge SiC-SS-IPM: **(a)** external appearance and **(b)** internal layout.

insulation, as shown for MF transformers, HVDC converters, and inverter-fed electrical machines [16], [17], [25], [26]. Such degradations are mainly explained by the following effects:

- *Partial Discharges* - The damages inflicted to insulation materials by partial discharges are proportional to the operating frequency. Moreover, fast switching transitions increase the amplitudes of the discharges. This leads to reduced breakdown voltages and accelerated ageing [16], [18], [26].
- *Resonances* - Fast switching transitions can excite resonances inside passive components (e.g., transformers, inductors, and electrical machines) or between passive components and cables (e.g., electrical machines connected through long cables). Such oscillations create an uneven voltage sharing inside the components and/or overvoltages between the terminals [25], [27].
- *Dielectric Losses* - The dielectric losses, which are proportional to the operating frequency, cannot be neglected for MV systems operated at MF. Additionally, the associated dielectric heating can lead to thermal breakdowns or thermal runaways [16], [17].

These problems become particularly critical for the JFET Super Cascode and the series connection of MOSFETs with snubbers. For these arrangements, all series connected devices are switched synchronously in order to guarantee equal voltage sharing. This implies that the switching speed at the output node of a bridge with n series connected semiconductors, each with a given $\mathrm{d}v/\mathrm{d}t$ (for a defined load current), is equal to $n(\mathrm{d}v/\mathrm{d}t)$. This means that, for increasing n, the switching speed becomes problematic for the electrical insulation but also from an EMI point of view [28]–[30]. The limitation of the switching speed (by the gate drivers or with a snubber) is possible but creates substantial additional losses.

This disadvantage does not appear in the presented Q2L-FCC since the series connected devices are switched sequentially. Hence, the $\mathrm{d}v/\mathrm{d}t$ during the staggered switching transition is independent of n [28]–[30]. Therefore, the Q2L-FCC reduces the partial discharge amplitudes, mitigates the impacts of resonances, and reduces the dielectric losses.

Figs. 8(a),(b) show the obtained waveforms for a 2-Level

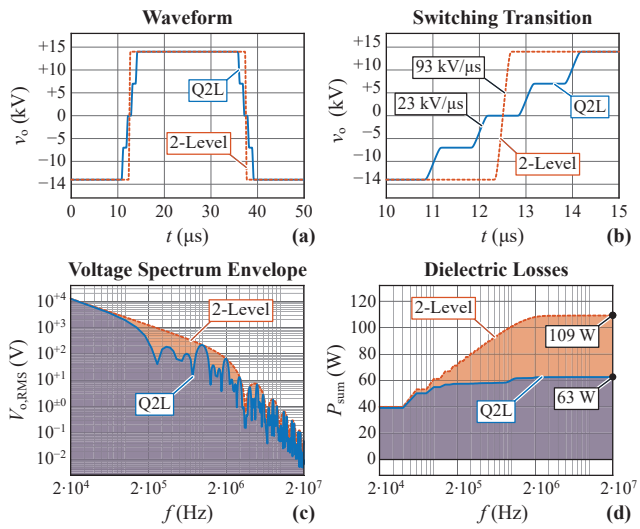

Fig. 8. A classical 2-Level bridge-leg is compared with the proposed Q2L-FCC: **(a)** voltage waveforms, **(b)** switching transitions, **(c)** voltage spectrum envelope, and **(d)** cumulative sum of the dielectric losses. The ratings shown in **Tabs. I(a),(c)** are considered and the system is operated at 20 kHz. ZVS is considered with a switched current of $I_{o,max}$. The dielectric losses are computed for a typical capacitance of 200 pF and a dissipation factor of 1 % [17].

bridge-leg realized with a series connection of MOSFETs and for the 5-Level-based Q2L-FCC according to the specifications in **Tabs. I(a),(c)**. The obtained switching speeds are 28 kV/300 ns = 93 kV/µs for the 2-Level bridge-leg and 7 kV/300 ns = 23 kV/µs for the Q2L-FCC. **Figs. 8(c),(d)** depict the voltage spectrum and the associated dielectric losses, determined according to [17]. As expected, the Q2L-FCC features reduced high-frequency harmonics and, therefore, reduced dielectric losses (63 W instead of 109 W).

VI. Conclusion

This paper presents a new 300 kVA / 40 kV Quasi-2-Level (Q2L) half-bridge SiC Super-Switch Intelligent Power Module (SiC-SS-IPM), which includes all circuits for gate drivers, measurements, and control. The module implements a 5-Level Flying Capacitor Converter (FCC) structure for defining the blocking voltages across the power semiconductors and the

Q2L-operation reduces the voltage slew rate during switching and minimizes capacitive energy storage requirements.

According to the results of detailed investigations of the switching operations in a Q2L-FCC, the flying capacitors are subject to charges that are proportional to the load current, independent of the selected operating frequency, and similar for ZVS and HS. It is further shown that balancing of the capacitor voltages can be achieved by means of passive and active balancing schemes. The passive scheme does not require sensors for measuring flying capacitor voltages, whereas the active scheme achieves a reduction of the flying capacitor's voltage ripple and / or capacitor volume and an immediate correction of capacitor voltage deviations in case of transients.

Compared to the Q2L-MMC counterpart, the Q2L-FCC features a lower component count (8 devices and associated gate drivers instead of 16) and substantially lower capacitor volume. Furthermore, the Q2L-FCC achieves a lower $\mathrm{d}v/\mathrm{d}t$ of the switching transitions (23 kV/µs) than a direct series connection of MOSFETs or a JFET Super Cascode (93 kV/µs) without increasing switching losses. In this regard a respective analysis is conducted and reveals that Q2L-operation reduces the stress applied to the electrical insulation. Thus, the Q2L-FCC provides a balanced trade-off between complexity and practicability.

With the very compact design presented in this work, a low boxed volume box of the overall Q2L-FCC SiC-SS-IPM of 2.9 dm^3 is achieved, which results in a module-specific power density of 102 $\mathrm{kVA/dm}^3$.

Acknowledgment

The authors are very much indebted to the Swiss Centre for Competence in Energy Research on the Future Swiss Electrical Infrastructure (SCCER-FURIES) for the support of the research in the area of Solid-State Transformer Technology at the ETH Zurich.

References

[1] C. Zhao, D. Dujic, A. Mester *et al.*, "Power Electronic Traction Transformer - Medium Voltage Prototype," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3257–3268, 2014.

[2] J. E. Huber and J. W. Kolar, "Applicability of Solid-State Transformers in Today and Future Distribution Grids," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 317–326, 2019.

[3] S. Parashar, A. Kumar, and S. Bhattacharya, "High Power Medium Voltage Converters Enabled by High Voltage SiC Power Devices," in *Proc. of the IEEE Energy Conversion Congr. and Expo. (ECCE Asia)*, May 2018.

[4] PowerAmerica, "PowerAmerica Strategic Roadmap for Next Generation Wide Bandgap Power Electronics." [Online]. Available: https://poweramericainstitute.org/.

[5] *Railway applications. Supply Voltages of Traction Systems*, British Standards Institution Std. BS EN 50 163:2004+A1:2007.

[6] K. Vechalapu, A. Negi, and S. Bhattacharya, "Comparative Performance Evaluation of Series Connected 15 kV SiC IGBT Devices and 15 kV SiC MOSFET Devices for MV Power Conversion Systems," in *Proc. of the IEEE Energy Conversion Congr. and Expo. (ECCE USA)*, Sep. 2016.

[7] J. Rodriguez, S. Bernet, B. Wu *et al.*, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, 2007.

[8] J. Biela, D. Aggeler, D. Bortis, and J. W. Kolar, "Balancing Circuit for a 5-kV/50-ns Pulsed-Power Switch Based on SiC-JFET Super Cascode," *IEEE Trans. Plasma Sci.*, vol. 40, no. 10, pp. 2554–2560, 2012.

[9] Z. Li and A. Bhalla, "USCi SiC JFET Cascode and Super Cascode Technologies," in *Proc. of the Int. Conf. for Power Electron. and Intell. Motion (PCIM Asia)*, Jun. 2018.

[10] I. A. Gowaid, G. P. Adam, S. Ahmed *et al.*, "Analysis and Design of a Modular Multilevel Converter with Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5439–5457, 2015.

[11] D. Aeloiza, F. Canales, and R. Burgos, "Power Converter Having Integrated Capacitor-Blocked Transistor Cells," U.S. Patent 9,525,348 B1, 2016.

[12] I. A. Gowaid, G. P. Adam, A. M. Massoud *et al.*, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer with DC Fault Isolation Capability," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 108–123, 2015.

[13] M. Schweizer and T. B. Soeiro, "Heatsink-Less Quasi 3-Level Flying Capacitor Inverter Based on Low Voltage SMD MOSFETs," in *Proc. of the European Conf. on Power Electronics and Applications (EPE)*, Sep. 2017.

[14] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and Comparison of 4-kV Neutral-Point-Clamped, Flying-Capacitor, and Series-Connected H-Bridge Multilevel Converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, 2007.

[15] P. Papamanolis, D. Neumayr, and J. W. Kolar, "Behavior of the Flying Capacitor Converter under Critical Operating Conditions," in *Proc. of IEEE Int. Symposium on Industrial Electronics (ISIE)*, Jun. 2017.

[16] D. Fabiani, G. C. Montanari, and A. Contin, "Aging Acceleration of Insulating Materials for Electrical Machine Windings Supplied by PWM in the Presence and in the Absence of Partial Discharges," in *Proc. of the IEEE Conf. on Solid Dielectrics (ICSD)*, Jun. 2001.

[17] T. Guillod, R. Färber, F. Krismer *et al.*, "Computation and Analysis of Dielectric Losses in MV Power Electronic Converter Insulation," in *Proc. of the IEEE Energy Conversion Congr. and Expo. (ECCE USA)*, Sep. 2016.

[18] P. Wang, G. C. Montanari, and A. Cavallini, "Partial Discharge Phenomenology and Induced Aging Behavior in Rotating Machines Controlled by Power Electronics," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 7105–7112, 2014.

[19] D. Rothmund, D. Bortis, and J. W. Kolar, "Highly Compact Isolated Gate Driver with Ultrafast Overcurrent Protection for 10 kV SiC MOSFETs," *IEEE CPSS Trans. Power Electron. and Appl.*, vol. 3, no. 4, pp. 278–291, 2018.

[20] G. Gateau, M. Fadel, P. Maussion *et al.*, "Multicell Converters: Active Control and Observation of Flying-Capacitor Voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 998–1008, 2002.

[21] K. Antoniewicz, M. Jasinski, M. P. Kazmierkowski, and M. Malinowski, "Model Predictive Control for Three-Level Four-Leg Flying Capacitor Converter Operating as Shunt Active Power Filter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5255–5262, 2016.

[22] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate Transient Calorimetric Measurement of Soft-Switching Losses of 10kV SiC MOSFETs and Diodes," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5240–5250, 2018.

[23] FTCAP GmbH, "High Voltage Capacitors." [Online]. Available: https://www.ftcap.de/en/downloads/.

[24] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1% Efficient 10kV SiC-Based Medium Voltage ZVS Bidirectional Single-Phase PFC AC/DC Stage," *IEEE J. Emerg. Sel. Topics Power Electron. (Early Access)*, 2018.

[25] L. Paulsson, B. Ekehov, S. Halen *et al.*, "High-Frequency Impacts in a Converter-Based Back-to-Back Tie; The Eagle Pass Installation," *IEEE Trans. Power Del.*, vol. 18, no. 4, pp. 1410–1415, 2003.

[26] P. Wang, A. Cavallini, and G. Montanari, "The Influence of Repetitive Square Wave Voltage Parameters on Enameled Wire Endurance," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 21, no. 3, pp. 1276–1284, 2014.

[27] M. Popov, L. van der Sluis, G. C. Paap, and H. De Herdt, "Computation of Very Fast Transient Overvoltages in Transformer Windings," *IEEE Trans. Power Del.*, vol. 18, no. 4, pp. 1268–1274, 2003.

[28] A. Rahmati, M. Arasteh, S. Farhangi, and A. Abrishamifar, "Flying Capacitor DTC Drive with Reductions in Common Mode Voltage and Stator Overvoltage," *Journal of Power Electronics*, vol. 11, no. 4, pp. 512–519, 2011.

[29] T. Fuchslueger, M. Vogelsberger, and H. Ertl, "Reducing dv/dt of Motor Inverters by Staggered-Edge Switching of Multiple Parallel SiC Half-Bridge Cells," in *Proc. of the Int. Conf. for Power Electron. and Intell. Motion (PCIM Europe)*, May 2017.

[30] A. Marzoughi, R. Burgos, and D. Boroyevich, "Investigating Impact of Emerging Medium-Voltage SiC MOSFETs on Medium-Voltage High-Power Industrial Motor Drives," *IEEE J. Emerg. Sel. Topics Power Electron. (Early Access)*, 2018.