Power Electronic Systems
Laboratory

IEEE Transactions on Electron Devices, Vol. 60, No. 2, pp. 587-597, February 2013

Modeling of Soft-Switching Losses of IGBTs in High-Power High-Efficiency Dual-Active-Bridge DC/DC Converters

G. Ortiz,
H. Uemura,
D. Bortis,
J. W. Kolar,
O. Apeldoorn

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Modeling of Soft-Switching Losses of IGBTs in High-Power High-Efficiency Dual-Active-Bridge DC/DC Converters

Gabriel Ortiz, *Member, IEEE*, Hirofumi Uemura, Dominik Bortis, *Student Member, IEEE*, Johann Walter Kolar, *Fellow, IEEE*, and Oscar Apeldoorn

(Invited Paper)

***Abstract*—Soft-switching techniques are very attractive and often mandatory requirements in medium-voltage and medium-frequency applications such as solid-state transformers. The effectiveness of these soft-switching techniques is tightly related to the dynamic behavior of the internal stored charge in the utilized semiconductor devices. For this reason, this paper analyzes the behavior of the internal charge dynamics in high-voltage (HV) semiconductors, giving a clear base to perform overall converter optimizations and to understand the previously proposed zero-current-switching techniques for insulated-gate bipolar-transistor (IGBT)-based resonant dual active bridges. From these previous approaches, the two main concepts that allow switching loss reduction in HV semiconductors are identified: 1) shaping of the conducted current in order to achieve a high recombination time in the previously conducting semiconductors; and 2) achieving zero-voltage-switching (ZVS) in the turning-on device. The means to implement these techniques in a triangular-current-mode dual-active-bridge converter, together with the benefits of the proposed approaches, are analyzed and experimentally verified with a 1.7-kV IGBT-based neutral-point-clamped (NPC) bridge. Additionally, the impact of the modified currents in the converter's performance is quantified in order to determine the benefits of the introduced concepts in the overall converter.**

***Index Terms*—Charge carrier lifetime, insulated gate bipolar transistors (IGBT), zero current switching, zero voltage switching.**

I. Introduction

TRANSFORMERS operating in line frequency (50 Hz/60 Hz) are key components within today's electric power systems as they provide the link between grids with different voltage levels, namely, high-voltage (HV), medium-voltage (MV), and low-voltage (LV) grids. These transformers, however, are characterized by several limitations such as large size/weight, ideally equal input and output active and reactive power values, equal input and output operating frequencies, and tightly linked input and output voltages.

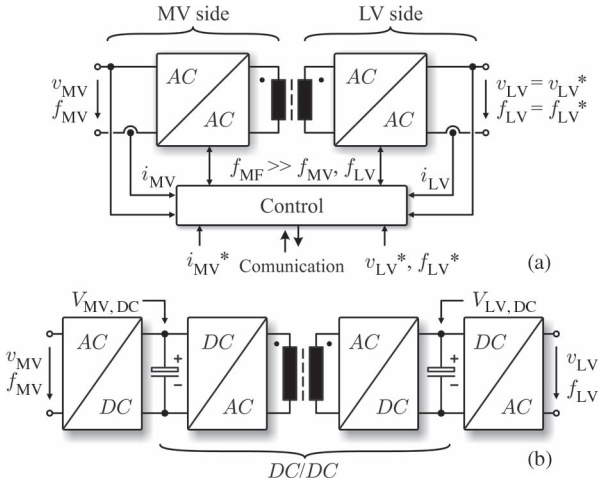

Fig. 1. SST: (a) single-phase structure; (b) three-stage concept comprising a high-power dc/dc converter.

These limitations can be overcome by building a transformer based on power electronic devices, i.e., a solid-state transformer (SST). An example of a single-phase SST is shown in Fig. 1(a). Here, the MV side ac/ac converter is used to actively shape the input current i_{MV}, for example, to reach a unity power factor or in other cases, to act as an active filter and/or a static var compensator. The link between the MV and the LV ac/ac converters is done through a transformer whose operating frequency f_{MF} lies in the medium-frequency (MF) range, thus achieving a small size/weight and a faster dynamic response. On the LV side, the characteristics of the output ac voltage, namely, amplitude v_{LV} and frequency f_{LV}, can be actively controlled with little dependence on the MV side voltage v_{MV} and frequency f_{MV}. These additional functionalities are envisioned as the key enabling features for future compact traction solutions [1], [2], grid integration of renewable energy generation [3]–[5], and smart grid implementation [6], [7], among others.

One possible structure for the SST is a three-stage concept [6] presented in Fig. 1(b). In this concept, ac/dc MV and LV converters are connected to the MV and LV ac grids, respectively. The dc links of these ac/dc converters are linked through

Manuscript received July 17, 2012; revised September 19, 2012; accepted September 27, 2012. Date of publication January 4, 2013; date of current version January 18, 2013. The review of this paper was arranged by Editor E. Seebacher.

G. Ortiz, H. Uemura, D. Bortis, and J. W. Kolar are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8006 Zurich, Switzerland (e-mail: ortiz@lem.ee.ethz.ch).

O. Apeldoorn is with the Power Electronics and Medium Voltage Drives Business Unit, ABB Switzerland AG, 5300 Turgi, Switzerland.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2012.2223215

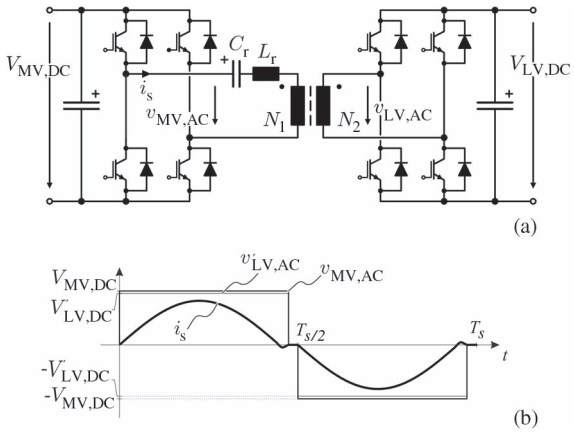

Fig. 2. HC-DCM-SRC: (a) power circuit linking MV to LV dc buses; (b) voltage and current in the ac link.

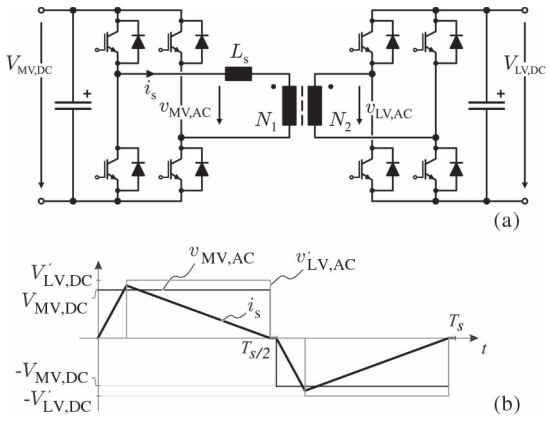

Fig. 3. Triangular current DAB: (a) power circuit linking MV to LV dc buses; (b) voltage and current in the ac link.

a high-power dc/dc converter, where the isolation and voltage step-down is provided through an MF ac link. In the dc/dc converter, the semiconductors in the MV side bridge are required to block voltages in the kilovolt range; therefore, IGBTs are a very attractive choice. These semiconductors, however, are characterized by a bipolar power stage that, in order to block these HVs, comprises a considerably large N-base region, which stores a large amount of charge during the conduction phase of the semiconductor. When the switch is turned off, this stored charge is evacuated from the semiconductor, causing tail currents that overlap with the blocking voltage, hence generating high switching losses. If operated in the MF range, these switching losses would be unbearable, unless the current through the semiconductors is conveniently shaped during its conduction phase in order to achieve zero-current switching (ZCS).

A widespread topology that can allow bidirectional power flow and ZCS operation, investigated mainly in traction applications, is the half-cycle discontinuous-conduction-mode series-resonant converter (HC-DCM-SRC) [1], [8]–[12] (cf. Fig. 2). This topology consists of two active bridges linked through an MF transformer in series with a resonant tank. When operated below resonant frequency, this converter allows the MV and LV side switches to operate in ZCS, thus reducing their switching losses. Nevertheless, these switching losses are not negligible despite ZCS operation. For this reason, several enhancements to the ZCS modulation scheme that allow a further reduction in the switching losses have been previously reported, whereby the main approaches are revised in this paper.

The main disadvantage of the HC-DCM-SRC, in addition to its lower power density and high current requirement of the series resonant capacitor C_r, is its incapability to control the transferred power while still achieving ZCS. In case power transfer control is required, the triangular-current-mode dual active bridge (TCM DAB) presents an attractive solution [13] (cf. Fig. 3). In this converter, the resonant tank is replaced by a series inductor L_s. By properly selecting the transformer turns ratio, the MV side switches can be operated in ZCS mode in both power directions while actively controlling the transferred power by adjusting the LV side duty cycle [14], [15]. In this case, however, it is not possible to achieve ZCS on the LV side.

Accurate model for estimating the switching losses in these ZCS-operated converters is the key missing element within the converter modeling that would enable an overall system optimization, e.g., aiming for maximum power density or efficiency. The dynamics of the internal charge behavior in IGBTs have been previously reported in literature [16]–[19]. However, in these publications, a simple model that links the stored charge dynamics to the semiconductors' conducted current, in order to perform the aforementioned overall system optimization, has not been analyzed. For this reason, this paper analyzes in Section II the behavior of the stored charge in bipolar semiconductor devices for an arbitrary current shape, which would later enable an estimation of the ZCS losses. This stored charge analysis gives the base to study in Section III the previously proposed ZCS methods in the HC-DCM-SRC. With this revision, novel concepts for switching loss reduction in the TCM DAB converter by means of soft-switching techniques are proposed and experimentally validated in Section IV. The reduction in switching losses in the MV side of the TCM DAB results in modified current shapes in the converter; therefore, the impact of these new current shapes in the overall converter performance is quantitatively studied at the end of Section IV.

II. Semiconductor Stored Charge Dynamics

HV bipolar semiconductor devices, as aforementioned, store large amounts of charge during their conduction phases. This charge, if not allowed to recombine internally, is translated into switching losses when the device is taken back to the blocking state. Since this stored charge is directly related to the dissipated energy during the switching process, it is useful to analyze the behavior of the charge $Q(t)$ stored in the switch during its conduction phase. In order to perform this analysis, first, the minority carrier (hole) concentration $p_0(t)$ in the N-base layer needs to be analyzed. Consider the following expression that describes the relation between carrier concentration $p_0(t)$ and hole current density (diffusion current) $J_{p0}(t)$:

$$p_0(t) = \frac{L_a}{2qD_p} \tanh\left(\frac{W_N}{L_a}\right) J_{p0}(t) \tag{1}$$

$$L_a = \sqrt{\tau D_a} \tag{2}$$

where L_a is the ambipolar diffusion length, D_p is the hole diffusion constant in the N-base layer, W_N is the thickness of the N-base layer, q is the electron charge, τ is the recombination time constant, and D_a is the ambipolar diffusion constant. Within the N-base layer, the carrier distribution decays exponentially due to recombination [20]; hence

$$p(x,t) = p_0(t) \cdot e^{\left(-\frac{x}{L_a}\right)}. \tag{3}$$

Integrating (3) over the N-base layer and multiplying by the elementary electric charge q and the device area S gives the total charge $Q(t)$ in the N-base layer

$$Q(t) = qS \int_0^{W_N} p(x,t) \cdot dx \tag{4}$$

$$= qS \cdot L_a \cdot p_0(t) \cdot \left(1 - e^{\left(-\frac{W_N}{L_a}\right)}\right). \tag{5}$$

This charge $Q(t)$ recombines in a lossless manner as long as the collector–emitter voltage $V_{\rm CE}$ remains close to zero. If a positive collector–emitter voltage $V_{\rm CE}$ is applied to the device before total recombination is achieved, the remaining charge will be externally removed from the N-base layer, causing switching losses in the semiconductor. In HV devices, the N-base layer width W_N is made large in order to withstand the blocking voltage. In (5), it is shown that a large N-base directly increases the amount of stored charge $Q(t)$ in the device, hence increasing the switching losses. Additionally, in HV devices, the carrier lifetime τ is made long in order to decrease the ON-state voltage, which increases the amount of stored charge. In some applications, however, lifetime control can be applied in order to decrease the lifetime τ, i.e., reducing switching losses, but with increased ON-state voltage and hence higher conduction losses.

In order to calculate the instantaneous value of stored charge $Q(t)$ for an arbitrary current $i_s(t)$, the following equation, the time-dependent ambipolar diffusion equation, is used:

$$\frac{dp(x,t)}{dt} = -\frac{p(x,t)}{\tau} + D_a \frac{d^2p(x,t)}{dx^2} \tag{6}$$

which is valid while the collector–emitter voltage $V_{\rm CE}$ is constant and ≈ 0 V. By differentiating (4) with respect to time and combining with (6), the following expression is obtained:

$$\frac{dQ(t)}{dt} = qS \int_0^{W_N} \left(-\frac{p(x,t)}{\tau} + D_a \frac{d^2p(x,t)}{dx^2}\right) dx$$

$$= \underbrace{-qS\frac{L_a}{\tau} \cdot p_0(t) \cdot \left(1 - e^{\left(-\frac{W_N}{L_a}\right)}\right)}_{\frac{Q(t)}{\tau}}$$

$$+ qS\frac{D_a}{L_a} p_0(t) \left(1 - e^{\left(-\frac{W_N}{L_a}\right)}\right). \tag{7}$$

The first term on the right-hand side of (7) is equal to $Q(t)/\tau$. Replacing (1) in (7), the following expression is found:

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau}$$

$$+ qS\frac{D_a}{L_a}\frac{L_a}{2qD_p}\tanh\left(\frac{W_N}{L_a}\right)\left(1 - e^{\left(-\frac{W_N}{L_a}\right)}\right) J_{p0}(t). \tag{8}$$

The hole current density $J_{p0}(t)$ is proportional to the total current density $J_s(t)$ through the switch

$$J_{p0}(t) = J_s(t) \cdot K_{p0} = \frac{K_{p0}}{S} \cdot i_s(t) \tag{9}$$

where $i_s(t)$ is the instantaneous current through the switch, and K_{p0} is the proportional constant relating the total current density $J_s(t)$ to the diffusion current density $J_{p0}(t)$. This constant depends on the switch technology whereby the expressions for the field-stop (FS) and nonpunchthrough (NPT) technologies can be found in [21]. Replacing (9) into (8) yields

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau}$$

$$+ \underbrace{q\frac{D_a}{L_a}\frac{L_a}{2qD_p}\tanh\left(\frac{W_N}{L_a}\right)\left(1 - e^{\left(-\frac{W_N}{L_a}\right)}\right) K_{p0}}_{k_s} \cdot i_s(t). \tag{10}$$

The constant (nontime dependent) part of the second term on the right-hand side of (10) is condensed into term k_s (with $0 < k_s < 1$), which is a proportionality parameter tightly related to device construction and operating junction temperature T_j. Finally, the expression for the dynamic behavior of the stored charge $Q(t)$ in the semiconductor device for an arbitrarily shaped current $i_s(t)$ is found

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} + k_s \cdot i_s(t). \tag{11}$$

As shown, (11) provides a simple expression for the dynamic behavior of the stored charge $Q(t)$ in the semiconductor device, whereby only parameters τ and k_s are required in order to describe this behavior. These parameters, however, are usually confidential information from the semiconductor manufactures and therefore cannot be extracted from the device's datasheet, for example. For this reason, parameters τ and k_s were extracted for 1.7-kV FS and NPT semiconductor devices by performing the experiment described in the following.

Consider the circuit depicted in Fig. 4(a) where an IGBT-based bridge leg is presented. Here, a current source generates the triangular current i_s shown in Fig. 3(b) whereby switch S_1 is turned on at $t = 0$, i.e., the beginning of the switching period, and turned off at $t = \Delta T$. By increasing stepwise the value of ΔT from $\Delta T = 0$ to $\Delta T = t_{\rm off}$, as shown in Fig. 4(b), the current turned off by device S_1 is modified. By measuring the current i_{S1} through S_1 and integrating it during the switching process for each value of ΔT, the charge stored in the device during the conduction phase is constructed. This experiment was also performed in [19] for a resonant structure, where the dynamic behavior of the stored charge was observed.

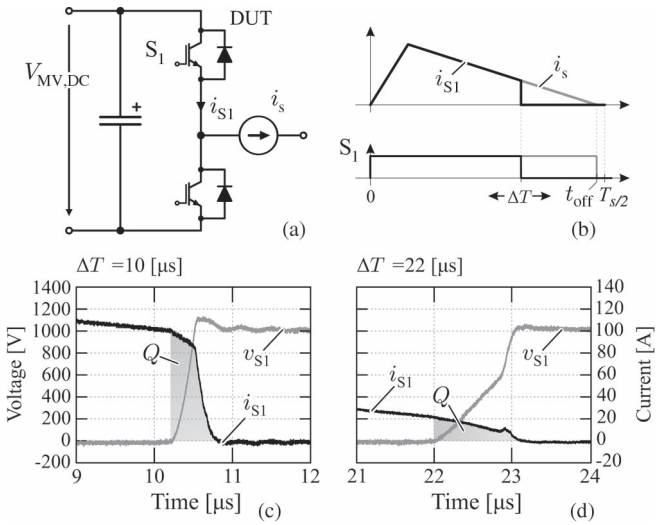

Fig. 4. In order to measure the semiconductor's stored charge, the circuit in (a) was used. The triangular current shape shown in (b) is generated by the current source in (a) and is used to measure the stored charge in the IGBT switches. Two values of switched current and the respective measurement of the evacuated charges are shown in (c) and (d).

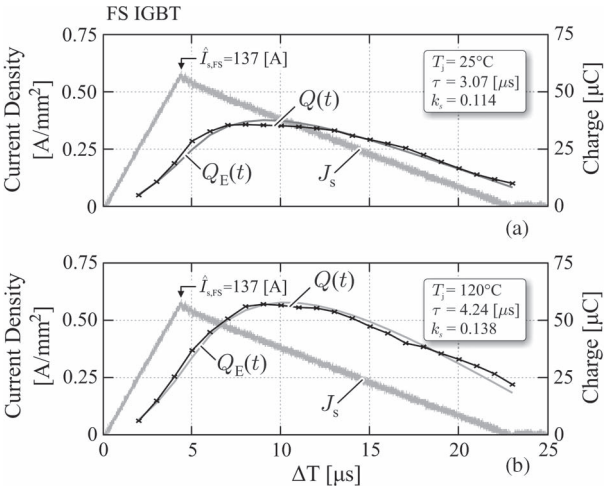

Fig. 5. Experimentally measured charge behavior $Q(t)$ for TCM modulation in the FS IGBT at (a) 25 °C and (b) 120 °C. The charge behavior was also analytically calculated with (11) and the shown fitted values for τ and k_s, leading to the waveforms of estimated charge $Q_E(t)$.

The aforementioned test was realized with two bridge legs based on 1.7-kV FS (FF150R17KE4) and NPT (IXGN100N170) IGBTs operating at 20 kHz with a dc-link voltage of $V_{\mathrm{MV,DC}} = 1$ kV. The voltage and current waveforms in S_1 using the FS IGBT for $\Delta T = 10$ μs and $\Delta T = 22$ μs are shown in Fig. 4(c) and (d), respectively. Here, the area considered for measurement of the stored charge for different switched currents is highlighted.

Since the utilized FS and NPT IGBTs are rated for different current levels, the described experiment was performed considering equal peak current densities J_s in both devices. Therefore, their chip areas were measured, whereby values of $S_{\mathrm{FS}} = 228$ mm^2 and $S_{\mathrm{NPT}} = 152$ mm^2 were obtained for the FS and NPT IGBTs, respectively. Considering a maximum current density of $\hat{J}_s = 0.6$ A/mm^2, the peak currents reached

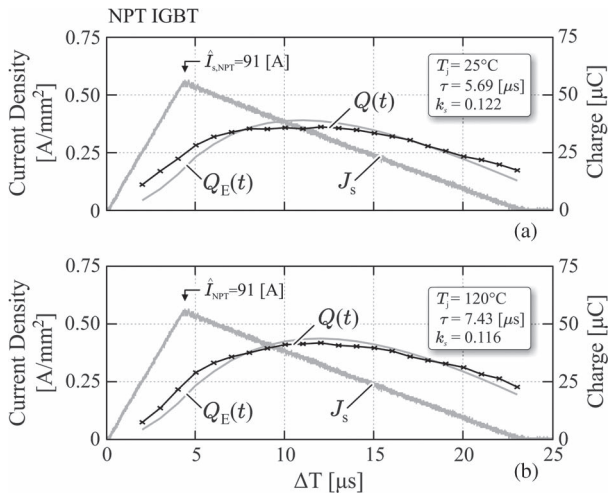

Fig. 6. Experimentally measured charge behavior $Q(t)$ for TCM modulation in the NPT IGBT at (a) 25 °C and (b) 120 °C. The charge behavior was also analytically calculated with (11) and the shown fitted values for τ and k_s, leading to the waveforms of estimated charge $Q_E(t)$.

TABLE I
EXTRACTED PARAMETERS FOR THE 1.7-kV FS AND NPT IGBTS AT JUNCTION TEMPERATURES OF $T_j = 25$ °C AND $T_j = 120$ °C

Switch	Temperature T_j	τ	k_s
FS	25 °C	3.07 µs	0.114
FS	120 °C	4.24 µs	0.138
NPT	25 °C	5.96 µs	0.122
NPT	120 °C	7.43 µs	0.116

with the FS and NPT IGBTs are $\hat{I}_{s,\mathrm{FS}} = 137$ A and $\hat{I}_{s,\mathrm{NPT}} = 91$ A, respectively.

The results for the measured behavior of the charge $Q(t)$ in the FS and NPT IGBTs are presented in Figs. 5 and 6, respectively, for junction temperatures of 25 °C and 120 °C. In each case, the measured behavior of charge $Q(t)$ was used to estimate the values of τ and k_s in (11) in order to analytically describe the behavior of the charge. These parameters were extracted using the least squares method, whereby the obtained values are summarized in Table I and the resulting estimated charge $Q_E(t)$ behavior is also presented in Figs. 5 and 6.

In the case of the FS IGBT (cf. Fig. 5), the dynamic behavior of the charge $Q(t)$ can be clearly seen. For this converter, this means that the switching losses in the IGBT do not depend on the instantaneous value of switched current. This means, for example, that by switching the peak current of $\hat{I}_{s,\mathrm{FS}} = 137$ A at $t = 4$ μs, less charge is removed; hence, lower switching losses are generated, in comparison to switching at $t = 10$ μs, when the value of the switched current is considerably lower. Moreover, at time $t = 23$ μs, when the current reaches zero, a considerable amount of charge remains stored in the device; thus, turning S_1 off in ZCS conditions would not result in zero switching losses. In other cases, e.g., in inverter applications, the conduction phase is usually long enough (e.g., three to four times the time constant τ), and therefore, the static behavior of the charge

$$Q(t) = \tau \cdot k_s \cdot i_s(t) \tag{12}$$

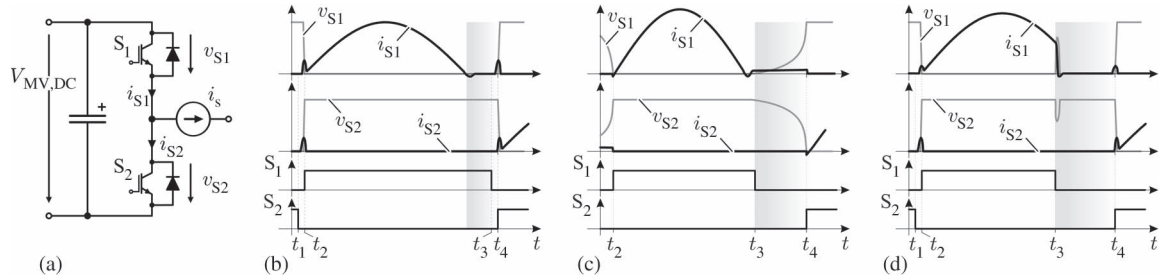

Fig. 7. Previously reported enhancements to the ZCS HC-DCM-SRC: (a) IGBT phase leg; (b) interlock time introduced; (c) increased magnetizing current; and (d) non-ZCS.

is reached. In this case, the stored charge, hence switching losses, is proportional to the switched current, as commonly stated in IGBTs' datasheets.

In Fig. 5(b), the behavior of the charge $Q(t)$ for junction temperature T_j of 120 °C is shown, whereby a considerable sensitivity of the stored charge behavior with respect to temperature is visible. This is confirmed by the values of τ and k_s estimated in this case, which are both higher in comparison to the one obtained with operation at 25 °C, as expected for this type of IGBT technology [18]. It should be noted that for both temperature values, an accurate fitting of (11) is achieved; thus, for this device, the analytical description of the stored charge proves useful to estimate the charge behavior in the device.

In comparison with the FS device, it can be observed that the NPT switch features a larger recombination time constant τ (cf. Fig. 6) for both tested junction temperatures, as expected for this type of switch technology [18]. Moreover, it can be seen that the sensitivity to operation at higher temperatures is lower for this type of IGBT, which is also in agreement with the expected behavior. It should be noted that, similar to the FS IGBT, (11) with the fitted values of τ and k_s in this case also represents the behavior of the charge $Q(t)$ in the NPT device during its conduction phase. However, the accuracy of this equation is lower than that in the case of the FS switch, as can be seen by the behavior of $Q_E(t)$ in Fig. 6(a) and (b). This difference can be explained by light dependence of parameter K_{p0} with respect to conducted current $i_s(t)$, as described in [20] and [22].

Table I summarizes the extracted parameters of the two analyzed IGBTs at $T_j = 25$ °C and $T_j = 120$ °C. It can be observed that the FS device features a faster time constant at both measured temperatures. This makes the FS IGBT more suitable for ZCS modulation schemes, where fast recombination of the internal charge is a key feature to reach low switching losses and hence high efficiency. On the other hand, the NPT IGBT shows a lower sensitivity to temperature, and therefore, it may be attractive for applications where a high operating temperature of the IGBT's junction is necessary in order to reduce the heat-sink size and therefore increase power density. In the following, only the FS IGBT will be considered in the verification of the proposed ZCS techniques.

The aforementioned analysis of the stored charge in FS and NPT IGBTs provides the base for modeling the ZCS losses in this type of semiconductor devices. This model represents the last missing element within the converter model, which would enable an overall converter optimization, e.g., based on a Pareto front analysis [23]. Moreover, based on the previous stored charge analysis, the first observation regarding soft-switching techniques in HV semiconductors can be made: The shape of the current during the conduction phase highly influences the remaining stored charge that needs to be evacuated from the switch when entering the blocking state. Therefore, it is desirable to conveniently shape this current in order to minimize the ZCS losses, as reported in previous publications on the HC-DCM-SRC (cf. Fig. 2) whereby the main approaches are revised in the next section.

III. Previously Proposed ZCS Techniques in Resonant Converters

Consider the bridge leg presented in Fig. 7(a) where the current source i_s represents the resonant tank together with the rest of the HC-DCM-SRC circuit [cf. Fig. 2(a)]. This current source generates the sinusoidal pulses shown in Fig. 7(b)–(d) used to analyze three of the main previously proposed enhancements in the ZCS modulation scheme for this converter structure: *A interlock time*; *B increased magnetizing current;* and *C giving up ZCS*.

A. Interlock Time

As described in [9] and [24], the resonant converter offers the possibility to introduce an interlock time in the conduction of S_1 between zero crossing of the current and the turn-on event of S_2, as shown in Fig. 7(b). This interlock time provides additional time for the IGBT to recombine its carriers in a lossless manner; thus, the switching losses generated when S_2 is turned on are considerably reduced.

B. Increase in Magnetizing Current

In the HC-DCM-SRC, the bridge providing the power also needs to provide the magnetization current for the isolation transformer. This means that when the resonant pulse is finished, the magnetizing current continues flowing through the previously conducting IGBTs, as shown in Fig. 7(c). Therefore, if the magnetizing current is made high enough, it can be used to extract stored charge from the IGBT, as described in [11] and [24]. It should be noted that, if enough time is provided to change the voltage in S_1 and S_2, the turn-on process of S_2 is done under ZVS conditions; thus, a great reduction in switching losses can be achieved.

C. Giving Up ZCS

As reported in [9] and [24], switch S_1 in Fig. 7(a) can be turned off before the resonant pulse has reached zero current. This way, the charges stored in the IGBT can be removed by the resonant inductor, and under certain conditions, ZVS can be achieved in the turning-on IGBT. In order to achieve this, the resonant inductor L_r must store enough energy to charge/discharge S_1 and S_2.

A large resonant inductor, however, is undesirable in this converter since it affects its dynamic performance and it can cause problems related to the reverse recovery of the rectifying diodes. For this reason, turning off S_1, as shown in Fig. 7(d), does not result in traditional inductive switching. Nevertheless, this type of switching strategy has reported reduction in switching losses in previous implementations [9], [24] due to the additional time that can be provided for carrier recombination [see the shaded area in Fig. 7(d)].

D. Applications to the TCM DAB Converter

The aforementioned enhancements to the ZCS modulation in the HC-DCM-SRC suggest the use of similar techniques in the TCM DAB. In the case of the additional interlock time, its implementation in the TCM DAB is not straightforward. This is due to the reverse recovery of the rectifying diodes in the LV side. In the HC-DCM-SRC, the series inductor L_r is typically kept as low as possible to improve the converter dynamic response. This results in a large resonant capacitor C_r value; thus, the peak voltage in this component is low in comparison to the dc-link voltages. The peak resonant capacitor voltage must be blocked by the diodes in the rectifying bridge after their respective conduction phases; therefore, since this voltage step is considerably low, the reverse recovery effects are negligible, as reported in [9], [11], and [24].

On the other hand, in the TCM DAB, this voltage step is considerably larger as it corresponds to the MV side applied voltage times the turns ratio of the transformer, resulting in large oscillations in the ac-link voltages due to the reverse recovery of the rectifying diodes. Therefore, other strategies to provide longer recombination time need to be implemented in the case of the TCM DAB.

Since the value of the series inductor L_s in the case of the TCM DAB is considerably higher than its resonant counterpart L_r, the stored energy in this component is considerably higher. This means that, by properly adjusting the control signals in the TCM DAB, the switches can perform switching of current, thus giving up ZCS, with high-enough value to completely remove the stored charge in the devices while achieving ZVS in the complementary switch. This can be achieved without reducing the magnetizing inductance value, as in the HC-DCM-SRC, and therefore without increasing the reactive power in the circuit. The modification to the modulation scheme that allows this behavior is introduced and experimentally verified in the next section.

IV. Proposed Enhancements to the TCM DAB

As discussed in the previous sections, there are two main strategies that can help reduce switching losses in HV semiconductors. The first one is related to the time provided for the recombination of the charge that the device stores during its conduction phase by introducing a time interval before the semiconductor blocks when the current is considerably lower than the peak current. The second one is the reduction or total elimination of turn-on losses by achieving ZVS in the turning-on device. This can be achieved by turning off a current (giving up ZCS) through a modification in the modulation scheme in the TCM DAB. The means to implement these strategies will be discussed in this section together with their experimental verification.

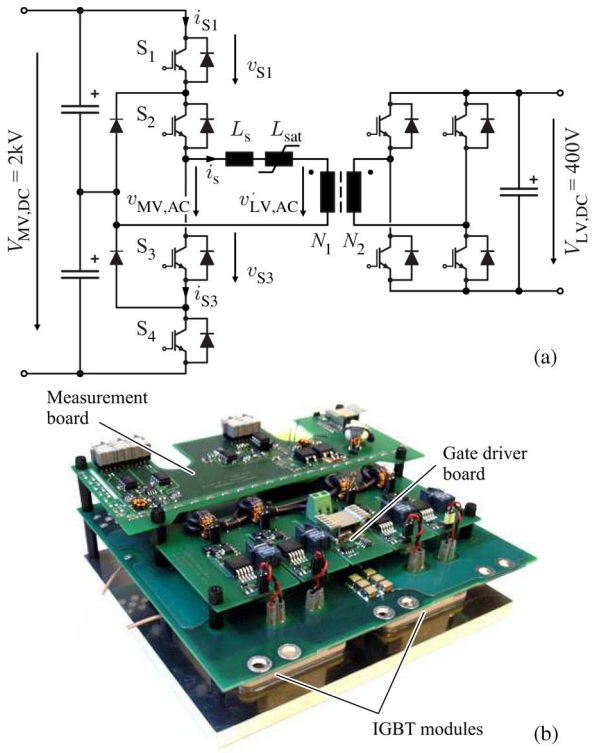

Fig. 8. DAB converter used to test the 1.7-kV FS IGBTs: (a) NPC-based bridge linked to the LV full bridge through an $N_1/N_2 = 3/1$ transformer; (b) hardware realization of the MV side NPC 2-kV bridge.

A. Standard ZCS Modulation

In order to benchmark the proposed modulation strategies for the TCM DAB, first, the switching losses in the standard ZCS modulation scheme studied in [13]–[15] were measured. These measurements were performed with the aforementioned 1.7-kV FS IGBT module (FF150R17KE4) building a 2-kV NPC-based bridge [with super fast recovery clamping diodes (DSDI 60)], as shown in Fig. 8(a), which was designed for nominal power of 166 kW and 20 kHz of switching frequency. The hardware realization of this bridge is shown in Fig. 8(b). The nonlinear inductor $L_{\rm sat}$ shown in Fig. 8(a) will be used in the third part of this section to shape the current in order to reduce the switching losses in the MV side switches. The transformer turns ratio is $N_1/N_2 = 3/1$, and the LV side bridge is a 400-V full-bridge structure utilized to generate the desired current waveforms. Planar current transformers and passive voltage probes were used to measure the currents and voltages, respectively, in switches S_1, S_2, S_3, and S_4 [cf. Fig. 8(a)].

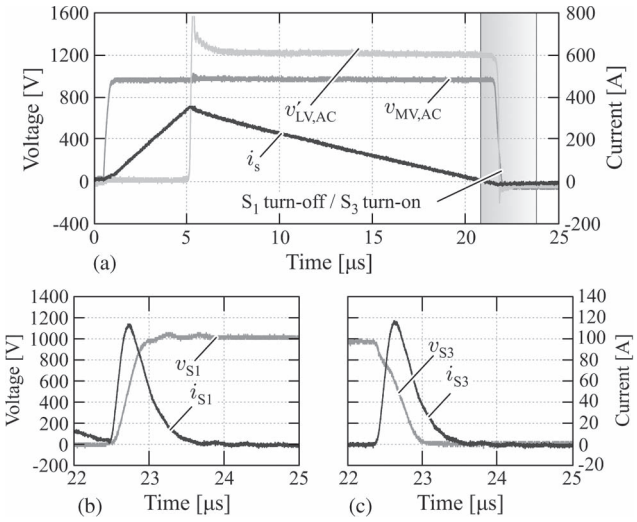

Fig. 9. Main waveforms in standard ZCS with TCM DAB and power from the MV side to the LV side: (a) ac-link waveforms for half switching period; (b) voltage and current in S_1 during the time instant highlighted in (a); and (c) voltage and current in S_3 during the time instant highlighted in (a).

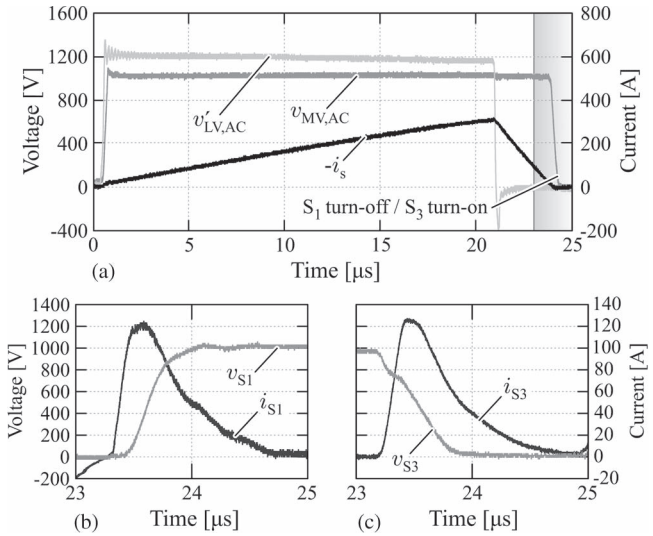

Fig. 10. Main waveforms in standard ZCS with TCM DAB and power from the LV side to the MV side: (a) ac-link waveforms for half switching period; (b) voltage and currents in S_1 during the time instant highlighted in (a); and (c) voltage and current in S_3 during the time instant highlighted in (a).

A detailed description of the operation of the TCM DAB converter together with the respective analytical formulation can be found in [15]. The turn-off and turn-on processes of complementary switches S_1 and S_3, respectively, are used herein in order to exemplify the ZCS process and the further enhancements. It should be noted, however, that for a comprehensive switching loss analysis, all switching events were measured and used to calculate the total losses in the NPC bridge. The switching process of devices S_1 and S_3 during the highlighted time interval in Fig. 9(a) is shown in Fig. 9(b) and (c), respectively. Here, it can be seen that, since S_1 was conducting the current during the positive semicycle, it contains a considerable amount of stored charge, which is removed when S_3 is turned on causing turn-off losses in S_1 and considerable turn-on losses in S_3.

The current and voltage waveforms in the transformer for power flowing from LV to MV are shown in Fig. 10(a), where the phase shift and duty cycles of the LV and MV side bridges have been adjusted to achieve the power flow in the reverse direction while still achieving ZCS in the MV side. The switching behavior of switches S_1 and S_3 is shown in Fig. 10(b) and (c), respectively, where it should be noted that, for this power direction, the respective antiparallel diodes of each switch conduct the triangular current and are therefore responsible for the generated switching losses. As can be seen, the turn-on process of S_3 generates losses in the antiparallel diode of S_1 as this last device was previously conducting the full current; thus, it contains a considerable amount of stored charge. The current peak in Fig. 10(b) and (c) representing the evacuation of charge stored in the antiparallel diode of S_1 flows through S_3 during its turn-on process, thus causing turn-on losses also in this last device [cf. Fig. 10(c)].

The waveforms shown in Figs. 9 and 10 suggest the use of a modified modulation scheme where a certain amount of current is switched off by S_1. This way, the stored charge accumulated during its conduction phase is evacuated through the load, thus decreasing the voltage of S_3 before its gate signal is applied and achieving ZVS in this last device.

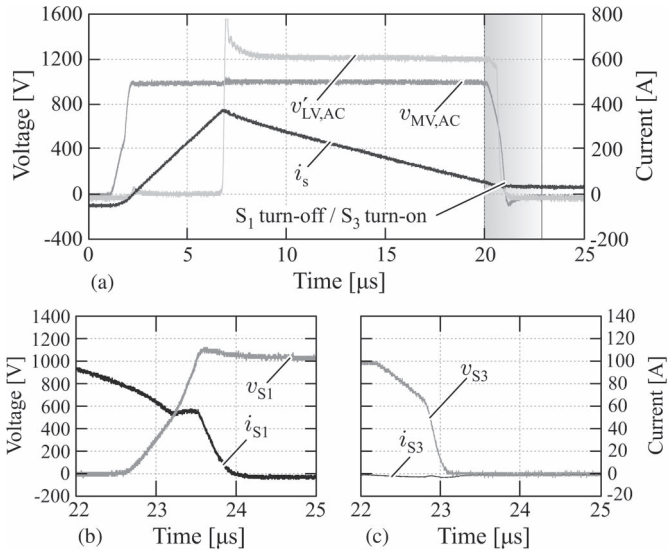

Fig. 11. Main waveforms in ZVS with TCM DAB and power from the MV side to the LV side: (a) ac-link waveforms for half switching period; (b) voltage and current in S_1 during the time instant highlighted in (a); and (c) voltage and current in S_3 during the time instant highlighted in (a).

B. Modified ZVS Modulation

The operation under ZVS was studied for the converter displayed in Fig. 8 (without the saturable inductor L_{sat}). The waveforms for power from MV to LV are shown in Fig. 11(a), where the duty cycles and phase shift are adjusted in order to achieve ZVS in the MV side bridge. In this case, S_1 is turned off before the current reaches zero, thus loosing ZCS, as shown in Fig. 11(b). Since the current is not zero when S_1 is turned off, its voltage increases before the gate signal is applied to its

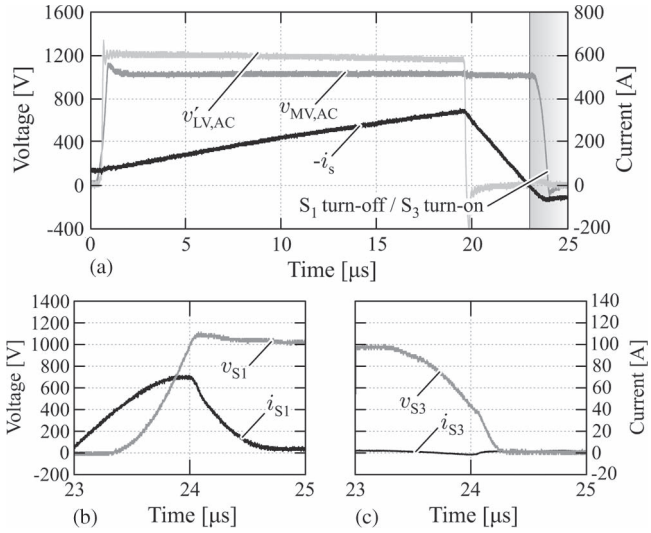

Fig. 12. Main waveforms in ZVS with TCM DAB and power from the LV side to the MV side: (a) ac-link waveforms for half switching period; (b) voltage and current in S_1 during the time instant highlighted in (a); and (c) voltage and current in S_3 during the time instant highlighted in (a).

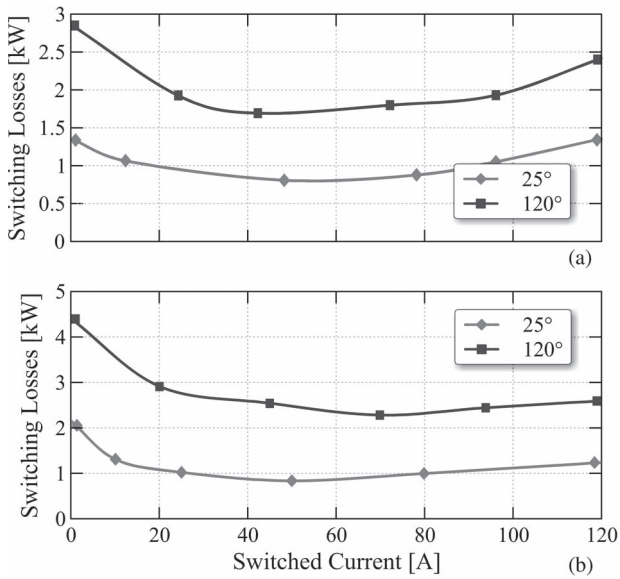

Fig. 13. Optimal switched current for switching loss minimization: (a) power from the MV to the LV side; (b) power from the LV to the MV side.

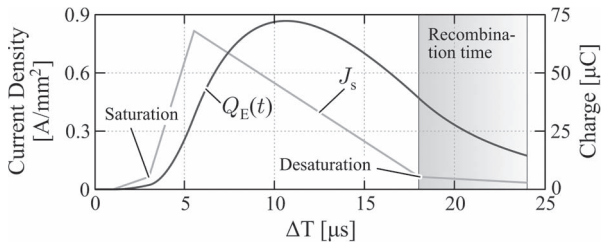

Fig. 14. IGBT-simulated charge profile for saturable inductor concept considering the FS IGBT at 120 °C ($\tau = 4.24$ μs and $k_s = 0.138$).

complementary switch S_3. This means that S_3 is turned on with ZVS and no current peak must be conducted during its turn-on process [cf. Fig. 11(c)], in contrast to the switching process shown in Fig. 9(c), thus reducing the turn-on losses in S_3 to a negligible value.

In Fig. 12(a), the operation for power from the LV to the MV side is shown with a modification in the modulation scheme, which allows the antiparallel diode of S_1 to conduct in the reverse direction by keeping the gate signals of its respective switch on until the reverse recovery charge has been evacuated. The results of this modification in the switching performance of S_1 and S_3 are shown in Fig. 12(b) and (c), respectively. As previously explained, the current is allowed to reverse its direction in S_1 before it is turned off; thus, its voltage is increased by the switched current and not by the turn-on process of switch S_3. Therefore, the turn-on losses in S_3 are considerably reduced, as shown in Fig. 12(c).

Taking all switching processes into account, the switching losses in all switches and diodes of the MV side bridge were measured under ZVS operation for different switched currents, at 25 °C and 120 °C, and for power in both directions. In Fig. 13(a), the results for power transfer from MV to LV side are presented. Here, an optimum can be found around 40 A of switched current for operation at 120 °C, reaching a reduction of 40% in the total switching losses. Above this current value, no further reduction on the turn-on losses is achieved whereas the turn-off losses are increased; consequently, the overall switching losses are also increased.

The results for power flow from LV to MV are shown in Fig. 13(b). It can be seen that the switching losses have an optimum value around 70 A for operation at 120 °C, where a 48% reduction with respect to operation in ZCS is achieved. It can be seen that if higher currents are switched off, no further reduction of turn-on losses is achieved whereas the turn-off losses are increased.

C. Saturable Inductor

By inserting a saturable inductor $L_{\rm sat}$ (cf. Fig. 8) in series to the series inductor L_s, the current through the transformer, and consequently through the switches, can be conveniently shaped in order to stay in a low value for a considerable portion of the switching period right before the devices are taken to blocking state, as shown in Fig. 14 where a simulation of the stored charge behavior for the FS IGBT operated at 120 °C is presented. When compared with the amount of charge removed in normal ZCS mode [cf. Fig. 5(b)], an improvement is achieved since less charge must be evacuated when the voltage is reapplied. This new current shape is merged with the previously introduced ZVS modulation, thus combining the features of long recombination time and ZVS.

For the analyzed converter, a saturable inductor with a saturation current of 35 A was used. While keeping this saturation current constant, the inductance value was modified, whereby three different values were tested, i.e., 40, 70, and 100 μH. The resulting current waveforms for power from the MV side to the LV side, i.e., IGBTs conducting the current, are shown in Fig. 15 for a saturable inductor value of $L_{\rm sat} = 100$ μH. As shown in Fig. 15(a), the saturable inductor introduces a time interval before the bridge is taken to freewheeling when the current is comparatively low, thus allowing S_1 and S_2 to

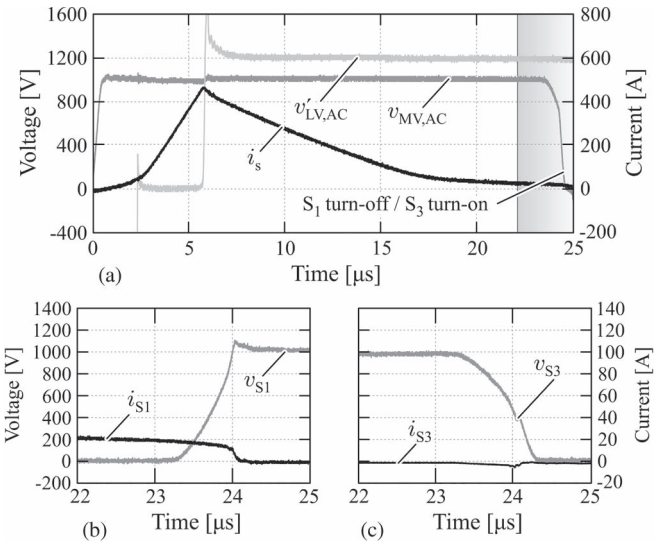

Fig. 15. Main waveforms TCM DAB with a 100-μH saturable inductor and power from the MV side to the LV side: (a) ac-link waveforms for half switching period; (b) voltage and current in S_1 during the time instant highlighted in (a); and (c) voltage and current in S_3 during the time instant highlighted in (a).

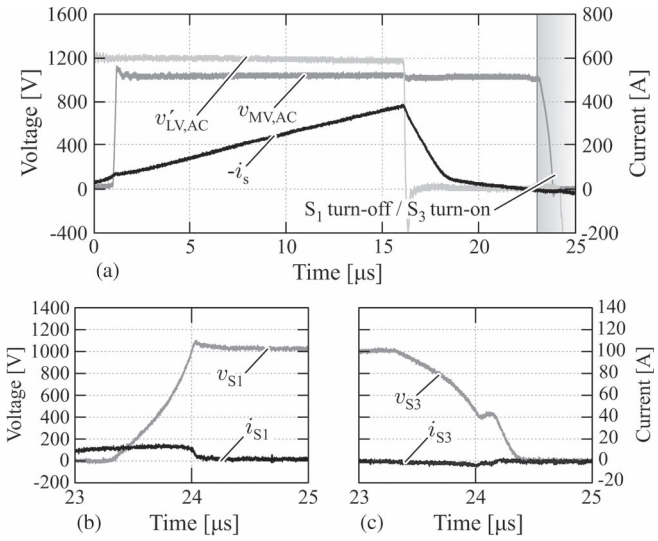

Fig. 16. Main waveforms TCM DAB with a 100-μH saturable inductor and power from the LV side to the MV side: (a) ac-link waveforms for half switching period; (b) voltage and current in S_1 during the time instant highlighted in (a); and (c) voltage and current in S_3 during the time instant highlighted in (a).

recombine a large amount of the charge generated during the conduction phase. In addition, a certain amount of current is turned off by S_1 [cf. Fig. 15(b)]; thus, ZVS is achieved in S_3, as shown in Fig. 15(c) and described in the previous section.

The waveforms for power from the LV to the MV side and a saturable inductor $L_{\rm sat} = 100$ μH are shown in Fig. 16(a) whereby the diodes in the MV side bridge benefit from the additional time for recombination. In order to achieve soft switching, the current is allowed to reverse its direction through the antiparallel diode of S_1 by keeping this last device turned on until the reverse recovery current has been reached, as shown in Fig. 16(b), thus achieving ZVS in S_3 [cf. Fig. 16(c)].

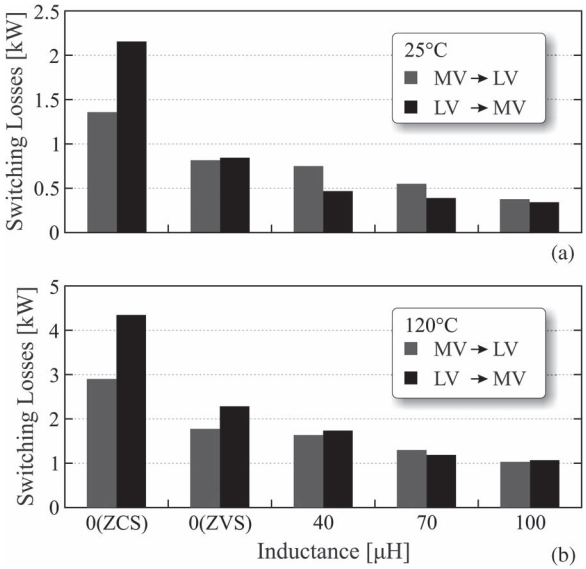

Fig. 17. Summary of reduction in switching losses in MV switches with the presented soft-switching strategies: (a) junction temperature of 25 °C; (b) junction temperature of 120 °C.

It should be noted that the addition of the saturable inductor $L_{\rm sat}$ to the circuit introduces time intervals, as long as this inductor is not saturated, when comparatively low power is transferred from the MV to the LV side. Since the required power to be transferred remains constant, this results in an increased peak current through the circuit, thus higher conducted and switching losses in the LV side. In order to reduce the impact of the saturable inductor inclusion, the voltages in the MV and LV sides are conveniently modified with respect to the traditional modulation in order to rapidly bring the saturable inductor to saturation at the beginning of the half switching period. This is shown in Fig. 15(a) before $t = 2.5$ μs when the full difference between $v'_{\rm LV,AC}$ and $v_{\rm MV,AC}$ is applied to the inductors. The result is a moderate increase in the peak current through the circuit resulting in moderate increase in conduction and switching losses, as will be quantitatively analyzed in Section IV-D.

The aforementioned tests were performed for the three values of saturable inductor, 120 °C and 25 °C junction temperatures, and power in both directions. The results for these tests are analyzed and compared with the standard ZCS and the analyzed ZVS modulations in the next section.

D. Switching Loss Reduction Summary and Impact on Converter Performance

A summary of the previously described switching loss reduction strategies is provided in Fig. 17 for power in both directions and at 25 °C and 120 °C junction temperatures. As can be seen, a considerable loss reduction can be achieved by combining ZVS techniques together with the saturable inductor. In the best case, with a 100-μH saturable inductor, the switching losses are more than four times lower for operation at 25 °C and more that three times lower when operating at 120 °C.

The introduction of the saturable inductor to shape the current through the switches increases the conduction losses in

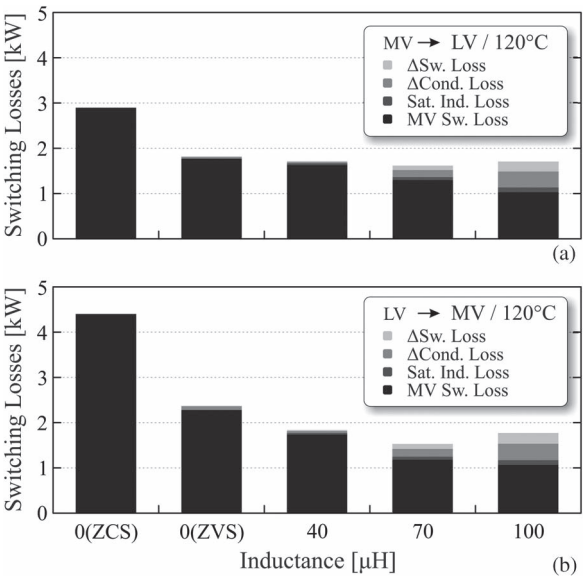

Fig. 18. Impact of modified current waveforms on converter performance for junction temperature of 120 °C. The losses in the saturable inductor plus the additional conduction and LV side switching losses are included: (a) power from the MV to the LV side; (b) power from the LV to the MV side.

the whole converter (details about the design of the complete converter are matters of upcoming publications) and switching losses in the LV side. Moreover, the saturable inductor generates by itself additional losses, which should be added to the total converter losses. In Fig. 18, the aforementioned additional losses are added to the switching losses of the MV side switches obtained from Section IV for the different strategies (please note that these are the additional conduction and switching losses and not the total conduction and switching losses). As can be seen, for power in both directions, the use of a 70-μH saturable inductor is advantageous with respect to the 100-μH inductor as the additional losses introduced by the modified current shape overcome the reduction in switching losses in the MV side in this last case. This means that, for this application, the use of a 70-μH saturable inductor would result in the lowest losses in the overall converter.

V. Conclusion

Analytical and experimental analyses have been performed in order to visualize the behavior of the internal charge dynamics in HV semiconductors. This analytical model is focused on calculation of the internal charge behavior for soft-switching applications enabling an estimation of the switching losses without the need to simulate the complete switching transient in a circuit simulator. Moreover, the simple analytical model can be used as part of an overall system optimization where no circuit simulator, including, e.g., the Hefner or HiSIM IGBT models, is required to estimate the converter's switching losses. The performed experiments, which enable the extraction of the model parameters, have been also described in detail.

Furthermore, by studying the previously proposed ZCS techniques for resonant converters, the two main strategies that help reduce switching losses in MV MF applications were identified: 1) shaping of current through the semiconductors to allow a high internal carrier recombination in the device before the blocking voltage is reapplied; and 2) achievement of ZVS in the turn-on events. These two techniques were implemented in a TCM DAB. By achieving ZVS in the turning-on events, a reduction of up to 40% at 120 °C junction temperature was achieved. The shaping of current in this converter is achieved by means of a saturable inductor in series to the converter's main inductor. With this component, the current was conveniently shaped in order to stay in a low value before the device enters the blocking state, therefore achieving high stored charge recombination.

The combination of these two approaches, ZVS, and the saturable inductor, for switching loss reduction, resulted in up to four times lower switching losses of the MV side semiconductors with respect to standard ZCS modulation. The impact of the modified current shapes due to the introduction of the saturable inductor on the complete converter resulted in an optimum value for the saturable inductor of 70 μH, which minimizes the overall converter power losses.

References

[1] D. Dujic, F. Kieferndorf, F. Canales, and U. Drofenik, "Power electronic traction transformer technology," in *Proc. Power Electron. Motion Control Conf.*, 2012, pp. 636–642.
[2] C. Zhao and S. Lewdeni-Schmid, "Design, implementation and performance of a modular power electronic transformer (PET) for railway application," in *Proc. Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
[3] C. Meyer, *Key Components for Future Offshore DC Grids*. Aachen, Germany: Shaker, 2007.
[4] S. Meier, S. Norrga, and H. P. Nee, "New topology for more efficient AC/DC converters for future offshore wind farms," in *Proc. Nordic Workshop Power Ind. Electron.*, 2004, pp. 1–6.
[5] P. Monjean, J. Delanoe, J. Auguste, C. Saudemont, J. Sprooten, A. Mirzaian, and B. Robyns, "Topologies comparison of multi-cell medium-frequency transformer for offshore farms," in *Proc. Int. Conf. AC DC Power Transmiss.*, 2010, pp. 1–5.
[6] L. Heinemann and G. Mauthe, "The universal power electronics based distribution transformer, an unified approach," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 2001, pp. 504–509.
[7] J. Wang, A. Huang, W. Sung, Y. Liu, and B. Baliga, "Smart grid technologies," *IEEE Ind. Electron. Mag.*, vol. 3, no. 2, pp. 16–23, Jun. 2009.
[8] A. Esser and H. Skudelny, "A new approach to power supplies for robots," *IEEE Trans. Ind. Appl.*, vol. 2, no. 5, pp. 872–875, Sep./Oct. 1991.
[9] H. Reinold and M. Steiner, "Characterization of semiconductor losses in series resonant DC–DC converters for high power applications using transformers with low leakage inductance," in *Proc. Eur. Conf. Power Electron. Appl.*, 1999, pp. 1–10.
[10] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.
[11] H. Hoffmann and B. Piepenbreier, "High voltage IGBTs and medium frequency transformer in DC–DC converters for railway applications," in *Proc. Int. Symp. Power Electron. Elect. Drives Autom. Motion*, 2010, pp. 744–749.
[12] D. Dujic, A. Mester, and T. Chaudhuri, "Laboratory scale prototype of a power electronic transformer for traction applications," in *Proc. Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
[13] N. Schibli, "Symmetrical multilevel converters with two quadrant DC–DC feeding," Ph.D. dissertation, École Polytech. Fédérale de Lausanne, Lausanne, Switzerland, 2000.
[14] F. Krismer, J. Biela, and J. Kolar, "A comparative evaluation of isolated bidirectional DC/DC converters with wide input and output voltage range," in *Conf. Rec. IAS Annu. Meeting*, 2005, pp. 599–606.
[15] G. Ortiz, J. Biela, D. Bortis, and J. W. Kolar, "1 Megawatt, 20 kHz, isolated, bidirectional 12 kV to 1.2 kV DC–DC converter for renewable energy applications," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 3212–3219.
[16] I. Widjaja, A. Kurnia, K. Shenai, and D. Divan, "Switching dynamics of IGBTs in soft-switching converters," *IEEE Trans. Electron Devices*, vol. 42, no. 3, pp. 445–454, Mar. 1995.

[17] M. Trivedi and K. Shenai, "Internal dynamics of IGBT under zero-voltage and zero-current switching conditions," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1274–1282, Jun. 1999.
[18] A. Elasser and V. Parthasarathy, "A study of the internal device dynamics of punch-through and nonpunch-through IGBTs under zero-current switching," *IEEE Trans. Power Electron.*, vol. 12, no. 1, pp. 21–35, Jan. 1997.
[19] P. Renstad and H. P. Nee, "On dynamic effects influencing IGBT losses in soft-switching converters," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 260–271, Jan. 2010.
[20] J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York: Springer-Verlag, 2008.
[21] A. R. Hefner, "An improved understanding for the transient operation of the power insulated gate bipolar transistor (IGBT)," *IEEE Trans. Power Electron.*, vol. 5, no. 4, pp. 459–468, Oct. 1990.
[22] Y. Kim, M. Choi, and S. Chung, "Temperature dependence of the NPT-IGBTs characteristics," *J. Korean Phys. Soc.*, vol. 39, no. 91, pp. 74–77, Dec. 2001.
[23] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstübner, "Performance trends and limitations of power electronics systems," in *Proc. Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–20.
[24] L. Lindenmuller, R. Alvarez, P. Kleinichen, and S. Bernet, "Characterization of a 6.5 kV/500 A IGBT module in a series resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 4138–4143.

Gabriel Ortiz (M'10) received the M.Sc. degree in 2008 at Universidad Tecnica Federico Santa María, Valparaíso, Chile. Since 2009, he has been working toward the Ph.D. degree at the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland.

Hirofumi Uemura received the Ph.D. degree from Kyushu Institute of Technology, Kitakyushu, Japan, in 2008. Since 2011, he has been working toward the Ph.D. degree at the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland.

Dominik Bortis (S'06) received the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2008.

He is currently a Postdoctoral Fellow in the Power Electronic Systems Laboratory, ETH Zurich.

Johann Walter Kolar (F'10) received the Ph.D. degree from Vienna University of Technology, Vienna, Austria.

He became a Professor and Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2001.

Oscar Apeldoorn received the Ph.D. degree from the Technical University Aachen, Aachen, Germany, in 1997.

He is currently a Local Technology Manager at the Power Electronics and Medium Voltage Drives Business Unit, ABB Switzerland AG, Turgi, Switzerland.