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Load-Independent Voltage Balancing of Multi-Level Flying Capacitor Converters in Quasi-2-Level Operation

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Abstract: Quasi-2-level (Q2L) operation of multi-level bridge-legs, especially of flying-capacitor converters (FCC), is an interesting option for realizing single-cell power conversion in applications whose system voltages exceed the ratings of available power semiconductors. To ensure equal voltage sharing among a Q2L-FCC's switches, the voltages of a Q2L-FCC's minimized flying capacitors (FCs) must always be balanced. Thus, we propose a concept for load-independent FC voltage balancing: For non-zero load current, we use a model predictive control (MPC) approach to identify the commutation sequence of the individual switches within a Q2L transition that minimizes the FC or cell voltage errors. In case of zero load current, we employ a novel MPC-based approach using cell multiple switching (CMS), i.e., the insertion of additional zero-current commutations within a Q2L transition, to exchange charge between the FCs via the charging currents of the switches' parasitic capacitances. Experiments with a 5-level FCC half-bridge demonstrator confirm the validity of the derived models and verify the performance of the proposed load-independent balancing concept.

Keywords: quasi-2-level (Q2L); flying capacitor converter (FCC); model predictive control (MPC); flying capacitor balancing; multi-level converter

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1. Introduction

Stringent efficiency requirements for the supply of high-power DC applications such as hyperscale data centers [1–4] and high-power electric vehicle (EV) charging stations [5–8] drive the interest in direct power electronic interfaces between a medium-voltage (MV) AC grid and a low-voltage (LV) DC bus. Such flexible isolation and voltage-scaling MVAC-LVDC interfaces are commonly referred to as solid-state transformers (SSTs) [2,3,9,10]. Given the typical MV grid voltage levels of 6.6 kV rms line-to-line (3.8 kV line-to-neutral) in Europe [2] and 4.16 kV rms line-to-line (2.4 kV line-to-neutral) in the USA [3,9], clearly either latest technology wide-bandgap (WBG) power semiconductors with extreme blocking voltage ratings of up to 15 kV [11–14] or, alternatively, multi-cell topologies employing production-grade LV power semiconductors (e.g., 1.2 kV–3.3 kV SiC MOSFETs or SI IGBTs) are necessary.

Even though multi-cell SSTs can achieve a high conversion performance by configuring the cells in an input-series/output-parallel (ISOP) fashion, they are highly complex due to the typically high number of sub-units, the required communication system, and ultimately, the high component count. Therefore, recently the research focus has shifted to single-cell SST realizations, i.e., 2- or 3-level topologies enabled by new 6.5 kV–15 kV SiC MOSFETs or IGBTs [2,15]. However, the availability of these HV transistors is limited (mainly engineering samples), and prices remain high despite strong activity towards commercialization and manufacturing [16].

Alternatively, bridge-legs for single-cell SSTs can be realized with a series connection of semiconductors [17,18], super-cascode configurations [19,20], or multi-level converter structures, i.e., modular multi-level converter (MMC) [21–25] and flying capacitor converter (FCC) structures [18,26–28]. However, due to unavoidable differences (manufacturing tolerances etc.) of the semiconductor and gate driver properties, direct series connections of semiconductors require additional circuitry, i.e., (lossy) snubbers, to ensure equal transient and stationary blocking voltage sharing. The super-cascode approach [19,20] employs a series connection of several HV SiC (normally-on) JFETs and a LV Si (normally-off) MOSFET for initiating turn-on and turn-off. Similarly, it requires a passive network that is adapted to the parasitic capacitances of the SiC JFETs to ensure proper operation with balanced blocking voltages. Furthermore, only a few suppliers of MV SiC JFETs exist. The main drawbacks of an MMC topology are the high total chip area usage, the high number of gate drivers, and the presence of branch inductors. Finally, an FCC half-bridge (HB) features several advantages such as reduced switching losses (snubberless, on the contrary to direct series connection) and robust voltage balancing without additional chip area and gate drivers (compared to an MMC HB). However, conventional multi-level operation of MMC and FCC bridge-legs, while resulting in low harmonic content of the generated output voltage, requires a relatively large total volume of the flying capacitors (FCs).

The large capacitor volumes required for the MMC and FCC can be reduced by employing a quasi-2-level modulation scheme (Q2L-MMC, Q2L-FCC). With Q2L modulation, the intermediate voltage levels are only used during the switching transitions. The bridge-leg's output voltage thus transitions between the two DC voltage levels (positive and negative) in a staggered fashion [22–24,28–34]. Note that these staggered transitions of the the Q2L-MMC and Q2L-FCC topologies feature lower average $\mathrm{d}v/\mathrm{d}t$ compared to the (MV) 2-level converters, which is beneficial for the design of EMI filters and magnetics such as medium-frequency transformers, and lowers the stress of the electric insulation [29,35–38].

However, whereas in conventional multi-level operation of a FCC bridge-leg, balancing of the FC voltages occurs naturally [39], balancing is not automatically ensured in Q2L operation. Recently, the evaluation of Q2L modulation, including the selection of number of levels, dimensioning of FCs, switching frequency and modulation index have been considered in [33]. In [31], methods of FC voltage balancing through adaptation of delay times without using redundant switching sequences are presented for a Q2L-operated 5-level FCC (Q2L-5L-FCC). In this context, *switching sequence* refers to the order in which the individual FC cells are commutated during a single Q2L transition. The authors of [32] present a balancing algorithm incorporating all switching sequences based on FC voltage errors by prioritizing the FC with the largest voltage error. As shown in [32] due to the opposite voltage ripple on FCs, the switch voltages can by unbalanced by a maximum peak-to-peak voltage ripple of the FCs, which leads to a strong asymmetry of the switches' blocking voltages. To mitigate this asymmetry, further investigations of active balancing methods are required, and experimental verification of such methods, which, to the knowledge of the authors, is so far missing in literature, is needed. In addition, so far no method to ensure voltage balancing in no-load operation, i.e., with zero output current, has been presented.

In this context, in [29] we have proposed a Q2L-5L-FCC half-bridge and provided the fundamental description of Q2L operation as well as the passive and active balancing of the FC voltages for a Q2L-3L-FCC. Addressing the need discussed above, this paper generalizes these analyses and proposes a new, comprehensive concept for load-independent FC voltage balancing of Q2L-FCC bridge-legs, which so far is lacking in the literature. Similarly, so far literature does not report experimentally validated Q2L operation of FCC bridge-legs with non-sinusoidal (i.e., DC) or even zero output currents. This paper addresses this need by providing a comprehensive experimental validation of the proposed concept for load-independent FC voltage balancing. This concept comprises an original method of active cell voltage balancing using all switching sequences and it includes a novel method to balance the FC voltages even without a load current flowing (e.g., during start-

up). Figure 1a presents the considered 5L-FCC. Aiming for generic results, we consider two exemplary DC-link/load configurations resulting in symmetric (typical, e.g., for an isolated DC-DC converter) or asymmetric (typical, e.g., for a PFC rectifier or a motor inverter) output currents. Figure 1b,c show corresponding exemplary waveforms and the characteristic staggered Q2L transitions of the bridge-leg's output voltage in case of zero-voltage switching (ZVS) and hard-switching (HS).

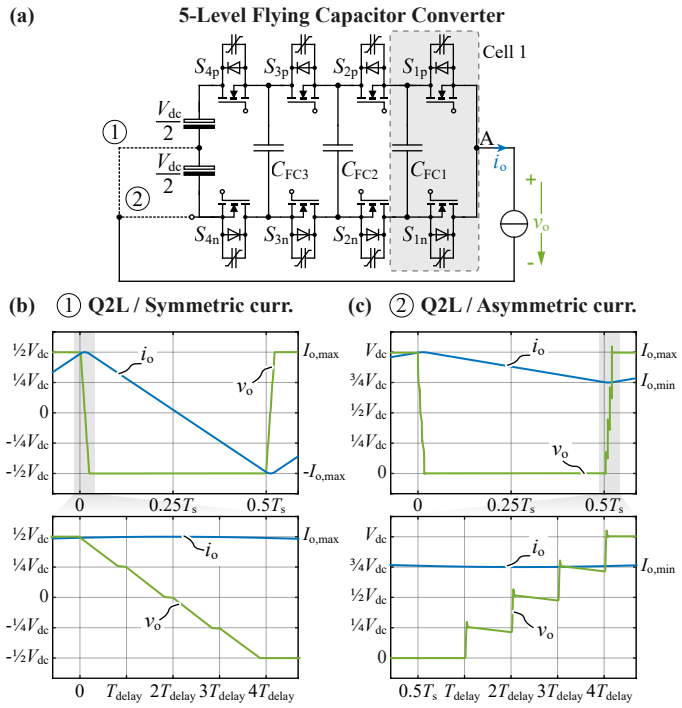

Figure 1. (**a**) Considered 5-level flying capacitor converter (5L-FCC) HB with two alternative load/DC-link connections (① and ②). Corresponding exemplary output waveforms and characteristic staggered Q2L transitions of the output voltage v_o for: (**b**) Symmetric output current i_o (ZVS transitions), (**c**) asymmetric output current i_o (ZVS & HS transitions).

This paper is organized as follows: Section 2 describes the Q2L operating principle of the 5L-FCC half-bridge for ZVS and HS transitions with non-zero output current. In addition, Q2L transitions with zero output current are analyzed, too, and a generic description of resulting charge and voltage increments is derived. Section 3 briefly recapitulates open-loop (passive) balancing of FCs, before then Section 4 presents the proposed concept of load-independent closed-loop FC voltage balancing using a model predictive controller (MPC) with FC voltage or cell voltage reference tracking. Furthermore, we introduce the cell multiple switching (CMS) concept to facilitate FC voltage balancing with zero output current. Section 5 covers the hardware demonstrator used to experimentally validate the proposed concepts. The experimental results are presented and discussed in Section 6, before Section 7 provides a concluding discussion. Finally, Appendix A investigates the behavior of CMS for semiconductors of different voltage classes. Appendix B complements the analysis of load-independent FC voltage balancing in Q2L-FCCs by discussing the behavior under overload and short-circuit conditions.

2. Q2L Operation of the 5L-FCC

This section recapitulates the processes in the Q2L-operated 5L-FCC for ZVS and HS transitions employing consecutive switching sequences described in [29]. Next, the analysis is extended by first considering also non-consecutive switching sequences and second including operation of the Q2L-FCC with zero output current. The in-depth analysis of the switching transitions given here is required to determine the total net charge exchange

of the flying capacitors during Q2L transitions and ultimately to enable the development of a robust FC voltage balancing concept for Q2L-FCCs. Note that the obtained results are generic and apply to N-level Q2L-FCCs. However, we exemplify the considerations using a 5L-FCC (see Figure 1) for clarity. The corresponding circuit simulations employ an exemplary MOSFET equivalent circuit that consist of a voltage-controlled current source, the non-linear parasitic MOSFET capacitances, the antiparallel body diode, the diode reverse recovery, and the package inductances.

2.1. Operating Principle with Non-Zero Output Current

As it can be seen in Figure 1, a 5L-FCC consists of 4 cells (in general, an N-level FCC consists of $n = N - 1$ cells), each comprising two complementary switches (S_{xp} and S_{xn}) and a flying capacitor (C_{FCx}), whereas the cell which is the closest to the DC-link includes the DC-link capacitance. A Q2L (switching) transition is a commutation of the load current from all upper switches (S_{1p}-S_{4p}) in state *on* to all bottom switches (S_{1n}-S_{4n}) in state *on*, cf. Figure 1a, or vice versa. The bride-leg output voltage v_o thus attains two distinct voltage levels ($V_{dc}/2$ and $-V_{dc}/2$) for most of the time and the several intermediate voltage levels appear only shortly during the Q2L transitions. A Q2L transition is characterized by a switching sequence (SEQ) that defines the order in which the individual cells are commutated. For example, in a 5L-FCC SEQ_{1234} means that the cells are commutated consecutively starting from cell 1 and ending with cell 4, see Figure 2a.

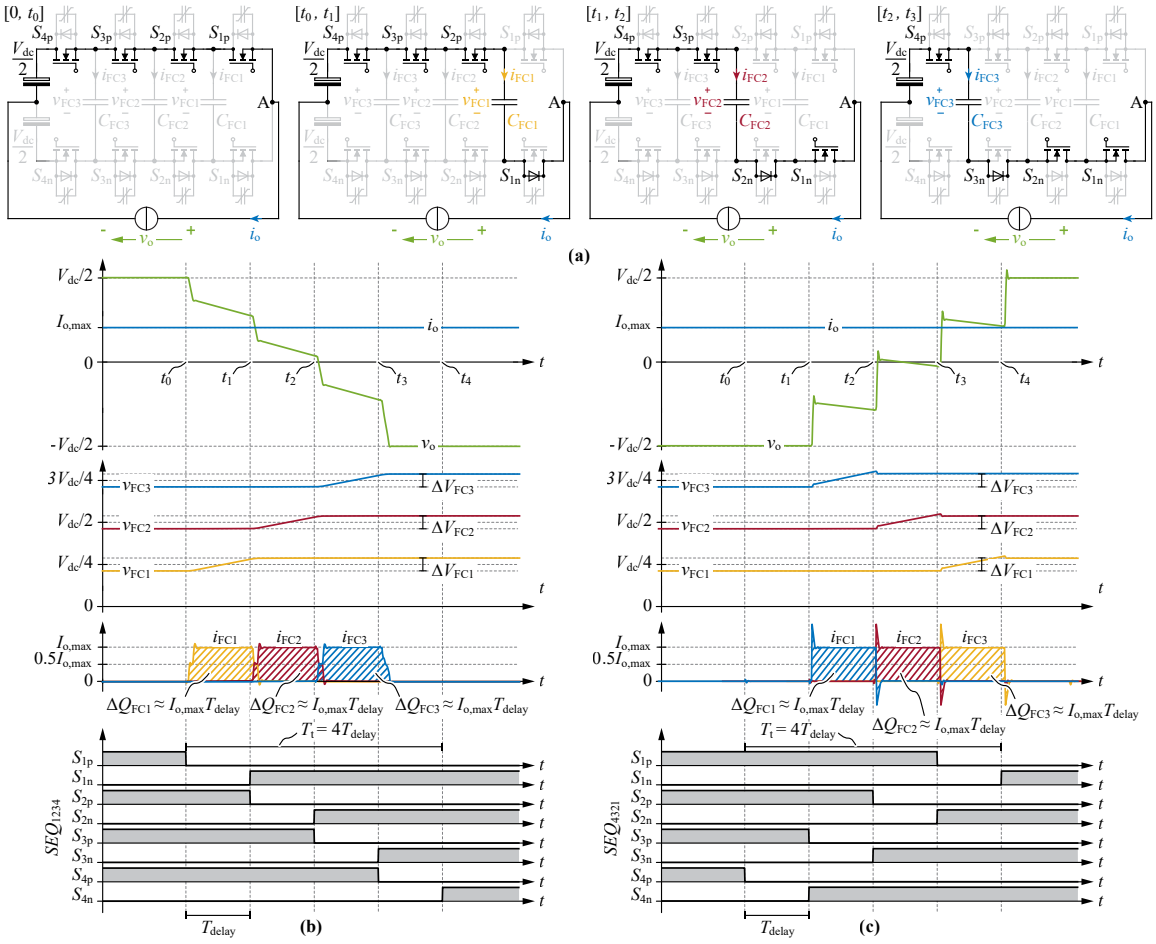

Figure 2. Simulation results for Q2L operation of the 5L-FCC: (**a**) Switching states of a FCC HB with constant positive output current ($I_{o,max}$) during a Q2L switching transition with negative slope of v_o, resulting in ZVS. (**b**) Corresponding time intervals and simulated waveforms of output current (i_o) and output voltage (v_o), FC voltages ($v_{FC\{1,2,3\}}$) and currents ($i_{FC\{1,2,3\}}$), and MOSFET gating signals. (**c**) Time intervals and simulated waveforms for the HS case with positive slope of v_o and constant output current.

Figure 2a illustrates such a Q2L transition and defines selected time intervals for the example of a falling slope of v_o, positive output current i_o and SEQ_{1234} which results in ZVS transitions for all switches. Figure 2b shows the simulated key waveforms of this transition. Similarly, Figure 2c shows key waveforms for a HS transition, i.e., constant positive output current ($I_{o,max}$) during the switching transition with positive slope of v_o and SEQ_{4321}. For a more in-depth description of processes in the sub-intervals of ZVS and HS commutations we refer to [29].

Note that consecutive sequences, i.e., SEQ_{1234} or SEQ_{4321}, lead to FC charge increments given by

$$|\Delta Q_{FC\{j\}}| \approx T_{delay\{j\}}|I_{o,max}|, \tag{1}$$

where j is the number of the FC and T_{delay} is the time allocated for the transition of an individual cell. Note that the selection of T_{delay} is discussed in detail in Section 2.3. To facilitate the modeling and balancing of FC voltages, we assume equal delay times T_{delay} for all cells and thus identical base charge increments result:

$$\Delta Q_{FC0} = \Delta Q_{FC1} = \Delta Q_{FC2} = \Delta Q_{FC3} \approx T_{delay} I_{o,max}. \tag{2}$$

It is worth noting that the transferred charges are independent of the switching frequency and the number of levels. However, the sign of the net charge exchange of an FC during a Q2L transition for a given sequence depends on the sign of the load current and the direction of the voltage slope.

For FCC realizations with more than two cells, i.e., $n > 2$ ($N > 3$), the cells can also be switched in a non-consecutive manner and thus a total of $(n!)$ different consecutive and non-consecutive sequences exists. The subset of non-consecutive sequences contains $(n! - 2)$ sequences. Figure 3 presents an example of a Q2L transition with the non-consecutive sequence SEQ_{1324}: FC_1 and FC_3 are charged with $2\Delta Q_{FC0}$, whereas the FC_2 is discharged with ΔQ_{FC0}. Therefore, in contrast to consecutive sequences, non-consecutive sequences lead to non-equal charge exchanges of the individual FCs (for the same T_{delay} and $I_{o,max}$). Therefore, even charging of some FCs and discharging of others during the same Q2L transition can be achieved. Note, however, that all FCs experience a charge exchange, and hence are coupled through a sequence in the sense that it is not possible to influence only a selected subset of the FCs.

Considering the exemplary 5L-FCC, Table 1 summarizes all sequences, denoted henceforth as set $\mathcal{S}_{CL}$, and their effects on the FCs' charge for the case of ZVS transitions. It is found that for the HS transition, the sequences have opposite effect. Therefore, the values from Table 1 need to be multiplied by (-1) to obtain the charge increments for HS transitions. Furthermore, Table 1 is simplified by utilizing symmetry, i.e., the fact that sequences SEQ_{3xxx} and SEQ_{4xxx} result in the same absolute values of total charge exchanges as SEQ_{2xxx} and SEQ_{1xxx}, respectively. However the order of FCs and delay times is reversed, and the values from the table must be multiplied with (-1) to obtain the actual FC charge exchanges, which is denoted by the $-$ sign preceding the sequence's name (see right & bottom labels in Table 1).

Based on this analysis, we formulate the total change of charge provided to the FCs as

$$\boldsymbol{\Delta Q}_{FC} = \begin{bmatrix} \Delta Q_{FC1} \\ \dots \\ \Delta Q_{FC\{j\}} \end{bmatrix} = I_{o,max}(\boldsymbol{S} \times \boldsymbol{T}_{delay}), \tag{3}$$

where

$$\boldsymbol{T}_{delay} = \begin{bmatrix} T_{delay1} & \dots & T_{delay\{n\}} \end{bmatrix}^T \tag{4}$$

is a delay time vector and $\boldsymbol{S}$ is a matrix which specifies how the particular delay times influence the charge change of the FCs and is equivalent to the rows in Table 1. The matrix $\boldsymbol{S}$ is constructed by stacking the effects that the sequence has on each FC, hence it has dimensions of $j \times n$. From Table 1 it is apparent that the charge increments can be equal to values from the following set: $\pm\Delta Q_{\mathrm{FC0}} \cdot \{1, 2, ..., j\}$. In order to ensure well defined voltage levels across the switches and ease of balancing, equal values C_{FC} of all FCs are selected, which consequently leads to the voltage increments

$$\boldsymbol{\Delta V}_{\mathrm{FC}} = \begin{bmatrix} \Delta V_{\mathrm{FC1}} \\ \cdots \\ \Delta V_{\mathrm{FC}\{j\}} \end{bmatrix} = \frac{\boldsymbol{\Delta Q}_{\mathrm{FC}}}{C_{\mathrm{FC}}}. \tag{5}$$

Henceforth, for the sake of simplicity, we will consider equal delay times T_{delay} for all cells, and the implications of that assumption are discussed further in Section 4. Taking as an example the sequence SEQ_{1324} (cf. Figure 3) and equal delay times T_{delay} we obtain:

$$\boldsymbol{\Delta V}_{1324} = \frac{I_{\mathrm{o,max}}}{C_{\mathrm{FC}}} \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 1 & 1 & 0 \end{bmatrix} \times \begin{bmatrix} T_{\mathrm{delay}} \\ T_{\mathrm{delay}} \\ T_{\mathrm{delay}} \\ T_{\mathrm{delay}} \end{bmatrix}, \tag{6}$$

$$\boldsymbol{\Delta V}_{1324} = \frac{\Delta Q_{\mathrm{FC0}}}{C_{\mathrm{FC}}} \begin{bmatrix} 2 \\ -1 \\ 2 \end{bmatrix}. \tag{7}$$

which corresponds to the FC voltage waveforms in Figure 3.

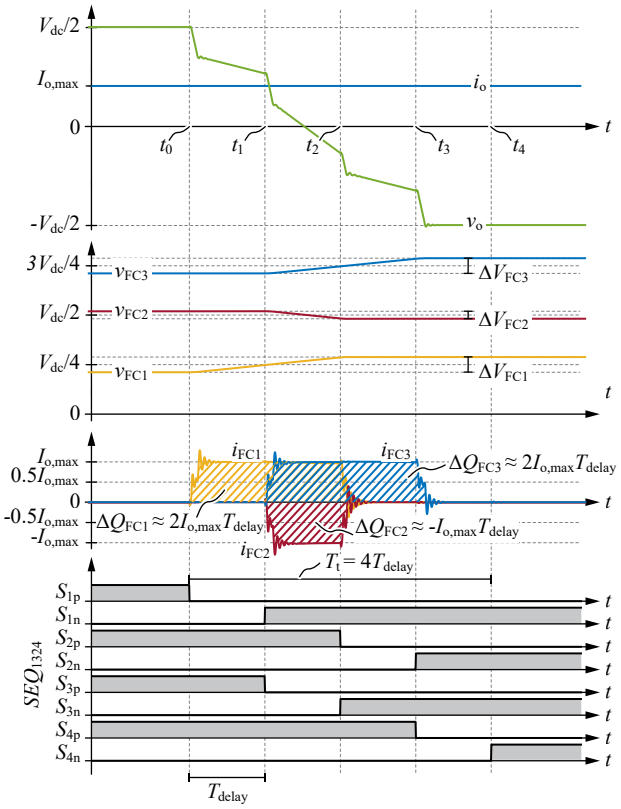

Figure 3. Simulation results for Q2L operation of the 5L-FCC with constant positive output current (I_{o}) during the switching transition with negative slope of v_{o}, exemplifying the effect of a non-consecutive sequence SEQ_{1324}: Charging of FC_1 and FC_3, discharging of FC_2.

Table 1. Effect of all sequences available ($\mathcal{S}_{\mathrm{CL}}$) for Q2L-5L-FCC on FC charge increments in the function of delay times for Q2L ZVS transition (for HS transition, the same value but opposite signs apply): (+1) charge, (−1) discharge, (0) no effect. Scaling the values with the respective $T_{\mathrm{delay}\{n\}}$ and $I_{\mathrm{o,max}}$ gives the charge increment values. Note that the table is simplified and values for $SEQ_{3\mathrm{xxx}}$ and $SEQ_{4\mathrm{xxx}}$ are obtained by using symmetry and multiplying the respective values by (−1).

⇵	$\mathbf{FC_1}$				$\mathbf{FC_2}$				$\mathbf{FC_3}$				
Sequence	$T_{\mathbf{delay1}}$	$T_{\mathbf{delay2}}$	$T_{\mathbf{delay3}}$	$T_{\mathbf{delay4}}$	$T_{\mathbf{delay1}}$	$T_{\mathbf{delay2}}$	$T_{\mathbf{delay3}}$	$T_{\mathbf{delay4}}$	$T_{\mathbf{delay1}}$	$T_{\mathbf{delay2}}$	$T_{\mathbf{delay3}}$	$T_{\mathbf{delay4}}$	
SEQ_{1234}	+1	0	0	0	0	+1	0	0	0	0	+1	0	$-SEQ_{4321}$
SEQ_{1243}	+1	0	0	0	0	+1	0	+1	0	0	0	−1	$-SEQ_{4312}$
SEQ_{1324}	+1	0	+1	0	0	0	−1	0	0	+1	+1	0	$-SEQ_{4231}$
SEQ_{1342}	+1	0	+1	+1	0	0	−1	−1	0	0	+1	0	$-SEQ_{4213}$
SEQ_{1423}	+1	0	0	+1	0	+1	0	0	0	−1	0	−1	$-SEQ_{4132}$
SEQ_{1432}	+1	0	+1	+1	0	0	−1	0	0	0	0	−1	$-SEQ_{4123}$
SEQ_{2134}	0	−1	0	0	+1	+1	0	0	0	0	+1	0	$-SEQ_{3421}$
SEQ_{2143}	0	−1	0	0	+1	+1	0	+1	0	0	0	−1	$-SEQ_{3412}$
SEQ_{2314}	0	−1	−1	0	0	+1	0	0	+1	0	+1	0	$-SEQ_{3241}$
SEQ_{2341}	0	−1	−1	−1	0	+1	0	0	0	0	+1	0	$-SEQ_{3214}$
SEQ_{2413}	0	−1	0	−1	+1	+1	0	+1	−1	0	0	−1	$-SEQ_{3142}$
SEQ_{2431}	0	−1	−1	−1	0	+1	0	+1	0	0	0	−1	$-SEQ_{3124}$
	T_{delay4}	T_{delay3}	T_{delay2}	T_{delay1}	T_{delay4}	T_{delay3}	T_{delay2}	T_{delay1}	T_{delay4}	T_{delay3}	T_{delay2}	T_{delay1}	Sequence
	$\mathrm{FC_3}$				$\mathrm{FC_2}$				$\mathrm{FC_1}$				⇵

2.2. Operating Principle with Zero Output Current: Cell Multiple Switching

From (3) it is obvious that in case of zero output current, the charge increments of the FCs are expected to be zero. Figure 4 presents the simulation results for Q2L operation with $i_{\mathrm{o}} = 0$ during the switching transition with negative slope of v_{o}. It can be seen that during each commutation, due to the hard-switching and charging of the switches' output capacitances, the commutation loop current leads to an exchange of charges, i.e., subtraction of charge from a cell's input-side capacitor and addition of charge to the output-side capacitor of the respective converter cell. This can be seen, e.g., in Figure 4 between $t_2 < t < t_3$ where the exchange of charges between $\mathrm{FC_1}$ and $\mathrm{FC_2}$ occurs. Note that in case of zero-current switching of cell 1, the charge is delivered to the load, whereas in case of cell 3, the charge delivered to $\mathrm{FC_3}$ is subtracted from the DC-link. For an in-depth analysis we refer to [40]. However, the net charge exchange of each FC over the entire transition is approximately zero. Nevertheless, the exchange of charge between the FCs during no-current Q2L transitions can be utilized in a novel method for balancing the FC voltages in case of zero output current.

To do so, we insert additional commutations in one or more cells during a Q2L transition. This leads to additional hard-switching events of one or several of the MOSFETs. This concept that we refer to as cell multiple switching (CMS) thus allows to obtain non-zero net charge exchange of certain FCs over a Q2L transition, therefore offering a means of balancing the FC voltages even in case of zero output current.

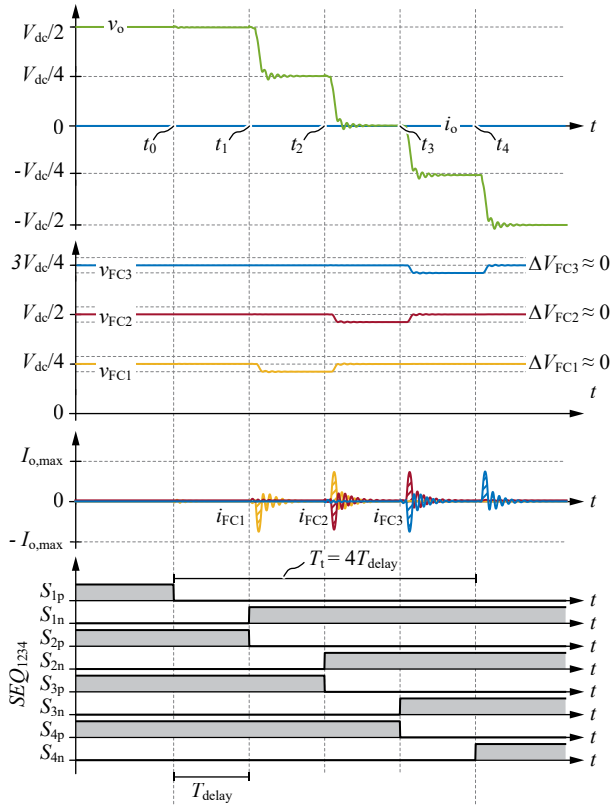

Figure 4. Simulation results for the 5L-FCC in configuration ① with zero output current during the Q2L transition with negative slope of v_o: Zero net charge increments of the FCs result.

Figure 5 shows the exemplary simulation results for a 5L-FCC in split DC-link configuration with zero output current during the Q2L transition with negative slope of v_o and a CMS event inserted in cell 3. It can be noticed that until $t < t_3$ the processes in the transition occur as for a sequence SEQ_{1234} (see Figure 4). However, at $t = t_4$, S_{3n} turns off and the circuit remains in steady-state during $[t_4, t_5]$ and $v_o = -V_{dc}/4$ applies. The time interval between t_3 and t_4, in which S_{3n} is *on*, has a duration of one pulse time T_p. Two additional switching operations are inserted between $t_5 < t < t_8$: First, v_o is switched back to 0 during $t_5 < t < t_7$, and, subsequently, v_o is switched to $-V_{dc}/4$ during $t_7 < t < t_8$. During $t_3 < t < t_4$, the charge of FC_2 is increased by ΔQ_{S3p} and FC_3 is discharged by the same value, where

$$\Delta Q_{S3p} = Q_{oss,3p} + Q_{rr,3p}, \tag{8}$$

with $Q_{oss,3p}$ and $Q_{rr,3p}$ being the charges stored in the output capacitance C_{oss} of the MOSFET and the reverse-recovery charge of the anti-parallel diode, respectively. During $t_5 < t < t_6$, FC_2 is again charged, whereas FC_3 is discharged by ΔQ_{S3n}. Finally, at $t = t_8$, S_{4n} turns on and the last commutation is completed. It can be seen that the presented sequence introduces two additional switching pulses in cell 3, therefore it is denoted as $SEQ_{123(33)4}$, where subscript (33) denotes the CMS event in cell 3.

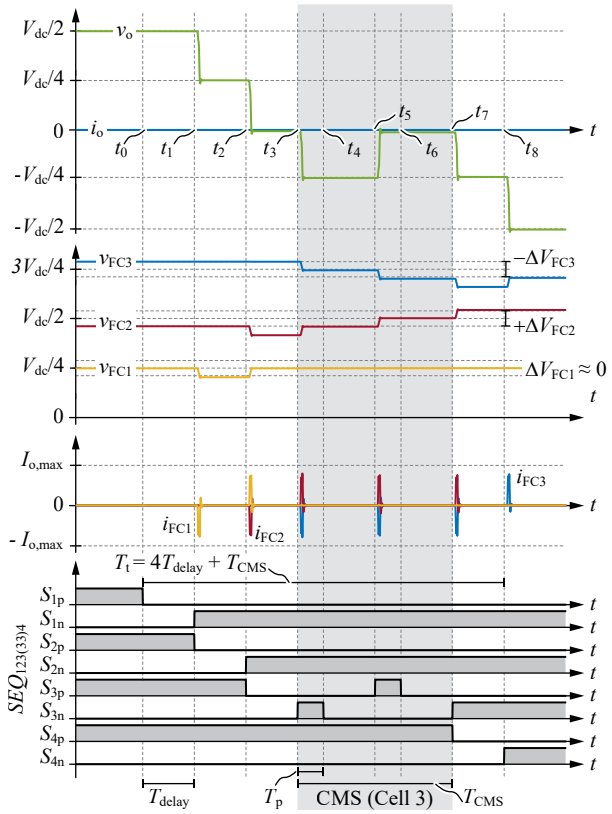

Figure 5. Simulation results for the 5L-FCC in configuration ① with zero output current during the Q2L transition with negative slope of v_o: Note the single cell multiple switching event of cell 3. A delay T_{delay} and a pulse time $T_p = 0.5T_{delay}$ are used. Note that the same T_{delay}, however a different time base are used compared to Figure 4.

Assuming that the charge increment from each switch is approximately the same and equal to ΔQ_S, a CMS event results in total net charge increment of the affected FCs equal to:

$$\Delta Q_{FC} \approx 2\Delta Q_S. \tag{9}$$

The corresponding voltage increment per CMS event is thus:

$$\Delta V_{CMS} \approx \frac{\Delta Q_{FC}}{C_{FC}} \approx \frac{2\Delta Q_S}{C_{FC}}. \tag{10}$$

Using the linear charge-equivalent output capacitance $C_{Q,eq}$ and assuming that $Q_{rr} \approx 0$, (10) can be further simplified to:

$$\Delta Q_S = \int_0^{V_{ds}} C_{oss}(v) \cdot \mathrm{d}v = C_{Q,eq} \cdot V_{ds}, \tag{11}$$

$$\Delta V_{CMS} \approx \frac{2C_{Q,eq} \cdot V_{ds}}{C_{FC}}. \tag{12}$$

Therefore, the CMS balancing controllability depends on the capacitance ratio $k_c = 2C_{Q,eq}/C_{FC}$ and is discussed in detail for semiconductors of different voltage classes in Appendix A.

2.3. Duty Cycle Limitation / Selection of T_{delay}

For a certain output current $I_{o,max}$ the charge increments of the FCs during a Q2L transition are proportional to the delay times, see (3). Hence this parameter is a degree of

freedom in the design of Q2L-FCCs and its constraints are discussed in the following. The duration T_t of a complete Q2L transition, cf. Figure 2b,c, in the NL-FCC is given by

$$T_t \approx (N-1)T_{delay}, \tag{13}$$

$$\approx 4T_{delay}, \text{ for } N = 5. \tag{14}$$

Thus, the Q2L transitions limit the maximum duty cycle to

$$d_{max} = 1 - \frac{2T_t}{T_s}, \tag{15}$$

$$= 1 - \frac{8T_{delay}}{T_s}, \text{ for } N = 5. \tag{16}$$

Therefore, the delay time can be selected only within certain boundaries

$$T_{delay} \in [T_{min}, T_{max}]. \tag{17}$$

The maximum boundary T_{max} follows from the allowable duration of the switching transition, i.e., from the application-specific d_{max}, given that increased commutation times decrease the available output voltage-time product. The minimum boundary T_{min} follows from the system's physical limitations, i.e., the required interlock delay time to prevent shoot-through events. In practical applications additional constraints can be considered, e.g., in soft-switching Q2L-FCCs the time required to achieve ZVS in partial-load operation increases T_{min} above the minimum required to prevent shoot-through.

Note that if CMS is activated in the Q2L-FCC, the duration of the transition increases due to the inserted additional pulses. In case of inserting n_{CMS} events of duration T_{CMS} (cf. Figure 5), the transition time is:

$$T_{CMS} \approx 2n_{CMS}(T_p + T_{delay}), \tag{18}$$

$$T_t \approx (N-1)T_{delay} + T_{CMS}, \tag{19}$$

$$\approx 6T_{delay} + 2T_p, \text{ for } N = 5, n_{CMS} = 1. \tag{20}$$

Therefore, based on the application specific d_{max}, the allowable number of CMS events, the number of involved cells, and T_p must be defined together with T_{delay}.

3. Open-Loop FC Balancing

As described earlier in [29], the balancing of the FC voltages can be achieved with a passive modulation that employs consecutive sequences, hence either by charging or discharging all FCs with the same charge increment during a Q2L transition, see Table 1. For a versatile HB realization, i.e., designed for operation with asymmetrical or symmetrical output currents, the following modulation scheme has been proposed:

$$\mathcal{S}_{OL} = \{SEQ_{1234}, SEQ_{1234}, SEQ_{4321}, SEQ_{4321}, ...\}. \tag{21}$$

The scheme results in open-loop balancing over two switching periods (4 Q2L transitions). However, the maximum peak-to-peak voltage ripple is

$$\Delta V_{pp} \approx 2\frac{T_{delay} \cdot I_{o,max}}{C_{FC}}, \tag{22}$$

due to the charging characteristic with asymmetric currents. Please refer to [29] for an in-depth discussion.

While in principle this modulation scheme is sufficient to achieve balanced FC voltages, the controllability is limited and results in a non-optimal FC voltage ripple. Advantageously, this approach does not require FC voltage measurements. On the other hand, balancing

resistors connected in parallel to the switches are necessary to ensure balanced FC voltages in case of zero output current. We refer to this approach as open-loop (OL) balancing and provide experimental evaluation in Section 6.2.

4. Load-Independent Closed-Loop Balancing

In this section we propose a concept for load-independent closed-loop (CL) balancing. The most straightforward approach is to implement a controller which uses measurements of the FC voltages and of the output current to achieve close tracking of the FC voltage references. However, as indicated in [32] due to the opposite voltage ripple on FCs, the switches can be operated with a strong asymmetry of the blocking voltages. To address this issue, alternatively the controller can be built to equalize the cell voltages, derived as differences between the voltages of capacitors adjacent to the switches, and hence ensuring equal voltage sharing among the series-connected switches. We present the two aforementioned approaches in detail in Section 4.1. Furthermore, the proposed balancing concept is eventually implemented and tested (see Section 6) up to the nominal output current of the FCC; for the discussion of extreme load cases, i.e., an overload and short-circuit currents we refer to Appendix B.

Figure 6a shows the block diagram of an FCC HB with Q2L voltage balancing controller. The measured HB output current i_o is fed to the output quantity controller which specifies the reference output voltage V_o^* for the modulator and the Q2L voltage balancing controller. The design and realization of the output quantity controller is decoupled from Q2L operation and not within the scope of this paper. For that reason, the considered Q2L-FCC is operated with a fixed duty cycle of $d = 50\%$ in the following.

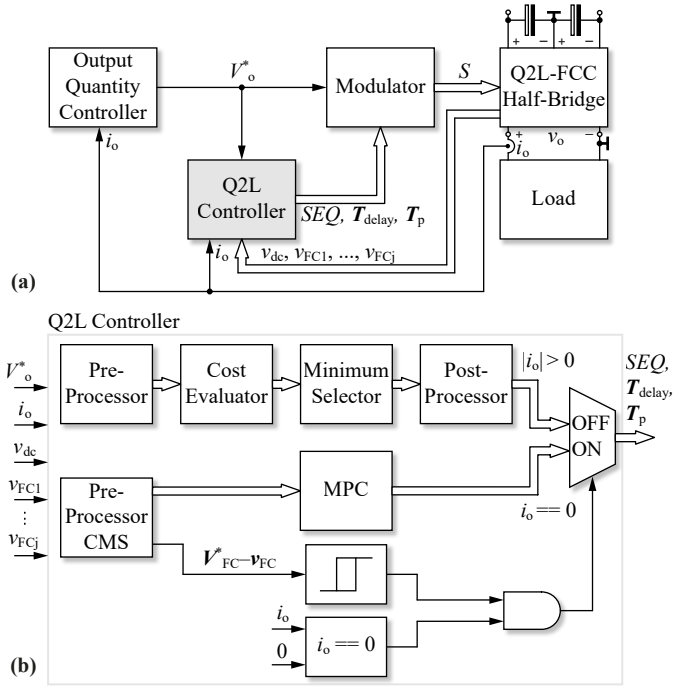

Figure 6. (**a**) Block diagram of an FCC HB with Q2L voltage balancing controller and modulator. Note that the output quantity (e.g., load current) controller is not in this paper's scope and hence we consider an exemplary fixed duty cycle of $d = 50\%$. (**b**) Control block diagram of the proposed load-independent Q2L voltage balancing controller.

As mentioned before, a given switching sequence affects several FC voltages, i.e., they are coupled through the selection of the sequences. Therefore, controlling all FC voltages is a multiple-input multiple-output (MIMO) control problem. MIMO systems can be easily addressed by model predictive control (MPC) which is formulated in the time

domain [41,42]. Therefore, we use MPC with reference tracking to realize a Q2L voltage balancing controller.

Essentially, based on the slope of the reference output voltage V_o^*, the measured FC voltages $v_{FC1}, \ldots, v_{FCj}$, the measured output current i_o, and the DC-link voltage v_{dc}, the Q2L voltage balancing controller selects a switching sequence SEQ and respective times T_{delay}, T_p, which are the input to the actual Q2L modulator. Figure 6b presents the detailed block diagram of the controller which contains two distinct parallel paths (sub-controllers), i.e., one for control without load current using CMS ($i_o = 0$, based on FC voltage tracking, see Section 4.1.1) and one for operation with non-zero load current ($|i_o| > 0$, based on cell voltage tracking, see Section 4.1.2). The implementation of these sub-controllers is explained in the following subsections. In the last part of the Q2L controller, based on the value of i_o, the multiplexer decides which of the two sub-controllers is activated.

Ultimately, both controllers define a certain commutation sequence (SEQ) for a given Q2L transition (e.g., $SEQ = 123(33)4$ for the example shown in Figure 4) and also the values for T_{delay} and T_p to be used. During the Q2L transition, the modulator translates this information into gate signals for the individual switches according to the state machine shown in Figure 7.

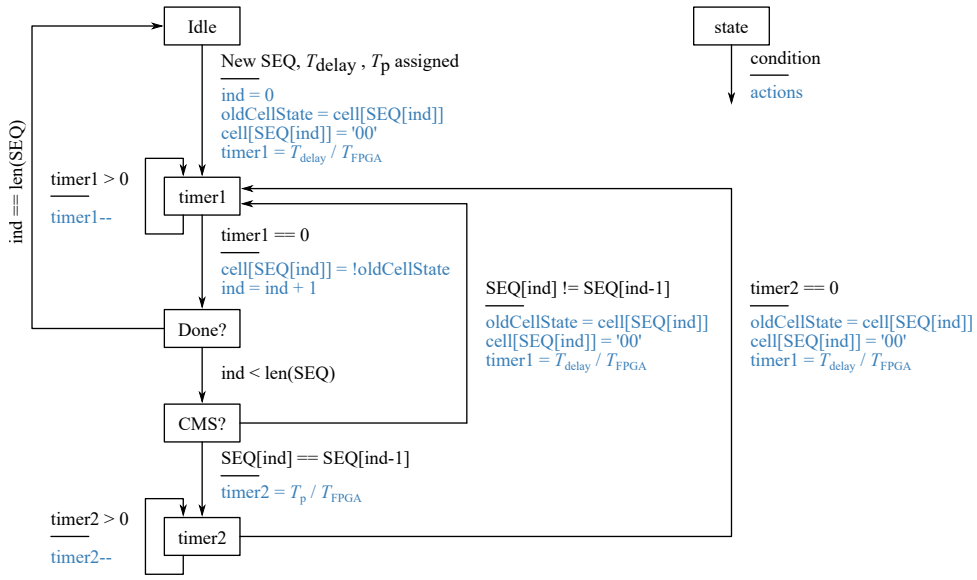

Figure 7. Detailed state machine of the modulator shown in Figure 6a. `Cell[i]` stores the two gate signals of the two switches of cell i; T_{FPGA} denotes the FPGA clock period. Note that T_{delay} and T_p are shown as scalars for simplicity (i.e., all commutations within one Q2L transition use the same values), but it would be possible to specify vectors indexed by `ind` such that individual values for each commutation could be used.

4.1. Closed-Loop Control with Non-Zero Output Current

In [29] we have proposed an active method for FC voltage balancing in a Q2L-3L-FCC. This method relies on the determination of an optimal ripple of v_{FC} and then the computation of individual delay times that eliminate any voltage ripple error in the next transition, similarly to a deadbeat controller. This method is however complex and computationally expensive for FCC realizations with $N > 3$: For each of the $(N-1)!$ available sequences, $(N-1)$ different delay times for $(N-2)$ FCs need to be considered. For that reason, in this work we propose a different approach that still utilizes all available sequences. However, to limit the degrees of freedom, we make the following simplifications:

- All delay times in a given switching transition are equal, i.e., $T_{delay1} = T_{delay2} = T_{delay3} = T_{delay4} = T_{delay}$.

- Two discrete delay time values are used: $T_{\text{delay}} \in \{T_{\text{min}}, T_{\text{max}}\}$, where T_{min} is intended to be selected by the controller in the steady-state in order to keep the voltage ripple small. On the other hand, T_{max} is selected in cases of significant unbalance to reduce the error more aggressively.

For the exemplary 5L-FCC, there are thus only 48 different possible actions that the controller needs to consider (24 unique sequences $\times$ 2 unique delay times). Note that with a higher number of levels, the number of possible actions increases substantially, as does the computation effort. However, to reduce the computation effort, the solution to the optimization problem can be solved offline and stored in a look-up table (LUT), see more details of implementation presented in Section 4.2.

As presented in Section 2.1 the charge increments in the FCs occur during the switching transition only, whose duration is relatively short compared to the switching period. Therefore, a discrete time domain with constant sampling interval $k(0.5T_{\text{s}})$ is defined, where $k \in \mathbb{N}$ denotes the time steps, cf. Figure 8a. Note that this simplified expression is valid for a fixed duty cycle of 50 % only. For realizations with variable duty cycle, the sampling intervals would need to be changed such that the sampling instants coincide with the Q2L transitions. Figure 8b shows the timing of the measurement data acquisition and the control routine execution in the FPGA within the highlighted Q2L transition. It can be noticed that the measured value of the output current is delayed by a measurement delay T_{ADC} due to analog-to-digital conversion (ADC). Furthermore, T_{comp} denotes the delay resulting from performing the required computations in the FPGA. For the experimental system considered in this paper (cf. Section 5 for details) the total delay amounts to approx. 600 ns and the deviation between the measured current used for the controller execution and the current value present during the actual switching transition is found to be less than 2.6 %; therefore we do not employ delay compensation.

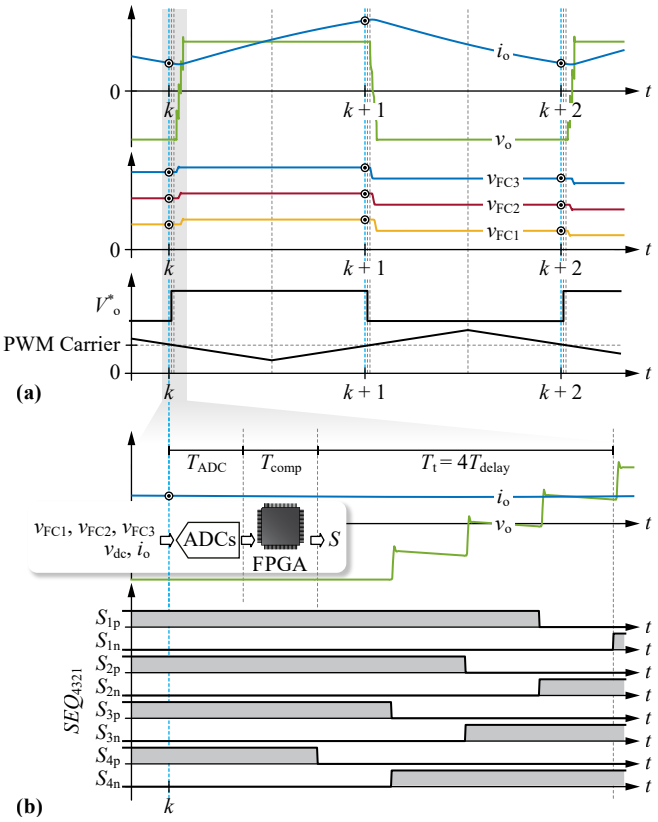

Figure 8. (**a**) Simulation results illustrating the PWM carrier, output voltage switching transition reference V_{o}^* and main waveforms. Note that the ADCs are triggered shortly before the switching transition. (**b**) Gate signals, output voltage and current waveforms at discrete time step k including the delay times introduced by the ADC conversion and FPGA computation.

4.1.1. FC Voltage Tracking

In this approach the proposed MPC relies on the model of the voltage increment (cf. (5)) to predict the future FC voltages,

$$\boldsymbol{V}_{\mathrm{FC}}(k+1) = \boldsymbol{V}_{\mathrm{FC}}(k) + \boldsymbol{\Delta V}_{\mathrm{FC}}(k), \tag{23}$$

where

$$\boldsymbol{V}_{\mathrm{FC}} = \begin{bmatrix} v_{\mathrm{FC1}} & \dots & v_{\mathrm{FC}\{j\}} \end{bmatrix}^T \tag{24}$$

and it depends on the available control actions and input variables:

$$\boldsymbol{\Delta V}_{\mathrm{FC}}(k) = f_1(V_{\mathrm{o}}^*, \mathcal{S}_{\mathrm{CL}}, \boldsymbol{T}_{\mathrm{delay}}, i_{\mathrm{o}})(k). \tag{25}$$

In order to keep the computation effort low and eliminate the need to predict the future output current, a one-step prediction horizon is used, i.e., $N_{\mathrm{p}} = 1$, which is found to provide sufficient performance. The control problem at time step k of tracking the FC voltage reference can be mapped into the cost function:

$$J_1 = \sum[(\boldsymbol{V}_{\mathrm{FC}}^* - \boldsymbol{V}_{\mathrm{FC}}(k+1))^2], \tag{26}$$

using the squared 2-norm, where

$$\boldsymbol{V}_{\mathrm{FC}}^* = \frac{V_{\mathrm{dc}}}{N-1}\begin{bmatrix} 1 & 2 & \dots & j \end{bmatrix}^T \tag{27}$$

$$= V_{\mathrm{dc}}\begin{bmatrix} 1/4 & 1/2 & 3/4 \end{bmatrix}^T, \text{for } N = 5. \tag{28}$$

Using the squared 2-norm, possible control actions that would lead to large voltage deviations and hence poor reference tracking are heavily penalized, which ultimately ensures good tracking performance. The optimization problem can be stated as

$$[SEQ_{\mathrm{opt}}(k), \boldsymbol{T}_{\mathrm{opt}}(k)] = \text{arg minimize } J_1 \tag{29a}$$

$$\text{subject to } \boldsymbol{T}_{\mathrm{delay}} \in \mathbf{1}_{1,\mathrm{n}} \times \{T_{\mathrm{min}}, T_{\mathrm{max}}\} \tag{29b}$$

$$SEQ(k) \in \mathcal{S}_{\mathrm{CL}} \tag{29c}$$

4.1.2. Cell Voltage Tracking

In the second approach, to ensure well defined voltage levels across the switches, the controller is built to equalize the cell voltages,

$$\boldsymbol{V}_{\mathrm{cell}} = \begin{bmatrix} v_{\mathrm{FC1}} \\ v_{\mathrm{FC2}} - v_{\mathrm{FC1}} \\ \dots \\ v_{\mathrm{dc}} - v_{\mathrm{FC}\{j\}} \end{bmatrix}, \tag{30}$$

instead of the FC voltages. Note that unlike the FC voltages, all cell voltages are ideally equal. Using the cell voltage increments defined as

$$\boldsymbol{\Delta V}_{\mathrm{cell}} = \begin{bmatrix} \Delta V_{\mathrm{cell1}} \\ \Delta V_{\mathrm{cell2}} \\ \dots \\ \Delta V_{\mathrm{cell}\{n\}} \end{bmatrix} = \begin{bmatrix} \Delta V_{\mathrm{FC1}} \\ \Delta V_{\mathrm{FC2}} - \Delta V_{\mathrm{FC1}} \\ \dots \\ -\Delta V_{\mathrm{FC}\{j\}} \end{bmatrix}, \tag{31}$$

the MPC can predict the cell voltages at the next time step as

$$\boldsymbol{V}_{\mathrm{cell}}(k+1) = \boldsymbol{V}_{\mathrm{cell}}(k) + \boldsymbol{\Delta V}_{\mathrm{cell}}(k), \tag{32}$$

which, similar to (25), depends on the available control actions and input variables

$$\boldsymbol{\Delta V}_{\text{cell}}(k) = f_2(V_{\text{o}}^*, \mathcal{S}_{\text{CL}}, \boldsymbol{T}_{\text{delay}}, i_{\text{o}})(k). \tag{33}$$

The function f_2 maps the sequences to effects on the cell voltage increments in dependence of the delay times based on Table 1. Consequently, the following cost function describes the control problem of tracking the cell voltage references at time step k:

$$J_2 = \sum[(\boldsymbol{V}_{\text{cell}}^* - \boldsymbol{V}_{\text{cell}}(k+1))^2], \tag{34}$$

where

$$\boldsymbol{V}_{\text{cell}}^* = \frac{V_{\text{dc}}}{n} \times \mathbf{1}_{1,\text{n}}. \tag{35}$$

Finally, the optimization problem is stated as (29), however in this case minimizes the cost function J_2. Both proposed control targets, i.e., tracking of FC voltages or cell voltages, result in good FC voltage balancing performance. However, the cell voltages controller ensures more balanced and symmetrized switch voltages and is used in experiments presented in Section 6.

Regarding implementation (cf. Figure 6b), first a pre-processor computes (32)–(33), i.e., based on the required V_{o}^* slope, the sign of i_{o}, the expected cell voltage increments $\boldsymbol{\Delta V}_{\text{cell}}$ for all combinations of sequences (cf. Table 1) and $\{T_{\text{min}}, T_{\text{max}}\}$ are computed and the cell voltages at time step $k+1$ are predicted. Next, the cost function (34) is evaluated and the optimization problem (29) for J_2 solved, resulting in the selection of the control action (i.e., one sequence and either T_{min} or T_{max}) with the minimum cost, i.e., leading to cell voltages at time step $k+1$ that are as close as possible to the reference values. Note that Table 1 shows the effect on charge increments for the ZVS-type of transitions, therefore, in the last step, the post-processor by using the symmetry, adapts the signs if the next transition is of HS-type instead (note that the transition type follows from the desired output voltage change and the output current direction). In the prototype system described below in Section 5, this control algorithm has been implemented in a high-performance Xilinx Zynq Z-7020 SoC.

4.2. Closed-Loop Control with Zero Output Current

As discussed above in Section 2.2, CMS can be utilized to charge/discharge FCs even in case of zero output current. The following assumptions are considered for the realization of the corresponding CMS-based controller, i.e., the second path shown in Figure 6b:

- The delay times T_{delay} are set to the minimum value T_{min} as their duration does not impact the balancing when $i_{\text{o}} = 0$.
- Similarly, the sequence of the switching actions within a Q2L transition does not influence the total voltage increments when $i_{\text{o}} = 0$. Therefore only the sequence SEQ_{1234} is used for simplicity when CMS is active.
- The pulse time T_{p} of a CMS event must be sufficiently long for a zero-current HS transition to complete. Therefore, we set $T_{\text{p}} = T_{\text{min}}$.

Note that using short delay and pulse times is preferable to minimize the overall transition times T_{t}.

The analysis presented above in Section 2.2 indicates that theoretically there is an infinite number of ways to insert CMS events if the number of events inserted per Q2L transition is not limited. However, practically, it is desirable to keep the number of CMS events per transition low (duty cycle limitation) and it is found that for the considered exemplary 5L-FCC a selection of only 6 CMS sequences (given in Table 2) is sufficient to achieve robust controllability. The reasoning behind the selection of these CMS sequences is explained in the following.

Interestingly, it can be seen from Table 2 that inserting a CMS event in the mth cell leads to a discharge of FC_{m} (in case of $m = n$, the energy is exchanged with the DC-link

capacitor), and charges FC_{m-1} (for $m = 1$ there is no FC to charge). Furthermore, the CMS events can be superimposed to achieve desired charge increments, e.g., events '0001' and '0010' inserted over two subsequent Q2L switching transitions yield the same effect as the same two events '0011' within one Q2L transition. However, the latter results in a longer Q2L transition time and hence a reduction of the available duty cycle. This characteristic can be used to obtain individual balancing of FCs (charge/discharge) over two Q2L transitions. Note that in the following design of the controller, for flexibility reasons, we use all CMS events shown in Table 2.

Table 2. Effect on charge increments of the FCs in dependence of different CMS events/sequences: (+1) charge, (−1) discharge, (0) no effect. Scaling the values by $2\Delta Q_S$ gives the charge increment values.

CMS Events	CMS seq.	ΔQ_{FC1}	ΔQ_{FC2}	ΔQ_{FC3}
0001	$SEQ_{1234(44)}$	0	0	+1
0010	$SEQ_{123(33)4}$	0	+1	−1
0100	$SEQ_{12(22)34}$	+1	−1	0
1000	$SEQ_{1(11)234}$	−1	0	0
0011	$SEQ_{123(33)4(44)}$	0	+1	0
1100	$SEQ_{1(11)2(22)34}$	0	−1	0

Similar to the approach used in case of non-zero output current, again we employ an MPC with reference tracking over a finite prediction horizon, but in this case of length $N_p = 6$, to accommodate the aforementioned superposition of CMS events in the controller. Moreover, we use FC voltage tracking (not cell votlage tracking), because for zero output current operation, no large voltage ripples occur. Based on Table 2 the set of available CMS sequences is defined as

$$\mathcal{U} = \{0001, 0010, 0100, 1000, 0011, 1100\}. \tag{36}$$

We introduce a vector of CMS sequences for the considered prediction horizon:

$$\boldsymbol{U}(k) = \begin{bmatrix} u(k) & u(k+1) & \dots & u(k+N_p-1) \end{bmatrix}. \tag{37}$$

The prediction model of FC voltages is

$$\boldsymbol{V}_{FC,CMS}(k+1) = \boldsymbol{V}_{FC}(k) + \boldsymbol{\Delta V}_{CMS}(k), \tag{38}$$

$$\boldsymbol{\Delta V}_{CMS}(k) = f_3(\mathcal{U})(k). \tag{39}$$

The control problem can be described by the cost function

$$J_3 = \sum_{l=k}^{k+N_p-1} [\sum[(\boldsymbol{V}^*_{FC} - \boldsymbol{V}_{FC,CMS}(l+1))^2]], \tag{40}$$

and the solution to the optimization problem is the choice of $\boldsymbol{U}(k)$ that minimizes this cost function J_3:

$$\boldsymbol{U}_{opt}(k) = \text{arg minimize } J_3 \tag{41a}$$

$$\text{subject to } \forall l = k, \dots, k+N_p-1 \tag{41b}$$

$$\boldsymbol{U}(k) \in \mathbb{U} \tag{41c}$$

where $\mathbb{U}$ is the N_p-times Cartesian product of the set of CMS sequences $\mathcal{U}$, cf. (36). Following the principle of receding horizon policy, only the first element of the optimal CMS sequence $\boldsymbol{U}_{opt}(k)$ is applied at time step k, and another optimization is performed at the next time step.

The CMS controller (cf. Figure 6b) relies on the solution to the optimization problem (41) which is solved offline: The FC voltage errors $(\boldsymbol{V}^*_{FC} - \boldsymbol{V}_{FC})$ as well as the expected voltage increments $\boldsymbol{\Delta V}_{CMS}$ are normalized by the capacitance ratio k_c (cf. Section 2.2) and then stored in a look-up table (LUT) for the considered voltage error range. In the online implementation, the CMS pre-processor computes the voltage errors $(\boldsymbol{V}^*_{FC} - \boldsymbol{V}_{FC}(k))$ and normalizes them. This information is fed to the MPC block which retrieves the optimum solution from the precomputed LUT in the FPGA's memory. To avoid unnecessary CMS activation, especially when the FC voltages are close to the references (small errors), a voltage hysteresis is considered. Again, the online part of the algorithm has been implemented in a high-performance Xilinx Zynq Z-7020 SoC.

5. Hardware Implementation

In order to validate the proposed concepts, a LV proof-of-concept hardware demonstrator of a 5L-FCC HB has been designed according to the schematic presented in Figure 9. Depending on the connection of the load, two types of operation can be achieved (see also Figure 1): ① Symmetrical output current with ZVS transitions, and ② asymmetrical output current ZVS and HS transitions. In order to test OL balancing, resistors R_b can be placed in parallel to the switches.

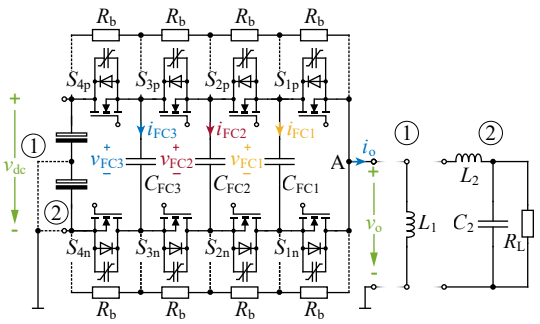

Figure 9. Schematic (cf. also Figure 1) of the 5L-FCC used in experiments with two configurations: ① Split DC-link at the input and inductive load connected to the DC-link mid-point to obtain symmetrical currents; ② full DC-link at the input and LC filter with resistive load in the output to achieve asymmetrical currents.

Figure 10 shows the photos of the realized 5L-FCC bridge-leg demonstrator and Table 3 summarizes the main specifications and the selected control parameters. Even though 150 V GaN e-FETs are used (EPC2033) and hence a DC link voltage of up to 400 V would be possible, all experiments have been carried out with a reduced DC-link voltage of 100 V for safety reasons. Note that the DC voltage level does not impact the validity of the experimental verification (see also Appendix A). The converter is operated with 50 kHz switching frequency and a fixed 50 % duty cycle. For demonstration purposes, a relatively large maximum peak-to-peak FC voltage ripple of 20 V is selected. With a maximum output current of 6.6 A and a maximum delay time of 100 ns, the required capacitance value of the FCs is 66 nF, see (22). The FCs are realized with C0G ceramic capacitors due to their linearity (1 kV CAA572C0G3A663J640LH).

The FC voltage measurement circuitry is placed on a separate PCB that is mounted on top of the main power board (cf. Figure 10a) and it can be disconnected for the tests with OL balancing. The power board, cf. Figure 10b contains the switching-cell daughter boards (carrying the GaN eFETs) on top and the FCs on the bottom. Furthermore, it contains the DC-link voltage and output current measurements circuitry. The Q2L controller and modulator are implemented in a high-performance Xilinx Zynq Z-7020 SoC.

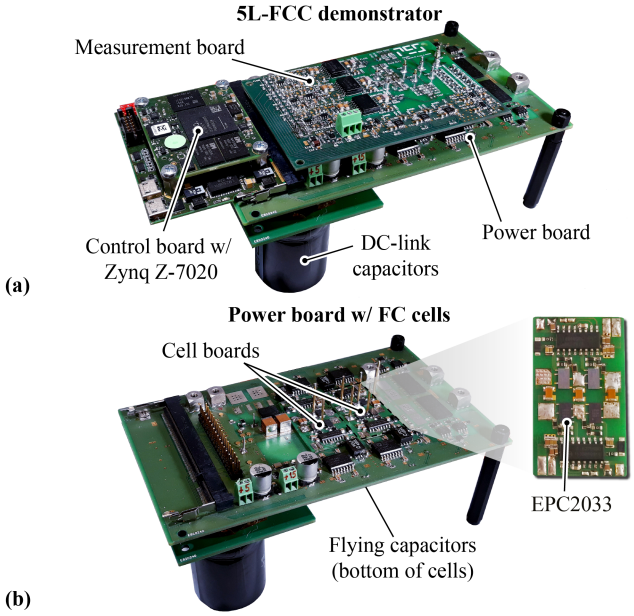

Figure 10. Photos of the realized 5L-FCC HB demonstrator: (**a**) General assembly, (**b**) power board and detail view of the switching cell PCBs.

Table 3. Specifications and control parameters of the Q2L-5L-FCC proof-of-concept demonstrator.

V_{dc}	100 V	DC-link voltage
$I_{o,max}$	6.6 A	output current maximum
f_s	50 kHz	switching frequency
d	50 %	duty cycle
Flying capacitors		
C_{FC}	66 nF	CAA572C0G3A663J640LH
$\Delta V_{pp,max}$	20 V	max. peak-to-peak volt. ripple
Semiconductors		
S	150 V/7 mΩ	GaN eFET EPC2033
$C_{oss,eq}$	760 pF	charge eq. capacitance
Control parameters		
$T_{t,max}$	400 ns	max. transition time
T_{min}	50 ns	min. delay time
T_{max}	100 ns	max. delay time
T_p	50 ns	pulse time

6. Measurement Results

This section presents experimental results obtained with the 5L-FCC hardware demonstrator introduced in Section 5. In order to demonstrate the Q2L operation and the proposed concepts for FC voltage balancing, two synchronized LeCroy HDO4054A 12-bit oscilloscopes are used to measure waveforms of the DC-link voltage (v_{dc}), all FC voltages ($v_{FC\{1,2,3\}}$), and the half-bridge output voltage (v_o) as well as the output current (i_o), see Figure 9. Consequently, for each experiment two (temporally aligned) oscillograms are presented. Unless stated otherwise, resistive balancers $R_b = 30\,k\Omega$ are connected in parallel to the switches.

6.1. Q2L Transitions

First, Q2L output voltage transitions are analyzed to confirm the Q2L operation and the description of charge and voltage increments presented in Section 2. Figure 11 shows measured waveforms during the switching transition with a positive slope of v_o and negative output current ($i_o \approx I_o = -5.9\,A$), which results in a ZVS transition. Figure 12 shows waveforms of the switching transition with a positive slope of v_o and positive

output current ($i_o \approx I_o = 2.9$ A), which results in a HS transition. Based on the employed delay times and FC capacitance values, the voltage increments are calculated according to (5) and compared with the measured voltage changes (see oscillograms). The average absolute relative deviation of the estimated from the measured voltage changes is 3.7 % for ZVS (cf. Figure 11) and 13.3 % for HS (cf. Figure 12), thus confirming good accuracy of the estimation.

Figure 13 shows an exemplary CMS sequence $SEQ_{1(11)234}$ (events in cells '1000') during a switching transition with negative slope of v_o and zero output current. It can be seen that the voltage change of FC_1 is about -0.7 V, whereas the expected voltage change calculated with (12) is -0.8 V, again showing good agreement with a deviation of 13 % between calculation and measurement. Moreover, it can be noticed that also the voltages of FC_2 and FC_3 change slightly, i.e., by -0.11 V and -0.19 V, respectively, which is due to the non-idealities of the circuit.

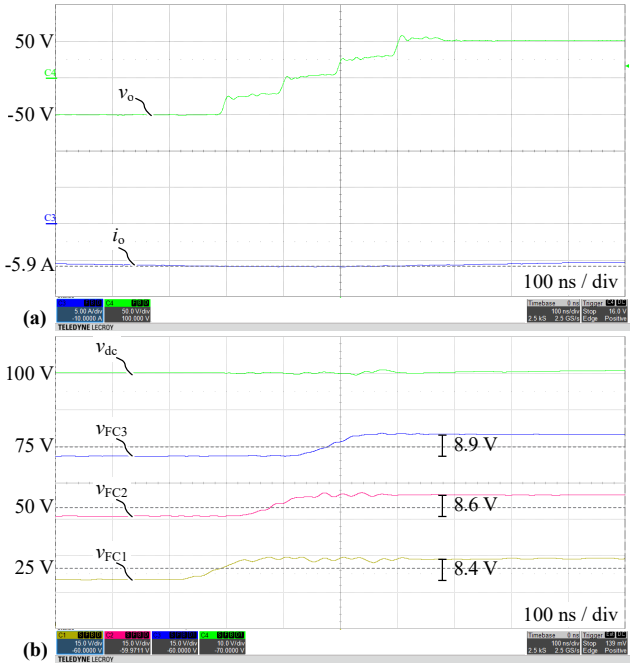

Figure 11. Measured waveforms for Q2L-5L-FCC in configuration ① with negative output current ($I_o = -5.9$ A) during the switching transition with positive slope of v_o, which results in a ZVS transition: (**a**) Output voltage v_o and current i_o, (**b**) DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. A delay time of $T_{delay} = 100$ ns is used.

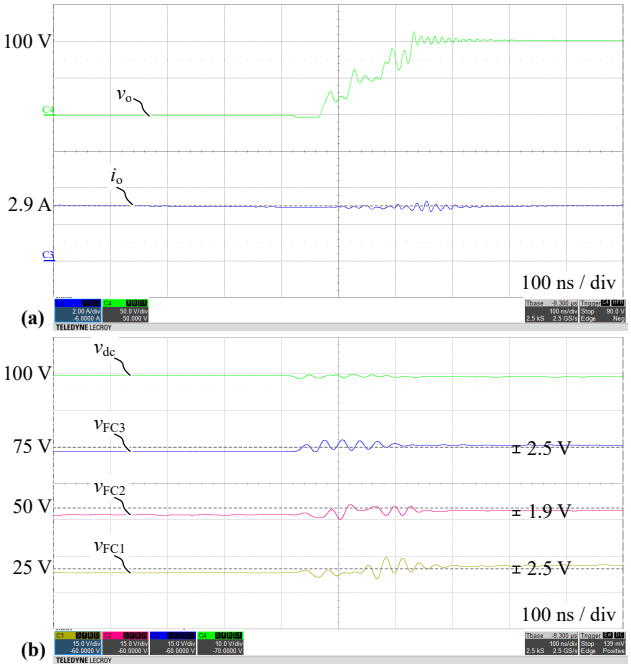

Figure 12. Measured waveforms for Q2L-5L-FCC in configuration ② with positive output current ($i_o = 2.9$ A) during the switching transition with positive slope of v_o, which results in a HS transition: (**a**) Output voltage v_o and current i_o, (**b**) DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. A delay time of $T_{delay} = 50$ ns is used.

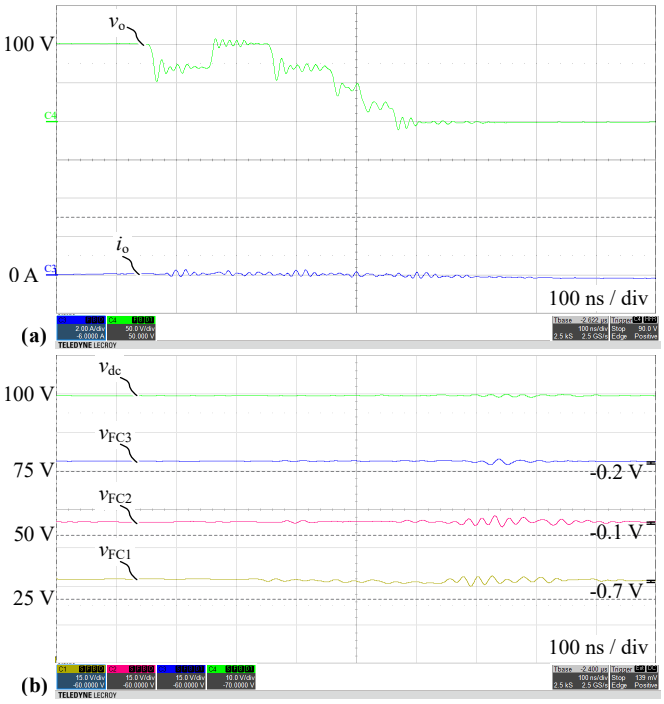

Figure 13. Measured waveforms for Q2L-5L-FCC in configuration ② with zero output current ($I_o = 0$ A) during the switching transition with negative slope of v_o and CMS sequence $SEQ_{1(11)234}$ (events in cells '1000'): (**a**) Output voltage v_o and current i_o, (**b**) DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. Delay times and pulse time $T_{delay} = T_p = 50$ ns are used.

6.2. Open-Loop Balancing

Next, we present measurement results confirming the OL balancing concept proposed in [29] and briefly described in Section 3. The modulation scheme from (21) is implemented

with $T_{\text{delay}} = 100\,\text{ns}$ for all cells. Consequently, all of the capacitors are charged/discharged with the same charge value in each transition, and open-loop balancing over two fundamental switching periods is achieved.

Figure 14 shows measured waveforms for split DC-link configuration with OL balancing and triangular current ($I_{\text{o,max}} = 7.0\,\text{A}$, $I_{\text{o,min}} = -5.8\,\text{A}$). The average absolute relative deviation of the estimated peak-to-peak voltage ripple (19.4 V, cf. (22)) from the measured value is 3 %, which corroborates the proposed model. However, note that in steady-state the mean values of the FC voltages deviate from the reference values (cf. (27)), on average by 4.9 V (15 %). This is a consequence of the circuit's equivalent impedances formed by the switches and the resistive balancers.

Figure 15 presents measured waveforms for full DC-link configuration with OL balancing during a negative load step from 100% to 67% of the nominal load ($I_{\text{o}} = 4.6\,\text{A} \rightarrow 3.0\,\text{A}$, $\Delta I_{\text{pp}} = 4\,\text{A}$). Note that balancing is maintained despite the transient at the FCC bridge-leg's output. It can be concluded that even without closed-loop voltage balancing, load steps within the nominal load range are not critical regarding FC voltage balancing thanks to correctly dimensioned FCs.

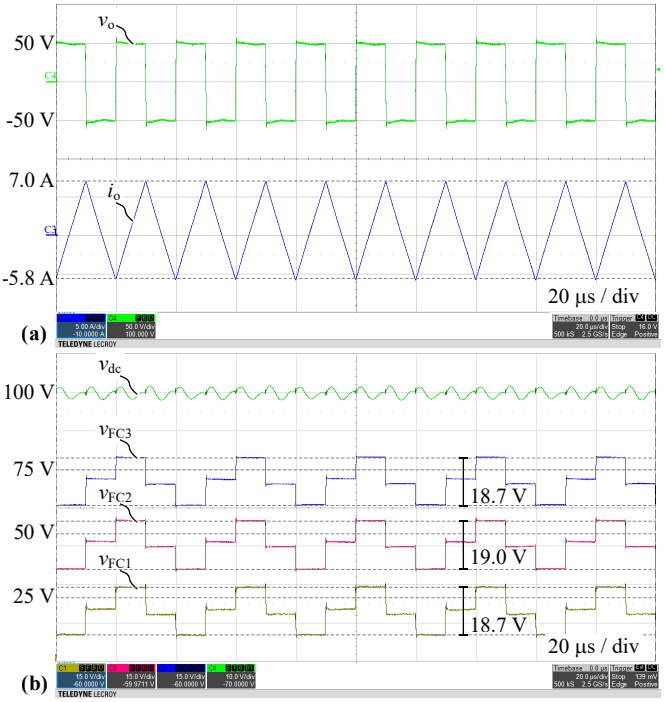

Figure 14. Measured waveforms for Q2L-5L-FCC in configuration ① with OL balancing and triangular current ($I_{\text{o,max}} = 7.0\,\text{A}$, $I_{\text{o,min}} = -5.8\,\text{A}$): (**a**) Output voltage v_{o} and current i_{o}, (**b**) DC-link capacitor voltage v_{dc} and FC voltages $v_{\text{FC}\{1,2,3\}}$. A delay time $T_{\text{delay}} = 100\,\text{ns}$ is used.

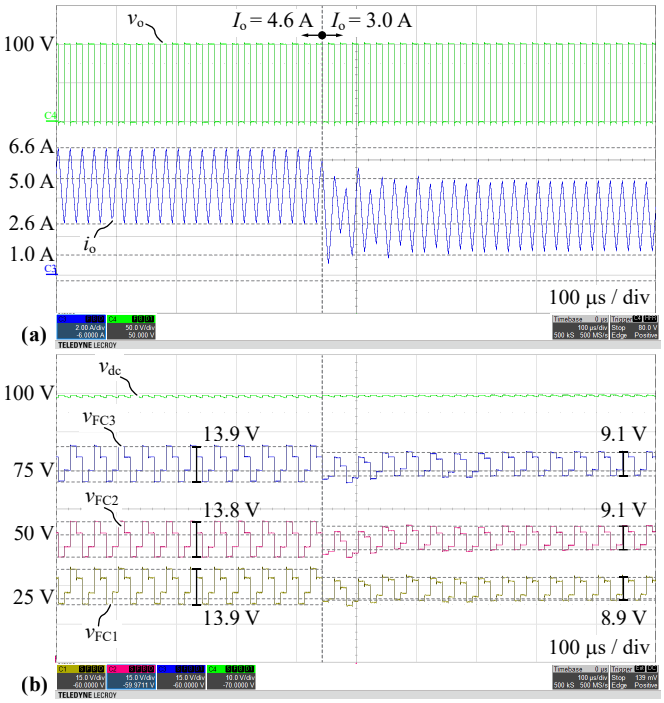

Figure 15. Measured waveforms for Q2L-5L-FCC in configuration ② with OL balancing during a negative load step from 100% to 67% of the nominal load ($I_o = 4.6\,\text{A} \rightarrow 3.0\,\text{A}$, $\Delta I_{pp} = 4\,\text{A}$): (**a**) Output voltage v_o and current i_o, (**b**) DC-link capacitor voltage (v_{dc}) and FC voltages $v_{FC\{1,2,3\}}$. A delay time $T_{delay} = 100\,\text{ns}$ is used.

6.3. Closed-Loop Balancing

This section presents experimental verification of the CL balancing concept proposed in Section 4. First, operation with non-zero load currents is demonstrated, cf. Section 4.1, where the cell voltage tracking MPC with horizon one, see (31)–(35), is employed and $T_{delay} = \{50, 100\}$ ns for all cells is used. Next, for the operation with zero load current, the FC voltage tracking MPC with a horizon of six steps ($N_p = 6$) is employed, see (36)–(41), and $T_{delay} = T_p = 50\,\text{ns}$ are used, cf. Section 4.2.

6.3.1. Balancing with Non-Zero Output Current

Figure 16 shows measured waveforms for split DC-link configuration with CL balancing and triangular current ($I_{o,max} = 5.9\,\text{A}$, $I_{o,min} = -5.8\,\text{A}$). The average absolute relative deviation of the estimated peak-to-peak voltage ripple (4.5 V) from the measured value is 11 %, which again corroborates the proposed model. Note that compared to OL balancing, an approx. 4× smaller peak-to-peak voltage ripple is achieved for the following two reasons. First, with CL balancing in steady-state a minimum delay time ($T_{delay} = 50\,\text{ns}$) is selected by the optimization, whereas with OL balancing the FCs operate with voltage ripples that are characteristic for the maximum delay time ($T_{delay} = 100\,\text{ns}$), which is a consequence of the need to account for the the worst-case output current type (cf. Section 3). Second, in OL operation balancing occurs over 4 output voltage transitions, cf. (21), whereas in CL balancing, the optimization is carried out in every transition, ensuring minimum FC voltage ripple. Furthermore, under CL voltage balancing, the mean values of the FC voltages deviate in steady-state from the ideal reference values (cf. (27)) on average only by 1.9 V (3 %), which results in more symmetric voltage sharing among the switches compared to OL balancing (cf. Figure 14).

Figure 17 presents measured waveforms for the full DC-link configuration with CL balancing during a negative load step from 100% to 67% of the nominal load (similar to Figure 15, $I_o = 4.6\,\text{A} \rightarrow 3.0\,\text{A}$, $\Delta I_{pp} = 4\,\text{A}$). It can be seen that CL with MPC does not feature a symmetric balancing cycle of fixed length like OL, which explains why the voltage

ripple shows a stochastic pattern. At a first glance, it seems as if the FC voltages in case of CL are not as well balanced as in the OL case, i.e., during nominal load operation, the maximum voltage ripples in CL are {11.4 V, 15.0 V, 8.5 V} compared to {13.9 V, 13.9 V, 13.9 V} in OL. This is, however, an intended result of the employed MPC that regulates the cell voltages (and not directly the FC voltages) and is addressed in more detail in the following.

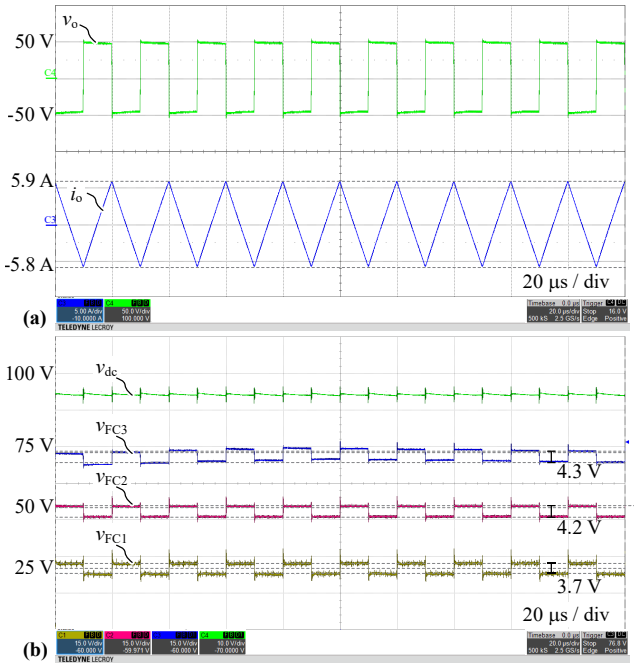

Figure 16. Measured waveforms for Q2L-5L-FCC in configuration ① with CL balancing and triangular current ($I_{o,max} = 5.9\,A$, $I_{o,min} = -5.8\,A$): (**a**) Output voltage v_o and current i_o, (**b**) DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. A delay time $T_{delay} = 50\,ns$ is used.

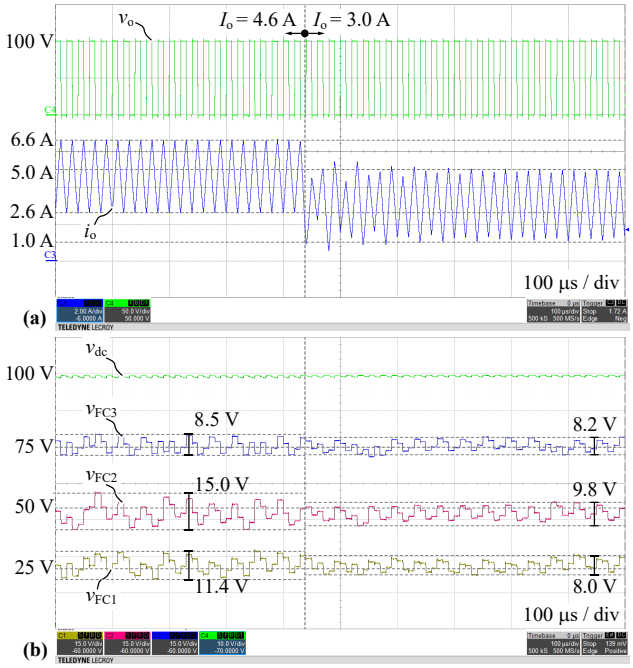

Figure 17. Measured waveforms for Q2L-5L-FCC in configuration ② with CL balancing during a negative load step from 100% to 67% of the nominal load ($I_o = 4.6\,A \rightarrow 3.0\,A$, $\Delta I_{pp} = 4\,A$): (**a**) Output voltage v_o and current i_o, (**b**) DC-link capacitor voltage v_{dc} and FC voltages $v_{FC\{1,2,3\}}$. Delay times $T_{delay} = \{50, 100\}$ ns are used.

Subsequently, Figure 18 demonstrates measured waveforms during the switch-over from OL balancing ($T_{\text{delay}} = 100\,\text{ns}$) to the CL balancing ($T_{\text{delay}} = \{50, 100\}\,\text{ns}$) in a full DC-link configuration with nominal output current $I_{\text{o}} = 4.6\,\text{A}$. It is clear that the CL balancing enables better FC voltage reference tracking. Furthermore, based on the stored waveforms, we compute the corresponding cell voltages $\boldsymbol{V}_{\text{cell}}$ and Figure 19 presents the results. It can be observed for the OL balancing that even though the FC voltages are nicely balanced, the outermost cells, i.e., cell 1 and 4, operate with the maximum voltage ripple across their switches, whereas the middle cells (2 and 3) see an almost constant voltage. As can be seen from the example of voltage sharing on the lower arm of the HB (①, cf. Figure 19) this leads to a large asymmetry of blocking voltages (e.g., $V_{\text{S1n}} = 36.6\,\text{V}$ and $V_{\text{S4n}} = 15.0\,\text{V}$).

On the other hand, with CL balancing (worst-case example, cf. ② in Figure 19) the voltage sharing among the cells is symmetrical, which ensures well-defined voltage levels across the switches. To quantify those differences, we analyze the cell voltage error $(\boldsymbol{V}^{*}_{\text{FC}} - \boldsymbol{V}_{\text{cell}})$ for OL and CL intervals, and average it for each cell over the number of considered half-periods. Considering all cells, the mean voltage deviation with CL balancing is approximately half that observed with OL balancing, i.e., 10.8 % instead of 21.8 %, respectively.

The proposed CL balancing concept compared to methods proposed in the literature, e.g., [31,32], avoids the operation with opposite voltage ripple on FCs, therefore, the switch voltages are not unbalanced by a maximum peak-to-peak voltage ripple of the FCs, which significantly improves the symmetry of the switches' blocking voltages as shown above. This highlights the superiority of the proposed CL balancing concept.

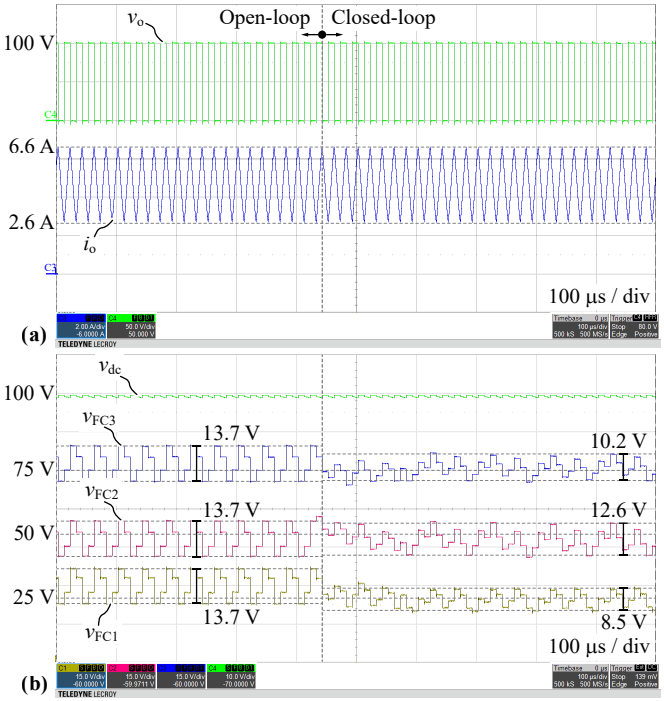

Figure 18. Measured waveforms for Q2L-5L-FCC in configuration ② with transition from OL ($T_{\text{delay}} = 100\,\text{ns}$) to CL ($T_{\text{delay}} = \{50, 100\}\,\text{ns}$) balancing with nominal output current ($I_{\text{o}} = 4.6\,\text{A}$): (**a**) Output voltage v_{o} and current i_{o}, (**b**) DC-link capacitor voltage v_{dc} and FC voltages $v_{\text{FC}\{1,2,3\}}$.

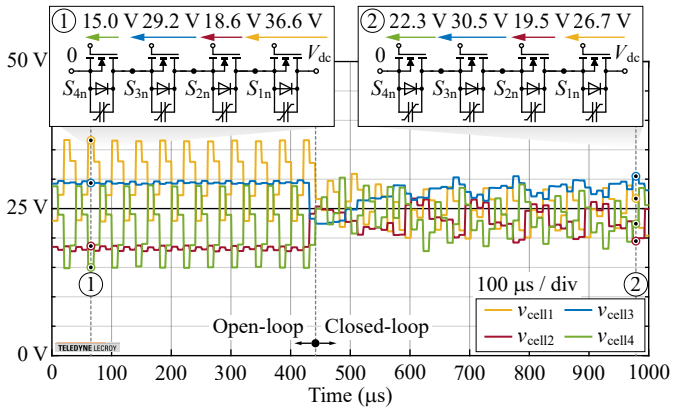

Figure 19. Cell voltages $\boldsymbol{V}_{\text{cell}}$, cf. (31), corresponding to the experiment from Figure 18 (transition from OL to CL balancing with nominal current). Data computed and filtered from oscilloscope waveforms. Note that the ideal cell voltages should be equal to 100 V/4 = 25 V.

6.3.2. Balancing with Zero Output Current

Figure 20 compares no-load FC voltage balancing for OL and CL balancing during full load shedding ($I_{\text{o}} = 5\,\text{A} \rightarrow 0\,\text{A}$) in a full DC-link configuration. Figure 20a shows the operation with resistive balancers and OL balancing, whereas Figure 20b illustrates the proposed CL controller concept employing CMS, cf. Section 4.2. Note the delay before CMS activation which is a consequence of the implemented hysteresis. Nevertheless, the CL controller achieves better dynamics as the steady-state is achieved after approx. 130 µs compared to appox. 540 µs settling time in case of resistive/OL balancing. It is noteworthy that the resistive balancers need to be selected considering the leakage currents of the switches and capacitors, therefore the time constant of the resistive balancing is determined by the circuitry and there are only limited tuning possibilities, especially if the losses in the balancing resistors must be limited. Furthermore, the resistive balancers are generating continuous losses, whereas in case of balancing with CMS, the zero-current hard-switching losses occur only during activation of CMS, i.e., several events at most over tens of switching transitions which leads to negligible average losses.

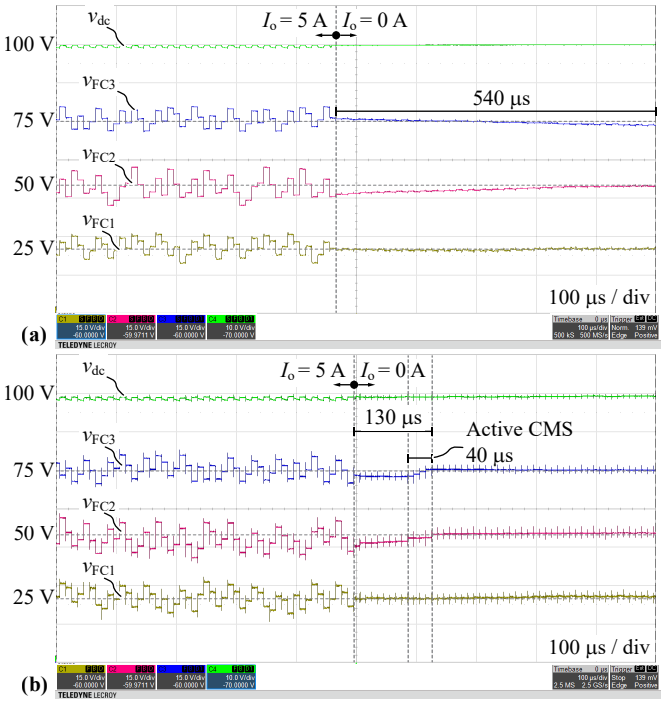

Figure 20. Comparison of measured waveforms (DC-link capacitor voltage v_{dc}, FC voltages $v_{FC\{1,2,3\}}$) for Q2L-5L-FCC in a full DC-link configuration during load disconnection ($I_o = 5\,A \rightarrow 0\,A$): (**a**) OL with resistive balancers; (**b**) CL balancing with CMS. Delay times $T_{delay} = T_p = 50\,ns$ are used.

6.4. Start-Up and Shut-Down

In the last part of experimental validation we demonstrate voltage balancing during start-up and shut-down of the Q2L-5L-FCC. Note that in both experiments CL balancing is used.

Figure 21a presents measured waveforms in a full DC-link configuration with resistive balancers. The operation profile consists of the following intervals: A DC-link precharge via a resistor (disconnected load) $\rightarrow$ idle operation of Q2L-FCC after bridging the precharging resistor $\rightarrow$ connection of the load (nominal FC voltage ripple) $\rightarrow$ disconnection of the input supply and dissipation of the DC-link energy in the load. It can be noticed that the FC voltages are brought smoothly to and remain close to the their reference average values in the steady-state. Note that the jump in the capacitor's voltage at the transition from *precharge* to *idle* interval is caused by the bridging of the precharging resistor. Furthermore, from the start of the *idle* interval the CL controller is active.

Figure 21b shows measured waveforms of a similar operation profile but in a split DC-link configuration without resistive balancers, however, in this case, the load is connected at all times. Again, it can be stated that the proposed CL balancing concept ensures balanced FC voltages and thus defined voltage levels on the switches in all operating modes of the Q2L-FCC.

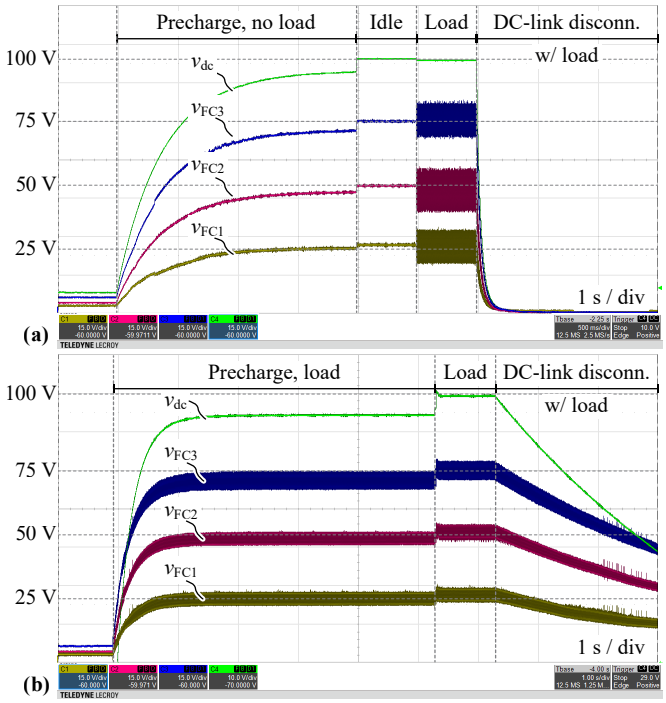

Figure 21. Measured waveforms (DC-link capacitor voltage v_{dc}, FC voltages $v_{FC\{1,2,3\}}$) for start-up (precharging) and shut-down of Q2L-5L-FCC: (**a**) Full DC-link configuration with resistive balancers (precharge → idle → nominal load → DC-link voltage disconnection under load). (**b**) Split DC-link configuration without resistive balancers (precharge under load → nominal load → DC-link voltage disconnection under load). Note the different time bases due to the different DC-link capacitance values.

7. Conclusions

This paper presents a new, comprehensive control concept for load-independent voltage balancing of flying capacitor converters (FCCs) operated in quasi-2-level mode (Q2L-FCC). This new and fully experimentally-verified concept ensures well-defined FC voltages and equal blocking voltages across the series-connected switches with and without load current flowing in the bridge-leg's output terminal.

The proposed closed-loop voltage balancing control concept comprises two methods which are activated depending on the output current of the bridge-leg. In case of a non-zero output current, a first method of active cell voltage balancing involves a model predictive controller (MPC) that selects the most suitable sequence of FC cell commutations within one Q2L transition (1-step horizon) from all possible permutations by minimizing the predicted deviation from the reference values. On the other hand, when the output current is zero, a novel method to balance the FC voltages by means of cell multiple switching (CMS) is used. CMS utilizes the fact that during zero-current hard-switching of a switch, the commutation loop current leads to an exchange of charge (subtraction of charge in a cell's input-side capacitor and addition of that charge to the output-side capacitor) which is equal to the charge stored in the switch's parasitic capacitance. By adding additional switching actions during a Q2L transition, the FC voltages can be adjusted. Again, an MPC approach is utilized to select the optimum CMS sequence, however, using FC voltage reference tracking over a 6-step horizon.

The proposed voltage balancing control concept is thoroughly validated with a 5-level FCC half-bridge demonstrator for hard-switching and soft-switching output voltage transitions, during load transients, as well as for start-up and shut-down operation modes. The hardware experiments demonstrate an excellent average FC voltage tracking as well as symmetric cell voltages. More importantly, the results prove the validity of the proposed description of charge and voltage increments in FCs. The presented closed-loop cell voltage

control concept, compared to open-loop (passive) balancing or active balancing directly controlling FC voltages, results in voltages across the switches that are close to the ideal values and optimum FC voltage ripples. The versatility of the proposed solution comes at the price of the required measurement circuitry to sense the FC voltages. In return, however, the proposed controller is computationally efficient and can be easily implemented in an FPGA, partially using offline-generated look-up tables.

Alternatively, the future research should focus on the FC voltages estimation from the switching sequence and the output voltage since the FC voltages combined with the DC-link voltage appear in the output voltage during the Q2L transitions, which would enable 'sensor-less' FC voltages balancing.

The proposed closed-loop voltage balancing turns the Q2L-FCC into a robust versatile half-bridge power semiconductor stage for various hard-switched and soft-switched applications such as AC-DC rectifiers and isolated DC-DC converters, where the system voltages exceed the voltage ratings of available power semiconductors.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

CMS	Cell multiple switching
FC	Flying capacitor
FCC	Flying capacitor converter
HS	Hard-switching
MPC	Model predictive control
MS	Mixed sequences
Q2L	Quasi-2-level
ZVS	Zero voltage switching
$\mathbf{1}_{i,j}$	Matrix of ones of dimensions $i \times j$
C_{FC}	FC value
$C_{\mathrm{Q,eq}}$	Charge equivalent output capacitance
d	Duty cycle
ΔI_{pp}	Peak-to-peak output current ripple
ΔV_{FC}	Voltage increment on the FC
ΔV_{pp}	Peak-to-peak voltage ripple
ΔV_{CMS}	Voltage increment in CMS
ΔQ_{FC}	Charge increments in FC
i_{c}	Instantaneous FC current
i_{o}	Instantaneous output current
I_{o}	Average output current
$I_{\mathrm{o,max}}$	Maximum peak output current

j	Number of FCs
J	Cost function
k	Discrete time step
N	Number of FCC voltage levels
n	Number of FCC cells ($n = N - 1$)
N_p	Prediction horizon
SEQ	Sequence of cell commutations
T_t	Transition time
T_delay	Delay time
T_p	Pulse time
T_CMS	CMS time
T_s	Switching period
v_c	Instantaneous FC voltage
v_o	Instantaneous output voltage
V_dc	DC-link voltage

Appendix A. CMS for Semiconductors of Various Voltage Classes

The proposed method for balancing the FC voltages without load current, i.e., cell multiple switching (CMS), relies on the charge stored in the output capacitances of the switches, cf. (12). Section 6.3.2 shows experimental validation for 150 V GaN eFETs (EPC2033) operated at a reduced (for safety reasons) $V_\mathrm{s} = 25\,\mathrm{V}$, cf. ① in Table A1. However, the question arises whether this result is representative also for higher voltages, and then for power semiconductors of different voltage classes.

Therefore, we consider the following semiconductors in Q2L-5L-FCC designs with typical ratings for the given device: 150 V GaN eFET (EPC2033), 1.7 kV SiC MOSFET (C2M0045170P) and 10 kV SiC MOSFET (QPM3-10000-0300), cf. Table A1. Figure A1 shows the absolute voltage increment per CMS event, cf. (12) as a function of the capacitance ratio $k_\mathrm{c} = 2C_\mathrm{Q,eq}/C_\mathrm{FC}$. For a fixed delay time and a maximum output current, a higher allowed FC voltage ripple results in a lower FC capacitance requirement, and therefore, for a given switch voltage, in a better controllability (i.e., larger voltage increment per CMS event). Moreover, it can can be noticed that for the GaN eFETs operated at 25 V (for $\Delta V_\mathrm{pp,\%} = 20\%$, see ☆), the value of $\Delta V_\mathrm{CMS} = 1.1\,\mathrm{V}$ corresponds to approx. half of the maximum increment when operated at 100 V (2.3 V). This can be explained by the 4× higher switch voltage but approx. factor of 2 lower $C_\mathrm{Q,eq}$ in case of ② which indicates that the controllability at 100 V would be better for the same absolute value of voltage ripple which is discussed in detail in the following.

To assess CMS controllability, a relative voltage increment k_V defined as ratio of $\Delta V_\mathrm{CMS}/\Delta V_\mathrm{pp}$ is introduced. Since the value of the FCs is designed for a desired voltage ripple, the relative voltage increment is constant for the considered semiconductor and operating parameters, and the respective values are shown in Table A1. We use the same absolute voltage ripple in the experiments with the demonstrator at 25 V as for operation at 100 V, hence reducing the controllability (5.6% vs. 11.5%), therefore the measurements represent the worst-case scenario. Finally, it can be seen that CMS events in case of 1.7 kV and 10 kV SiC MOSFETs provide even more controllability than Q2L-FCC with 150 V GaN eFETs.

Table A1. Parameters for CMS controllability analysis for semiconductors of various voltage classes for the considered relative peak-to-peak FC voltage ripple range $\Delta V_{pp,\%} = \Delta V_{pp} / V_s \in [5\%, 20\%]$.

Param.	**150 V GaN (EPC2033)**		**1.7 kV SiC (C2M0045170P)**	**10 kV SiC (QPM3-10000-0300)**	
	①	②	③	④	
V_{dc}	100 V	400 V	4.4 kV	26.8 kV	DC-link voltage
V_s	25 V	100 V	1.1 kV	6.7 kV	switch voltage
$C_{oss,eq}$	1480 pF	760 pF	727 pF	200 pF	charge eq. capacitance
$I_{o,max}$	6.6 A	6.6 A	28 A	10.75 A	max. output current
$I_{o,ZVS}$	2.5 A	2.5 A	8 A	6 A	min. output current w/ ZVS
T_{delay}	100 nF	100 nF	200 nF	1000 nF	max. delay time
Relative controllability					
$k_V = \frac{\Delta V_{CMS}}{\Delta V_{pp}}$	5.6%	11.5%	14.7%	12.4%	relative CMS controllability
ΔV_{pp}	5–20 V [1]	5–20 V	57–227 V	0.33–1.33 kV	peak-to-peak volt. ripple

[1] Note that in case ① in experiments a relative peak-to-peak FC voltage ripple of 80% is used.

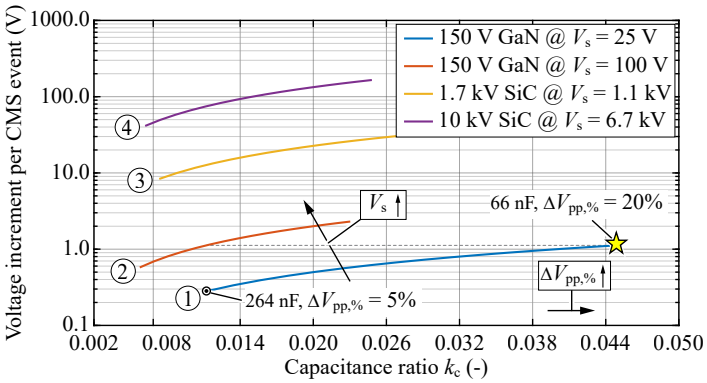

Figure A1. Absolute voltage increment per CMS event (ΔV_{CMS}) for semiconductors of various voltage classes as functions of the capacitance ratio $k_c = 2C_{Q,eq}/C_{FC}$ for the considered relative peak-to-peak FC voltage ripple range $\Delta V_{pp,\%} = \Delta V_{pp} / V_s \in [5\%, 20\%]$.

Appendix B. Discussion of Overload and Short-Circuit Operation

In case of excessive currents, i.e., overload or short-circuit currents (e.g., 10× higher than nominal) at the output of Q2L-operated half-bridge, there is a risk of overcharging the FCs. Moreover, unequal voltage sharing among the switches could ultimately lead to their destruction. However, from the Q2L operation description in Section 2 we know that a fault needs to be present during the switching transition, therefore in a relatively short interval compared to the dynamics of the system (di/dt), to create hazardous conditions for the capacitors and their voltages. To mitigate the eventual overvoltage conditions, we propose to set an ultra-short delay time $T_{delay} = T_{sh}$ (with T_{sh} in the range of rise/falling switching times of the semiconductors, as hard-switching is expected), which is applied in the Q2L switching transitions following an overcurrent detection. If the gate drivers are equipped with (ultra)-fast overcurrent detection, the fault can be cleared within ≈ 100 ns for LV GaN switches [43] and within ≈ 200 ns for MV SiC MOSFETs [44]. Thus, in the worst-case scenario, only a single Q2L transition will be impacted by excessive currents. In this regard, a correctly dimensioned T_{sh} should be sufficient to avoid harmful voltage deviations.

Furthermore, in case of some MOSFETs, e.g., 10 kV SiC MOSFETS, due to the excessively high drain current in the conducting switches the so-called *self turn-off* occurs, caused by the voltage drop across the source inductance [44]. This phenomenon effectively leads to the simultaneous switching of series connected MOSFETs as in a 2L bridge-leg. As a result, the commutations of the individual cells overlap, leading to a continuous output voltage change instead of a staggered transition. Hence, the charge increments of the FCs are negligible and it can be concluded that under such conditions the operation of Q2L-FCC

is not critical. Further investigations are out of the scope of this paper, but should be performed in the course of further analysis of the proposed FC voltage balancing concept.

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