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***Abstract*—Hybrid battery/fuel cell power supplies for all-electric Vertical Takeoff and Landing (eVTOL) aircraft enable a high peak power capability as well as long-range operation. However, the wide and overlapping voltage ranges of the battery and the fuel cell require an interconnecting bidirectional DC-DC converter with buck-boost capability. For such a converter system, the gravimetric power density is a key metric. Therefore, this paper systematically investigates the weight limits of several converter topology concepts: Starting from a standard two-level four-switch non-inverting buck-boost converter benchmark system, fully soft-switched operation, as well as flying-capacitor multilevel and partial-power-processing variants are compared by means of a comprehensive Pareto optimization (mission-profile efficiency vs. gravimetric power density). Aiming at a mission profile efficiency of $\bar{\eta} > 98.5\,\%$, the results indicate the feasibility of converter realizations with gravimetric power densities of up to $\gamma > 62\,\mathrm{kW/kg}$ with a three-level flying capacitor multilevel converter. Further, a virtual prototype of a two-level four-switch non-inverting buck-boost benchmark system is presented with $\gamma = 46\,\mathrm{kW/kg}$, hence illustrating the trade-off between converter performance and complexity.**

***Index Terms*—DC-DC Converter, Non-Isolated, Buck-Boost, eVTOL, Gravimetric Power Density, Ultra-Lightweight**

I. Introduction

With the present rapidly increasing share of electric vehicles in land-based transportation, the next challenge is given by the electrification of air travel. There, electric propulsion technologies enable new design options, and promote all-electric Vertical Takeoff and Landing (eVTOL) aircraft (cf., **Fig. 1**) with minimum horizontal space requirements during takeoff and landing [1], [2]. In contrast to land-based transportation, weight is *the* crucial performance metric for electric energy supply systems in airborne applications [3], [4], and the specific advantages of Fuel Cells (FCs) (high energy density) and batteries (high peak power capability) promote interest in hybrid power architectures [3], [5]. The power supply architecture considered in this paper is presented in **Fig. 2a** and comprises a bidirectional $150\,\mathrm{kW}$ DC-DC converter system interconnecting the FC and the battery. It is important to highlight that this converter is subject to extremely wide and overlapping input and output voltage ranges (i.e., $U_\mathrm{F} \in 480\,\mathrm{V}$ to $800\,\mathrm{V}$ and $U_\mathrm{B} \in 450\,\mathrm{V}$ to $730\,\mathrm{V}$, cf., **Fig. 2b**), such that the lightweight DC-DC converter must provide buck-boost capability.

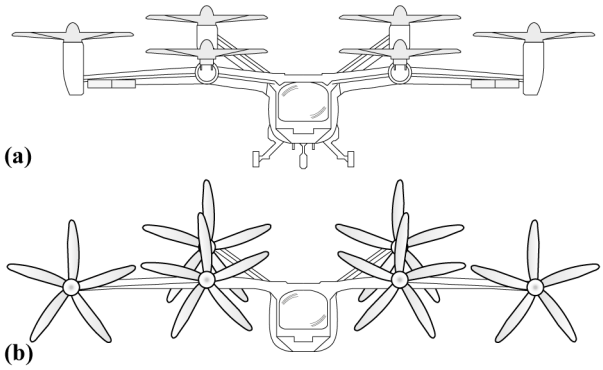

Fig. 1. Conceptual drawing of an all-electric Vertical Takeoff and Landing (eVTOL) aircraft in **(a)** hover propulsion configuration for takeoff and landing, and **(b)** forward propulsion configuration for cruising (from [1]).

Although a plurality of publications on weight optimization of power electronic converters (e.g., [6]–[11]) does exist, no comprehensive Pareto comparison [12] among converter topology concepts has yet been conducted for the application and specifications outlined above, i.e., lightweight DC-DC conversion with buck-boost capability. Accordingly, this paper investigates the performance limits (i.e., gravimetric power density and efficiency) of buck-boost DC-DC converter topology concepts: Starting from a standard two-level benchmark system, fully soft-switched, flying capacitor multilevel, and partial power processing topologies (cf., **Fig. 3**) are compared by means of comprehensive Pareto optimizations. Aiming at redundancy (and to enable the use of semiconductors in high-performance packages) converter modules with $P_\mathrm{M,N} = 15\,\mathrm{kW}$ are optimized, and the rated system power $P_\mathrm{N} = 150\,\mathrm{kW}$ is then realized by paralleling ten such converter modules [13].

The paper is structured as follows: **Section II** discusses the operating concepts and modulation strategies for the topologies of interest, **Section III** presents the optimization framework and **Section IV** the optimization results. Finally, **Section V** summarizes the main findings and provides an outlook for future research topics.

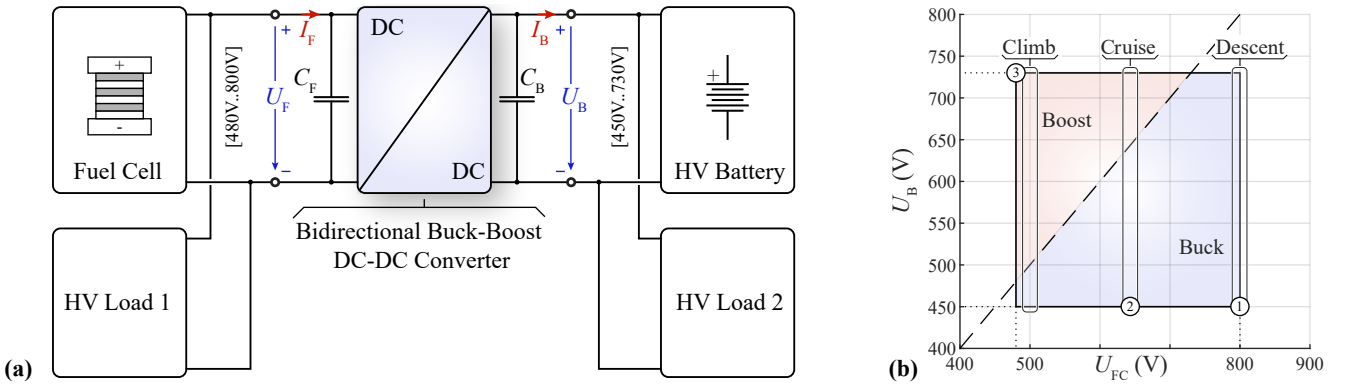

Fig. 2. (a) Considered eVTOL aircraft hybrid-electric power distribution architecture; a bidirectional buck-boost DC-DC converter interconnects the Fuel Cell (FC) and the battery. **(b)** DC-DC converter input and output voltage ranges. The system has to provide $P_N = 150\,\text{kW}$ within the complete input-output voltage range, where ten parallel converter modules with $P_{N,M} = 15\,\text{kW}$ are considered. The exemplary operating points ① - ③ are investigated in more detail in **Fig. 3**.

II. Considered Topologies / Concepts

Fig. 3a-e depicts the main power circuits of the considered topologies as well as the corresponding main converter waveforms at rated system power for the exemplary operating points ① - ③ highlighted in **Fig. 2.**

In the most simple case, a four-switch Two-Level (2L) non-inverting buck-boost converter (cf., **Fig. 3a**) with 1.2 kV SiC MOSFETs is employed. As can be observed in **Fig. 3a.i-a.iii**, the buck (T_F, T_F') and boost half-bridge (T_B, T_B') semiconductors can be advantageously operated in quasi-single-stage PWM operation [14], such that for any given operating point, only one of the two half-bridges generates switching losses. Apart from the switching frequency f_s, the sizing of the buck-boost inductor L has a major impact on the resulting component current stresses. Alternatively, as illustrated in **Fig. 3b**, when operating both half-bridges of the 2L converter with Constant-Frequency (CF) Zero-Voltage-Switching (ZVS) modulation [15], completely soft-switched operation can be achieved. However, this comes at the cost of increased peak and rms current stresses compared to the conventional operation presented in **Fig. 3a**, especially for high voltage step-up or step-down ratios. It is also important to highlight that for a given module power $P_{M,N}$ an upper bound for the inductance value L exists for CF ZVS operation.

Employing Flying-Capacitor Multilevel (FC-ML) bridge-legs enables higher effective switching frequencies (and hence typically smaller magnetic components), as well as the use of low-voltage semiconductors with improved performance [7]. Both, Three-Level (3L-FC) with 600 V SiC/GaN (cf., **Fig. 3b**) and Seven-Level (7L-FC) realizations with 200 V Si/GaN MOSFETs are presented in **Fig. 3c** and **Fig. 3d**, respectively. Note that for a given maximum high-frequency inductor current ripple, the required inductance value decreases with the number of levels squared, and hence can be decreased by a factor of four for the 3L-FC and by a factor of forty for the 7L-FC compared to the 2L converter in **Fig. 3a**.

Last, as the required voltage step-up and step-down ratios (cf., **Fig. 2b**) remain below a factor of two, also the non-isolated Resonant Switched Capacitor (RSC) Partial Power Processing (PPP) concept [11], [12], [16], [17] depicted in **Fig. 2c** is applicable. Here, two fully-soft-switched resonant symmetrizers (with 3L-FC bridge-legs) set the capacitor voltages of C_{TF} and C_{TB} to half the FC and half the battery voltage, respectively, thereby enabling a 2L PPP buck-boost converter processing only half the system power. Advantageously, 600 V SiC/GaN MOSFETs can be employed for all power semiconductors, and, compared to the 3L-FC, fewer power semiconductors are located in the inductor current path. This, however, comes at the cost of an increased component count. Also, the inductance value L is only reduced by a factor of two compared to the conventional system in **Fig. 3a**, as the topology does not realize an increased effective switching frequency (the buck-boost stage, after all, operates as a 2L buck-boost converter, albeit with only half the system's DC voltage). It is important to highlight that the RSC bridges are assumed to only operate at integer multiples of the 2L PPP switching frequency. Further, the resonance capacitor voltage swing (cf., u_{CrF} and u_{CrB}) has to be limited in order not to exceed the RSC semiconductor blocking voltage.

III. Multi-Objective Pareto Optimization

In order to take into consideration all relevant Degrees of Freedom (DOF) for the system realizations of the considered topologies (cf., **Fig. 3**), a multi-objective Pareto optimization [12] is conducted. The employed optimization framework is outlined in **Fig. 4**, and is supplied with the system specifications and main design constrains (**Section III-A**), and then sweeps the main converter-level (**Section III-B**), and the component-level DOF (**Section III-C**). Finally, the resulting converter designs are evaluated with respect to the rated power capability and system performance (**Section III-D**), allowing to identify the limits in gravimetric power density and efficiency of each topology.

A. Specifications and Constraints

As mentioned, the number of parallel modules is set to ten (i.e., nominal module power $P_{M,N} = 15\,\text{kW}$), whereas

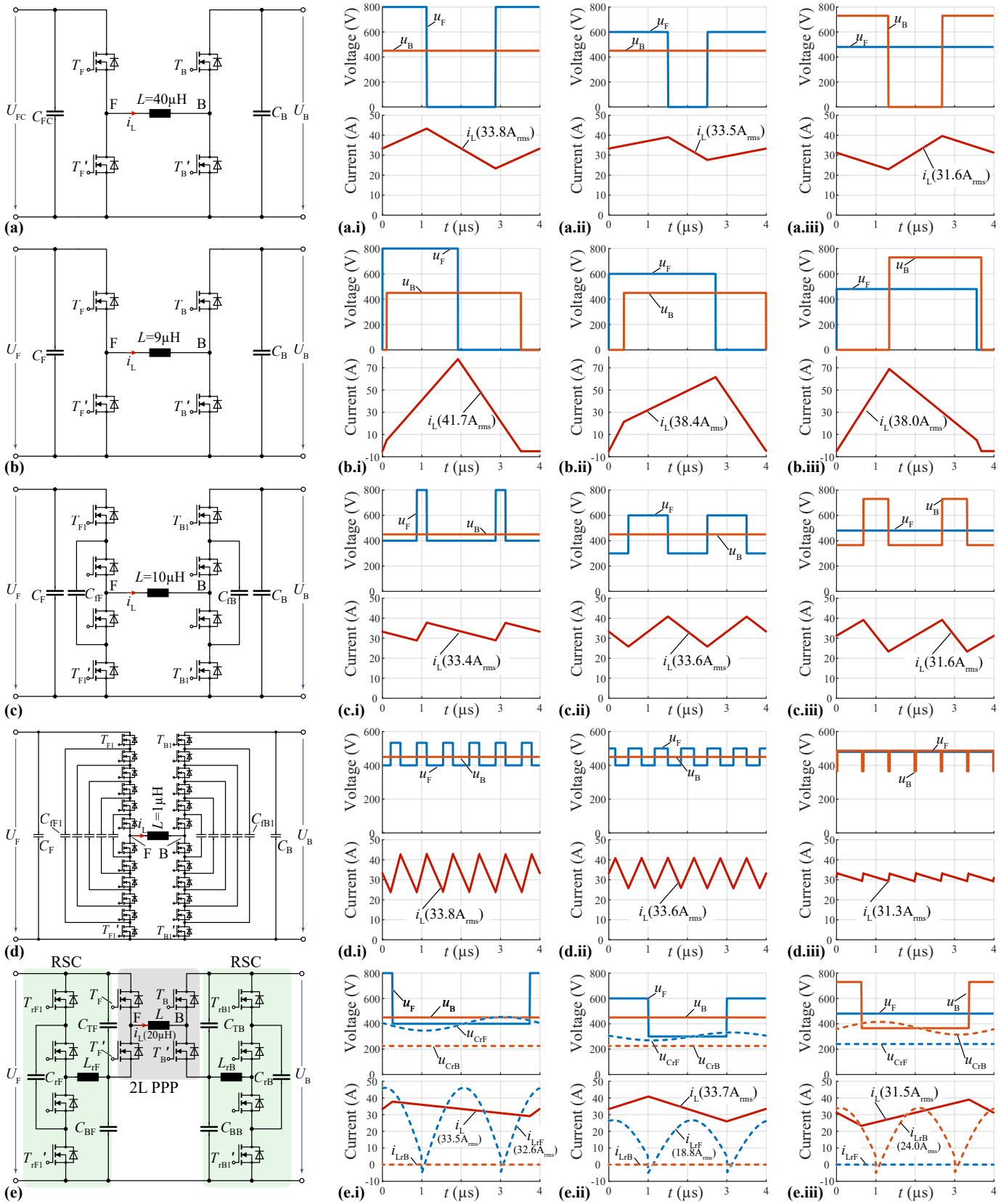

Fig. 3. Main power circuits of the considered buck-boost converter topologies: **(a)** standard hard-switched and **(b)** Constant-Frequency (CF) Zero-Voltage-Switching (ZVS) Two-Level (2L), **(c)** Three-Level (3L-FC) and **(d)** Seven-Level (7L-FC) Flying-Capacitor Multilevel (FC-ML), and **(e)** non-isolated Resonant Switched Capacitor (RSC) Partial Power Processing (PPP) converter. The corresponding main converter waveforms with $P_{\mathrm{M}} = 15\,\mathrm{kW}$ are shown in **x.i** (U_{F}=800 V, U_{B}=450 V), **x.ii** (U_{F}=600 V, U_{B}=450 V) and **x.iii** (U_{F}=480 V, U_{B}=730 V), i.e., for the exemplary operating points ① - ③ highlighted in **Fig. 2.** Here, all power semiconductors operate with f_{s} = 250 kHz and the buck-boost inductance value is (if applicable, i.e., not for (b)) set such that a maximum high-frequency current amplitude of 30 % results.

future research could further investigate the number of parallel modules as an additional system-level DOF. There, advanced control strategies that adapt the number of active modules based on the instantaneous power level could allow a further performance increase, especially at partial load. Further, a liquid cooling system with a maximum coldplate inflow temperature of $T_{\mathrm{h,max}} = 80\,^{\circ}\mathrm{C}$ is available. Note that the liquid-to-ambient heat exchanger is shared with other onboard systems and hence not considered part of the DC-DC converter. The tolerable high-frequency voltage variation on the converter terminals is set to $\Delta V_{\mathrm{pp}} = 5\,\%$ relative to the maximum value of U_{F} and U_{B}, hence defining the sizing of the input and output capacitors for a given switching frequency. Note that eventually additional filter stages on the FC and the battery side would be required to limit high-frequency currents and/or assure electromagnetic compatibility, which is not considered here. As the high-frequency voltage ripple of flying capacitors (if present) is confined within the system, a relaxed voltage ripple criterion of $\Delta V_{\mathrm{f,pp}} = 10\,\%$ (relative to the maximum voltage value of the flying capacitor with the lowest voltage rating) is considered. Last, an overhead performance penalty of $50\,\mathrm{g}$ and $20\,\mathrm{W}$ is added to each converter design to account for the weight and loss contributions of auxiliary supplies, measurement circuitry, power connectors and the Digital Signal Processor (DSP) control board.

B. Converter-Level Degrees of Freedom

The converter-level DOF impact the main converter waveforms of the considered topologies (cf. **Fig. 3**) and the relevant parameters are listed here:

- The switching frequency f_{s} of the buck and boost bridge-legs is a key DOF for all topologies and impacts the sizing of the passive components, as well as the resulting semiconductor switching losses.
- Similarly, the high-frequency buck-boost peak inductor current ripple ΔI_{Lp} (relative to the maximum low-frequency inductor current) is a DOF applicable to all topologies with hard-switched bridge-legs (i.e., all except the CF ZVS converter). For a given value of f_{s} it directly defines the buck-boost inductor value L and represents a trade-off between conduction losses and the hard-switched current values.
- In contrast, an upper bound L_{max} exists for the inductor value L of the CF ZVS converter (cf. **Fig. 3b**), which is defined by the rated module power $P_{\mathrm{M,N}}$, the input and output voltage ranges, and the switching frequency f_{s} [15]. Accordingly, L/L_{max} is considered as DOF for this topology.
- The selected ZVS current I_{ZVS} is a further DOF for the CF ZVS converter and also for the resonant symmetrizers of the RSC PPP. Note that **Fig. 3b,e** considers $I_{\mathrm{ZVS}} = 5\,\mathrm{A}$.
- The integer ratio of the RSC and buck-boost bridge-leg switching frequency $f_{\mathrm{r}}/f_{\mathrm{s}}$, as well as the allowable peak high-frequency voltage variation of the resonant capacitors $\Delta V_{\mathrm{Cr,p}}$ (defining the sizing of the resonant capacitor C_{r} and inductor L_{r}) are further DOF for the symmetrizers of the RSC PPP.

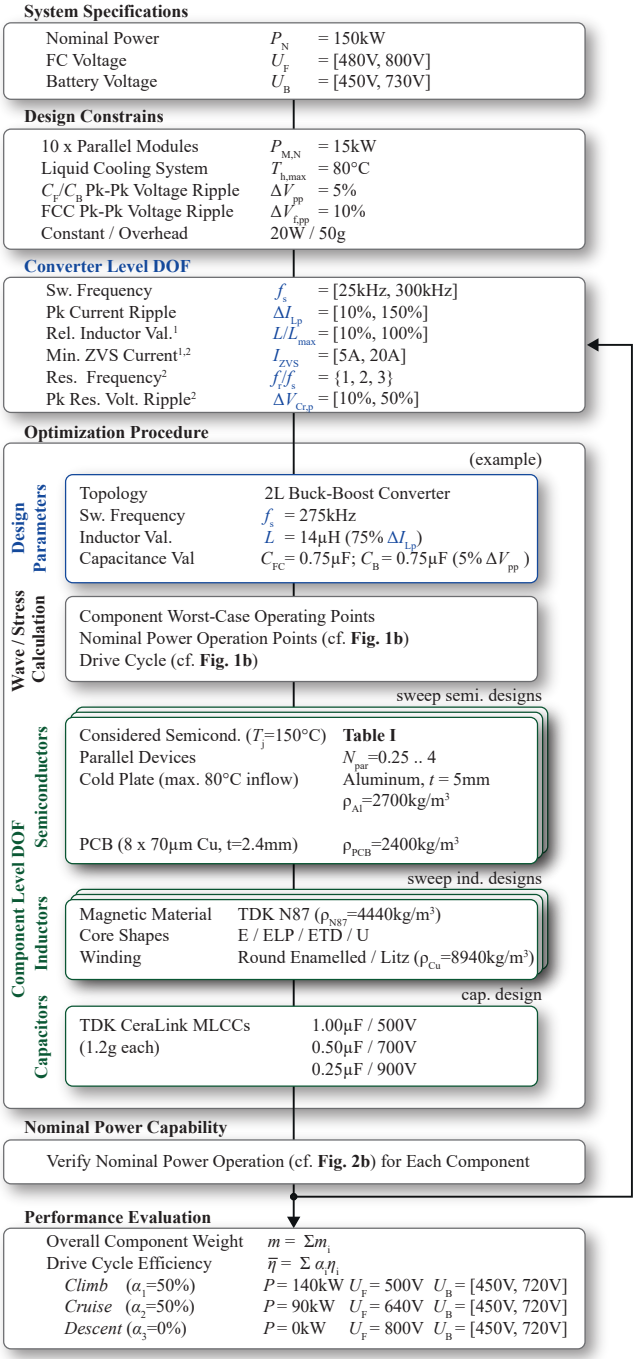

Fig. 4. Flowchart of the employed Pareto optimization summarizing the system specifications, the considered design constraints and optimization variables, the component realization options, and finally the design verification and performance evaluation.
[1] DOF only applicable for the CF ZVS converter.
[2] DOF only applicable for the RSC PPP converter.

C. Component-Level Degrees of Freedom

For a given topology and defined component values, in a first step the main converter waveforms (cf., **Fig. 3**) are

TABLE I
CONSIDERED SEMICONDUCTOR DEVICES

V_{ds}	Mat.	R_{on}[1]	Manuf.	Pt. Number	Package	Weight	A_{PCB}[2]	R_{jc}	R_{ch}[3]	P_{max}[4]	Esw
1.2 kV	SiC	16mΩ	Cree	C3M0016120K	To 247-4	6 g	6 cm^2	0.3 K/W	0.2 K/W	150W	Ref. [18]
650 V	SiC	27mΩ	Infineon	IMZA65R027M1H	To 247-4	6 g	6 cm^2	0.7 K/W	0.2 K/W	80W	Ref. [19]
600 V	GaN	37mΩ	Infineon	IGOT60R042D1[5]	PG-DSO	2 g	3 cm^2	0.8 K/W	0.4 K/W	60W	**Fig. 5**
200 V	GaN	10mΩ	EPC	EPC2034C	BGA	<1 g	1 cm^2	0.3 K/W	2.7 K/W	25W	Ref. [20]

[1]For a junction temperature T_{j}= 25 °C; [2]Estimated PCB area of one device (incl. gate drive); [3]Case-to-heatsink thermal resistance R_{ch} based on the device thermal pad area and assuming a thermal interface material of 0.5 mm thickness and 17.8 W/(mK); [4]Maximum device power based on R_{jc} and R_{ch} assuming a maximum junction temperature T_{j} = 150 °C and a maximum coldplate temperature T_{h}=80 °C; [5]Early engineering samples.

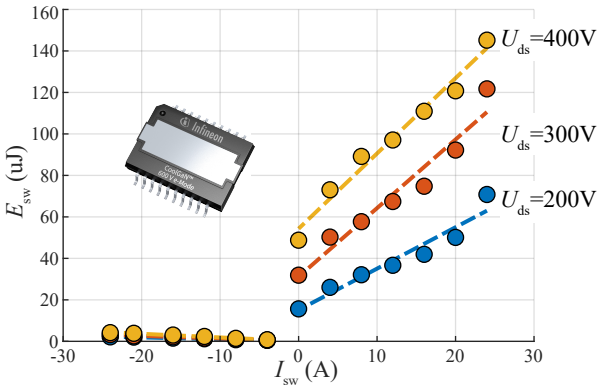

Fig. 5. Calorimetrically measured switching energies of the considered 600 V GaN semiconductors (IGOT60R042D1 early engineering samples, cf. **Table I**) for several voltage U_{ds} and switched current levels I_{sw} in hard-switching (i.e., $I_{\mathrm{sw}} \geq 0$ A) and soft-switching operation.

calculated for all relevant operating points, i.e., the expected worst-case operating point of each power component (for the component design), nominal power operating points across the complete input-output voltage range (cf., **Fig. 2b**), and drive cycle operating points (cf., **Section III-D**). Knowing the voltage and current stresses of all relevant active and passive components then allows to investigate the component-level DOF, where possible practical realizations of power semiconductors, inductors and capacitors can be freely recombined to form converter systems for the given design parameters:

1) Semiconductors: As discussed, different voltage ratings and technologies can be used depending on the considered topology, and **Table I** lists the considered devices. Measured switching energy data can be found in Refs. [18]–[20] and **Fig. 5** further presents the calorimetrically measured [21] hard- and soft-switching energies of early engineering samples of a new, low-on-state-resistance 600 V GaN power semiconductor from Infineon.The devices are assumed to operate at a junction temperature $T_{\mathrm{j}} = 150\,^{\circ}\mathrm{C}$, such that a minimum $\Delta T = 70\,^{\circ}\mathrm{C}$ results between junction and the worst-case coldplate temperature. Considering the data sheet junction-to-case R_{jc} and case-to-coldplate R_{ch} thermal resistances, the maximum device power dissipation P_{max} is calculated (cf. **Table I**), which defines an upper bound for the admissible worst-case device losses. For a given power semiconductor, the selected number of parallel devices N_{par} impacts the resulting switching and conduction losses. Note that also $N_{\mathrm{par}} < 1$ is considered to take into consideration the availability of devices with higher on-state resistance in the same package. The required PCB area A_{PCB} per device (including the gate drive circuitry) is listed in **Table I** and is also utilized to calculate the weight of the coldplate (solid aluminum with $t = 5\,\mathrm{mm}$ assumed, i.e., neglecting the cooling channels).

2) Inductors: Magentic components have a large number of DOF and here, various core geometries (E, ELP, ETD, U), N87 ferrite material, varying air gap lengths, and various winding types (solid enamelled, litz wire) are considered. The resulting losses and thermal equivalent circuits are calculated according to [22].

3) Capacitors: Given the extreme power densities of ceramic capacitors [23], other technologies such as film or electrolytic capacitors are not considered. Further, due to their anti-ferroelectric behavior (i.e., $C(V)$ increases with voltage), only CeraLink capacitors [24] are considered. Note that eventually other capacitor technologies (i.e., with voltage-independent capacitance values) would need to be considered for the realization of the RSC resonance capacitors, which is not done here due to the marginal weight contribution of these resonance capacitors.

D. Design Evaluation and Performance Assessment

For a given converter realization, in a first step the component losses for the nominal power operating points across the input-output voltage range (cf. **Fig. 2b**) are calculated, and designs with invalid component realizations (e.g., thermal limit exceeded) are omitted. Finally, the mission profile / drive cycle efficiency $\overline{\eta}$ is calculated (see also **Fig. 4**) considering *Climbing* (i.e., high power, low FC voltage) and *Cruising* operation (i.e., moderate power, medium FC voltage) (cf. **Fig. 2b**) with identical weights $\alpha_1 = \alpha_2 = 50\,\%$. Note that during *Descent* no power is required from the FC (resulting in a high FC voltage) allowing to shut down the DC-DC converter in this operating mode such that $\alpha_3 = 0\,\%$. By summing up the individual component weights, the gravimetric power density γ of a design can be calculated. This finally allows to identify and compare the Pareto trade-offs between gravimetric power density and (drive-cycle) efficiency, i.e., the performance limits of the considered topologies.

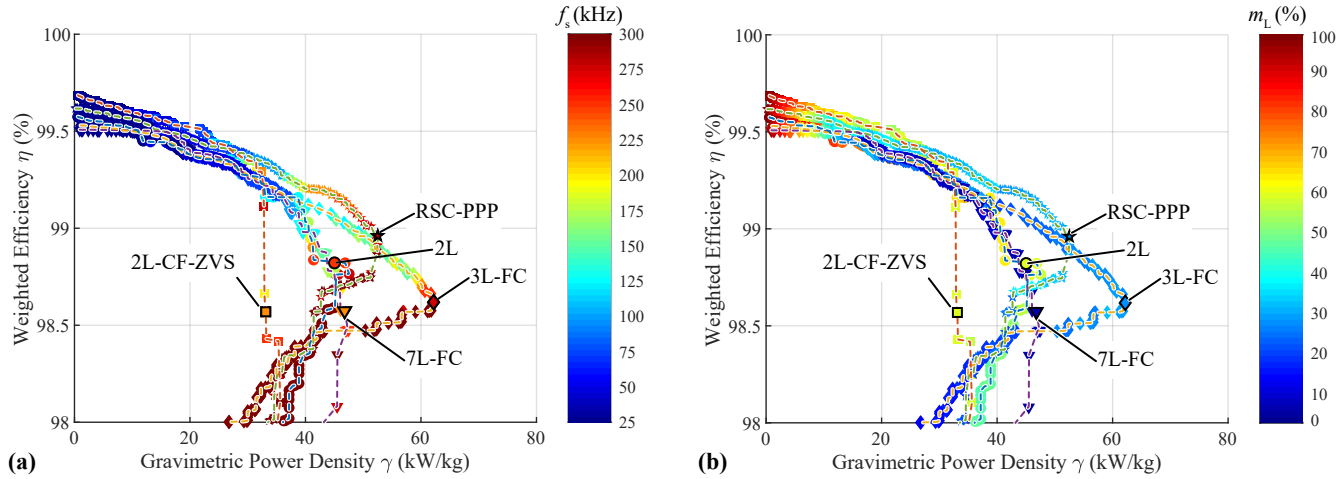

Fig. 6. Pareto optimization results comparing the performance (weighted/mission-profile efficiency $\overline{\eta}$ vs. gravimetric power density γ) of the standard Two-Level (2L), the soft-switched 2L Constant-Frequency (CF) Zero-Voltage-Switching (ZVS), the Three-Level (3L-FC) and Seven-Level (7L-FC), and the Resonant Switched Capacitor (RSC) Partial Power Processing (PPP) buck-boost converter topologies (cf., **Fig. 3**). In **(a)** the colors represent the converter switching frequency f_s and in **(b)** the relative weight contribution of the magnetic components m_L. The detailed weight distributions of the highlighted designs (i.e., for each topology the converter realization with the highest gravimetric power density that still achieves a mission-profile efficiency of at least $\overline{\eta} \geq 98.5\,\%$) are provided in **Fig. 7a**.

IV. Results and Discussion

The results of the Pareto optimization are depicted in **Fig. 6**, where the well known trade-off between (gravimetric) power density and (weighted/mission-profile) efficiency can be observed. The color scale represents the switching frequency f_s in **Fig. 6a** and the relative weight contribution of the magnetics m_L in **Fig. 6b**. The highlighted designs represent the most lightweight converter realizations with $\overline{\eta} \geq 98.5\,\%$ of each topology concept and the detailed weight distributions are provided in **Fig. 7a**.

As can be noted for the standard 2L topology (cf., **Fig. 3a**), increasing the switching frequency enables substantial gravimetric power density gains up to $\gamma \approx 46\,\mathrm{kW/kg}$, i.e., an improvement by more than a factor of two compared to commercial buck-boost systems with $\gamma = 20\,\mathrm{kW/kg}$ [25]. The weight contribution of the magnetics m_L reduces from a major share at low values of f_s to approximately $m_L = 60\,\%$ at $f_s = 275\,\mathrm{kHz}$. The limited switching frequency (caused by the high hard-switching losses and the maximum allowable power dissipation of the considered semiconductors) hence translates into large and heavy magnetics which remain the dominant driver of the system weight.

The soft-switched 2L-CF-ZVS topology outperforms all other topologies in weighted efficiency for low gravimetric power densities, but cannot achieve power densities of more than $\gamma = 33\,\mathrm{kW/kg}$. Note that this is a consequence of the large high-frequency current variation of this topology (cf., **Fig. 3b**) resulting in large high-frequency core and conduction losses in the inductor, which translates into a minimum core size and weight. Further, the considered liquid cooling system does not impose a substantial weight penalty on the high switching losses of the competing hard-switching topologies.

The 3L-FC topology (cf., **Fig. 3c**) achieves a substantial weight reduction with gravimetric power densities of up to $\gamma \approx 62\,\mathrm{kW/kg}$ (i.e., more than a factor of three compared to commercial systems with $\gamma = 20\,\mathrm{kW/kg}$ [25]), which is mainly enabled by the excellent performance of the employed 600 V GaN semiconductors and the increased effective switching frequencies (allowing to cut the inductor value L by a factor of four compared to a 2L converter operating with the same device switching frequency), which results in a corresponding reduction in magnetics volume and weight with $m_L < 30\,\%$ (cf. **Fig. 7b**).

Surprisingly, the 7L-FC topology is limited to similar gravimetric power densities as the 2L benchmark system. This is a consequence of the fact that with increasing number of levels, the magnetic weight contribution m_L becomes less and less dominant, and reaches $m_L < 10\,\%$ for the 7L-FC. At the same time the large number of flying capacitors and power semiconductors (with associated gate drive, PCB and coldplate area and the corresponding weight contributions) limits the achievable gravimetric power density. It is important to highlight that the performance of the 7L-FC is also limited by the poor thermal performance of the 200 V GaN semiconductors (cf., **Table I**).

Last, the non-isolated Resonant Switched Capacitor (RSC) Partial Power Processing (PPP) topology achieves high efficiency enabled by the ultra efficient soft-switched RSC symmetrizers and the partial power processing buck-boost bridge-legs. It outperforms the 3L-FC converter in terms of efficiency in a wide range of gravimetric power densities. However, the additional weight contribution of the RSC components limits the maximum achievable power density to $\gamma \approx 53\,\mathrm{kW/kg}$. Further, from a practical considerations, some control effort is required to assure the proper soft-switching operation of

TABLE II
2L BENCHMARK DESIGN DETAILS

Component	Details
System	$\bar{\eta} = 98.7\,\%$ $\gamma = 46\,\mathrm{kW/kg}$
Semiconductor	$T_\mathrm{F}/T_\mathrm{B}$: f_s = 275 kHz 1x Cree C3M0016120K 1.2 kV SiC / 16 mΩ
Inductor	L = 15 µH (ΔI_Lp=75 %) 2x stacked ELP 43/10/28 Total airgap: 2mm 6x turns / 4600x40 µm litz wire
Capacitor	$C_\mathrm{F} = C_\mathrm{B} = 0.75\,\mu\mathrm{F}$ 3x TDK CeraLink B58031U9254M062 (900 V / 0.25 µF)
Controller	TMS320C2834X

the RSC symmetrizers in such a converter, which increases the realization complexity [17].

In summary, an outstanding gravimetric power density of $\gamma \approx 46\,\mathrm{kW/kg}$ can be achieved with a standard 2L four-switch non-inverting buck-boost converter, which especially also features a comparably low system complexity. The electric specifications and the component realization details of a corresponding 2L benchmark converter are presented in **Table II**. Further, the system-level loss performance across the considered mission profile (cf., **Fig. 2b**, i.e., for climbing and cruising) and a virtual prototype system are presented in **Fig. 7b** and **Fig. 7c**, respectively. Note that calculated peak efficiency values close to 99 % result for operation close to a unity input-output voltage ratio, and the overall mission profile efficiency is $\bar{\eta} = 98.7\,\%$. It is important to highlight that the ratio of switching and conduction losses is heavily tilted towards switching losses (cf., **Fig. 7b**). However, selecting a smaller semiconductor chip area (i.e., higher on-state resistance, lower C_oss) would also result in a higher internal junction-to-case thermal resistance, which in turn would require more parallel devices (and the associated weight overhead of PCB and coldplate) to enable sufficient cooling. Higher performance (about 30 % higher gravimetric power density with an only slightly lower mission-profile efficiency) could of course be achieved with a 3L-FC FC-ML converter prototype, which clearly illustrates a trade-off between performance and converter complexity.

V. CONCLUSION

All-electric Vertical Takeoff and Landing (eVTOL) aircraft are a key technology for the electrification of air travel, and hybrid battery/Fuel Cell (FC) power supplies enable excellent peak power capability and long-range travel. For the thus needed hybrid power architecture, a bidirectional DC-DC converter with buck-boost capability is required to interconnect the battery and the FC, as both DC voltages vary in wide ranges. For such a converter system, the *gravimetric* power density is a key metric and this paper systematically investigates the weight limits of several converter topology

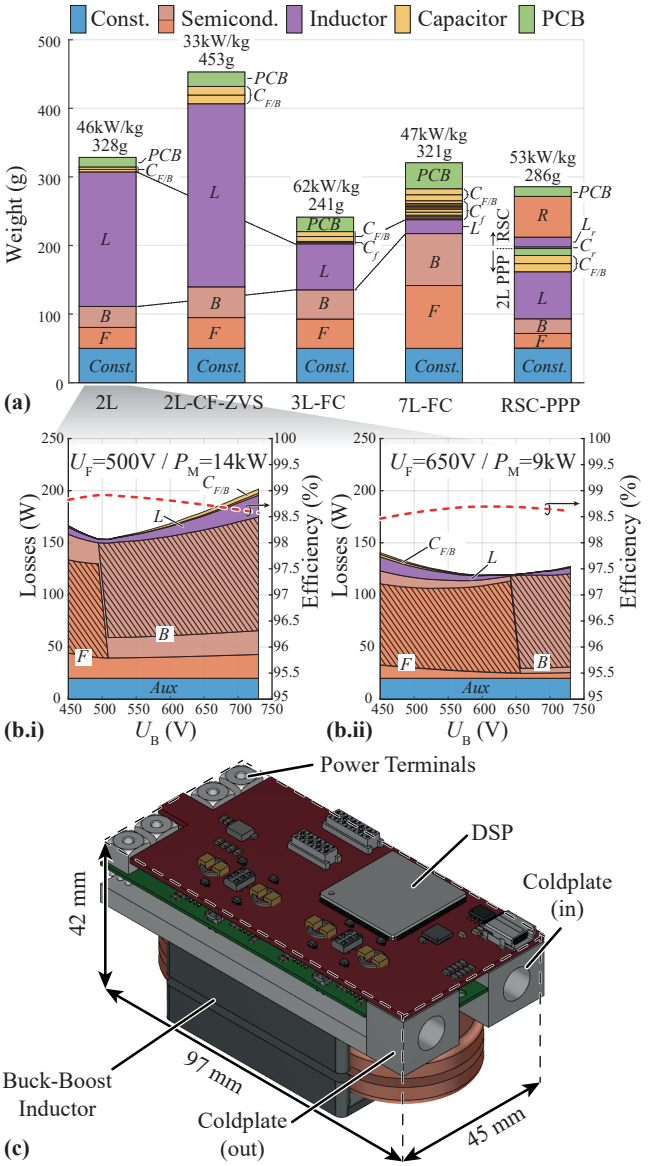

Fig. 7. **(a)** Detailed weight distributions of the converter designs with maximum gravimetric power densities[1] highlighted in **Fig. 6.** 'B' refers to the semiconductors on the battery side, 'F' to those on the fuel-cell side, and 'R' to those of the resonant symmetrizers. **(b)** Calculated loss distribution and efficiency as a function of the battery voltage U_B for the relevant drive cycle operating points (defined by U_F and P_M), and **(c)** virtual prototype of the 2L benchmark design with $\bar{\eta} = 98.7\,\%$ and $\gamma = 46\,\mathrm{kW/kg}$ (component and performance details are provided in **Table II**).

[1]Note that for the 2L converter topology, the highlighted design shows a gravimetric power density $\gamma = 46\,\mathrm{kW/kg}$ slightly below the maximally achievable value of $\gamma = 48\,\mathrm{kW/kg}$ and was selected based on engineering considerations to enable an extremely compact design (see **(c)**).

concepts by means of a comprehensive Pareto optimization (weighted/mission-profile efficiency vs. gravimetric power density). The results indicate the feasibility of power converters with a mission-profile efficiency of $\bar{\eta} > 98.5\,\%$ and a gravimetric power density of $\gamma = 46\,\mathrm{kW/kg}$ for a Two-Level

(2L) four-switch non-inverting buck-boost converter employing $1.2\,\mathrm{kV}$ SiC semiconductors. A virtual benchmark prototype system is presented exceeding the state-of-the-art gravimetric power density by more than a factor of two. When aiming at even higher gravimetric power densities, up to $\gamma = 62\,\mathrm{kW/kg}$ can be achieved with a 3L-FC FC-ML converter employing low-R_{on} $600\,\mathrm{V}$ GaN semiconductors, however, increased complexity has to be accepted.

Future research could further investigate the impact of the module power rating (i.e., the optimum number of converter modules for realizing the given total system power rating) on the overall system performance. Further, the development of low on-state-resistance WBG power semiconductors in packages enabling excellent switching *and* thermal performance, as well as advanced cooling concepts [26] promise ever-more lightweight converter systems for future airborne applications.

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