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Accurate Transient Calorimetric Measurement of Soft-Switching Losses of 10kV SiC MOSFETs

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***Abstract*—The characterization of soft-switching losses of modern high-voltage SiC MOSFETs is a difficult but necessary task in order to accurately model converter systems such as medium-voltage-connected Solid-State Transformers (SSTs), where soft-switching techniques are employed for an increased efficiency. Usually, switching losses in general are measured with the well-known double pulse method. However, in case of soft-switching loss measurements, this method is very sensitive to several effects such as probe skew and limited measurement accuracy, among others, and thus unsuitable for the characterization of fast switching high-voltage MOSFETs. This paper presents an accurate and reliable calorimetric method for the measurement of soft-switching losses using the example of $10\,\mathrm{kV}$ SiC MOSFETs. Finally, measured soft-switching loss curves of these $10\,\mathrm{kV}$ SiC MOSFETs are presented for different DC-link voltages, currents and gate resistors.**

I. Introduction

Soft-switching techniques are widely utilized in power electronic converters for the reduction of switching losses, especially in DC/DC applications [1]–[3] and also in TCM operated AC/DC applications [4], [5]. Although Wide Band-Gap (WBG) devices such as SiC MOSFETs offer superior switching behaviour compared to Silicon devices [6]–[9], the soft-switching losses of these devices (especially in case of high blocking voltage devices in the range of $10\,\mathrm{kV}$) are not negligible, as will be shown in this paper. Therefore, it is very important to consider the soft-switching losses during the design process. However, most of the device datasheets only provide measurement data for hard-switching losses which means that it is necessary to measure the soft-switching losses of the particular devices. Since soft-switching losses are typically small compared to hard-switching and conduction losses, it is challenging to measure soft-switching losses accurately under different operating conditions such as different chip temperatures and independently of external factors such as the PCB-layout and parasitic inductances of e.g the DC-link capacitors.

There are basically two types of switching loss measurement methods, namely electrical measurement methods and calorimetric measurement methods. Electrical methods, such as the well-known double pulse test, feature the advantage that the measurement time is rather short, since only pulse measurements have to be performed. Furthermore, with the same measurement setup both, the hard- and soft-switching losses can be directly determined at different chip temperatures by electrically measuring the device voltage and current during a turn-on and turn-off transient. However, due to the fast switching transients, the accuracy of the measured waveforms and thus the measured switching losses suffers e.g. from improper deskew and jitter between the current and voltage probes, from signal offsets and amplitude errors, from limited bandwidths of the passive or active probes, or from any other measurement distortion such as common mode. In addition, also the post-processing of the measured waveforms is very crucial, e.g. the selection of the proper interval in which the measured power has to be integrated in order to extract the correct loss energy. In contrast to electrical measurements, with a calorimetric measurement setup the semiconductor losses, i.e. the sum of the switching and conduction losses, are determined by measuring the dissipated heat of the device under test (DUT) in continuous operation and, since no fast switching transients have to be measured, typically a higher measurement accuracy can be achieved. Unfortunately, due to the large thermal time constants, calorimetric measurements consume a considerable amount of time until the thermal equilibrium is reached. Furthermore, in order to obtain the pure switching losses, the conduction losses have to be subtracted from the total measured semiconductor losses after the data acquisition. The conduction losses can be calculated based on the DUT's on-state resistance $R_{\mathrm{DS,on}}$ given in the manufacturer's datasheet. The on-state resistance of the examined $10\,\mathrm{kV}$ SiC MOSFETs, however, is strongly depending on the device current, the chip temperature, the current direction (above approximately $10\,\mathrm{A}$, the anti-parallel diode chip starts to conduct due to the flatter characteristic compared to the MOSFET) and even deviates from device to device for more than $20\,\%$ because the MOSFETs at hand are prototype devices.

As can be noticed, both types of measurement methods show certain disadvantages in terms of accuracy and separation of switching and conduction losses. However, there is no quantitative comparison of the measurement accuracy of different measurement methods so far. Therefore, in Section II of this paper, a short overview of electrical and calorimetric measurement methods is given. Based on the performed error analysis it becomes clear that electrical measurement methods known up to now could lead to tremendously wrong results and thus are not suited for soft-switching loss measurements. On the other hand, the accuracy achieved with calorimetric measurements strongly depends on the accurate determination of the conduction losses. Therefore, in Section III a novel calorimetric measurement method is presented, which also eliminates the problem of the switching and conduction loss separation and thus results in a superior measurement accuracy. In section IV, this method is applied to $10\,\mathrm{kV}$ SiC MOSFETs. The obtained soft-switching losses for different DC-link voltages, currents and gate resistors are presented and can be utilized for the design of medium-voltage converters such as DC/DC stages in Solid-State Transformers [10], among others. Section V finally provides a conclusion and an outlook.

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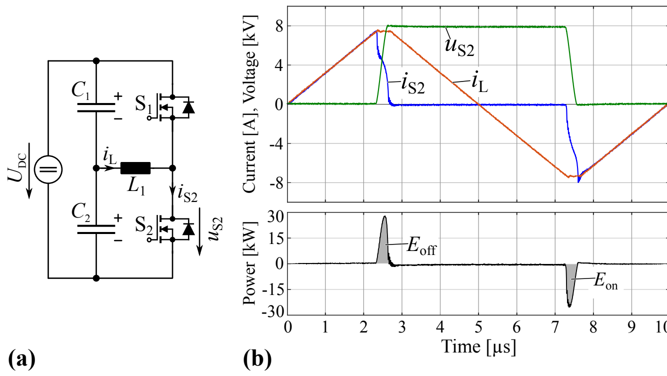


Fig. 1: **(a)** Circuit diagram for the electrical switching loss measurement. **(b)** Measured waveforms and indicated soft-switching energies E_{on} and E_{off}.

II. Existing Switching Loss Measurement Methods

A. *Electrical measurement methods*

A commonly used electrical method for the measurement of switching losses is the double pulse test which is originally intended for the measurement of hard-switching losses. However, by adapting the modulation scheme, this circuit can also be used for the measurement of soft-switching losses. **Fig. 1 (a)** shows the double pulse test circuit which consists of a half bridge, a split DC-link and an inductor. Furthermore, in **Fig. 1 (b)** the inductor current i_{L}, as well as the low-side MOSFET's drain current i_{S2} and its drain-source voltage u_{S2} are shown for a single measurement pulse obtained with the adapted modulation scheme. There, S_2 performs a soft turn-off for a positive inductor current and a soft (i.e. under zero voltage) turn-on for a negative inductor current. For a given DC-link voltage U_{DC} and inductance value L_1, the pulse timings and the dead time are adjusted such that the switched current reaches its desired value and the conduction time of the body diodes are minimized. In order to obtain the switching energies, the drain-source voltage and the drain current of S_2 are multiplied and integrated over the particular switching transitions, leading to E_{off} and E_{on}, as indicated in **Fig. 1 (b)**. The net switching energy loss (per transition) is finally obtained via $E_{\mathrm{SW}} = E_{\mathrm{off}} + E_{\mathrm{on}}$ due to the fact that in each switching transition, one of the two MOSFETs stores E_{off} while the other feeds E_{on} back to the DC-link, because E_{on} is negative. Since there are two transitions per cycle, each of the MOSFETs dissipates the net energy E_{SW} per cycle, such that the corresponding switching losses per switch are obtained via $P_{\mathrm{SW}} = E_{\mathrm{SW}} \cdot f_{\mathrm{SW}}$, where f_{SW} denotes the switching frequency.

However, this method is subject to large measurement errors due to the fact that the soft-switching losses only consist of a small portion of E_{on} and E_{off}, e.g. for this particular type of MOSFET ($10\,\mathrm{kV}, 30\,\mathrm{A}$ from Wolfspeed), E_{SW} is in the range of $10\,\%$ of the returned energy $|E_{\mathrm{on}}|$, i.e. $E_{\mathrm{SW}} \approx 0.1 \cdot |E_{\mathrm{on}}|$. This means that small errors in the measurement of E_{off} and E_{on} can lead to large errors in E_{SW}, as the following example shows. Assuming that $E_{\mathrm{off}} \approx 1.1 \cdot |E_{\mathrm{on}}|$ and both, E_{on} and E_{off} contain a measurement error of $\pm 5\,\%$ (which would be already very accurate, having in mind that E_{on} and E_{off} arise from the integration of a multiplication of a voltage and a current measurement), the measured worst case switching loss energy would result in $E_{\mathrm{SW,meas}} = 1.05 \cdot E_{\mathrm{off}} - 0.95 \cdot |E_{\mathrm{on}}| \approx 1.05 \cdot (1.1 \cdot |E_{\mathrm{on}}|) - 0.95 \cdot |E_{\mathrm{on}}| = 0.205 \cdot |E_{\mathrm{on}}|$ which compared to the assumed $0.1 \cdot |E_{\mathrm{on}}|$ is a relative error of $+105\,\%$, i.e. factor two higher switching losses. In the other case, if E_{off} is measured $5\,\%$ too small and $|E_{\mathrm{on}}|$ is measured $5\,\%$ too large, the relative error is $-105\,\%$, i.e. energy would be generated in each switching cycle which clearly is not the case. This shows that already small measurement errors can lead to tremendously wrong results, thus the double pulse method and probably also other electrical measurement methods are not suitable for the measurement of soft-switching losses of these $10\,\mathrm{kV}$ devices. In order to have a quantitative statement of the achievable accuracy, a detailed error analysis is performed in the following.

Error analysis for electrical soft-switching loss measurement methods

Figs. 2 (a) & **(b)** show measurements of the drain-source voltage u_{S2} and the drain current i_{S2} of MOSFET S_2 in **Fig. 1 (a)** for $8\,\mathrm{kV}$, $10\,\mathrm{A}$ soft turn-off and soft turn-on transitions, respectively. In order to analyze the influence of the probe skew on the measurement accuracy, the originally measured current waveform i_{S2} is delayed for t_{sk}, exemplary $8\,\mathrm{ns}$ in the figure for better visualization. Below the waveforms, the power and the cumulated energy in S_2 are shown for both, the original and the skewed measurements. It can be seen that the skewed turn-off energy $E_{\mathrm{off,sk}}$ is larger than the original energy whereas the absolute value of the skewed turn-on energy $|E_{\mathrm{on,sk}}|$ is smaller than the original one. In this case, more energy seems to be dissipated in the turning-off switch whereas less energy seems to be regained from the turning-on switch, leading to an increase of the net switching losses. If the delay is negative, the overlap of voltage and current decreases compared to its original value, resulting in too low net switching losses. **Fig. 2 (c)** shows the relative error of the net switching losses in dependency of the skew for different DC-link voltages and a switched current of $i_{\mathrm{Switched}} = 10\,\mathrm{A}$ (since the effect is almost independent of the switched current). It can be noted that a skew of only $2\,\%$ of the switching transition's rise/fall time can lead to a switching loss error of 30...40 %, depending on the voltage. In this particular case, where u_{S2} is in the kV-range, the skew of the $20\,\mathrm{kV}$ voltage probe (PHV 4002 from PMK in combination with a 12-bit oscilloscope) is mainly a problem due to the lack of a reference voltage which is necessary for the deskewing of the probe.

As already mentioned, further sources for measurement errors are possible DC offsets and amplitude errors in the voltage and current measurements during the switching transitions. Thereby, especially the $20\,\mathrm{kV}$ voltage probe is again causing problems, because it is not possible to accurately compensate the probe to a proper low-frequency gain, high-frequency gain (responsible for overshoots) and zero voltage offset at the same time. Therefore, a compromise between these factors is necessary which means that in a certain extent these effects are always present.

Hence, a similar error analysis to the one in **Fig. 2** can be performed concerning DC offsets and amplitude errors, assuming a certain DC offset difference or amplitude difference in the voltage measurement between the E_{off} and E_{on} transitions. Accordingly, if the voltage u_{S2} is offset free during the turn-on transition but shows a slight positive offset during the turn-off transition (which could arise from a non-ideal compensation of

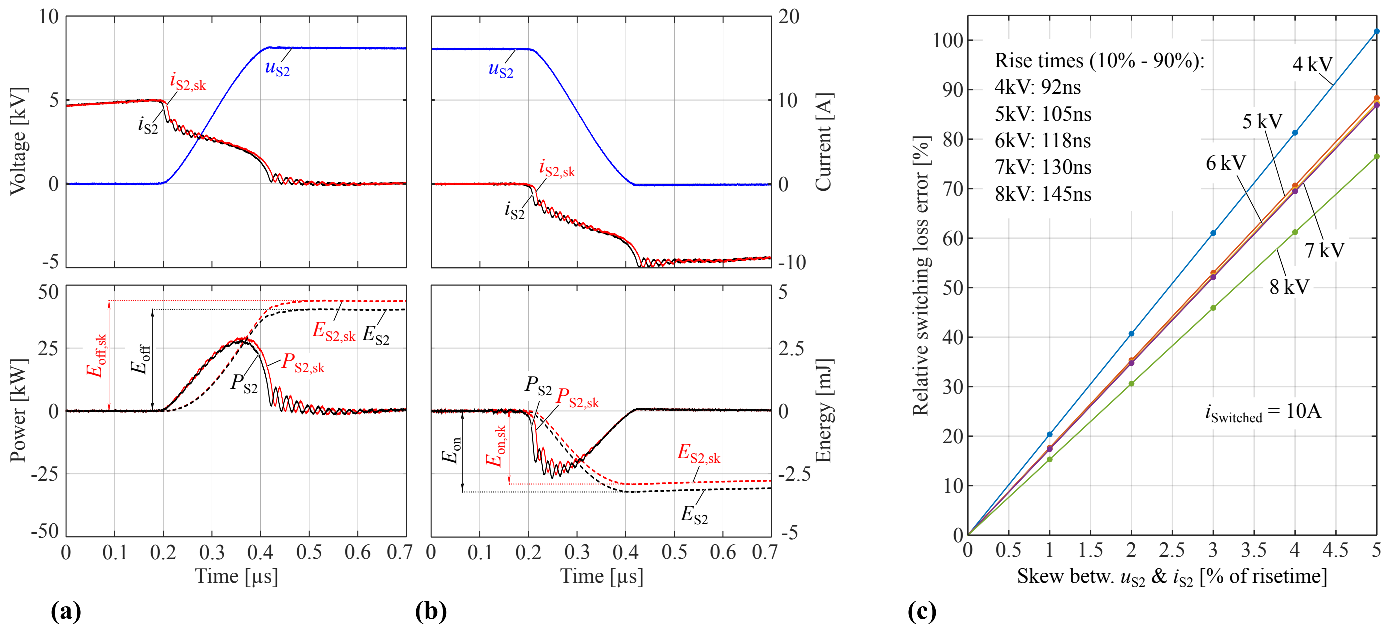


Fig. 2: (a) & **(b)** Measured turn-off and turn-on waveforms together with the power and the switching energies for both, the original and the skewed case. **(c)** Relative switching loss error due to the skew between u_{S2} and i_{S2} for a switched current of $10\,A$ and different DC-link voltages.

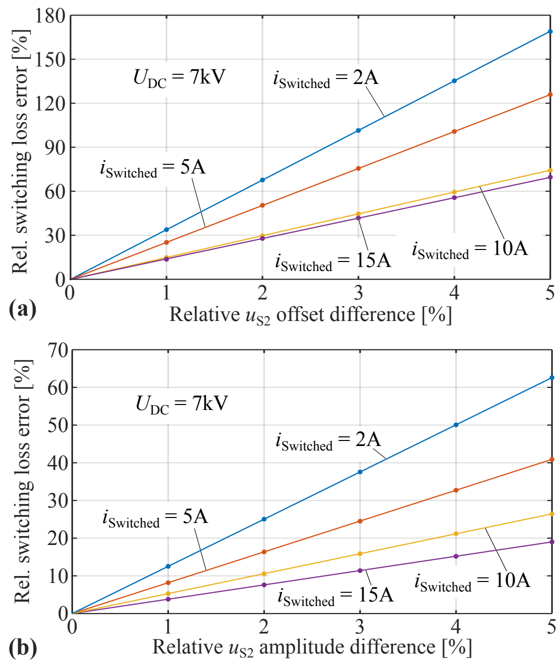


Fig. 3: (a) Relative switching loss error due to an offset difference in the u_{S2} drain-source voltage measurements for the determination of E_{off} and E_{on}. **(b)** Relative switching loss error due to a voltage amplitude difference in the u_{S2} drain-source voltage measurements.

the voltage probe), the integration will lead to an increased turn-off energy E_{off}, whereas the turn-on energy E_{on} is assumed to be measured correctly for this analysis. Since the net switching loss energy is again only in the range of $10\,\%$ of E_{on}, the error in the measurement of E_{on} and E_{off} is strongly amplified which leads to large switching loss errors in E_{SW} as shown in **Fig. 3 (a)**. Depending on the switched current, an offset difference of only $1\,\%$ of the DC-link voltage can lead to a switching loss error of more than $30\,\%$.

Similarly, in **Fig. 3 (b)** the resulting relative switching loss error caused by an amplitude difference between the voltage measurements during the turn-off and turn-on transitions is given. As an example, if for the measurement of the soft-switching losses for $7\,kV$, $2\,A$, the amplitude of the rising voltage edge is measured $2\,\%$ too large whereas the falling edge is assumed to be measured correctly, this leads to a switching loss error of $25\,\%$.

Another source of measurement error can be found in the limited bandwidth of active and passive probes, since frequency harmonics which are contained in the original signal and are located above the probe's cut-off frequency, are filterd out and thus could lead to wrongly measured waveforms with e.g. decreased voltage and current slopes. Assuming that the transfer functions of the probes show first order low-pass characteristics, the original signal can be reconstructed by transforming the measured signal into the frequency domain, multiplying it with the inverse of the probe's low-pass transfer function and transforming the result back into the time domain. For a voltage probe bandwidth of $100\,MHz$ (according to the datasheet), it turns out that the measured and reconstructed waveforms (voltage rise times in the range of $100\,ns$) are virtually identical apart from a slight skew which has to be compensated experimentally in order not to cause large switching loss measurement errors, as explained above. Aside from the skew, the bandwidths of the utilized voltage probe and current transformer (with a bandwidth $> 100\,MHz$) seem to be high enough for this application. However, if the measurement bandwidth is reduced, for the measurements at hand the signal quality starts to suffer if the bandwidth falls below $70\,MHz$ which in this case is considered as the lower bandwidth limit. The reader should note that for the switching loss measurement of e.g. $600\,V$ GaN switches which can reach voltage rise times between $10\,ns$ and $20\,ns$, the probe (and oscilloscope)

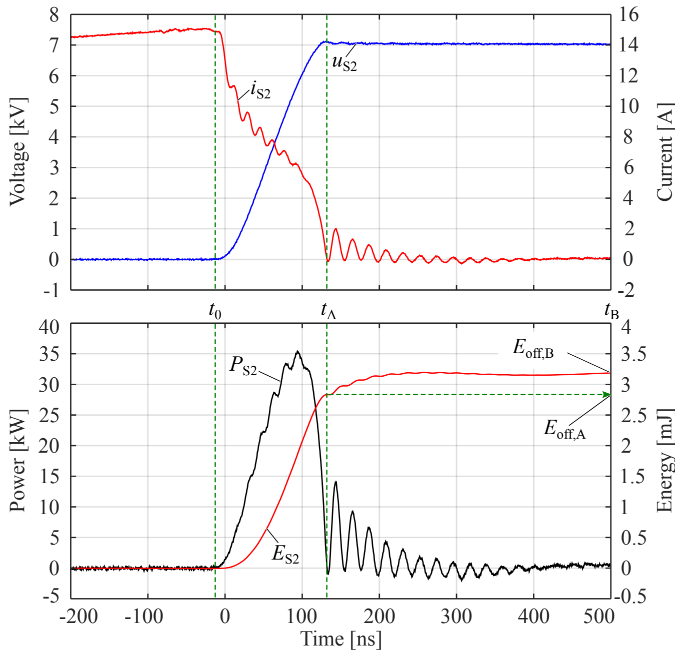


Fig. 4: Exemplary measured 7 kV, 15 A turn-off transition together with the power P_{S2} and the energy E_{S2} for the illustration of the influence of the integration limits on the measured soft-switching losses. Due to the oscillations, the choice of the end of the integration is not clear. t_0 denotes the start of the integration, whereas t_A and t_B are two options to select the end of the integration.

bandwidths have to be higher than 350 MHz to 700 MHz for a sufficient accuracy, respectively.

Besides the described measurement errors, further errors can be introduced in the post-processing of the measured data. For example the proper selection of the time interval in which the switching losses are integrated is aggravated by possible ringing, which in consequence results in wrong turn-on and turn-off switching energies. This is also shown in **Figs. 2 (a) & (b)**, where the current i_{S2} exhibits certain oscillations at the end of each switching transient. In case of the turn-on transition, these current oscillations are, in order to obtain the power P_{S2}, multiplied with u_{S2} which has already decayed to zero at that time. Hence, these oscillations vanish in the power calculation, resulting in a smooth waveform and it is clear where to set the integration limits. However, for the turn-off transition, the current oscillations are multiplied with the full DC-link voltage, leading also to large oscillations in the calculated power waveform and thus making the proper selection of the integration time more difficult. As an example, **Fig. 4** shows a 7 kV, 15 A turn-off transition together with the calculated power and the resulting switching energy, where t_0 denotes the beginning of the integration interval. As can be noted, due to the appearing oscillations in the power calculation, the determination of the integration interval's end is not clear any more. There are basically two reasonable possibilities to select this integration limit as denoted with t_A and t_B. t_A corresponds to the first zero crossing of the current and t_B is selected such that both, the HF and the LF oscillations have decayed. Accordingly, the obtained turn-off energies are $E_{off,A} = 2.83\,\text{mJ}$ and $E_{off,B} = 3.19\,\text{mJ}$, whereas the corresponding turn-on energy is $E_{on} = -2.45\,\text{mJ}$. The associated soft-switching losses are thus $E_{SW,A} = 380\,\mu\text{J}$ and $E_{SW,B} = 740\,\mu\text{J}$ which results in a relative soft-switching loss error of 48.6 % or 94.7 %, depending on which value is considered as the reference. Hence, the post-processing with the selection of the integration limits is very crucial and can lead to similar errors as obtained during the measurement procedure.

Since the impact of the skew, the offset/amplitude difference, the probe bandwidths and the selection of the integration limits on the measurement error is large and might all in all lead to switching loss errors which are higher than 200 % (although the assumed skew, offset and amplitude difference values are very small and fairly realistic), it is concluded that the double pulse measurement method is unsuitable for the measurement of soft-switching losses. Therefore, other measurement methods with improved accuracy have been developed in the recent years as will be shortly described in the following.

In [11], for example, the switching losses are measured electrically based on the energy conservation principle during one switching cycle. It is claimed that, in a buck-type circuit, the switching losses equal the difference between the energy supplied by the DC-link capacitor and the energy stored in the load inductor, i.e. input power minus output power of the bridge-leg. Thus, in contrast to the double pulse method, where a transient MOSFET current is multiplied with a transient MOSFET voltage, with the method proposed in [11], the input power is found by multiplying the MOSFET current with the constant DC-link voltage and the output power is calculated by multiplying the drain-source voltage of the MOSFET with the constant output current. Consequently, the skew between the measured MOSFET voltage and current transients is no longer a problem. Nevertheless, the remaining measurement errors as well as the integration problem still exist. Furthermore, the output current is only constant if hard-switching losses are measured; for the measurement of soft-switching losses, a triangular current waveform as shown in **Fig. 1 (b)** is needed.

In [12] and [13], switching losses have been measured based on the opposition method, where in contrast to the described pulsed measurements, a full-bridge is operated continuously with an inductive load. Similar to [11], the semiconductor losses are obtained by electrically measuring the DC input power and subtracting the calculated ohmic losses of the inductor based on the inductor's AC-resistance and the measured inductor current. Thus, the AC-resistance of the inductor has to be well-characterized in terms of its frequency and temperature dependency in order to achieve a sufficiently accurate measurement of the semiconductor losses. Beneficially, the inductor is realized as an air core inductor (without magnetic material) in order to not include additional errors due to core losses into the measurement. Furthermore, the pure switching losses are obtained by subtracting the conduction losses (calculated based on the on-state resistance $R_{DS,on}$) from the measured total semiconductor losses. However, as already mentioned, since the $R_{DS,on}$ shows a certain dependency on the temperature, current and current direction - especially for the examined 10 kV SiC MOSFETs - significant measurement errors can be introduced. Thus this method is not suitable for the underlying application.

For the sake of completeness, as a combination of electrical and calorimetric switching loss measurement methods, the inductor losses in the opposition method can also be measured

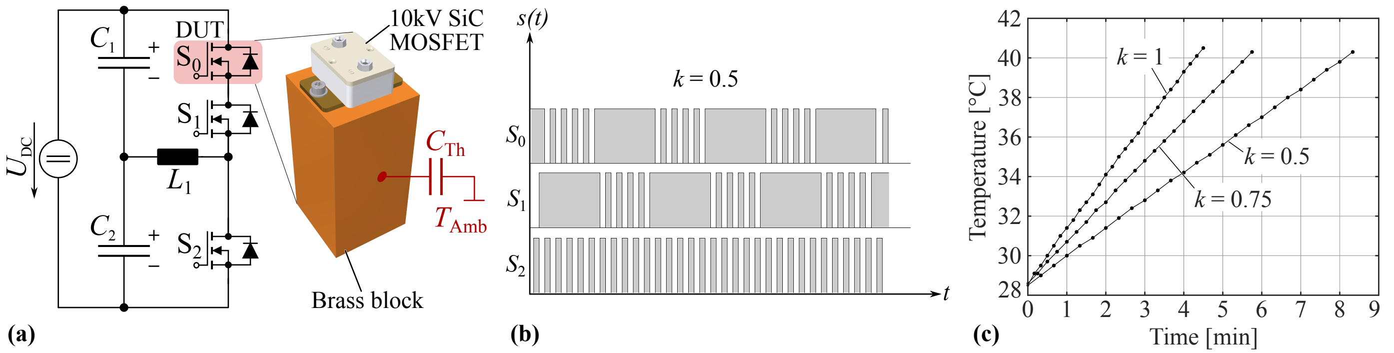


Fig. 5: (a) Circuit diagram with an additional MOSFET S_0 mounted on a brass block which acts as a thermal capacitance C_{Th}. **(b)** Gate signals of the three MOSFETs for the modified modulation scheme exemplary shown for a switching cycle share of $k = 0.5$. **(c)** Measured temperature curves for $U_{\mathrm{DC}} = 8\,\mathrm{kV}$, $i_{\mathrm{Switched}} = 7.5\,\mathrm{A}$ and different values of k.

calorimetrically [14]. On the one hand, this leads to more accurate results and on the other hand, a magnetic core material can be used. Nevertheless, the switching and conduction losses still have to be separated.

B. Calorimetric measurement methods

Instead of measuring the input and output power in a circuit, a more direct way of measuring switching losses is to exclusively measure the power dissipation of the switches in a calorimetric manner.

In [15], a half-bridge as part of a synchronous buck converter is operated continuously, whereby the two switches, their gate drivers and the DC-link capacitor are enclosed in a calorimeter in order to measure the power dissipation. In this method, the power dissipation of the gate drives (which are additionally measured electrically) have to be subtracted from the total power in the calorimeter in order to obtain the semiconductor losses. In [16], a similar calorimetric method is presented. Thereby, a metal block is attached to the switches of a half-bridge circuit which is continuously operated. The metal block acts as a thermal capacitance C_{Th} which is heated up by the dissipated power of the switches resulting in a certain temperature increase $\Delta\vartheta$. Based on the given thermal capacitance C_{Th} in combination with the time required to heat up the metal block, the dissipated power can be calculated. The advantage of this method is that the gate driver losses etc. do not influence the measurement due to the thermal decoupling. Still, the challenge for these methods is the separation of the conduction and switching losses.

In order to separate these losses directly in the measurement instead of calculating the conduction losses (with error-prone $R_{\mathrm{DS,on}}$ values) and subtracting them from the total semiconductor losses, a novel calorimetric soft-switching loss measurement method featuring a high accuracy is proposed in the following section.

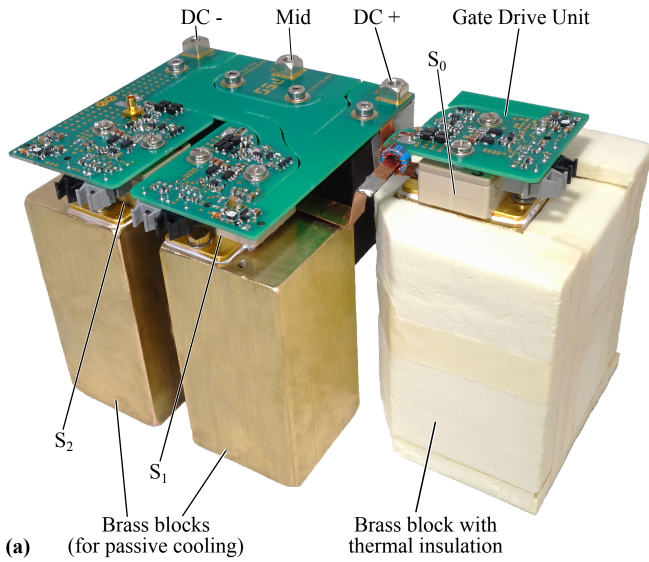
III. Functional Principle of the Proposed Measurement Method

The basic idea of the proposed method for the measurement of soft-switching losses is on the one hand to measure the semiconductor losses calorimetrically and on the other hand to measure switching and conduction losses separately. Therefore, as shown in **Fig. 5 (a)**, a third MOSFET S_0 has to be inserted in series to either the low-side switch S_2 or the high-side switch S_1. In the following it is assumed that S_0 is connected in series to the high-side switch S_1, since the cooling pad is connected to the drain potential of the MOSFET and thus in this configuration is fixed to a stable voltage. Furthermore, the MOSFET module S_0 is mounted on top of a $50 \times 50 \times 100\,\mathrm{mm}$ brass block, which absorbs the dissipated semiconductor losses and acts as a thermal capacitance C_{Th}. Brass is selected as heat sink material due to its high thermal capacitance per volume. In addition, the brass block is isolated with thermal insulation material in order to minimize the heat transfer to the ambient. Consequently, assuming a constant power dissipation in the semiconductor device S_0 (DUT), the temperature of the brass block linearly increases with time, whereas the temperature slope is proportional to the dissipated power of S_0. Hence, the power dissipation of S_0 can be calculated as

$$P = \frac{C_{\mathrm{Th}} \cdot \Delta\vartheta}{\Delta\tau}, \quad (1)$$

where $\Delta\vartheta$ denotes the temperature difference and $\Delta\tau$ equals the measurement time. Based on (1), the dissipated power of S_0 can be determined now by measuring the time which is required to heat up the insulated brass block from e.g. $30\,°\mathrm{C}$ to $40\,°\mathrm{C}$ while the system is continuously operated with a triangular inductor current, as already shown in **Fig. 1 (b)**. A picture of the corresponding $10\,\mathrm{kV}$ SiC hardware setup with the thermally insulated MOSFET is shown in **Fig. 6 (a)**. The reader should note that the MOSFETs S_1 and S_2 are also mounted on separate brass blocks instead of heat sinks in order not to influence the measured temperature of the insulated brass block with any air stream.

Now, in order to separate the switching and conduction losses, two different measurements M_1 and M_2 have to be performed at the same operating point, i.e. the same switched current. In the first measurement M_1, S_0 and S_2 are switching with a $50\,\%$ duty-cycle, while S_1 is always turned on. In this case, S_0 generates both, switching and conduction losses ($P_{\mathrm{S0}} = P_{\mathrm{Cond}} + P_{\mathrm{SW}}$), which is measured calorimetrically as described above. After the system has cooled down, in the second measurement M_2 the MOSFETs S_0 and S_1 swap their roles such that S_0 is now permanently on and S_1 is switching together with S_2 at exactly the same conditions as in the first measurement, i.e. equal switching frequency, dead time, inductance value and DC-link voltage. In this case, S_0 generates conduction losses only, namely exactly the same



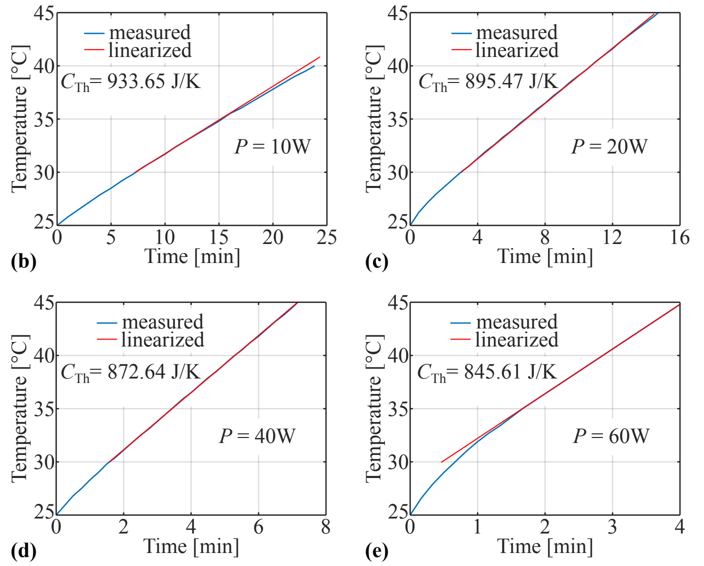


Fig. 6: **(a)**: 10 kV SiC half-bridge with the additional MOSFET S_0 on a thermally insulated brass block. **(b)-(e)**: Thermal calibration measurements at constant DC power levels, **(b)** 10 W, **(c)** 20 W, **(d)** 40 W, and **(e)** 60 W. Each temperature profile is linearized around the measurement temperature range and the corresponding thermal capacitance is calculated for the given slope. A high linearity can be achieved in the temperature range from 30 °C to 40 °C and the power range from 20 W to 40 W. Thus, all the switching loss measurements are carried out in this power and temperature range.

amount as before, if the dead time interval is neglected for the moment (i.e. $P_{\text{S0}} = P_{\text{Cond}}$). Subtracting the two measured powers from each other and dividing the difference by the switching frequency results in the net soft-switching losses of one switch. It should be noted that effects such as the dependency of the $R_{\text{DS,on}}$ on the drain current and the current direction don't influence the measured results due to the fact that both measurements are performed at the same conditions, i.e. exactly equal current waveforms, and thus cancel out when the two powers are subtracted. The only parameter which is slightly different in the two measurements is the average chip temperature. Although in both measurements the temperature range from 30 °C to 40 °C is equal, the thermal resistance R_{JB} between junction and brass block causes a slight difference of the chip temperature, because the power is not the same in the two measurements. However, assuming a thermal resistance of $R_{\text{JB}} = 0.5\,\text{K/W}$ (obtained from a finite element simulation) and a maximum power difference of around 20 W, the worst case chip temperature difference is 10 K which has a negligible effect on the conduction and the switching losses [17]–[19]. In order to keep this error small for all measured operating points, the power difference is limited to 20 W by adapting the switching frequency and the inductance value as well as utilizing a modified modulation scheme, as described below.

The problem of measuring only conduction losses is that for small switched currents the conduction losses are in the range of 1...2 W, whereby the optimum power range for the built setup is between 20 W and 40 W in order to keep the influence of the heat transfer to the ambient to a minimum and thus to still obtain a linear increase in temperature. In **Figs. 6 (b)-(e)**, the temperature profiles of the insulated brass block for different thermal calibration measurements at different power ratings are shown. For these calibration measurements, the same hardware configuration (including the copper busbar to the DC-link, the gate drive, etc.) is used and constant DC-power is fed into the MOSFET module, which is permanently turned-on, by driving a controlled current through the MOSFET such that the constant power levels of 10 W, 20 W, 40 W and 60 W are reached. It can be seen that the measurements for 20 W and 40 W are nicely linear between 30 °C and 40 °C, whereas for the 10 W measurement, the heat transfer to the ambient has a significant effect on the temperature profile because the steady state temperature of the thermally insulated brass block decreases with decreasing power dissipation which causes the temperature slope to flatten already at around 35 °C. On the other hand, the 60 W measurement suffers from a nonlinear behaviour in the lower temperature range due to certain effects of the heat propagation. Thus, all measurements are performed in the range of 20 W to 40 W. Furthermore, as indicated in the figure, the linearized thermal capacitance C_{Th} is not constant for the selected power range. Therefore, the thermal capacitance is interpolated iteratively from the calibration measurements for the purpose of obtaining the correct power dissipation.

In order to overcome the problem that the measurement M_2, in which only the conduction losses are measured, generates too low thermal power feed-in for the brass block to be operated in its linear region, the modulation scheme is modified as indicated in **Fig. 5 (b)**. Instead of permanently turning on S_0 in this measurement, S_0 and S_1 share the switching losses among each other. The share of the switching cycles which are actively switched by S_0 is defined as the switching cycle share k. A value of $k = 1$ means that S_0 is switching continuously while S_1 is permanently turned on. As an example, in **Fig. 5 (b)**, k is equal to 0.5 which means that both, S_0 and S_1 are actively switching 50 % of the switching cycles and are turned on for the other 50 % of the switching cycles. For practical reasons in the case of the 10 kV SiC MOSFETs, S_0 and S_1 are alternatingly switched for 100 cycles. Hence, with this modulation scheme, the dissipated power of S_0 can be brought into the mentioned power range of 20 W to 40 W resulting in a linear temperature

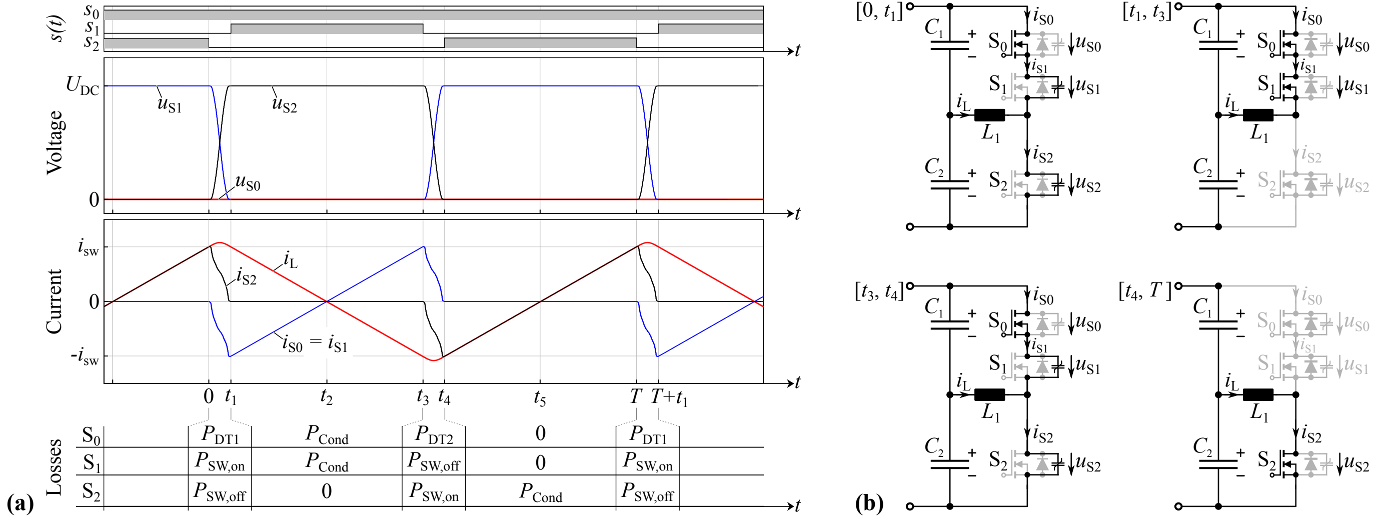


Fig. 7: (a) Current and voltage waveforms as well as the gate signals of the three switches and the corresponding share of losses in each time interval. **(b)** Schematic diagrams showing the current path during the specific time intervals. Shaded symbols do not conduct current.

profile. In **Fig. 5 (c)**, measured temperature profiles at $U_{\mathrm{DC}} = 8\,\mathrm{kV}$ and a switched current of $7.5\,\mathrm{A}$ (cf. **Fig. 1 (b)**) are shown for different values of k. As can be noticed, the measurements follow a linear characteristic which means that the thermal setup is operated in its linear region as desired. Furthermore, in **Fig. 7 (a)** the ideal (simulated) waveforms of the three switches, together with their gate signals and the power dissipation during the different time intervals are given. The shown section corresponds to a moment in time in which S_0 is turned on permanently whereas S_1 and S_2 are switching alternatingly. The switched current is chosen rather small in order to illustrate that the dead time interval, in which the output capacitances of the switches have to be charged/discharged, can occupy a significant share of a switching period. Actually, since S_0 is connected in series to S_1, S_0 should only generate conduction losses during the on-state interval of S_1. However, as shown in **Fig. 7 (b)** during the dead time intervals $[0, t_1]$ and $[t_3, t_4]$, the switched current of S_1, which flows through the nonlinear output capacitance of S_1, also flows through the MOSFET channel of S_0, generating additional conduction losses P_{DT1} and P_{DT2} in S_0. Due to the symmetric current excitation, the losses in both dead times are equal ($P_{\mathrm{DT1}} = P_{\mathrm{DT2}}$). As soon as S_0 and S_1 swap their roles, i.e. when S_0 is switching and S_1 is turned on, the current through both switches stays exactly the same with the difference that the switched current now flows through the nonlinear capacitance of S_0 instead of flowing through the MOSFET channel, generating switching losses $P_{\mathrm{SW,on}}$ and $P_{\mathrm{SW,off}}$, respectively. Averaging these losses over time and considering the switching cycle share k, the dissipated power of the MOSFET S_0 can be calculated as

$$\begin{aligned} P_{\mathrm{S0}} &= k\left(P_{\mathrm{SW}} + P_{\mathrm{Cond}}\right) + (1-k)\left(P_{\mathrm{DT}} + P_{\mathrm{Cond}}\right) \\ &= k \cdot P_{\mathrm{SW}} + P_{\mathrm{Cond}} + (1-k)\,P_{\mathrm{DT}}, \end{aligned} \tag{2}$$

where $P_{\mathrm{SW}} = P_{\mathrm{SW,on}} + P_{\mathrm{SW,off}}$ and $P_{\mathrm{DT}} = P_{\mathrm{DT1}} + P_{\mathrm{DT2}}$. In the first measurement M_1 where $k = 1$, the power dissipated in S_0 is

$$P_{\mathrm{M1}} = P_{\mathrm{S0}}\,(k=1) = P_{\mathrm{SW}} + P_{\mathrm{Cond}}. \tag{3}$$

In the second measurement M_2 where $k < 1$, the dissipated power in MOSFET S_0 is given as

$$\begin{aligned} P_{\mathrm{M2}} &= k \cdot P_{\mathrm{SW}} + P_{\mathrm{Cond}} + (1-k)\,P_{\mathrm{DT}} \\ &= k \cdot P_{\mathrm{M1}} + (1-k)\left(P_{\mathrm{Cond}} + P_{\mathrm{DT}}\right), \end{aligned} \tag{4}$$

whereby $P_{\mathrm{SW}} = P_{\mathrm{M1}} - P_{\mathrm{Cond}}$ is used. Since with $k > 0$ only two linear independent measurements M_1 and M_2 but three unknowns (P_{SW}, P_{Cond} and P_{DT}) exist, a further relation between P_{Cond} and P_{DT} is required in order to solve the system of equations consisting of (3) and (4). Therefore, it is assumed that the conduction losses during the dead time interval $[0, t_1]$ and the conduction interval $[t_1, t_2]$ (within one half-cycle (HC) $[0, t_2]$) arise from an ohmic behaviour of the MOSFET and can be described by $P_{\mathrm{ohm}} = R_{\mathrm{DS,on}} \cdot i^2$ if the dependency of the $R_{\mathrm{DS,on}}$ on the value and direction of the drain current is neglected at the moment (the resulting error is negligible as will be shown in the error analysis, since the current exhibits a similar and quasi triangular shape with equal peak value in both time intervals). Hence, based on the average conduction losses during the dead time and the conduction interval referred to one half-cycle, (cf. (5) and (6), respectively), the proportionality factor h_{P} of both contributions is introduced as additional equation, cf. (7).

$$P_{\mathrm{DT,HC}} = \frac{P_{\mathrm{DT}}}{2} = \frac{2}{T} \cdot \int_{0}^{t_1} R_{\mathrm{DS,on}} \cdot i_{\mathrm{S0}}^2 \cdot \mathrm{dt} \tag{5}$$

$$P_{\mathrm{Cond,HC}} = \frac{P_{\mathrm{Cond}}}{2} = \frac{2}{T} \cdot \int_{t_1}^{t_2} R_{\mathrm{DS,on}} \cdot i_{\mathrm{S0}}^2 \cdot \mathrm{dt} \tag{6}$$

$$h_{\mathrm{P}} = \frac{P_{\mathrm{DT,HC}}}{P_{\mathrm{Cond,HC}}} = \frac{\int_{0}^{t_1} i_{\mathrm{S0}}^2 \cdot \mathrm{dt}}{\int_{t_1}^{t_2} i_{\mathrm{S0}}^2 \cdot \mathrm{dt}} = \frac{P_{\mathrm{DT}}}{P_{\mathrm{Cond}}} \tag{7}$$

Due to the symmetry of the current i_{S0} within one switching cycle, the proportionality factor of one switching cycle remains the same as the one of a half-cycle, as indicated in (7). Since h_{P} is independent of the $R_{\mathrm{DS,on}}$ of the device, h_{P} can be

obtained by measuring the drain current and by solving the given integrals in (7). The system of equations can now be solved, whereby the conduction losses are given by

$$P_{\mathrm{Cond}} = \frac{P_{\mathrm{M2}} - k \cdot P_{\mathrm{M1}}}{1 - k + (1 - k) \cdot h_{\mathrm{P}}}, \tag{8}$$

and the dead time losses as well as the switching losses are calculated as

$$P_{\mathrm{DT}} = h_{\mathrm{P}} \cdot P_{\mathrm{Cond}} \quad \text{and} \tag{9}$$

$$P_{\mathrm{SW}} = P_{\mathrm{M1}} - P_{\mathrm{Cond}}, \tag{10}$$

respectively. Finally, the switching energy per MOSFET can be determined as

$$E_{\mathrm{SW}} = P_{\mathrm{SW}} / f_{\mathrm{SW}}. \tag{11}$$

It should be mentioned that for the soft-switching loss measurements of the $10\,\mathrm{kV}$ SiC MOSFETs, a switching cycle share of $k = 0.5$ has been chosen for the second and $k = 0.75$ for a third (verification) measurement, leading to stable and reproducible results.

IV. Discussion and Experimental Results

The following section analyzes the accuracy of the proposed soft-switching loss measurement method and discusses possible limitations and sources of measurement errors. Finally, the measured soft-switching losses are presented and discussed.

A. Error analysis for the proposed soft-switching loss measurement method

Although calorimetric measurements are probably the most direct and accurate way of measuring power dissipations, there are several effects that have to be considered in order to obtain accurate results. First of all, an accurate and EMI robust temperature measurement is required. Depending on the device package, the cooling terminal might be on drain potential of the MOSFET (which is the case for the $10\,\mathrm{kV}$ SiC MOSFETs at hand) such that the metal block including the temperature sensor is on (floating) potential and is possibly exposed to high $\mathrm{d}u/\mathrm{d}t$ values which could disturb the temperature measurement. Furthermore, the position of the temperature sensor on the metal block must not change between the calibration and the switching loss measurements. Otherwise, measurement errors could arise due to a possibly inhomogeneous temperature distribution within the metal block. Generally important for this measurement method is the thermal decoupling of the DUT and its brass block from the ambient (by applying thermal insulation material to the brass block) and especially from other heat sources contained in the hardware setup (such as the other switches) in order to prevent undesired heat transfers to the brass block. This is easily possible for the $10\,\mathrm{kV}$ SiC MOSFETs at hand due to the specific package design and the anyway required distances between the switch and other parts of the circuit for the reason of electrical isolation. For other device packages and especially lower voltage devices, however, the thermal decoupling of the DUT might be a problem since a thermal decoupling goes hand in hand with an increase of the commutation loop inductance which could lead to voltage overshoots and ringing. For the employed $10\,\mathrm{kV}$ devices operated with DC-link voltages in the kV-range, the voltage overshoot caused by the additional inductance of the third switch is negligible and not even measurable.

Since the measurement method includes a measurement of a rather small temperature difference $\Delta\vartheta$ of e.g. $10\,\mathrm{K}$, as in this case, the accuracy of the temperature measurement is the most critical parameter. Assuming a measurement error of $\Delta\vartheta = \pm 0.1\,\mathrm{K}$ (which corresponds to a relative error of $\pm 1\,\%$), a $\pm 2\,\%$ error in the thermal capacitance C_{Th} and a perfect time measurement (since time can be measured very precisely), the worst case error of a single power measurement is $\pm 3\,\%$ (cf. (1), $102\% \cdot 101\% \approx 103\%$). Hence, as a worst case estimation, if P_{M1} is measured $3\,\%$ too high and P_{M2} is measured $3\,\%$ too low, the relative errors in the switching losses are $5.8\,\%$ for the $7\,\mathrm{kV}$, $2.5\,\mathrm{A}$ case and $15.5\,\%$ for the $7\,\mathrm{kV}$, $15\,\mathrm{A}$ case, whereby measured values for P_{M1}, P_{M2} and h_{P} (cf. TABLE I) are inserted into equations (8) and (10) for the error analysis in order to give practical examples. Compared to the previously analyzed double pulse method, a 10 to 20 times higher accuracy can be achieved with the proposed calorimetric method. Furthermore, in all of the performed measurements, the $k = 0.5$ and the $k = 0.75$ (reference) measurements match within $5\,\%$ error which demonstrates that the worst case is not very likely to occur if the measurements are carried out carefully and indicates that the accuracy of the method is very high.

As can be noticed, the measurement error increases with increasing switched currents, thus the switching losses should hold the largest share of the overall measured power dissipation in order to keep the measurement accuracy high. This can be managed by choosing a rather high switching frequency, which however is limited by certain constraints such as the gate drive power capability, the total generated losses on the metal block (which might be too high and result in a nonlinear temperature profile at some point) or the fact that with higher switching frequencies the dead time interval consumes a major part of the overall switching cycle. Another (limited) possibility to increase the measurement accuracy is to increase the temperature difference $\Delta\vartheta$. However, the temperature dependency of the MOSFET properties might start playing a role for higher values of $\Delta\vartheta$. Furthermore, in the derivation of the switching losses from the two measurements M_1 and M_2, in equations (5)-(7) it is assumed that the on-state resistance $R_{\mathrm{DS,on}}$ is constant. As already mentioned, this is not true for the $10\,\mathrm{kV}$ SiC MOSFETs at hand since there is a dependency of the $R_{\mathrm{DS,on}}$ on temperature as well as on the direction and the value of the drain current. Hence, the $R_{\mathrm{DS,on}}$ doesn't cancel out in equation (7) and leads to a certain calculation error of h_{P}. However, the sensitivity of the soft-switching losses on calculation errors of h_{P} is very low. On the one hand, for low switched currents, the switching frequency is selected rather high (cf. TABLE I) in order to increase the switching losses until a total power dissipation between $20\,\mathrm{W}$ and $40\,\mathrm{W}$ is achieved on the brass block for the mentioned reasons. In this case, the dead time consumes a major part of the switching cycle ($h_{\mathrm{P}} \approx 1$), thus the corresponding losses P_{DT} are similar to the conduction losses P_{Cond} (cf. TABLE I). Due to the high switching frequency and the low current rating, however, the switching losses P_{SW} are orders of magnitudes higher than P_{DT} or P_{Cond}. Consequently, calculation errors of h_{P} hardly influence the switching losses. E.g. with the values given for the $7\,\mathrm{kV}$, $2.5\,\mathrm{A}$ measurement in TABLE I, the switching loss error stays below $0.012\,\%$, if for the determination of h_{P} a

TABLE I: Measured and calculated values for the case of low switched current ($7\,\mathrm{kV}$, $2.5\,\mathrm{A}$) and high switched current ($7\,\mathrm{kV}$, $15\,\mathrm{A}$).

Parameter	*Value for* $7\,\mathrm{kV}$, $2.5\,\mathrm{A}$	*Value for* $7\,\mathrm{kV}$, $15\,\mathrm{A}$
P_{M1}	37.50 W	38.54 W
P_{M2}	18.84 W	26.99 W
h_{P}	1.1883	0.0731
P_{Cond}	0.09 W	14.38 W
P_{SW}	37.41 W	24.16 W
P_{DT}	0.10 W	1.05 W
f_{SW}	200 kHz	100 kHz

calculation error of $\pm 10\%$ is assumed. On the other hand, for high switched currents, the charging/discharging of the MOSFET's output capacitances occurs much faster such that the dead time interval is short, i.e. $h_{\mathrm{P}} \approx 0$. Hence, errors in the calculation of h_{P} have an negligible impact on the switching losses. Assuming again an error of $\pm 10\%$ in h_{P}, for the case of $7\,\mathrm{kV}$, $15\,\mathrm{A}$ (cf. TABLE I), the switching loss error is below $0.41\,\%$. This demonstrates the superior numerical conditioning of the described measurement method and shows that the effect of errors in h_{P} on the switching loss measurement error is insignificant.

B. Measurement results

In order to cover a wide range of applications in which the analyzed $10\,\mathrm{kV}$ SiC MOSFETs could be utilized, soft-switching loss measurements have been performed for different DC-link voltages, currents and gate resistors.

Fig. 8 shows the net measured switching losses of the $10\,\mathrm{kV}$ SiC MOSFETs for DC-link voltages between $4\,\mathrm{kV}$ and $8\,\mathrm{kV}$ and switched currents between $2.5\,\mathrm{A}$ and $15\,\mathrm{A}$. Unless otherwise noted, the gate resistors are $R_{\mathrm{on}} = 20\,\Omega$ and $R_{\mathrm{off}} = 10\,\Omega$. It is clearly visible that the soft-switching losses are mainly depending on the DC-link voltage. The dependency of the soft-switching losses on the switched current is quasi linear with a rather flat and voltage-independent slope. It is also interesting that the switching loss curves would not cross the origin if they were extrapolated towards zero current. Instead,

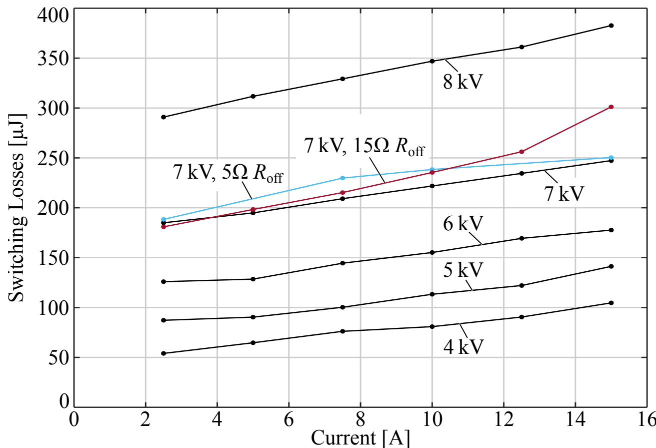


Fig. 8: Calorimetrically measured soft-switching losses of the $10\,\mathrm{kV}$ SiC MOSFETs for different DC-link voltages, switched currents and gate resistors. Unless otherwise noted, the turn-off gate resistor is $R_{\mathrm{off}} = 10\,\Omega$.

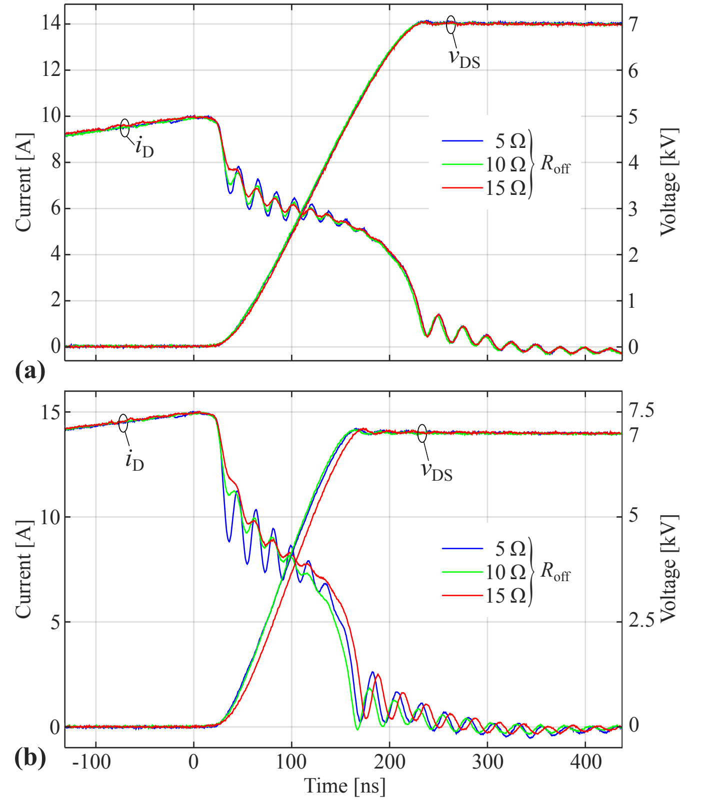


Fig. 9: Comparison of switching transitions for different turn-off gate resistors at $U_{\mathrm{DC}} = 7\,\mathrm{kV}$ for **(a)** $i_{\mathrm{Switched}} = 10\,\mathrm{A}$ and **(b)** $i_{\mathrm{Switched}} = 15\,\mathrm{A}$.

the curves would show an offset even for very low currents which means that there are voltage-dependent residual soft-switching losses which cannot be avoided. Future work will analyze the source of these residual soft-switching losses in more detail in order to gain a better understanding of the underlying loss mechanisms. Compared to the hard-switching operation of these $10\,\mathrm{kV}$ SiC MOSFETs, cf. [20], factor 100 lower switching losses can be achieved by applying soft-switching techniques which allows for much higher switching frequencies, efficiencies and power densities. Comparing the three $7\,\mathrm{kV}$ curves with different turn-off gate resistors R_{off} in **Fig. 8**, it is evident that a turn-off resistor of $R_{\mathrm{off}} = 10\,\Omega$ leads to the lowest soft-switching losses. The reader should note that the turn-on resistor does not or hardly influence the soft-switching losses. For the case of $R_{\mathrm{off}} = 15\,\Omega$, the dependency on the switched current shows a clear trend towards higher losses for higher switched currents which is an indication for increased channel losses due to a larger overlapping of the voltage and current transients during turn-off. This behaviour can be explained by analyzing the switching transitions given in **Fig. 9 (a)** for $7\,\mathrm{kV}$, $10\,\mathrm{A}$ and in **Fig. 9 (b)** for $7\,\mathrm{kV}$, $15\,\mathrm{A}$. While at $10\,\mathrm{A}$ all turn-off gate resistance values R_{off} result in the same voltage slope, the turn-off transition at $15\,\mathrm{A}$ is clearly slowed down in the beginning if a turn-off gate resistance of $R_{\mathrm{off}} = 15\,\Omega$ is used. Hence, at higher switched currents, the higher gate resistor leads to a stronger overlapping of the MOSFET voltage and channel current transients and thus to higher switching losses. On the other hand, a low turn-off gate resistance of $5\,\Omega$ results in stronger oscillations in the drain current due to parasitic inductances introduced by the

semiconductor packaging and thus cause higher soft-switching losses. Consequently, for the $10\,\mathrm{kV}$ SiC MOSFETs at hand, the optimal turn-off gate resistance is $R_{\mathrm{off}} = 10\,\Omega$, which could be probably slightly decreased if another package with lower parasitic inductances and/or with Kelvin source connection is used. However, even though the packaging can be improved, a substantial reduction of the soft-switching losses is not expected.

V. Conclusion

In this paper, an accurate calorimetric method for the measurement of soft-switching losses of $10\,\mathrm{kV}$ SiC MOSFETs is presented. It is shown that electrical measurement methods such as the double pulse test can lead to large measurement errors and thus are unsuitable for the characterization of the utilized $10\,\mathrm{kV}$ SiC MOSFETs and other fast-switching devices. On the other hand, with calorimetric measurement methods, the total semiconductor losses can be measured accurately. However, the calorimetric methods known up to now are not able to separate the switching losses from the conduction losses without calculations which could result again in certain measurement errors. Therefore, in this paper a novel calorimetric measurement method is proposed which eliminates this disadvantage. The proposed method introduces an additional switch into the well-known double pulse circuit which in combination with a novel modulation scheme enables to measure the conduction and switching losses separately with a high accuracy. The error analysis for the proposed measurement method shows that the worst case error is $15\,\%$ which is a factor 10 to 20 times more accurate than the accuracy obtained with the double pulse method. Based on the proposed measurement method, the soft-switching losses of the examined $10\,\mathrm{kV}$ SiC MOSFETs for different DC-link voltages, switched currents and gate resistors are presented and analyzed. Compared to the hard-switching losses of these $10\,\mathrm{kV}$ SiC MOSFETs, the soft-switching losses are around 100 times lower which allows for a higher system performance. However, the soft-switching losses are still relevant and have to be considered in the converter design, especially for applications utilizing high switching frequencies. In future work, the soft-switching losses of the $10\,\mathrm{kV}$ SiC MOSFETs will be analyzed further in order to figure out the underlying loss mechanisms.

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References

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics, Chapter 20: Soft Switching*, 2nd ed., 2001.

[2] A. Safaee, P. Jain, and A. Bakhshai, "A ZVS Pulsewidth Modulation Full-Bridge Converter With a Low-RMS-Current Resonant Auxiliary Circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4031–4047, 2016.

[3] A. Anurag, S. Bal, and B. Chitti Babu, "A Detailed Comparative Analysis between two Soft Switching Techniques used in PV Applications," in *Proc. IEEE India Int. Conf. (INDICON)*, Kochi, India, 2012, pp. 1234–1239.

[4] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, 2014.

[5] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$ -Pareto Optimization and Comparative Evaluation of Inverter Concepts considered for the GOOGLE Little Box Challenge," in *Proc. IEEE Workshop on Control and Model. of Power Electron. (COMPEL)*, Trondheim, 2016.

[6] R. Callanan, A. Agarwal, A. Burk, M. Das, B. Hull, F. Husna, A. Powell, and J. Richmond, "Recent Progress in SiC DMOSFETs and JBS Diodes at Cree," in *Ann. Conf. of the IEEE Ind. Electron. Society (IECON)*, Orlando, 2008, pp. 2885–2890.

[7] D. Han, J. Noppakunkajorn, and B. Sarlioglu, "Efficiency Comparison of SiC and Si-Based Bidirectional DC-DC Converters," in *Proc. IEEE Transportation Electrification Conference and Expo (ITEC)*, Detroit, 2013.

[8] O. Deblecker, Z. De Greve, and C. Versele, "Evaluation of Power Loss and Mass Gains of SiC versus Si-Based Switch-Mode Power Supplies using a Multiobjective Optimization CAD Tool," in *Proc. Int. Symposium on Power Electron., El. Drives, Automation and Motion (SPEEDAM)*, Ischia, Italy, 2014, pp. 43–49.

[9] R. M. Burkart and J. W. Kolar, "Comparative Evaluation of SiC and Si PV Inverter Systems Based on Power Density and Efficiency as Indicators of Initial Cost and Operating Revenue," in *Proc. IEEE Workshop on Control and Model. for Power Electronics (COMPEL)*, Salt Lake City, 2013.

[10] D. Rothmund, G. Ortiz, T. Guillod, and J. W. Kolar, "10kV SiC-Based Isolated DC-DC Converter for Medium Voltage-Connected Solid-State Transformers," in *Proc. IEEE Appl. Power Electronics Conf. (APEC)*, Charlotte, USA, 2015.

[11] Z. Zhang, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, Z. Liang, and P. Ning, "Methodology for Switching Characterization Evaluation of Wide Band-gap Devices in a Phase-leg Configuration," in *Proc. IEEE Appl. Power Electron. Conf. and Expo. (APEC)*, Fort Worth, 2014, pp. 2534–2541.

[12] J. Brandelero, B. Cougo, T. Meynard, and N. Videau, "A Non-Intrusive Method for Measuring Switching Losses of GaN Power Transistors," in *Ann. Conf. of the IEEE Ind. Electron. Society (IECON)*, Vienna, 2013, pp. 246–251.

[13] B. Cougo, H. Schneider, and T. Meynard, "Accurate Switching Energy Estimation of Wide Bandgap Devices used in Converters for Aircraft Applications," in *Proc. European Conf. on Power Electron. and Appl. (EPE)*, Lille, 2013.

[14] D. Bortis, O. Knecht, D. Neumayr, and J. W. Kolar, "Comprehensive Evaluation of GaN GIT in Low- and High-Frequency Bridge Leg Applications," in *Proc. Int. Power Electron. and Motion Control Conf. (IPEMC)*, Hefei, China, 2016.

[15] A. Tüysüz, R. Bosshard, and J. W. Kolar, "Performance Comparison of a GaN GIT and a Si IGBT for High-Speed Drive Applications," in *Proc. Int. Power Electron. Conf. (ECCE Asia)*, Hiroshima, 2014, pp. 1904–1911.

[16] L. Hoffmann, C. Gautier, S. Lefebvre, and F. Costa, "Optimization of the Driver of GaN Power Transistors Through Measurement of Their Thermal Behavior," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2359–2366, 2014.

[17] J. Thoma, D. Chilachava, and D. Kranzer, "A Highly Efficient DC-DC-Converter for Medium-Voltage Applications," in *Proc. IEEE Int. Energy Conf. (ENERGYCON)*, Dubrovnik, Croatia, 2014, pp. 140–144.

[18] K. Vechalapu, S. Bhattacharya, E. V. Brunt, S.-h. Ryu, and D. Grider, "Comparative Evaluation of 15 kV SiC MOSFET and 15 kV SiC IGBT for Medium Voltage Converter under Same dv / dt Conditions," in *Proc. IEEE Energy Conversion Congr. and Expo. (ECCE)*, Montreal, Canada, 2015, pp. 927–934.

[19] S. Madhusoodhanan, K. Mainali, A. Tripathi, K. Vechalapu, and S. Bhattacharya, "Medium Voltage (2.3 kV) High Frequency Three-Phase Two-Level Converter Design and Demonstration using 10 kV SiC MOSFETs for High Speed Motor Drive Applications," in *Proc. IEEE Appl. Power Electron. Conf. and Expo. (APEC)*, Long Beach, USA, 2016, pp. 1497–1504.

[20] J. B. Casady, E. V. Brunt, G.-y. Wang, J. Richmond, S. T. Allen, and D. Grider, "New Generation 10kV SiC Power MOSFET and Diodes for Industrial Applications," in *Proc. Conf. on Power Conversion and Intelligent Motion (PCIM)*, Nuremberg, 2015, pp. 96–103.