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Comparative Life Cycle Cost Analysis of Si and SiC PV Converter Systems Based on Advanced η-ρ-σ Multiobjective Optimization Techniques

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***Abstract*—This paper presents a novel virtual prototyping routine for power electronic converter systems. The approach facilitates a comprehensive and systematic benchmarking of different converter concepts based on a multiobjective optimization regarding the efficiency, power density, and costs. The underlying modeling framework is based on detailed and experimentally verified models. In particular, novel cost data as well as unpublished switching loss and core loss measurements are incorporated. The proposed virtual prototyping routine is employed to carry out a comparative study of the potential of Si and SiC semiconductors in a 10-kW residential three-phase photovoltaic inverter application. For this purpose, a state-of-the-art hard-switched three-level Si insulated-gate bipolar transistor (IGBT) system is compared to a hard-switched and to a soft-switched two-level SiC MOSFET system. The candidate systems for each concept are selected among the η-ρ-σ Pareto-optimized designs based on the life cycle costs. The hard-switched two-level SiC candidate system is found to be the most attractive solution featuring the lowest life cycle costs. When compared to the Si-based candidate system, not only a better power density and efficiency result. At the same time, besides the lower life cycle costs (-22%), lower component costs (-5%) can also be attained. The attractiveness of the found SiC solution is underlined by the simple control and the lowest component count among all concepts.**

***Index Terms*—Costs, dc–ac power conversion, life cycle costing, optimization methods, photovoltaic (PV) power systems, software prototyping.**

I. Introduction

In the course of a rapidly emerging market during the 1990s and 2000s, photovoltaic (PV) converter systems saw an unprecedented increase of the conversion efficiency from below 90 % to above 98% [1]–[4]. After several downturns of the global economy and a slower growth of the market in recent years, cost reduction has now become the dominant driver for PV converter systems [2], [4]–[6]. Against this background, there has been an ongoing discussion in the literature [3], [4], [6]–[13] on whether and how the introduction of SiC transistors can contribute to further improvements of PV converters and most notably toward lower costs. Although the advantages of SiC- over standard Si-based devices have unanimously been found to be the significantly decreased switching and conduction losses, divergent opinions exist on how to exploit these best. For typical residential grid-tied three-phase applications as depicted in Fig. 1, the authors of [3] and [7] propose to substitute the Si transistors of given converter systems by SiC without modifying the switching frequency and power density. It is argued that the improved efficiency allows for a higher operational revenue as a result of the increased grid feed-in. In contrast, the authors of [6], [8], and [9] mainly strive for increased power densities by means of higher switching frequencies facilitated by SiC. This strategy aims at lowering the overall component and system deployment costs. A mixed strategy of simultaneously increasing the power density and efficiency was pursued for the converter systems in [4] and [10]. Finally, the authors of [6], [9], and [11]–[13] point out that contrary to Si, the availability of SiC renders alternative topologies and modulation schemes attractive which offers further opportunities to lower the system costs in PV.

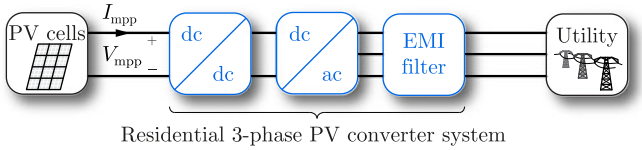

Fig. 1. Typical architecture of a residential PV converter system in a grid-tied three-phase application. The system consists of a dc/dc boost converter stage, a dc/ac inverter stage, and an EMI filter. The main specifications as considered in this paper are listed in Table I.

TABLE I
Main Specifications of the Three-Phase PV Converter System

Rated power	P_{r}	10 kW
Input voltage range	$[V_{\mathrm{mpp,min}}, V_{\mathrm{mpp,max}}]$	[400, 800] V
Maximum input current	$I_{\mathrm{mpp,max}}$	22.5 A
Peak grid voltage @ $f_{\mathrm{g}} = 50$ Hz	$\hat{V}_{\mathrm{g}}$	$(325 \pm 10\%)$ V

This paper makes three main contributions to the discussion outlined above.

- *Detailed quantitative cost analysis:* A large majority of the above cited papers [3], [4], [6]–[11], [13] discuss the cost-saving potential of SiC with qualitative considerations and/or relative cost data. Only paper [12] provides selected absolute component cost data, whereas [14] (single-phase systems) restricts itself to stating the overall system costs.

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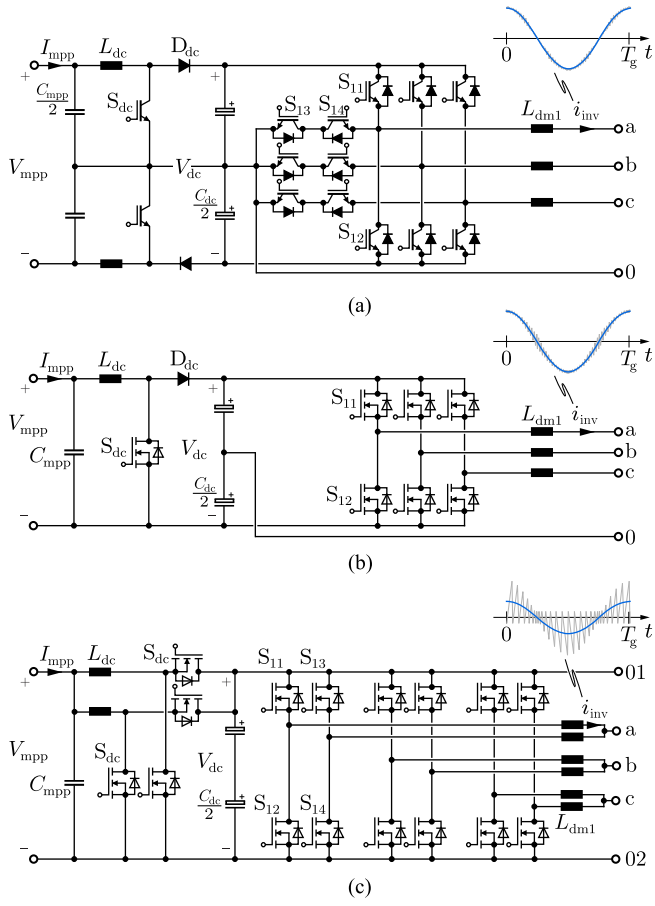

Fig. 2. Investigated combinations of dc/dc and dc/ac converter stages, modulation schemes, and semiconductor technologies for the grid-tied PV converter system in Fig. 1. (a) All Si IGBT hard-switched PWM-modulated three-level topology with a symmetric boost converter stage (3LPWM). (b) All SiC MOSFET hard-switched PWM-modulated two-level topology with a standard boost converter stage (2LPWM). (c) All SiC MOSFET soft-switched triangular current mode-modulated (TCM) double-interleaved two-level topology with a double-interleaved TCM boost converter stage (2LTCM).

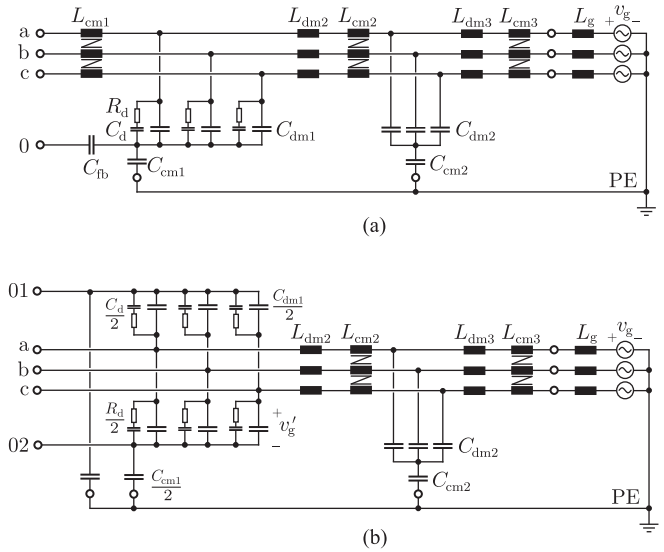

Fig. 3. Two-stage EMI filter topologies with connection to the grounded public 50-Hz mains grid. (a) EMI filter stage of the 2LPWM and 3LPMW topologies [cf., Fig. 2(a) and (b)]. The employed CM inductor L_{cm1} in conjunction with the feedback capacitor C_{fb} largely suppresses any CM currents. (b) EMI filter stage of the 2LTCM [cf., Fig. 2(c)]. The DM filter capacitors C_{dm1} are directly connected to the converter rails and no common mode inductor is employed. This allows for a largely decoupled TCM modulation of each phase.

In contrast, a main objective of this paper is the presentation of a detailed quantitative rather than qualitative cost analysis. Both the component hardware costs and the system life cycle costs (LCC) are calculated in a comprehensive way. Cost models for each component are proposed, where numerical values for the parameters, i.e., the cost data, are provided in detail.

- *Systematic multiobjective optimization:* The consideration of mere costs results in an incomplete picture, as other performance measures such as the efficiency or the power density are usually important as well. Moreover, a less significant comparison of Si versus SiC is attained if nonoptimized and incomplete systems (e.g., no electromagnetic interference (EMI) filter) are considered. The study in this paper is based on the Si and SiC converter topologies of Fig. 2, which include the EMI filters of Fig. 3. The performance comparison between the systems is exclusively based on designs that are obtained from a systematic and comprehensive multiobjective optimization regarding the efficiency, power density, and costs. This approach is in stark contrast to the previously cited literature in which largely systems without obvious optimization are compared. Exceptions are [13] and [14], in which, however, only a single performance measure is optimized. Eventually, [7]–[9] do not mention the consideration of an EMI filter.
- *Novel virtual prototyping routine:* In order to conduct the above-described comparative analysis of the potential of Si and SiC in PV, a novel virtual prototyping routine is proposed in this paper. It enables the systematic multiobjective optimization of entire converter systems involving a large number of design variables. The underlying modeling framework is based on comprehensive experimentally verified multiphysics and quantitative cost models, where partially unpublished model parameters are employed.

This paper is organized as follows. Sections II and III present the novel virtual prototyping routine and its models, which form the key element of this comparative study. Section IV reverts to the main topic of this paper and discusses the selection of the investigated Si- and SiC-based converter topologies, their modulation schemes, and components. In Section V, the multiobjective optimization of the selected topologies is performed using the proposed virtual prototyping routine. The obtained results are summarized and discussed. Finally, Section VI conducts the LCC analysis and determines the optimal candidate system for the application in Fig. 1.

II. Novel Virtual Prototyping Routine

This section presents the proposed novel virtual prototyping routine as employed in this paper. The first two parts of this section focus on its methodology and implementation, whereas the last part highlights the novelties and differences to existing approaches.

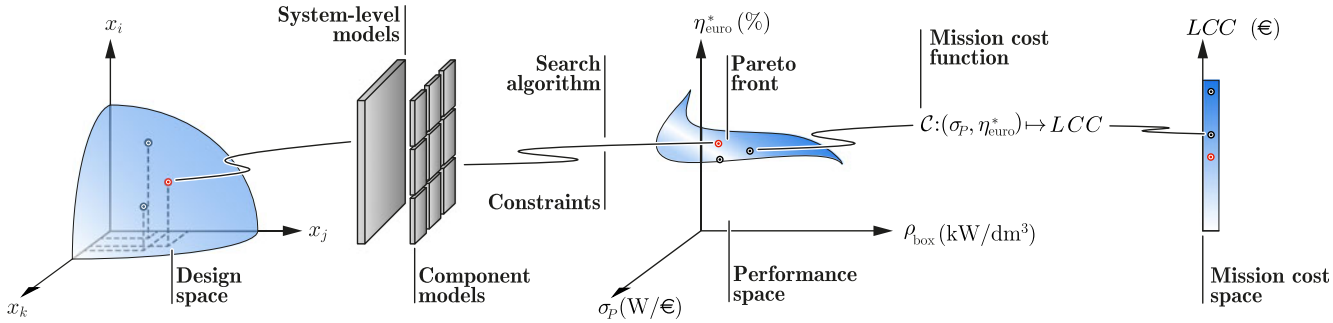

Fig. 4. Conceptual visualization of the proposed multiobjective optimization-based virtual prototyping routine. Mathematical system and component models are used to map different converter designs from the design space into the performance space by means of calculating their efficiency η^*_{euro}, boxed volume ρ_{box}, and specific costs σ_P. A suitable search algorithm identifies the Pareto front comprising the designs that offer the best possible performance tradeoffs. A cost function $\mathcal{C}(\eta^*_{\text{euro}}, \sigma_P)$ is employed to select the candidate system (marked red) that achieves the lowest LCC.

A. Methodology

The design of a power electronic converter system entails the specification of a vast number of different design variables. Typical variables may include the topology, the modulation scheme, the component values (e.g., inductance values), materials, and geometries. The possible combinations of design variable values form the set of available converter designs, which is referred to here as the design space. Usually, the converter design goal is the identification of those designs in the design space that achieve the highest performance while complying with the specifications and constraints. For this purpose, a systematic multiobjective optimization-based virtual prototyping routine is proposed here. The routine is conceptually visualized in Fig. 4. The core of the routine is formed by a large number of mathematical system-level and component models that describe the converter behavior and the component characteristics, respectively, and thus enable the calculation of the performance of each design in the design space. In this paper, the converter performance is defined by the triplet of the weighted efficiency η^*_{euro}, the power density ρ_{box}, and the specific component costs σ_P. Combining the models with a suitable multiobjective search algorithm then allows us to identify the Pareto front, i.e., the set of designs that offer the best possible tradeoffs between η^*_{euro}, ρ_{box}, and σ_P. The resulting Pareto front usually comprises a large number of system designs which all represent a compromise between the chosen performance measures. In order to arrive at a single candidate system, it is, therefore, proposed to assign each system of the Pareto front a single key figure as a function of its performance, $\mathcal{C} : (\eta^*_{\text{euro}}, \rho_{\text{box}}, \sigma_{\text{P}}) \mapsto \mathbb{R}$. Here, the mission cost function $\mathcal{C}$ may represent the (arbitrary) preferences of the design engineer. The candidate design is then found in a straightforward manner by selecting the system that achieves the best key figure value (cf., Fig. 4). In this paper, a mission cost function estimating the LCC depending on the efficiency η^*_{euro} and the component costs $\Sigma_{\text{tot}} = \sigma_P \cdot P_{\text{r}}$ is proposed. The advantage of this multiobjective two-step optimization approach in contrast to a conventional single-objective approach is twofold: on the one hand, the Pareto front is obtained, which provides valuable insight of the design tradeoffs. On the other hand, the design engineer's preferences of how to select the candidate system, i.e., the mission cost function $\mathcal{C}$, can be easily modified without reexecuting the time-consuming optimization step.

This section proceeds with a more in-depth description of the optimization routine, whereas the calculation of the LCC is detailed in Section VI.

B. Optimization Scheme

The multiobjective optimization scheme, i.e., the mapping of the design into the performance space and the search of the Pareto front (cf., Fig. 4) can be represented by the flowchart in Fig. 5. The required inputs are the design variables, constraints (cf., Section V), system specifications (cf., Table I), and the component and material database (cf., Section IV). The output is the set of Pareto-optimal system designs $\mathcal{D}_{\text{PV}}$.

1) Problem Simplification: The proposed optimization routine distinguishes the following two distinct categories of design variables:

i) Global design variables $\vec{\Pi}_{\text{glo}}$, which influence the waveforms, that is, the converter topology, the modulation scheme, as well as inductance and capacitance values.

ii) Groups of component-related local variables featuring no impact on the waveforms. That is:
- the semiconductor and cooling system design variables $\vec{\Pi}_{\text{SC}}$ (type of semiconductors, sink dimensions, # and type of fans);
- the dimensions and materials $\vec{\Pi}_L$ of each magnetic component (e.g., # and type of cores, # of turns, turn and strand diameter);
- the implementation $\vec{\Pi}_C$ (# and type) of each capacitor.

This distinction of the design variables enables an optimization approach as shown in Fig. 5. Here, the category i) variables are iterated in an outer system-level loop, where for each iteration, a new set of converter waveforms is calculated. Note that the EMI filter component values are not iterated as independent variables but chosen as dependent parameters by means of the filter design routine (cf., Section III). Based on the calculated waveforms, the components are independently designed in the respective inner component-level loops that

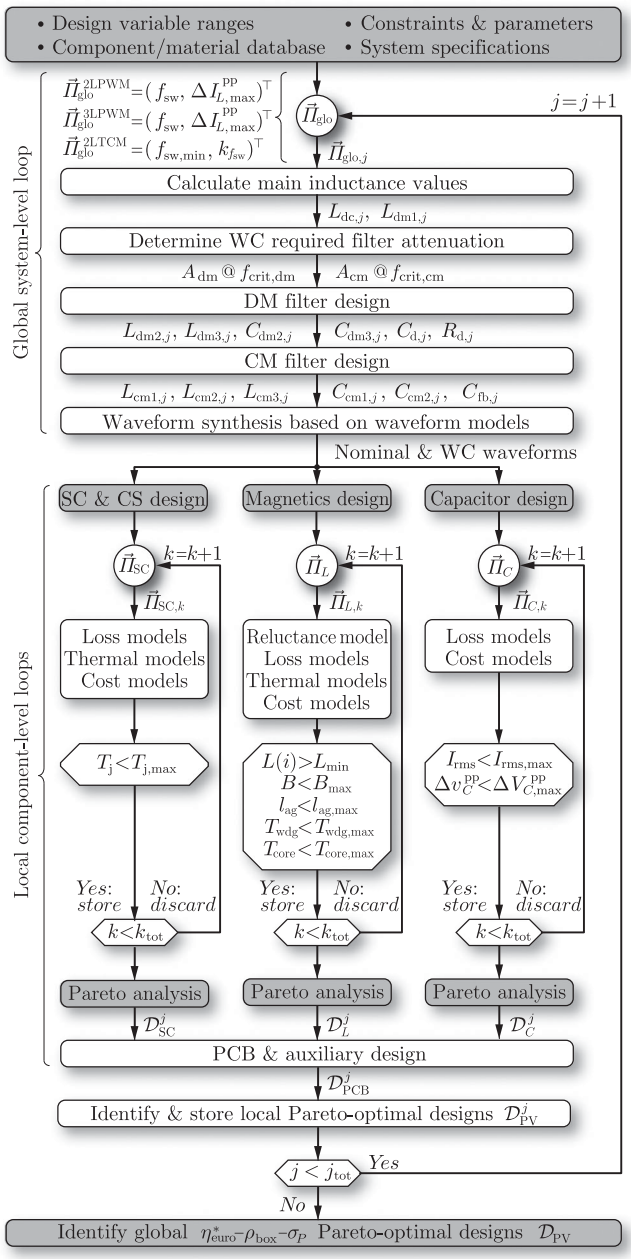

Fig. 5. Simplified flowchart of the multiobjective optimization scheme, i.e., the mapping of the design into the performance space and the search of the Pareto front as depicted in Fig. 4. For the definition of the symbols of the outer system-level loop, refer to Figs. 2 and 3 and Section V. The constraints employed for the semiconductor (SC), cooling system (CS), magnetics, and capacitor design are specified in Table VI. Note that the magnetics and capacitor design routines are executed for each individual inductor/capacitor.

iterate the corresponding category ii) variables. The main advantage of this conceptual approach is the dramatic reduction of the optimization complexity: instead of iterating all design variables in a single loop, a significant part of the problem, i.e., the specification of all component-related design variables, can be split into independent subproblems. The main drawback of this approach is the required assumption of ideal, i.e., lossless components without stray capacitances/inductances in the waveform synthesis as well as the neglect of parasitic electromagnetic and thermal coupling effects between the components. The resulting loss of accuracy is, however, tolerable as the efficiencies of PV converter systems are generally high, whereas the system layout normally aims at low parasitics.

2) Search Algorithm: The search algorithm is partly defined by the introduced loop architecture. For each iteration j of the outer system-level loop, the components are individually optimized. This is achieved by first executing the respective multiphysics models (e.g., the loss model; cf., Fig. 5) for a given design option. If the particular design $\vec{\Pi}_{X,k}$, $X \in \{\mathrm{SC}, L, C\}$ complies with the (user-defined) constraints (e.g., the maximum flux density $B_{\max}$), it is stored and otherwise discarded. After the iteration over all k_{tot} design options, a Pareto analysis is performed, where only the η^*_{euro}-ρ_{box}-σ_P Pareto-optimal options $\mathcal{D}^j_X$ are kept since nonoptimal components will never be part of an optimal overall system. In a next step, the locally (i.e., within the iteration j of the outer loop) Pareto-optimal system designs $\mathcal{D}^j_{\mathrm{PV}}$ as combinations of the components $\mathcal{D}^j_X$ are identified and stored. Finally, after the iteration of all j_{tot} system design variable options $\vec{\Pi}_{\mathrm{glo},j}$, the globally Pareto-optimal designs $\mathcal{D}_{\mathrm{PV}}$, i.e., the Pareto front is identified among the union set of locally optimal designs $\bigcup_j \mathcal{D}^j_{\mathrm{PV}}$. Note that the main benefit of the described multistep Pareto search compared to a single overall search at the end of the routine is the tremendously reduced computation time.

In contrast to a mere brute-force search, the proposed search algorithm is intelligent. It incorporates a range of additional heuristics that enable a reduction of the number of designs to be analyzed while finding the global optima is still guaranteed. This is attained by exploiting physical relationships and insight of the employed models. Two examples are given below.

- *Cooling system design:* Beyond a certain length of the heat sink (otherwise unchanged geometries and fixed fan), no further reduction of the thermal resistance can be expected due to the increasing pressure drop [15]. If this critical length is found during the optimization, longer heat sink designs can be safely ignored as they will not result in Pareto-optimal designs.
- *Magnetics design:* If a core with a given magnetic cross section cannot satisfy the maximum flux density constraint $B_{\max}$, cores with an even lower cross section will not result in a valid solution either and can thus be ignored (assumed are a fixed inductance and a maximum permissible air gap length) [16].

3) Software Implementation: The presented virtual prototyping routine is largely implemented in MATLAB. The code encompasses approximately 15 000 lines, of which 60 % is dedicated to the magnetics design. MATLAB was chosen mainly because of its broad diversity of in-built numerical methods and powerful options of organizing and handling complex data structures. Several strategies are pursued to further increase the execution speed:

- parallel computing and computationally inexpensive code is employed whenever applicable;
- embedded C code which can be up to a factor of 1000 faster than MATLAB code is used for simple and

repetitive tasks, e.g., the identification of the Pareto-optimal components and designs;
- contrary to the simplified illustration in Fig. 5, a particular component design $\vec{\Pi}_{X,k}$ can often be prematurely discarded without executing all models. For example, in the magnetics design routine, the satisfaction of the maximum flux density constraint $B_{\max}$ only requires the execution of the reluctance model and can thus be checked at an early stage.

C. Comparison to Existing Approaches

Using multiobjective optimization in virtual prototyping of power electronics converter systems is a relatively young research field. The theoretical concept was first proposed in [17] in 2010, whereas practical implementations can be found in [18]–[30]. The proposed virtual prototyping routine in this work differs to each of these contributions regarding at least one of the following aspects.

1) Performance Measures: The large majority of contributions considers two performance measures. [29]–[31] are the only exceptions considering three objectives as in this work.

2) Modeling Detail: The virtual prototyping routine of this paper employs a highly detailed modeling framework, which is largely based on experimentally verified parameters (cf., Section III). Several important differences to other contributions can be identified: contrary to [19], [23], [25], and [29], the temperature dependence of the semiconductor losses is considered in the models. Unlike [18], [22], [24], [27], and [29]–[31] that use data sheet information, the switching loss parameters are obtained based on extensive measurements. Furthermore, the impact of the core temperature and dc flux bias on the core losses is taken into account in this work while being neglected in [18], [22]–[27], and [29]–[31]. Finally, papers [26], [27], [29], and [31] miss to state the numerical values or origin of their cost model parameters, whereas this work explicitly provides all required values for the proposed cost models in detail.

3) Methodology: The author of [18], [22], [24], [27], and [29]–[31] employ metaheuristic evolutionary search algorithms in the optimization. Due to their stochastic nature, the found solutions are nondeterministic and thus usually only an approximation of the global solution. This is in stark contrast to the search algorithm employed in this work, which is based on systematic enumeration of all possible candidates and problem-specific heuristics to *a priori* reduce the number of candidates. This approach guarantees finding the global optima in a deterministic manner. Furthermore, no contribution could be found, which proposes how to systematically select a candidate system from the obtained Pareto front. In this paper, a selection of the candidate system based on the minimum achievable LCC is proposed (cf., Section VI).

4) Problem Complexity and Execution Speed: The virtual prototyping routine of this work can handle complex optimization problems encompassing 48 design variables. The problem of this work was solved within 15–20 h by means of a standard workstation (2 × 2.4 GHz Intel XEON quad-core CPUs, 64 GB of RAM). Contrarily, only a few contributions state the number of design variables (varying between 7 and 28). No information on the execution speeds or employed computational means could be found.

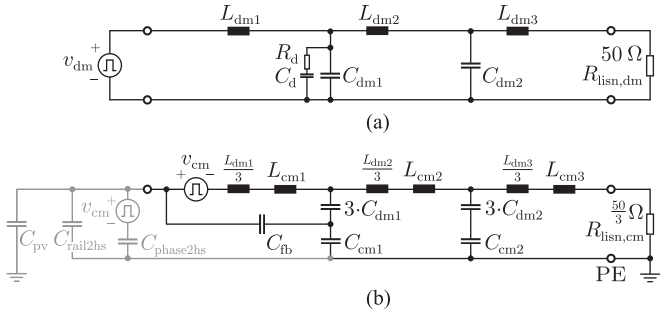

Fig. 6. Equivalent EMI filter design circuits. (a) Equivalent DM filter circuit with connected line impedance stabilization network (LISN) between filter and mains grid. (b) Equivalent CM filter circuit. Whereas the CM capacitors (C_{cm1}, C_{cm2}), the LISN, and the parasitic semiconductor to heat sink capacitances (C_{rail2hs}, C_{phase2hs}) are connected to the protective earth (PE) terminal, an additional CM noise path exists through the parasitic solar generator capacitance C_{pv} to ground.

III. Modeling

This section provides a brief overview of the multiphysics models used in the optimization scheme of Fig. 5. In this work, detailed and mostly experimentally verified models are considered to increase the accuracy and confidence level of the calculated results. Since the main inductors and semiconductors are typically responsible for the majority of the converter losses and volumes, special care has been taken regarding the modeling of these components. In particular, previously unpublished multiparametric switching and core loss measurements are presented, which are used to parameterize the respective switching and core loss models. Note that the cost modeling is discussed together with the component selection in Section IV-C.

A. System-Level Loop Models

The models of the system-level loop comprise the EMI filter design models and the waveform synthesis models.

1) EMI Filter Models: The EMI filter design is performed in three steps. In the first step, the worst-case EMI noise levels are identified based on the waveform model below and the methods presented in [32]. This is followed by the differential mode (DM) and common mode (CM) filter design. The procedure to determine the filter values so as to comply with the CISPR B standards [33] is largely based on the models and practical considerations presented in [32] and [34]–[37]. The equivalent filter circuits are depicted in Fig. 6 and take into account parasitic effects: a varying parasitic solar generator capacitance $C_{\mathrm{pv}} \in [0, 1.6]$ µF to earth [38] and parasitic capacitors C_{rail2hs} and C_{phase2hs} from the semiconductor packages to the heat sink in the range of a few hundred picofarads (determined by the number of packages and isolation distance [35]).

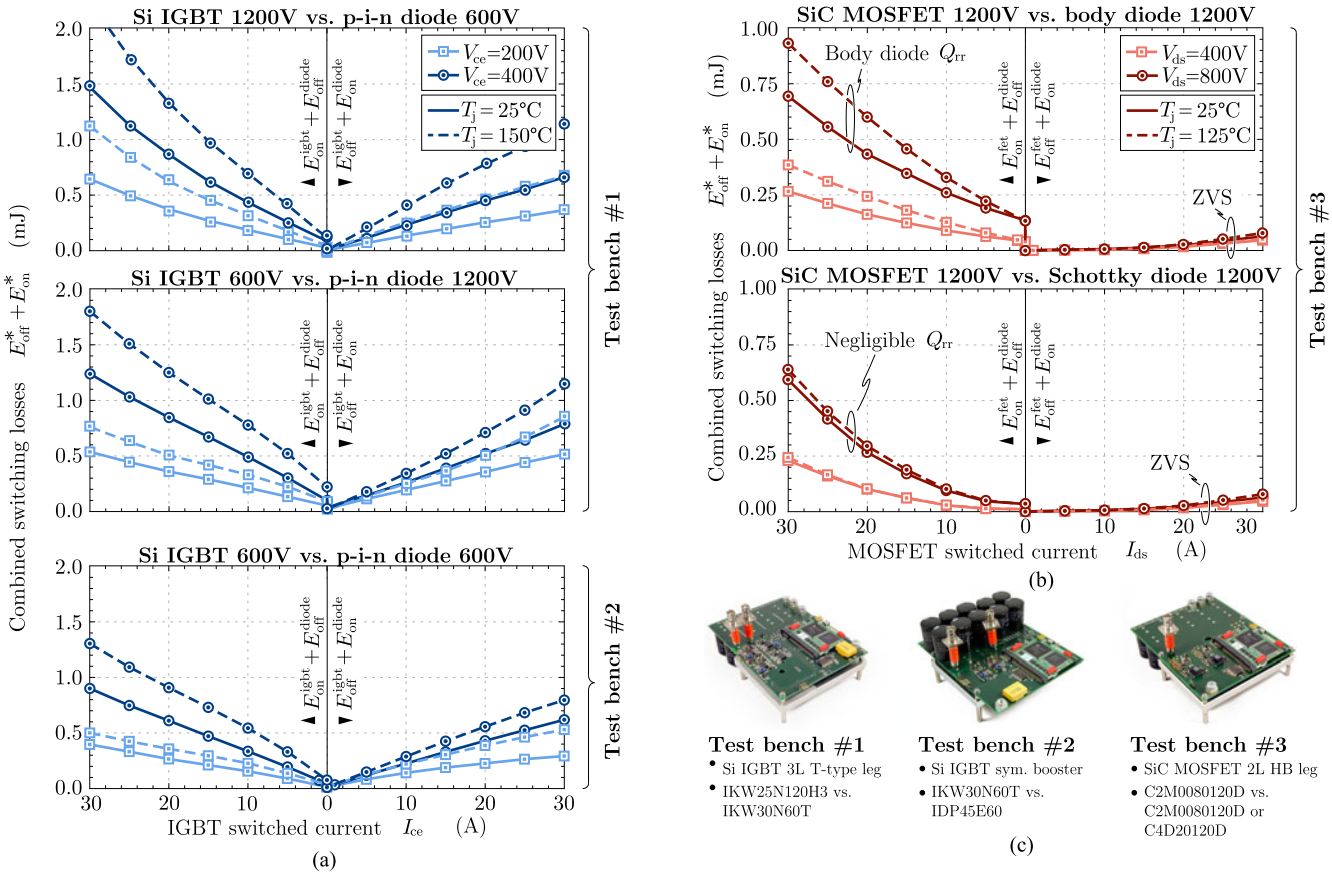

Fig. 7. Selection of the experimentally determined switching loss energies (left-hand side of the figures: sum of transistor turn-on and diode turn-off losses; right-hand side: sum of transistor turn-off and diode turn-on losses). (a) Si IGBT and p-i-n diode loss energies. (b) SiC MOSFET and Schottky diode switching loss energies. Notable reverse recovery charges Q_{rr} of the SiC MOSFET body diode can be observed when compared to the SiC Schottky diode. The superior ZVS capabilities of the SiC MOSFETs enable dramatically reduced turn-off losses when compared to Si IGBTs. (c) Employed switching loss measurement test benches implementing the topologies shown in Fig. 2.

2) Waveform Models: The waveform models are used to calculate the current and voltage waveforms in all components of the system as a function of the modulation scheme, the operating point, and the component values. The waveform synthesis is conducted in the time and frequency domain assuming lossless components (cf., Section II). The waveforms are synthesized for all nominal and worst-case operating points and represent a fundamental prerequisite for the component design.

B. Semiconductor Models

1) Conduction Losses: The conduction losses P_c are computed considering the current- and junction temperature-dependent output characteristics $V_{ce}(i_{ce}(t), T_j)$ and $R_{ds,on}(i_{ds}(t), T_j)$, respectively, of the considered IGBT, diode, and MOSFET devices. Interpolated data sheet parameters are employed.

2) Switching Losses: The switching losses P_{sw} are calculated taking into account the current-, voltage-, and temperature dependence of the switching loss energies $E_{on/off}(I_{on/off,i}, V_{on/off,i}, T_j)$. Due to the fact that the switching loss energies generally strongly depend on the topology and the layout, $E_{on/off}$ were experimentally determined rather than based on data sheets. Different Si and SiC switching loss energies were measured based on double pulse tests and high-bandwidth current shunts using the test benches depicted in Fig. 7(c). The obtained SiC switching losses of Fig. 7(b) are up to a factor of 10 (at same current/voltage) smaller when compared to the Si counterparts in Fig. 7(a).

C. Cooling System

The cooling system design routine is based on the advanced and experimentally verified thermal models presented in [15]. The fan power consumption P_{CS} includes the power supply losses due to an assumed efficiency of $\eta_{sup} = 75\,\%$.

D. Inductors

1) Reluctance Model: The reluctance model taken from [16] and [39] incorporates the nonlinear core material B–H curves and employs an experimentally verified approach for the air gap reluctance calculation.

2) Thermal Model: The employed thermal model assumes heat transfer based on natural convection and radiation to the ambient. It distinguishes the core and winding surface and

winding hot spot temperatures. The model is described in [16] and experimentally verified in [16] and [40].

3) Winding Loss Models: The temperature- and frequency-dependent winding loss models are largely based on the work in [41]. In particular, the models take into account the high frequency (HF) skin and proximity effects in detail.

4) Core Loss Models: The core losses P_{core} are computed by means of the improved–improved generalized Steinmetz equation according to [41]

$$P_{\text{core}} = V_{\text{core}} \cdot \frac{1}{T_{\text{g}}} \cdot \sum_i k_i \, \Delta T_i^{1-\alpha_i} \, |\Delta B_i|^{\beta_i} \, . \qquad (1)$$

ΔB_i denotes the peak-to-peak flux density swings of the piecewise linear HF flux density waveform and T_i the corresponding time intervals ($\sum T_i = T_{\text{g}}$). Operating point-dependent Steinmetz parameters (k_i, α_i, β_i) are determined for each interval. The parameterization of the model is based on novel core loss measurements obtained by means of the advanced resonant measurement circuit proposed in [42]. It enables wide measurement ranges also for gapped cores with a high Q-factor in contrast to the standard nonresonant circuit (e.g., [41], [43]). The systematic measurements put a high priority on the investigation of the effects of dc magnetization, temperature, and air gap length (relevant for tape-wound cores; cf., [21], [43]–[45]). The measured core losses for the materials N87 and 2605SA1 are depicted in Fig. 8. In order to validate the core loss measurements and the proposed loss models, 2605SA1-based inductors were analyzed using the calorimeter setup depicted in Fig. 9(a) and (b). Various N87-based inductors and transformers were analyzed in [40]. Both experiments showed a good agreement between the model-predicted and measured losses with a mean error of $< 10\,\%$ (cf., Fig. 9(c), [40]). The significant differences to the data sheet revealed in Figs. 8 and 9(c) emphasize the importance and value of the conducted measurements. The new data thus enable a greatly increased level of detail and accuracy in the inductor design routine.

E. Capacitors

The current-dependent losses P_C in the capacitors are calculated based on data sheet loss parameters.

F. Printed Circuit Board and Auxiliary Electronics

For simplicity, the printed circuit board (PCB) losses (such as dielectric and conduction losses) are neglected. The losses of the auxiliary circuits P_{AUX} include the gate driver losses P_{GD} and the power consumption of the control electronics, which is assumed to be constant $P_{\text{control}} = 5$ W. Again, the auxiliary supply efficiency is assumed to be $\eta_{\text{sup}} = 75\,\%$.

IV. Topologies, Modulation Schemes, and Components

In order to demonstrate and prove the value of the proposed virtual prototyping routine, a cost-aware comparative study on the employment of Si and SiC semiconductors in the PV converter system of Fig. 1 is carried out in the remainder of this

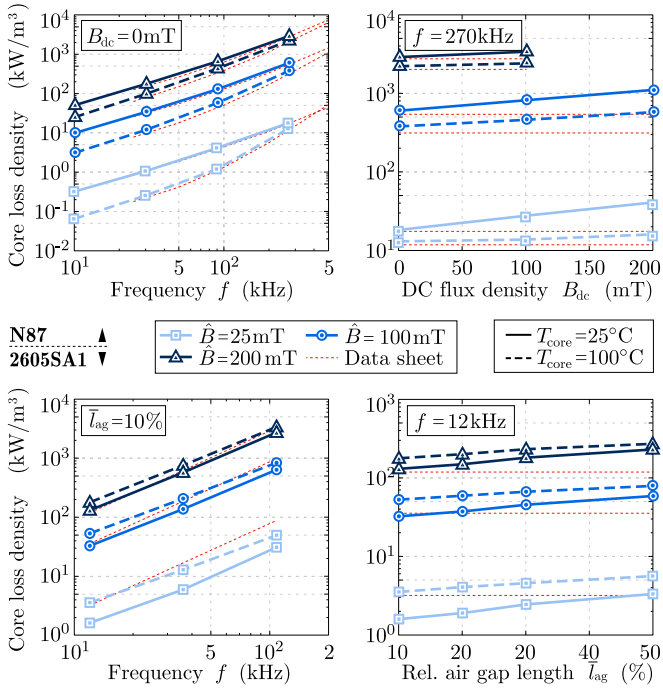

Fig. 8. Selection of the core loss measurements of the ferrite N87 and tape-wound amorphous iron 2605SA1. Besides the impact of the frequency f, (sinusoidal) flux density $\hat{B}$, and the core temperature T_{core}, additionally, the impact of the dc magnetization B_{dc} on N87 and the air gap length $\bar{l}_{\text{ag}}$ on 2605SA1 was studied. $\bar{l}_{\text{ag}}$ has no effect on N87 (bulk material) and B_{dc} was found to only moderately increase the 2605SA1 core losses (0–10%). The measured data reveal that B_{dc}, T_{core}, and $\bar{l}_{\text{ag}}$ significantly influence the losses which is not shown by the data sheet.

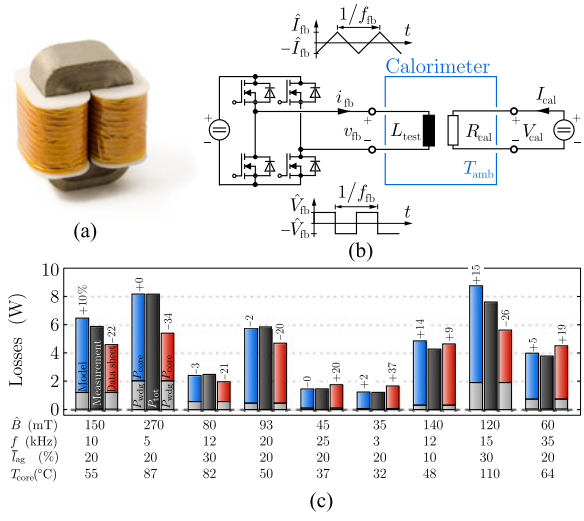

Fig. 9. Experimental verification of the 2605SA1 core loss measurements and the employed inductor loss models. (a) Sample test inductor. (b) Employed calorimetric measurement setup. The inductor under test L_{test} is excited with a triangular current whereas a high-precision shunt is used for the calibration. (c) Representative selection of the measured losses compared to calculated losses. The calculations using the measured core losses result in a mean absolute deviation of 8.6 % at a standard deviation of 5.0 % ($N_{\text{pop}} = 25$), whereas the data sheet-based approach achieves a mean error of 19.5 % at a standard deviation of 9.8 %.

paper. In this section, the selection of the compared topologies, modulation schemes, and components is reasoned in more detail.

A. Topologies

The achievable performance of Si and SiC is compared based on the three concepts depicted in Fig. 2. A widespread and state-of-the-art system in industry is the Si IGBT hard-switched PWM-modulated three-level T-type inverter topology (3LPWM) of Fig. 2(a) [3], [6], [46]. This topology in combination with a symmetric boost converter will, therefore, serve as the Si benchmark system in this work. The symmetric booster allows for the use of low-cost 600-V semiconductors and is able to contribute to the dc-link midpoint balancing [47].

The selected all Si 3LPWM benchmark system is compared to two all SiC concepts: following the argumentation of [6], [11], [12], the availability of efficient 1200-V SiC MOSFETs offers an opportunity to revert from a three-level to a two-level (PWM-modulated) topology. The simpler two-level topology is generally preferred due to the lower part count, which potentially translates into higher reliability and lower manufacturing and development costs. Furthermore, the two-level requires a minimum number of expensive SiC switches. This work investigates the achievable performance of this concept based on the two-level hard-switched PWM-modulated topology with a standard boost converter (2LPWM) as depicted in Fig. 2(b). A unique advantage of SiC MOSFETs when compared to Si IGBTs are the soft-switching capabilities (zero voltage switching—ZVS; cf., Fig. 7(b)). This advantage can be deliberately exploited when employing suitable modulation schemes. Therefore, the all SiC 2LTCM concept as shown in Fig. 2(c) is investigated where a triangular current mode (TCM) modulation scheme in a double-interleaved two-level system is employed. The interleaving of two branches per phase leg benefits the dc-link and EMI filter design and reduces the overall semiconductor conduction and turn-off switching losses.

The selected two-stage EMI filter topologies are depicted in Fig. 3.

B. Modulation Schemes

Whereas the 3LPWM and 2LPWM concepts are operated with a standard one-sixth third-harmonic CM injection PWM modulation scheme (e.g., [32]), the 2LTCM employs a TCM scheme both for the boost and inverter stage. The implementation and advantages of TCM are discussed in detail in [20]. Its main feature is soft switching, i.e., ZVS at all switching instants, which is achieved by a combination of varying switching frequencies and large current ripples (cf., Fig. 2(c)).

Following the specifications of typical commercial systems [46], a converter input voltage range of $[V_{\mathrm{mpp,min}}, V_{\mathrm{mpp,max}}] = [400, 800]$ V is chosen. It allows us to track the mainly temperature-dependent solar generator maximum power point (MPP) voltage V_{mpp}, which may vary up to a factor of 2 [9], [11]. The boost converter stages are employed to generate a dc-link voltage according to

$$V_{\mathrm{dc}} = \begin{cases} \max\{V_{\mathrm{dc,min}}, V_{\mathrm{mpp}} + \Delta V_{\mathrm{dc}}\}, & V_{\mathrm{mpp}} < V_{\mathrm{dc,min}} \\ V_{\mathrm{mpp}}, & V_{\mathrm{mpp}} \geq V_{\mathrm{dc,min}} \end{cases}$$
$$\text{where for PWM:} \quad V_{\mathrm{dc,min}} = 650\ \mathrm{V}, \quad \Delta V_{\mathrm{dc}} = 0\ \mathrm{V}$$
$$\text{and for TCM:} \quad V_{\mathrm{dc,min}} = 700\ \mathrm{V}, \quad \Delta V_{\mathrm{dc}} = 50\ \mathrm{V} \tag{2}$$

which enables grid feed-in independent from V_{mpp}. The boost converters are deactivated in case that $V_{\mathrm{mpp}} \geq V_{\mathrm{dc,min}}$. In order to control the strongly voltage-dependent switching frequency of TCM modulation [20], a higher minimum dc-link voltage $V_{\mathrm{dc,min}}$ is required than for PWM. For similar reasons, a minimum voltage difference of $\Delta V_{\mathrm{dc}} = 50$ V between V_{mpp} and V_{dc} is required in order to operate the activated boost converter stage, i.e., if $V_{\mathrm{mpp}} < V_{\mathrm{dc,min}}$.

C. Components and Materials

This section discusses the selection of the components and materials as listed in Table II. The presented cost data in this section were empirically collected from the respective component manufacturers using the same methods as in [48].

1) Semiconductors: State-of-the-art 600- and 1200-V discrete Si IGBTs and p-i-n diodes are employed in the 3LPWM system, whereas 1200-V SiC MOSFETs and Schottky diodes are considered for the 2LPWM and 2LTCM. Note that each concept is investigated assuming a fixed semiconductor configuration, i.e., paralleling of devices is not considered. For further details and unit cost data, refer to Tables II and III.

2) Cooling System: Cooling systems based on custom aluminum heat sinks and forced air cooling are considered. The calculation of the cooling system costs Σ_{CS} is based on the model from [48] assuming extrusion as the manufacturing process. The fan unit costs within the chosen fan series (cf., Table II) were found to vary between 6.32 and 6.78 €.

3) Inductors: Two core/winding material options are investigated for the main inductors L_{dc} and L_{dm1}, respectively (cf., Fig. 2). On the one hand, inductors made of tape-wound amorphous iron cores and solid round wires are considered. This combination features a high maximum permissible flux density $B_{\mathrm{max}} \approx 1.2$ T and a high winding fill factor enabling compact designs in the low-to-medium switching frequency and current ripple range [16], [21]. This choice is complemented by inductors made of low-loss ferrite and litz wire suitable for medium- to high-switching frequencies/current ripples.

The EMI filter inductors are implemented with gapless powder cores (DM) and nanocristalline toroids (CM). This choice minimizes the magnetic stray fields which may compromise the filter attenuation.

A refined version of the inductor cost model in [48] is proposed

$$\Sigma_L = \frac{1}{GM}\left(\Sigma_{\mathrm{core}} + \Sigma_{\mathrm{wdg}} + \Sigma_{\mathrm{lab}}\right) \tag{3}$$

TABLE II
SELECTION OF THE MAIN COMPONENTS AND MATERIALS

Component	3 LPWM (all Si)	2 LPWM (all SiC)	2 LTCM (all SiC)
S_{dc}	IGW30N60T	C2M0080120D	C2M0080120D
D_{dc}	IDP45E60	C4D20120D	-
S_{x1}, S_{x2}	IKW25N120H3	C2M0080120D	C2M0080120D
S_{x3}, S_{x4}	IKW30N60T	-	C2M0080120D
Heat sink	Custom optimized Al heat sink		
Fans	San Ace adjustable speed low power fans 9GA0412xxx 01		
L_{dc}, L_{dm1}	Litz wire [30, 355] µm 1–3 × stacked E-cores 1.5 EPCOS ferrite N87	OR	Solid round wire 1–2 × stacked U-cores METGLAS amorphous 2605SA1
C_{mpp}	EPCOS MKP film capacitors B3277x, $V_r \in \{575, 1200\}$ V		
C_{dc}	EPCOS long life electrolytic capacitors B43501x, $V_r = 500$ V		
$L_{dm\{2,3\}}$	Solid round wire & 1–3 × stacked E-cores MAGNETICS powder KoolMu {40, 60}µ		
$L_{cm\{1,2,3\}}$	Solid round wire & 1–5 × stacked toroidal cores VACUUMSCHMELZE nanocristalline Vitroperm 250F/500F		
$C_{dm\{1,2\}}$, $C_{\{d,fb\}}$	EPCOS X2 film capacitors B3292x, $V_r = 305$ V		
$C_{cm\{1,2\}}$	EPCOS Y2 film capacitors B3202x, $V_r = 300$ V		

TABLE III
SEMICONDUCTOR DATA

Component	Type	Ratings	Σ_{SC} (€)[1]
IDP45E60	Si p-i-n diode	600 V/175 °C	0.85
IGW30N60T	Si IGBT	600 V/175 °C	1.24
IKW30N60T	Si IGTB/p-i-n diode	600 V/175 °C	1.61
IKW25N120H3	Si IGTB/p-i-n diode	1200 V/175 °C	2.41
C4D20120D	SiC Schottky diode	1200 V/175 °C	8.11
C2M0080120D	SiC MOSFET	1200 V/150 °C	8.05

[1] based on manufacturer data for a minimum order quantity of MOQ = 50 k

where>

$$\Sigma_{\text{core}} = N_{\text{stack}} \cdot \Sigma^{\text{fc}}_{\text{core},x} + \sigma_{\text{core},x} W_{\text{core}} \tag{4}$$

$$\Sigma_{\text{wdg}} = \Sigma^{\text{fc}}_{\text{wdg},x} + \sigma_{\text{wdg},x} W_{\text{wdg}} \tag{5}$$

$$\Sigma_{\text{lab}} = \Sigma^{\text{fc}}_{\text{lab},x} + \sigma_{\text{lab},x} W_{\text{wdg}} \ . \tag{6}$$

$\Sigma_{\text{core},x}$, $\Sigma_{\text{wdg},x}$, and $\Sigma^{\text{fc}}_{\text{lab},x}$ represent fixed costs for the cores (N_{stack} being the stacking factor), for the connectors and coil formers as well as for labor. $\sigma_{\text{core},x}$, $\sigma_{\text{wdg},x}$, and $\sigma_{\text{lab},x}$ are relative costs per weight. The numerical cost parameters are listed in Table IV. As inductive components are often sourced from external suppliers, a cost premium of 33% ($GM = 0.75$) is added to the overall inductors costs.

D. Capacitors

The input MPP as well as all filter capacitances are realized with film technology. Contrarily, aluminum electrolytic capacitors are employed in the dc link as high capacitance values are required to attain sufficient control stability. The capacitor cost models and parameters are taken from [48].

TABLE IV
INDUCTOR COST DATA

Core[1]:	2605SA1 U-cores	N87 E-cores	KoolMu E-cores	Vitroperm Coated toroids
Winding[2]:	Round	Litz	Round	Round
$\Sigma^{\text{fc}}_{\text{core},x}$ (€)	5.10	0.08	0.60	1.05
$\sigma_{\text{core},x}$ (€/kg)	14.10	7.50	10.20	48.90
$\Sigma^{\text{fc}}_{\text{wdg},x}$ (€)	1.00	0.25	0.25	0.05
$\sigma_{\text{wdg},x}$ (€/kg)	10.00	variable[3]	10.00	10.00
$\Sigma^{\text{fc}}_{\text{lab},x}$ (€)	0.75	0.75	0.75	1.00
$\sigma_{\text{lab},x}$ (€/kg)	7.00	7.00	7.00	9.31

[1] MOQ = 50 k core sets
[2] MOQ = 1 metric ton
[3] AWG{48, 46, 44, 41, 38, 32, 27} $\triangleq$ {30, 40, 50, 71, 100, 200, 355} µm → {111.5, 58.5, 32.5, 23.5, 21.5, 18.5, 16.5} €/kg

TABLE V
AUXILIARY CIRCUIT UNIT COST DATA

Circuit:	GD	$\text{GD}^{\text{single}}_{\text{iso}}$	$\text{GD}^{\text{shared}}_{\text{iso}}$	M_v	M_i
Σ_x (€)	1.7	3.4	2.2	1.0	2.0
# 2LPWM	4	3	0	5	4
# 3LPWM	4	1	9	7	5
# 2LTCM	8	8	0	5	$4 + 2^1$

[1] the costs of eight zero crossing detection circuits [20] is equivalent to $2 \cdot \Sigma_{M_i} = 4$ €

E. PCB and Auxiliary Electronics

Standard four-layer 35-µm copper PCBs are assumed (cost model from [48]). The auxiliary equipment costs Σ_{AUX}

$$\Sigma_{\text{AUX}} = \Sigma_{\text{GD}} + \Sigma_{\text{M}} + \Sigma_{\text{AUX+}} \tag{7}$$

comprise the gate driver costs Σ_{GD}, measurement circuit costs Σ_{M}, and additional, roughly constant costs of $\Sigma_{\text{AUX+}} = 77$ €. The number of gate drivers, current, and voltage measurement circuits along with the estimated unit prices (based on the circuits of the test benches in Fig. 7(c)) are listed in Table V. It is distinguished between nonisolated, single isolated, and shared isolated (e.g., S_{x1}/S_{x4} in the 3LPWM; cf., Fig. 2(a)) gate drivers.

V. PERFORMANCE SPACE ANALYSIS

In this section, the optimization scheme of the virtual prototyping routine (cf., Fig. 5) is employed to find the Pareto fronts of the three PV converter concepts selected in the previous section. A total of 48 component and global design variables are considered. Among these, the selected global design variables $\vec{\Pi}_{\text{glo}}$ and the investigated respective intervals are the most interesting due to their significant impact on the overall system performance

$$\vec{\Pi}^{\text{2LPWM}}_{\text{glo}} : \ f_{\text{sw}} \in [12, 72] \text{ kHz}, \ \Delta I^{\text{pp}}_{L,\text{max}} \in [5, 60] \, \% \tag{8}$$

$$\vec{\Pi}^{\text{3LPWM}}_{\text{glo}} : \ f_{\text{sw}} \in [6, 36] \text{ kHz}, \quad \Delta I^{\text{pp}}_{L,\text{max}} \in [5, 60] \, \% \tag{9}$$

$$\vec{\Pi}^{\text{2LTCM}}_{\text{glo}} : \ f_{\text{sw,min}} \in [12, 84] \text{ kHz}, \quad k_{f_{\text{sw}}} \in [4, 12]. \tag{10}$$

For the PWM-modulated topologies, the switching frequency f_{sw} and the maximum peak-to-peak current ripple $\Delta I^{\text{pp}}_{L,\text{max}}$

TABLE VI
EMPLOYED OPTIMIZATION PARAMETERS AND CONSTRAINTS

Nominal ambient temperature	$T_{\text{amb,nom}}$	30 °C
Nominal displacement factor	$\cos(\phi_{\text{nom}})$	1.0
Nominal peak grid voltage	$\hat{V}_{\text{g,nom}}$	325 V
Max. ambient temperature	$T_{\text{amb,max}}$	60 °C
Max. MPP voltage ripple	$\Delta V_{C\,\text{mpp, max}}^{\text{pp}}$	2 V
Max. dc-link voltage ripple [1]	$\Delta V_{C\,\text{dc, max}}^{\text{pp}}$	6.5 V
Max. junction temperature [2]	$T_{\text{j,max}}$	$T_{\text{j},r} - 25$ °C
Max. winding hot spot temperature	$T_{\text{wdg,max}}$	125 °C
Max. 2605SA1 core temperature	$T_{\text{core,max}}^{\text{2605SA1}}$	125 °C
Max. N87 core temperature	$T_{\text{core,max}}^{\text{N87}}$	100 °C
Max. 2605SA1 flux density	$B_{\text{max}}^{\text{2605SA1}}$	1.2 T
Max. N87 flux density	$B_{\text{max}}^{\text{N87}}$	0.31 T
Max. inductance drop	$L(I_{L\,,\text{max}})/L_0$	0.75
Max. total relative air gap length [3]	$\tilde{l}_{\text{ag,max}}$	0.5

[1] also applicable to the 3LPWM midpoint potential of C_{dc}
[2] for rated semiconductor junction temperatures $T_{\text{j,r}}$, see Table III
[3] with respect to the leg width (U-cores) or center leg width (E-cores)

(defined at rated conditions) are iterated. For the 2LTCM, varying boundaries of the permissible switching frequency interval $f_{\text{sw}} \in f_{\text{sw,min}} \cdot [1, k_{f_{\text{sw}}}]$ are investigated. Note that in both cases, $\vec{\Pi}_{\text{glo}}$ implicitly determines the values of the main inductances L_{dc} and L_{dm1}. The performance of a specific design is assessed by means of the following three performance measures.

1) The efficiency at nominal conditions (cf., Table VI)

$$\eta_{\text{euro}}^{*} = \frac{\eta_{\text{euro}}^{525\text{ V}} + \eta_{\text{euro}}^{575\text{ V}} + \eta_{\text{euro}}^{625\text{ V}}}{3} \tag{11}$$

where the weighted European efficiency η_{euro} (e.g., [49]) is averaged for three different MPP voltages.

2) The power density $\rho_{\text{box}} = P_{\text{r}}/V_{\text{box,tot}}$ based on the total boxed volume of the converter components $V_{\text{box,tot}}$.
3) The specific costs $\sigma_P = P_{\text{r}}/\Sigma_{\text{tot}}$, based on the total component costs Σ_{tot}.

The values of the optimization constraints are listed in Table VI, whereas the main results are summarized in Figs. 10–12.

A. Core Materials

Fig. 10 shows the calculated Pareto fronts of the 2LTMC, 2LPWM, and 3LPWM concept. A remarkable feature of this figure is the distribution of the 3LPWM Pareto-optimal designs into two distinct clusters: an in-depth analysis reveals that the two clusters are a consequence of the two available main inductor material options (cf., Table II): on the one hand, a cluster of generally more compact designs results from amorphous iron inductors in combination with low-current ripples $\Delta I_{L,\text{max}}^{\text{pp}} \in [5, 15]\,\%$. On the other hand, a cluster comprising generally cheaper and more efficient designs results from the significantly lower cost ferrite in combination with medium- to high-current ripples. The situation is different with the 2LTCM and 2LPWM. These concepts inherently generate higher HF linked flux excitations than the 3LPWM which results in more pronounced HF inductor losses. As a consequence, ferrite-based designs are in any case superior to iron-based designs, i.e., do not only achieve lower losses and costs, but also lower volumes due to the thermal constraints of Table VI.

B. Comparison of Topologies

The performance of the three investigated PV systems is analyzed and compared in this section. For this purpose, consider Fig. 11 that depicts the component loss, volume, and cost breakdown of the (ferrite-based) Pareto-optimal designs that form the trajectories Γ on the Pareto fronts depicted in Fig. 10.

1) Losses: The main difference between the three concepts regarding the losses lies in the semiconductor share. The 2LTCM achieves the highest efficiencies due to the lowest semiconductor losses. On the other hand, the losses in the 2LTCM passives and the auxiliary (gate driver losses) are higher than for the 2LPWM and 3LPWM as a result of the HF high-ripple-current operation.

In order to obtain a deeper understanding of the semiconductor losses, consider Fig. 12 that shows the weighted relative conduction and switching losses as a function of the global design variables $\vec{\Pi}_{\text{glo}}$. It can be seen that the 2LPWM achieves $\approx 0.5\,\%$ lower weighted conduction losses than the 3LPWM. This is mainly due to the weighting of part load operation in (11), for which the ohmic MOSFET behavior is clearly superior over the IGBT with its inherent constant forward voltage drop. Although the 2LTCM features double the chip area, the weighted conduction losses are not half when compared to the 2LPWM. This is a direct consequence of the large ripple/triangular current waveform (cf., Fig. 2(c)) of TCM modulation causing increased rms values. It is thus found that the main reason for the highest semiconductor efficiency of the 2LTCM stems from the dramatically low switching losses due to ZVS in all operating points. When comparing the 2LPWM and 3LPWM, it is not only found that the 2LPWM SiC MOSFETs attain much lower switching losses for same switching frequencies (but double the blocking voltage), but also that the impact of varying current ripples $\Delta I_{L,\text{max}}^{\text{pp}}$ is opposite: whereas for the 2LPWM, elevated $\Delta I_{L,\text{max}}^{\text{pp}}$ reduce the switching losses, the same tend to increase for the 3LPWM. The origin of this effect is the fact that higher current ripples entail more current zero crossings (especially at part load). Current zero crossings in turn benefit the 2LPWM as they enable soft switching, i.e., ZVS of the SiC MOSFETs. In contrast, however, the 3LPWM cannot exploit the zero crossings as the turn-off tail currents of the Si IGBTs prohibit low-loss ZVS.

2) Volume: A general analysis of the volumes in Fig. 11 shows that achieving very high efficiencies entails the drawback of enormous volumes of the magnetics. The comparison of the three concepts shows that the most compact designs can be realized with the 2LTCM. It requires very low inductance values which results in the smallest inductors. The volumes of the 3LPWM are generally the largest, which is mainly due to the dc-link capacitor. The unavoidable presence of low-frequency currents flowing into the dc-link midpoint [50] asks for a large capacitance in order to limit the midpoint voltage imbalance. Despite the advantageous dc/dc converter topology that partially relaxes this problem (cf., Section IV), the largest dc link of all topologies results.

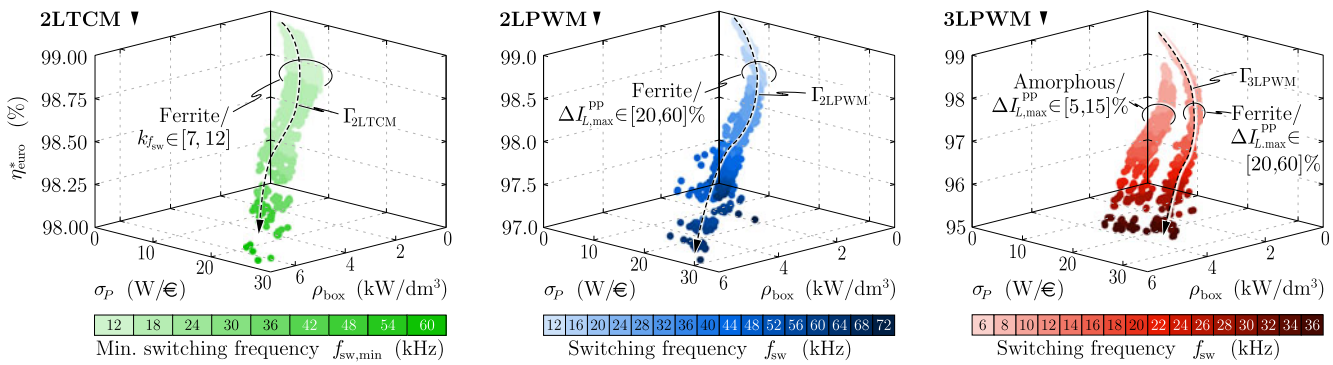

Fig. 10. η^*_{euro}-ρ_{box}-σ_P 3-D Pareto fronts of the investigated 2LTCM, 2LWPM, and 3LPWM PV system concepts of Fig. 2. Approximately 150 000 Pareto-optimal designs are found for each topology. The component loss, volume, and cost breakdown of Fig. 11 are based on the designs that form the sketched trajectories Γ shown in this figure.

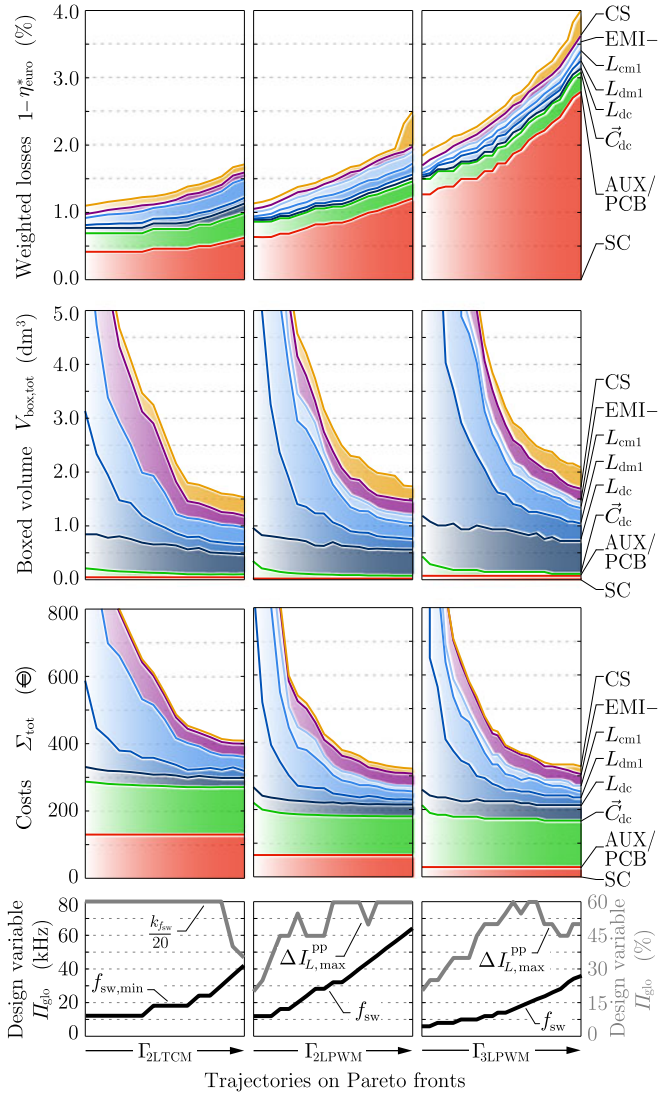

Fig. 11. Component loss, volume, and cost breakdown of the Pareto-optimal designs forming the trajectories Γ on the Pareto fronts depicted in Fig. 10. $\vec{C}_{dc}$ denotes the combined properties of C_{mpp} and C_{dc} whereas EMI− summarizes the filter components without L_{dm1} and L_{cm1}. It is furthermore shown how the global design variables $\vec{\Pi}_{glo}$ evolve along the chosen trajectories. For the purpose of presentation, the switching frequency multiple $k_{f_{sw}}$ has been scaled (e.g., $k_{f_{sw}} = 12 \Leftrightarrow k_{f_{sw}}/20 = 60\%$).

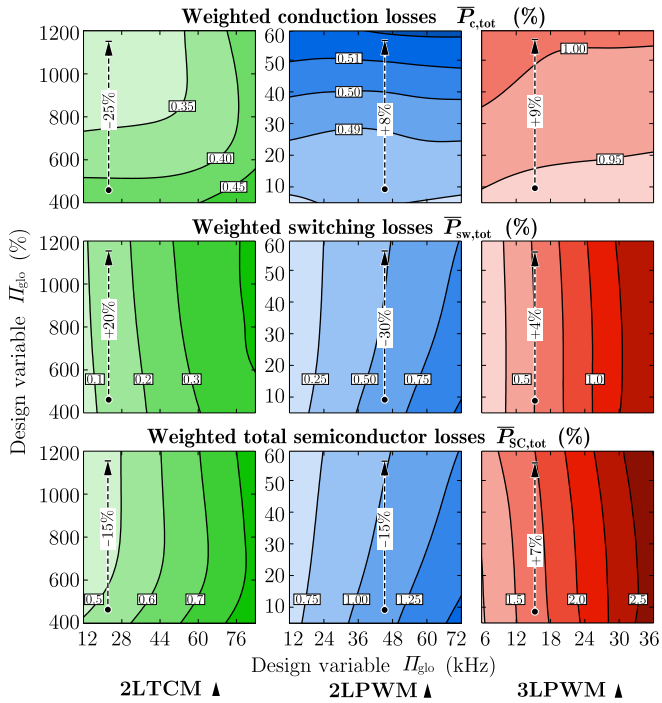

Fig. 12. Weighted (based on (11)) power semiconductor losses as a function of the global design variables $\vec{\Pi}_{glo}$. The losses are plotted considering the same cooling system for all topologies. In contrast to the Si IGBT-based 3LPWM concept, increasing the current ripple in the SiC MOSFET-based 2LPWM leads to lower overall losses due to more frequent ZVS transitions.

3) Costs: Finally, again with reference to Fig. 11, the systems are comparatively evaluated regarding costs. It is found that the highest component costs generally result for the 2LTCM. This is mainly due to the high number of expensive SiC switches and gate drivers, which dominate the total costs and which cannot be compensated by the lower costs of the passives. Despite twice the number of devices, the 3LPWM Si semiconductor costs are only half when compared to the SiC costs of the 2LPWM. However, the savings on the semiconductors are almost compensated by the increased costs for gate driver units. Apart from the semiconductors and the gate drivers, the cost breakdown of the 2LPWM and 3LPWM are similar: employing

a two- to threefold higher switching frequency in the 2LPWM results in similar costs of the passives as in the 3LPWM.

VI. LCC Mission Cost Space Analysis

The analysis of the Pareto fronts in the last section revealed the differences between the three considered concepts with respect to efficiency, power density, and specific costs. Since all concepts exhibit both strengths and weaknesses regarding the three performance measures (e.g., 2LTCM: efficient but expensive), determining the best concept and/or particular design solely based on the Pareto fronts is not possible. Therefore, the virtual prototyping routine as proposed in Section II includes a mission cost function $\mathcal{C} : (\eta^*_{\text{euro}}, \rho_{\text{box}}, \sigma_{\text{P}}) \mapsto \mathbb{R}$, which assigns each Pareto-optimal design a mission cost. Based on this single-dimensioned value, the best candidate system can be identified in a straightforward manner. Note that the mission cost function can arbitrarily be chosen and may only reflect the (subjective) preferences of the design engineer.

A. Mission Cost Function

In this work, it is proposed to employ a mission cost function $\mathcal{C}$, which approximates the LCC. A simple approach incorporating a net present value analysis is used

$$LCC = \Sigma_{\text{tot}} + \sum_{n=1}^{N_{\text{life}}} \left\{ \Sigma_{\text{cap}}(q) + \Sigma_{\text{rev}}(\eta^*_{\text{euro}}) \right\} \cdot \frac{1}{(1+q)^n} \,. \tag{12}$$

In (12), q denotes the interest rate and N_{life} the number of years, i.e., the considered lifetime. The LCC is composed of the following cost contributions.

1) *Initial costs*: The initial costs of all converter components Σ_{tot}.
2) *Capital costs*: The interests on the initially invested capital, i.e.,

$$\Sigma_{\text{cap}}(q) = q \cdot \Sigma_{\text{tot}}. \tag{13}$$

3) *Lost operating revenue costs*: The missed operating revenue, i.e., the value of the energy E_{loss} which is lost in the energy conversion of the PV system and which can thus not be sold to the utility

$$\Sigma_{\text{rev}}(\eta^*_{\text{euro}}) = \sigma_{\text{kWh}} \cdot E_{\text{loss}} \tag{14}$$

$$= \sigma_{\text{kWh}} \cdot P_{\text{r}} \cdot CF \cdot \frac{8760\ \text{h/year}}{1000} \cdot (1 - \eta^*_{\text{euro}}) \tag{15}$$

with σ_{kWh} being the costs of energy per kWh and CF the capacity factor of the PV system.

Clearly, a more comprehensive estimation of the LCC could also take into account manufacturing or housing costs. Furthermore, the effect of the inverter reliability on the LCC may be modeled by means of repair and downtime costs. However, the calculation of these costs would require the derivation of a large set of additional models and assumptions, which is beyond the scope of this paper.

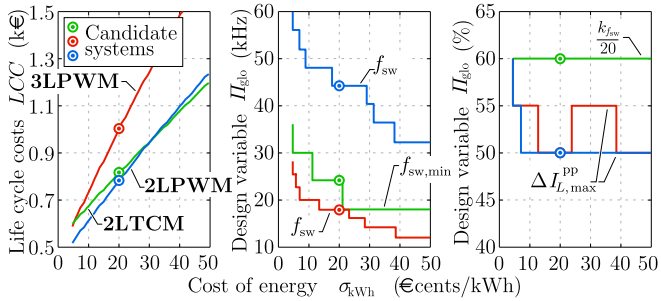

Fig. 13. Mission cost space analysis of the Pareto fronts of Fig. 10 based on the LCC evaluation of (12). The figures depict the minimum achievable LCC for varying costs of energy. Furthermore, the evolution of the global design variables of the corresponding designs are shown.

B. Analysis

Among the available parameters in (12), the cost of energy σ_{kWh} is clearly the most influential and therefore kept variable for the moment. Reasonable assumptions for the remaining parameters are

$$CF = 0.13, \quad q = 5\%/\text{year}, \quad N_{\text{life}} = 10\ \text{years}. \tag{16}$$

The above values for the capacity factor and the interest rate are typical for private residential PV systems in Central Europe. The considered lifetime was chosen based on standard warranties of large PV inverter manufacturers (usually 5 to 10 years) and the mean time between failure rates of PV inverters in the field as reported in [51]. Finally, it can be shown that moderate variations of up to $\approx \pm 50\,\%$ of the parameters in (16) do not change the general findings of this work.

Fig. 13 shows the best attainable LCC and the global design variables of the corresponding Pareto-optimal designs as a function of the energy costs σ_{kWh}. Increasing energy costs render more efficient systems with lower switching frequencies optimal, whereas high current ripples and wide frequency intervals seem to be invariably favorable. A comparison of the three concepts shows that the 2LPWM achieves the lowest LCC over a wide range of energy costs. Only at high energy costs of $\sigma_{\text{kWh}} \gtrapprox 0.32$ €/kWh, the 2LTCM becomes superior as a result of its unsurpassed efficiency helping to minimize the costs of lost operating revenue Σ_{rev}. In contrast, if very low energy costs of $\sigma_{\text{kWh}} \lessapprox 0.05$ €/kWh apply, the high initial costs of the 2LTCM render the concept the least attractive. Such energy costs typically apply to industries. There, usually higher interest rates of $q \approx 12\,\%/\text{year}$ are taken into account, which even more pronounces the importance of low initial costs. As the 2LPWM features the overall lowest attainable initial costs, this concept appears to be the best solution in either a residential or industrial application.

In a final step, the candidate systems for each topology are chosen assuming $\sigma_{\text{kWh}} = 0.20$ €/kWh. This number roughly averages the feed-in tariffs ($\sigma_{\text{kWh}} = 0.13$ €/kWh) and the remuneration for own consumption of the generated electricity ($\sigma_{\text{kWh}} = 0.30$ €/kWh) as applicable for residential PV system in Germany at the beginning of 2016. The details of the found candidate systems are shown in Fig. 14. It can be seen that

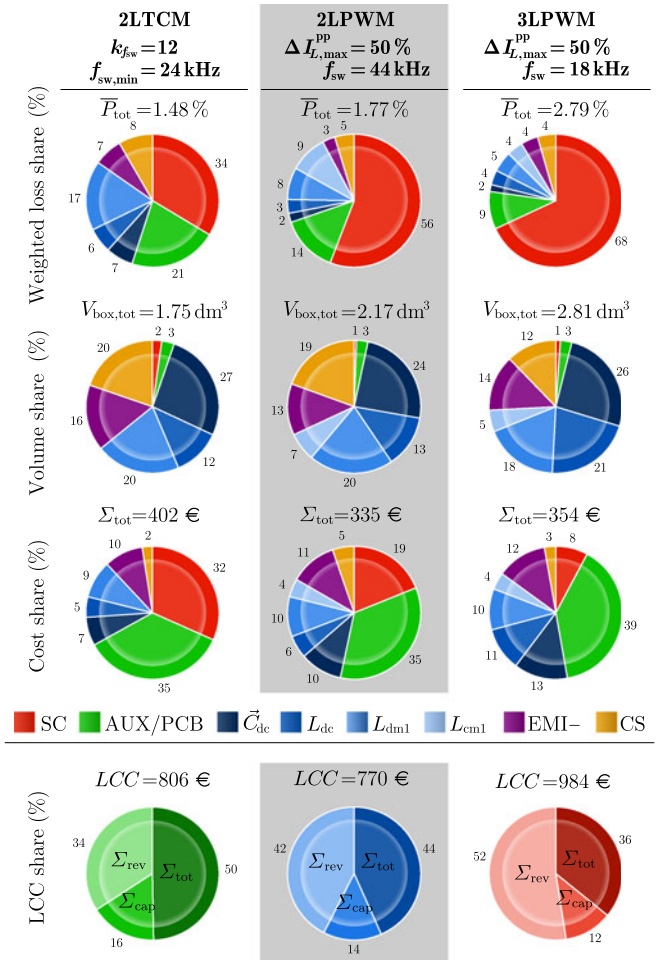

Fig. 14. Analysis of the loss, volume, component cost, and LCC shares of the selected candidate systems. It can be concluded that the identified 2LTCM candidate system achieves the lowest LCC and thus represents the optimal solution for the investigated PV converter application of Fig. 1.

the 2LPWM achieves 22 % lower LCC than the benchmark 3LPWM system and 5 % lower LCC than the 2LTCM system.

C. Proposed Candidate System

Based on the above analysis, it can be concluded that the 2LPWM design with $f_{sw} = 44$ kHz / $\Delta I^{pp}_{L,max} = 50\,\%$ as shown in Fig. 14 represents the most attractive solution for the investigated PV converter application of Fig. 1. Besides featuring a 22 % / 5 % lower LCC than the competitor systems, a range of other facts underline the attractiveness of the proposed solution: the selected 2LPWM candidate design offers the lowest initial costs (i.e., the component costs; cf., Fig. 14) and hence features the lowest costs already at the beginning of the considered lifetime. From an investment perspective, this is favorable as (in theory) it involves no uncertainty. Furthermore, the 2LPWM candidate system features by far the lowest complexity in terms of component count (semiconductors, gate drivers, passive components) and control effort (standard modulation scheme, no dc-link midpoint balancing, no current zero-crossing detection). This does not only facilitate a presumably higher reliability but also allows for low development and manufacturing costs and a short time to market.

Finally, it can be concluded that the found 2LPWM SiC-based solution outperforms the benchmark 3LPWM Si-based system. As evident from Fig. 14, the 2LPWM is not only more efficient and compact but also slightly less expensive. The main technical reasons for the superiority of the SiC-based solution are summarized and discussed below.

1) The chip utilization and symmetry of the semiconductor stresses in a two-level system is unsurpassed. Therefore, this topology is ideal for SiC as a maximum performance benefit using a minimum number of expensive SiC MOSFET switches can be attained.
2) The ohmic output characteristic of MOSFETs allows for much lower conduction losses in part load operation than bipolar IGBTs. Therefore, SiC MOSFETs prove to be a very good match for PV applications where part load efficiency is highly important.
3) The virtual prototyping routine identified the operation at high current ripples (here: $\Delta I^{pp}_{L,max} = 50\,\%$) to be optimal. The underlying reason is twofold: on the one hand, high current ripples in combination with SiC MOSFETs enables more frequent ZVS transitions and thus a considerably increased part load efficiency (contrary to IGBTs). That is, the optimized way of operating the 2LPWM exploits both the excellent hard- and soft-switching capabilities of SiC MOSFETs.
4) On the other hand, the operation at high ripple currents allows for the use of inexpensive and highly efficient ferrite inductors instead of costly and lossier amorphous iron cores.

VII. Conclusion

This paper presents a cost-aware comparative study of the potential of Si and SiC semiconductors in a 10-kW residential three-phase dc/ac PV converter application.

For this purpose, a novel virtual prototyping routine is proposed, which facilitates a systematic and comprehensive analysis of the topic. This is on the one hand accomplished by means of a multiobjective optimization scheme which enables the comparison of different converter concepts regarding the efficiency, power density and the specific costs. On the other hand, the virtual prototyping routine comprises an additional evaluation scheme based on the LCC. It facilitates the systematic selection of a candidate system from the obtained η-ρ-σ Pareto fronts. Advanced and largely experimentally verified multiphysics and quantitative cost models are used. Furthermore, previously unpublished multiparametric switching and core loss measurements as well as novel cost data are incorporated into the modeling framework. The virtual prototyping routine has proven its capability of deterministically solving complex optimization problems including 48 design variables with standard computational means.

Employing the virtual prototyping routine, three different Si and SiC converter concepts including the EMI filter were investigated. The results show that an optimized SiC two-level

system can concurrently improve the efficiency and power density when compared to an optimized state-of-the-art three-level Si-based system. At the same time, the SiC system achieves both lower component costs (-5 %) and LCC (-22 %). The industrial/commercial potential and attractiveness of the found solution is further underlined by its simplicity and low part count, which potentially translate into low development costs and high reliability.

REFERENCES

[1] H. Häberlin, "Evolution of inverters for grid connected PV-systems from 1989 to 2000," in *Proc. Eur. Photovoltaic Sol. Energy Conf.*, pp. 2008–2019.

[2] "A review of PV inverter technology cost and performance projections," Nat. Renewable Energy Lab., Golden, CO, USA, Tech. Rep. NREL/SR 620–38771, 2006.

[3] G. Deboy, H. Ludwig, R. Mallwitz, and R. Rupp, "New SiC JFET with integrated body diode boosts performance of photovoltaic systems," in *Proc. PCIM Eur. Conf.*, May 2011, pp. 220–228.

[4] R. Mallwitz, C. Althof, S. Buchhold, and E. Kiel, "First 99% PV inverter with SiC JFETs on the market—Future role of SiC," in *Proc. PCIM Eur. Conf.*, May 2012, pp. 368–373.

[5] Y. Xue, K. C. Divya, G. Griepentrog, M. Liviu, S. Suresh, and M. Manjrekar, "Towards next generation photovoltaic inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 2467–2474.

[6] U. Schwarzer, S. Buschhorn, and K. Vogel, "System benefits for solar inverters using SiC semiconductor modules," in *Proc. PCIM Eur. Conf.*, May 2014, pp. 1–8.

[7] B. Burger, D. Kranzer, and O. Stalter, "Cost reduction of PV-inverters with SiC-DMOSFETs," in *Proc. 5th Int. Conf. Integr. Power Syst.*, Mar. 2008, pp. 1–6.

[8] C. Wilhelm, D. Kranzer, and B. Burger, "Development of a highly compact and efficient solar inverter with silicon carbide transistors," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2010, pp. 1–6.

[9] S. V. Araújo, C. Nöding, B. Sahan, and P. Zacharias, "Exploiting the benefits of SiC by using 1700 V switches in single-stage inverter topologies applied to photovoltaic systems," in *Proc. PCIM Eur.*, May 2011, pp. 444–451.

[10] K. Mino, R. Yamada, H. Kimura, and Y. Matsumoto, "Power electronics equipments applying novel SiC power semiconductor modules," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 1920–1924.

[11] R. M. Burkart and J. W. Kolar, "Comparative evaluation of SiC and Si PV inverter systems based on power density and efficiency as indicators of initial cost and operating revenue," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, Jun. 2013, pp. 1–6.

[12] C. Sintamarean, E. Eni, F. Blaabjerg, R. Teodorescu, and H. Wang, "Wide-band gap devices in PV systems—Opportunities and challenges," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 1912–1919.

[13] D. Leuenberger and J. Biela, "Comparison of a soft switched TCM T-type inverter to hard switched inverters for a 3 phase PV grid interface," in *Proc. 15th Int. Power Electron. Motion Control Conf.*, Sep. 2012, pp. LS1d.1–1–LS1d.1-8.

[14] S. Saridakis, E. Koutroulis, and F. Blaabjerg, "Optimization of SiC-based H5 and conergy-NPC transformerless PV inverters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 555–567, Jun. 2015.

[15] C. Gammeter, F. Krismer, and J. W. Kolar, "Weight optimization of a cooling system composed of fan and extruded-fin heat sink," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 509–520, Jan. 2015.

[16] R. M. Burkart, H. Uemura, and J. W. Kolar, "Optimal inductor design for 3-phase voltage-source PWM converters considering different magnetic materials and a wide switching frequency range," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 891–898.

[17] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstübner, "Performance trends and limitations of power electronic systems," in *Proc. Int. Conf. Integr. Power Syst.*, Mar. 2010, pp. 1–20.

[18] O. Deblecker, C. Versèle, Z. De Greve, and J. Lobry, "Multiobjective optimization of a power supply for space application using a flexible CAD tool," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.

[19] M. Kasper, D. Bortis, and J. W. Kolar, "Classification and comparative evaluation of PV panel-integrated DC-DC converter concepts," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2511–2526, May 2014.

[20] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

[21] H. Uemura, F. Krismer, Y. Okuma, and J. W. Kolar, "η-ρ Pareto optimization of 3-phase 3-level T-type AC-DC-AC converter comprising Si and SiC hybrid power stage," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 2834–2841.

[22] M. Mirjafari and R. S. Balog, "Multi-objective design optimization of renewable energy system inverters using a descriptive language for the components," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2011, pp. 1838–1845.

[23] J. W. Kolar *et al.*, "Conceptualization and multiobjective optimization of the electric system of an airborne wind turbine," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 2, pp. 73–103, Jun. 2013.

[24] O. Deblecker, Z. De Greve, and C. Versèle, "Evaluation of power loss and mass gains of SiC versus Si-based switch-mode power supplies using a multiobjective optimization CAD tool," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion*, Jun. 2014, pp. 43–49.

[25] C. Gammeter, F. Krismer, and J. W. Kolar, "Comprehensive conceptualization, design, and experimental verification of a weight-optimized All-SiC 2 kV/700 V DAB for an airborne wind turbine," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 638–656, Jun. 2016.

[26] J. Pinne, A. Gruber, K. Rigbers, E. Sawadski, and T. Napierala, "Optimization and comparison of two three-phase inverter topologies using analytic behavioural and loss models," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2012, pp. 4396–4403.

[27] H. Mejbri, K. Ammous, and S. Abid, "Bi-objective sizing optimization of power converter using genetic algorithms: application to photovoltaic systems," *COMPEL*, vol. 33, no. 1, pp. 398–422, 2014.

[28] T. Diekhans and R. W. A. A. De Doncker, "A pareto-based comparison of power electronic topologies for inductive power transfer," in *Proc. PCIM Eur. Conf.*, May 2015, pp. 1–9.

[29] G. Adinolfi, G. Graditi, P. Siano, and A. Piccolo, "Multiobjective optimal design of photovoltaic synchronous boost converters assessing efficiency, reliability, and cost savings," *IEEE Trans. Ind. Informat.*, vol. 11, no. 5, pp. 1038–1048, Oct. 2015.

[30] M. Mirjafari, S. Harb, and R. S. Balog, "Multiobjective optimization and topology selection for a module-integrated inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4219–4231, Aug. 2015.

[31] C. Versèle, O. Deblecker, and J. Lobry, "Multiobjective optimal choice and design of isolated DC-DC power converters," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug. 2011, pp. 1–10.

[32] R. M. Burkart and J. W. Kolar, "Low-complexity analytical approximations of switching frequency harmonics of 3-phase N-level voltage-source PWM converters," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 3460–3467.

[33] *Industrial, Scientific and Medical (ISM) Radio-Frequency Equipment—Electromagnetic Disturbance—Characteristics Limits and Methods of Measurement*, CISPR 11, 2009.

[34] M. L. Heldwein, "EMC filtering of three-phase PWM converters," Ph.D. dissertation, ETH Zurich, Zurich, Switzerland, 2007.

[35] M. Hartmann, H. Ertl, and J. W. Kolar, "EMI filter design for a 1 MHz, 10 kW three-phase/level PWM rectifier," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1192–1204, Apr. 2011.

[36] D. O. Boillat, J. W. Kolar, and J. Mühlethaler, "Volume minimization of the main DM/CM EMI filter stage of a bidirectional three-phase three-level PWM rectifier system," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 2008–2019.

[37] D. O. Boillat, F. Krismer, and J. W. Kolar, "Design space analysis and ρ-η pareto optimization of LC output filters for switch-mode AC power sources," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6906–6923, Dec. 2015.

[38] *Capacitive Leakage Currents*, SMA Sol. Technol. AG, Niestetal, Germany, 2015.

[39] J. Mühlethaler, J. W. Kolar, and A. Ecklebe, "A novel approach for 3D air gap reluctance calculations," in *Proc. IEEE Energy Convers. Congr. Expo. Asia*, May 2011, pp. 446–452.

[40] R. M. Burkart and J. W. Kolar, "Comparative η-ρ-σ pareto-optimization of Si and SiC multi-level dual active bridge topologies with wide input voltage range," *IEEE Trans. Power Electron.*, submitted for publication.

[41] J. Mühlethaler, "Modeling and multi-objective optimization of inductive power components," Ph.D. dissertation, ETH Zurich, Zurich, Switzerland, 2012.
[42] M. Mu, "High frequency magnetic core loss study," Ph.D. dissertation, , Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2013.
[43] H. Fukunaga, T. Eguchi, Y. Ohta, and H. Kakehashi, "Core loss in amorphous cut cores with air gaps," *IEEE Trans. Magn.*, vol. 25, no. 3, pp. 2694–2698, May 1989.
[44] M. S. Ryłko, B. J. Lyons, J. G. Hayes, and M. G. Egan, "Revised magnetics performance factors and experimental comparison of high-flux materials for high-current DC-DC inductors," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2112–2126, Aug. 2011.
[45] T. Tera, H. Taki, and T. Shimizu, "Loss reduction of laminated core inductor used in on-board charger for EVs," in *Proc. Int. Power Electron. Conf.*, May 2014, pp. 876–882.
[46] SMA. *Sunny Tripower 5000TL-12000TL.* (2016). [Online]. Available: http://www.sma.de/en/products/solarinverters/sunny-tripower-5000tl-12000tl.html
[47] M. Frisch and T. Ernö, "Symmetrical boost concept for solar applications up to 1000 V," Vincotech GmbH, Munich, Germany, Tech. Rep., 2011.
[48] R. M. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2013, pp. 2139–2146.
[49] B. Bletterie *et al.*, "Redefinition of the European efficiency—Finding the compromise between simplicity and accuracy," in *Proc. Eur. Photovoltaic Sol. Energy Conf. Exhib.*, Sep. 2008, pp. 2735–2742.
[50] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.
[51] A. Ristow, M. Begovic, A. Pregelj, and A. Rohatgi, "Development of a methodology for improving photovoltaic inverter reliability," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2581–2592, Jul. 2008.

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