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***Abstract*—State-of-the-art variable speed drive inverter systems are typically employing 1200 V Si IGBTs with antiparallel freewheeling diodes, resulting in a large overall semiconductor chip area, relatively high switching losses and/or low switching frequencies, and causing a substantial on-state voltage drop in both current directions, which inherently limits the peak and part-load efficiency. SiC MOSFETs are seen as natural future replacement of Si IGBTs, since they benefit from high switching speeds and low on-state resistances, which drastically reduces switching and conduction losses. However, the high switching speed of SiC devices results in a d*v*/d*t*-stress on the motor windings of up to 60...80 V/ns, which must be limited to 3...6 V/ns in order to prevent partial discharge phenomena and/or progressive insulation aging. Full sinewave filtering could solve this issue, but would also reduce the achievable performance improvement, as a higher switching frequency and/or a bulky filter would be required. Therefore, this paper comparatively evaluates different d*v*/d*t*-limitation approaches proposed in literature, i.e. active, hybrid and passive filter concepts, for a next generation 10 kW SiC PWM inverter supplied from an 800 V DC-bus. First, the different filter concepts are described and analyzed, and in a second step their design procedure is explained based on the design space approach. Afterwards, a Pareto optimization is conducted and Pareto optimal designs are selected, evaluated and compared regarding efficiency and power density. All considered filter designs outperform a state-of-the-art typically 98.3% efficient IGBT inverter drive. The hybrid filter enables a part-load (at 8 kW) efficiency of 99.0% for a d*v*/d*t* limited to 6 V/ns. If higher d*v*/d*t*-values can be tolerated, e.g. 12 V/ns, 99.3% part-load efficiency with a power density above 80 kW/L can be achieved by the active concept.**

I. Introduction

State-of-the-art three-phase variable speed drive (VSD) inverter systems employ 1200 V Si IGBTs with antiparallel freewheeling diodes and are typically operated at switching frequencies up to 16 kHz [1]. For next generation VSDs SiC MOSFETs are offering an interesting alternative, as no explicit freewheeling diodes are required, i.e. the MOSFET-internal diodes can be utilized in combination with synchronous rectification, such that no constant on-state voltage drop is present for forward or reverse current conduction [2], [3]. Accordingly, besides a smaller overall inverter chip area, advantageously also a significantly higher part-load efficiency can be achieved [4]. In addition, due to the high switching speed of SiC MOSFETs and the largely missing internal diode reverse recovery current, lower switching losses are occurring, such that a switching frequency in the range of 48...100 kHz can be selected and full sinewave filtering of the inverter output voltage can be implemented [5], [6].

However, despite the relatively high switching frequency, an LC output filter still significantly impairs the overall inverter power density and increases the realization costs. Hence, approaches enabling a limitation to the absolutely necessary amount of filtering, i.e. only limiting the dv/dt of the voltage applied to the motor windings, are of main interest, cf. **Fig. 1**. Respecting according standards [7], [8], dv/dt-values of industrial IGBT inverters are typically in the range of 3...6 V/ns in order to prevent an unequal distribution of the inverter output voltage across the motor windings, or surge voltages for long motor cables, which both potentially result in partial discharge phenomena and/or progressive insulation aging [9], [10].

Accordingly, in this paper, active, passive and hybrid concepts ensuring a limitation of the dv/dt to 6 V/ns are introduced and analyzed. Furthermore, a limitation to only 12 V/ns is considered, in order to account for future improvements of motor insulation technology or a motor integration of the inverter stage, where no motor cable is present and/or no voltage reflections are occurring. A classification of different concepts described in literature for dv/dt-limitation is shown in **Fig. 2**. Selected solutions of each category are analyzed in this work for a 10 kW three-phase VSD SiC PWM inverter system supplied from a 800 V DC-link, assuming a relatively low switching frequency of 16 kHz, which is just out of the audible range, allows inverter output frequencies up to 500 Hz, ensures relatively low motor iron losses, and facilitates an immediate comparison with today's industry Si IGBT inverter systems [11]. The specifications of the targeted VSD system are summarized in **Tab. I**.

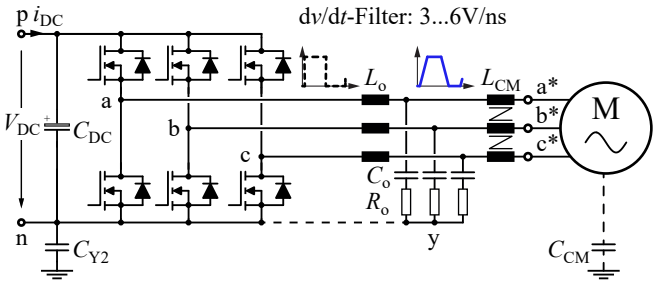

Fig. 1: Three-phase variable speed drive (VSD) PWM inverter system employing SiC MOSFETs. A passive dv/dt-filter is connected between the inverter bridge-leg outputs and the motor terminals in order to limit the voltage slope at the machine terminals to values of 3...6 V/ns and prevent partial discharge phenomena and/or progressive insulation aging. The star point y of the dv/dt-filter can be connected to the negative DC-link rail n to limit the dv/dt of the differential-mode (DM) *and* common-mode (CM) inverter output voltage components. An optional CM inductor L_{CM} can be added to prevent bearing currents and CM current spikes, due to the typically large parasitic CM capacitance C_{CM} of the machine windings to ground and to further reduce conducted and radiated electromagnetic emissions.

Description	Parameter	Nominal Value
Mechanical Output Power	$P_{M,max}$	10 kW
DC-Link Voltage	V_{DC}	800 V
Switching Frequency	f_{SW}	16 kHz
Voltage Slope Limit	dv/dt	6 V/ns or 12 V/ns

TABLE I: Three-Phase PWM Inverter System Specifications.

In the following, first a purely active concept, i.e. the reduction of the dv/dt through proper gate voltage control of the SiC MOSFETs in combination with explicit Miller feedback capacitors [12], is discussed (cf. **Section II-A** and **Fig. 3**) which doesn't require any additional power components for filtering. The concept results in increased switching losses, which can be kept minimal by minimizing the current rise-time at turn-on and the current fall-time at turn-off. However, still a high part-load efficiency can be achieved. A similar dv/dt-limitation can be obtained with variable gate resistors [13] or active gate drive circuits [14]–[17] including closed-loop control concepts [18]. The active concepts facilitate a detailed shaping of the bridge-leg output voltage during the switching transients, besides the dv/dt-limitation. Thus, high-frequency noise components can be further reduced and EMI-emissions are kept minimal, at the cost of increased complexity.

Next, passive concepts, i.e. a LCR dv/dt-filter [19] and a LC-filter with DRC damping [20] are considered (cf. **Section II-B**, **Fig. 4(a)** and **(b)**), where the filter capacitor is referenced to the negative DC-link rail [21], [22] in order to also limit the dv/dt of the common-mode (CM) component of the inverter output voltage, which contributes to reducing bearing currents [23], and conducted CM as well as radiated electromagnetic emissions [24]. The design of the filter elements is discussed based on a design space approach and the losses in the damping elements are calculated. RC- and RLC-filters located directly at the motor terminals in combination with a motor cable are described in [25] but are not considered here due to the limited general applicability and/or required adaption to

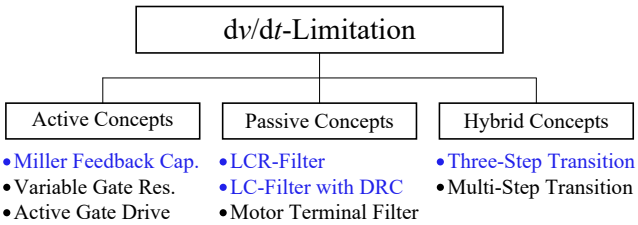

Fig. 2: Overview of different dv/dt-limitation concepts. *Active Concepts:* Miller feedback capacitor [12], variable gate resistor [13] and active gate drive circuit [15], [17], [18]. *Passive Concepts:* LCR- and LC-filters with DRC damping limiting only the dv/dt of the differential-mode (DM) component of the inverter output voltage [19], [20] or the dv/dt of the DM *and* of the common-mode (CM) component [21], [22]. *Hybrid Concepts:* Undamped LC-filter with additional off-on and on-off switching cycles [26], [27]. The concepts considered in this paper are indicated in blue.

specific motor parameters.

Finally, a hybrid concept is introduced (cf. **Section II-C** and **Fig. 4(c)**), which employs an undamped LC dv/dt-filter and uses an additional off-on switching cycle at turn-on and an additional on-off cycle at turn-off in order to ensure transitions of the inverter output voltage without overshoot [26]. As for the active concept, higher switching losses result, which however can be minimized with a high current gate drive as no dv/dt-limitation of the actual bridge-leg commutation needs to be respected. Further off-on and on-off switching cycles can be introduced in order to extend the design space [27], which however, again increases the switching losses.

In this paper, the mentioned dv/dt-limitation concepts are briefly summarized, analyzed and compared in order to identify the most promising approach for a SiC-based alternative to an Si IGBT inverter and evaluate the possible performance gain. **Section II** discusses the design of a conventional three-phase PWM inverter for a SiC-based VSD system, including the selection of the optimal chip area, and explains the operating principle of the active, passive and hybrid concepts. Filter constraints associated with certain machine properties are elaborated and serve as basis for the analytical filter design conducted in **Section III**. Afterwards, the results are generalized by means of a Pareto optimization in **Section IV**, in order to identify the performance limits of the individual concepts. The most promising approaches are compared with the state-of-the-art IGBT solution and a guideline based on the dv/dt-limit to select the preferred concept is proposed. Finally, **Section V** summarizes the findings of the work and gives an outlook to further research.

II. Inverter Design for SiC-based Drive System

The considered drive system is designed for a rated speed application with a mechanical speed of $n_\mathrm{M} = 4000\,\mathrm{rpm}$, i.e. $\omega_\mathrm{M} = 2\pi \cdot 67\,\mathrm{Hz}$, and a maximum mechanical power of $P_\mathrm{M,max} = 10\,\mathrm{kW}$, which results in a maximum load torque of $T_\mathrm{M,max} = 23.8\,\mathrm{Nm}$. However, since typical industrial drive systems are frequently operated in part-load, the inverter should be optimized for $P_\mathrm{M,opt} = 8\,\mathrm{kW}$, i.e. $T_\mathrm{M,opt} = 19.0\,\mathrm{Nm}$.

In accordance with these requirements, the permanent-magnet synchronous machine (PMSM) 1FT7084 from Siemens [28] is selected. With the given voltage constant $k_\mathrm{V} = \frac{V_\mathrm{LLrms}}{n_\mathrm{M}} = 83\,{}^\mathrm{mV}/_\mathrm{rpm}$ and the number of pole pairs $p = 5$, the amplitude $\hat{v}_\mathrm{I}$ and the electrical angular frequency ω_E of the induced phase voltage $v_\mathrm{Ia} = \hat{v}_\mathrm{I}\cos(\omega_\mathrm{E} t)$ are calculated as

$$\hat{v}_\mathrm{I} = \sqrt{\frac{2}{3}} k_\mathrm{V} n_\mathrm{M} = 270\,\mathrm{V} \tag{1}$$

$$\omega_\mathrm{E} = p\omega_\mathrm{M} = 2\pi \cdot 333\,\mathrm{Hz}, \tag{2}$$

while the amplitude of the phase current $i_\mathrm{a} = \hat{i}_\mathrm{a}\cos(\omega_\mathrm{E} t)$ is determined from the torque constant $k_\mathrm{T} = \frac{T_\mathrm{M}}{I_\mathrm{Lrms}} = 1.37\,{}^\mathrm{Nm}/_\mathrm{A}$, which can be obtained from the power balance. The maximum phase current amplitude results as

$$\hat{i}_\mathrm{a,max} = \sqrt{2}\frac{T_\mathrm{M,max}}{k_\mathrm{T}} = 25\,\mathrm{A}, \tag{3}$$

and the inverter should be optimized for $\hat{i}_\mathrm{a,opt} = 20\,\mathrm{A}$. The phase current causes an inductive voltage drop on the machine inductance $L_\mathrm{PH} = 2.8\,\mathrm{mH}$ [28] and thus, the peak phase voltage occurring at the machine terminal $\hat{v}_\mathrm{a}$ depends on the load current and increases from 270 V (cf. (1)) to 290 V. Consequently, the modulation index of the inverter $M = \frac{\hat{v}_\mathrm{a}}{V_\mathrm{DC}/2}$ rises from 0.68 to 0.8 and the load angle φ, which also determines the phase shift between inverter phase voltage v_a and current i_a, increases from 0° to 28°. Even though the modulation index M and the power factor $\cos\varphi$ are current dependent, their product is found to be load independent and equal to $M\cos\varphi \approx 0.68$ (for $n_\mathrm{M} = 4000\,\mathrm{rpm}$).

The inverter system is implemented as a conventional three-phase two-level topology employing 1200 V SiC MOSFETs with Kelvin-source connection [29], which are exhibiting excellent conduction and switching performance. A latest generation 1200 V SiC device (*C3M0016120K*, [30]), is selected and characterized in [31]. The nominal on-resistance is $R^*_\mathrm{DS} = 16\,\mathrm{m\Omega}$ and increases to $R_\mathrm{DS} = 20\,\mathrm{m\Omega}$ for a junction temperature of 100 °C. The current-dependent hard-switching energy losses (sum of turn-on and turn-off loss) are measured at a DC-link voltage of 800 V and can be modeled as $e_\mathrm{SW}(i_\mathrm{SW}) \approx k_0 + k_1 i_\mathrm{SW} + k_2 i_\mathrm{SW}^2$, with $k_0 = 312.2\,\mu\mathrm{J}$, $k_1 = 7.2\,{}^\mu\mathrm{J}/_\mathrm{A}$ and $k_2 = 120.8\,{}^\mathrm{nJ}/_{\mathrm{A}^2}$. Hence, assuming a purely sinusoidal phase current $i_\mathrm{a} = \hat{i}_\mathrm{a}\cos(\omega_\mathrm{M} p t)$, where the switching frequency-current ripple is neglected due to the large machine inductance in the mH-range, the total semiconductor losses of a single half-bridge result in

$$P_\mathrm{L,HB}\left(\hat{i}_\mathrm{a}\right) = R_\mathrm{DS}\frac{\hat{i}_\mathrm{a}^2}{2} + f_\mathrm{SW}\left(k_0 + \frac{2k_1}{\pi}\hat{i}_\mathrm{a} + \frac{k_2}{2}\hat{i}_\mathrm{a}^2\right). \tag{4}$$

For a given voltage rating, devices with different chip areas A_SiC are offered. Assuming a freely selectable chip area $A_\mathrm{SiC} = \alpha A^*_\mathrm{SiC}$ (where A^*_SiC corresponds to the $16\,\mathrm{m\Omega}$ device) with $\alpha > 0$, (4) thus can be generalized to [32]

$$P_\mathrm{L,HB}\left(\hat{i}_\mathrm{a}, \alpha\right) = \frac{R_\mathrm{DS}}{\alpha}\frac{\hat{i}_\mathrm{a}^2}{2} + f_\mathrm{SW}\left(\alpha k_0 + \frac{2}{\pi}k_1\hat{i}_\mathrm{a} + \frac{k_2}{2\alpha}\hat{i}_\mathrm{a}^2\right). \tag{5}$$

Increasing the chip area over A^*_SiC ($\alpha > 1$) leads to a reduction of conduction losses, as the effective on-resistance R_DS/α decreases (R_DS related to A^*_SiC), but also causes an increase of the capacitive switching losses $f_\mathrm{SW}\alpha k_0$. Thus, the minimum losses for a given semiconductor technology, phase peak current $\hat{i}_\mathrm{a,opt}$, and switching frequency f_SW can be found as

$$\alpha_\mathrm{opt} = \frac{A_\mathrm{SiC,opt}}{A^*_\mathrm{SiC}} = \hat{i}_\mathrm{a,opt}\sqrt{\frac{R_\mathrm{DS}}{2k_0 f_\mathrm{SW}} + \frac{k_2}{2k_0}}. \tag{6}$$

For $\hat{i}_\mathrm{a,opt} = 20\,\mathrm{A}$ and $f_\mathrm{SW} = 16\,\mathrm{kHz}$ (cf. **Tab. I**), an optimal chip area $A_\mathrm{SiC,opt} = 0.92 A^*_\mathrm{SiC}$ results, which corresponds to a nominal on-resistance of $R^*_\mathrm{DS}/\alpha_\mathrm{opt} = 17.4\,\mathrm{m\Omega}$. Accordingly, the available $16\,\mathrm{m\Omega}$ device is chosen without significantly affecting the semiconductor losses, cf. $P_\mathrm{L,HB}(\hat{i}_\mathrm{a,opt}, \alpha_\mathrm{opt}) = 10.6\,\mathrm{W}$ and $P_\mathrm{L,HB}(\hat{i}_\mathrm{a,opt}, 1) = 10.7\,\mathrm{W}$.

Finally, the inverter semiconductor efficiency η_INV can be calculated for $\alpha = 1$ and different load currents $\hat{i}_\mathrm{a}$ (neglecting the power consumption of the gate drives, control electronics, fans, etc.), according to

$$\eta_\mathrm{INV} = \frac{P_\mathrm{INV}}{P_\mathrm{INV} + P_\mathrm{L}} \approx 1 - \frac{P_\mathrm{L}}{P_\mathrm{INV}} = 1 - \frac{P_\mathrm{L,HB}\left(\hat{i}_\mathrm{a}, \alpha\right)}{\frac{1}{4}V_\mathrm{DC}\hat{i}_\mathrm{a} M\cos\varphi}. \tag{7}$$

The peak efficiency is achieved for $\hat{i}_\mathrm{a,opt}$ and results in $\eta_\mathrm{INV,opt} = 99.6\%$. However, this superior performance partially originates from the high switching speed, i.e. high dv/dt of the switching transitions, which is not admissible at the motor terminals. Therefore, active, passive and hybrid concepts are analyzed and compared in the following and evaluated regarding their performance, especially in terms of part-load efficiency, and are also compared to a Si IGBT inverter system.

A. Active dv/dt-Limitation Concept

The detailed discussion of the switching characteristics of a power MOSFET [12] reveals that an explicit Miller feedback capacitor C_M connected between gate and drain, cf. **Fig. 3(a)**, allows a reduction

of the drain-source and/or bridge-leg output voltage slope (e.g. of a turn-off transient)

$$\frac{dv_{\mathrm{DS}}}{dt} \approx \frac{dv_{\mathrm{DG}}}{dt} = \frac{V_{\mathrm{Miller}} - V_{\mathrm{G,N}}}{R_{\mathrm{G}}\left(C_{\mathrm{GD}} + C_{\mathrm{M}}\right)}, \tag{8}$$

(V_{Miller} denominates the Miller voltage, $V_{\mathrm{G,N}}$ is the negative gate drive voltage) while the rise- and fall-time of the current remains almost unaffected and are assumed as negligible in the following analysis.

Hence, the active concept requires no additional power components for the dv/dt-filtering and only a sufficiently large Miller capacitance C_{M} must be placed between gate and drain to reduce the high dv/dt of SiC MOSFETs in the range of $50\,\mathrm{V/ns}$ to the maximum allowed voltage transient slope. Based on (8), to limit the dv/dt below $6\,\mathrm{V/ns}$ or $12\,\mathrm{V/ns}$, Miller capacitances of $C_{\mathrm{M}} = 120\,\mathrm{pF}$ or $C_{\mathrm{M}} = 55\,\mathrm{pF}$ are required.

The considered phase-leg generates the average output voltage $\bar{v}_{\mathrm{a*n}} = v_{\mathrm{a}} + \frac{V_{\mathrm{DC}}}{2}$ and supplies the phase-shifted machine current i_{a} (cf. **Fig. 3(b)**). Focusing on a single switching period emphasizes the reduced slope of the output voltage $v_{\mathrm{a*n}}$. The rise (fall)-time of $v_{\mathrm{a*n}}$ is defined as time interval between 10% and 90% (90% and 10%) of the steady state value and can be calculated as $t_{\mathrm{R}} = t_{\mathrm{F}} = \frac{0.8 V_{\mathrm{DC}}}{dv/dt} = 107\,\mathrm{ns}$, while the total transition time is given by $t_{\mathrm{R0}} = t_{\mathrm{F0}} = \frac{V_{\mathrm{DC}}}{dv/dt} = 133\,\mathrm{ns}$. **Fig. 3(c)** shows the voltage spectrum of $v_{\mathrm{a*n}}$ for the maximal and the minimal modulation index $M_{\mathrm{max}} = 0.8$ and $M_{\mathrm{min}} = 0$, respectively. $M = 0$ is applied during the start-up and is identical to DC/DC operation with a fixed duty-cycle of $50\,\%$ and also corresponds to the worst-case harmonics generation and is thus analyzed in detail. The spectral component maximal amplitude $\frac{V_{\mathrm{DC}}}{2}\frac{4}{\pi} = 174\,\mathrm{dB\,\mu V}$ is located at the switching frequency f_{SW} and defines the envelope of the spectrum, which for frequencies between f_{SW} and the (second) corner frequency $f_{\mathrm{C}} = \frac{1}{\pi t_{\mathrm{R0}}} = 2.4\,\mathrm{MHz}$, defined by the non-zero voltage rise/fall-time, decays with $20\,\mathrm{dB/dec}$. For higher frequencies the spectrum decays even faster, i.e. with $40\,\mathrm{dB/dec}$, which is beneficial as conducted and radiated emissions are reduced.

The waveform of the voltage across the low-side transistor of a bride-leg, i.e. the output voltage $v_{\mathrm{a*n}}$, and the corresponding transistor current i_{T} are shown in **Fig. 3(d)**. In the considered interval, the phase current i_{a} is negative and thus the low-side switch initiates the current commutation from the complementary freewheeling diode at turn-on and the turn-off switching transition. When the low-side switch is turned-off, the output voltage first rises to the DC-link voltage with the dv/dt defined by C_{M}, before the high-side diode/switch can take over the load current and vice versa for the turn-on [12]. Consequently, a voltage/current overlap occurs at the low-side switch during both the turn-on and the turn-off transients and energy losses e_{Loss} occur, cf. **Fig. 3(f)**, similar to a hard-switching transition. As e_{Loss} depends linearly on the switched current,

$$e_{\mathrm{Loss}} = V_{\mathrm{DC}} t_{\mathrm{R0}} \cdot i_{\mathrm{a}} = \frac{V_{\mathrm{DC}}^2}{dv/dt} \cdot i_{\mathrm{a}} = \tilde{k}_1 \cdot i_{\mathrm{a}}, \tag{9}$$

the optimal chip area remains unaffected and the half-bridge losses can be calculated with (5) by replacing k_1 with $\tilde{k}_1 = \frac{V_{\mathrm{DC}}^2}{dv/dt}$. As the additional Miller capacitor is small, with respect to the MOSFET output capacitance C_{OSS}, the increase of the capacitive switching losses $f_{\mathrm{SW}} \alpha k_0$ is negligible. Thus, the phase losses of the active dv/dt limitation concept result for $\hat{i}_{\mathrm{a,opt}}$ in $P_{\mathrm{L,PH}} = 30.6\,\mathrm{W}$. Even though the total losses almost triple due to the increased voltage-current overlap, still a semiconductor efficiency of $\eta_{\mathrm{INV,opt}} = 98.8\%$ can be achieved. The resulting efficiency reduction $\Delta\eta$ compared to an inverter without any dv/dt-limitation can be approximated as

$$\Delta\eta \approx -\frac{2}{\pi}\frac{f_{\mathrm{SW}}\tilde{k}_1 \hat{i}_{\mathrm{a}}}{P_{\mathrm{INV}}/3} = -\frac{8}{\pi}\frac{f_{\mathrm{SW}}}{M\cos\varphi}\frac{V_{\mathrm{DC}}}{dv/dt} \tag{10}$$

and results in $\Delta\eta = -0.8\%$ for dv/dt=$6\,\mathrm{V/ns}$ and $\Delta\eta = -0.4\%$ for dv/dt=$12\,\mathrm{V/ns}$, which means that the efficiency reduction is independent of the output current and only increases with lower dv/dt-limits (cf. **Fig. 3(e)**).

B. Passive dv/dt-Limitation Concept

Passive dv/dt-filters comprise a damped LC-circuit, where the energy stored in the filter capacitor is dissipated at each switching

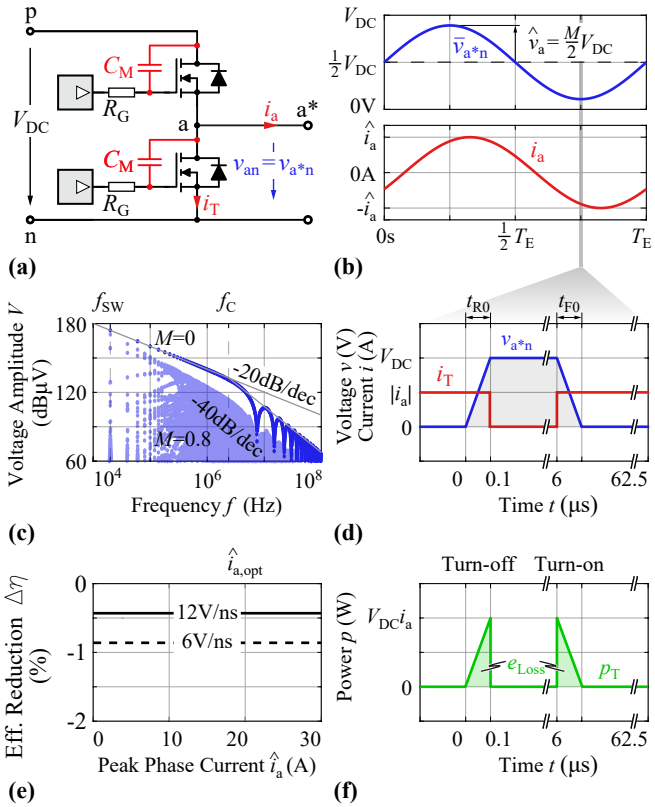

Fig. 3: Active dv/dt-limitation: **(a)** Phase-leg with explicit Miller feedback capacitor C_{M} to limit the dv/dt. **(b)** Average phase voltage $\bar{v}_{\mathrm{a*n}}$ and phase current i_{a} over one electrical fundamental output voltage period $T_{\mathrm{E}} = 1/f_{\mathrm{E}}$. **(c)** Spectrum of the PWM bridge-leg output voltage for the maximal (light blue) and the minimal modulation index ($M = 0$, dark blue) with the indicated corner frequency $f_{\mathrm{C}} = 2.4\,\mathrm{MHz}$, which is defined by the total voltage transition time $t_{\mathrm{R0}} = t_{\mathrm{F0}} = 133\,\mathrm{ns}$. **(d)** Voltage across the low-side transistor $v_{\mathrm{a*n}}$ and corresponding current i_{T}, showing the voltage-current overlap during the switching transitions. **(e)** Efficiency reduction $\Delta\eta$ for different dv/dt-values over the output current compared to a reference design without any dv/dt-limitation. **(f)** Transistor losses p_{T} caused by the dv/dt-limitation over a switching period $T_{\mathrm{SW}} = 62.5\,\mathrm{\mu s}$, resulting in the energy losses e_{Loss}.

transition. In order to limit the dv/dt of the DM and the CM component of the inverter output voltage, a filter referenced to the negative DC-rail is considered. The resulting phase-modular structure advantageously facilitates a potential integration into power modules on a per phase basis.

The simplest implementation of a damped LC-circuit [21] consists only of an inductor L_{o}, a capacitor C_{o} and a resistor R_{o}, cf. **Fig. 4(a.i)**. The fast switching event excites an oscillatory transition, which quickly converges to the steady state defined by $v_{\mathrm{C}} = V_{\mathrm{DC}}$ and $i_{\mathrm{La}} = i_{\mathrm{a}}$, as shown in **Fig. 4(a.ii)**.

An alternative LC-filter structure with DRC damping [22] is shown in **Fig. 4(b.i)**. As long as the bridge-leg voltage is between $0\,\mathrm{V}$ and V_{DC}, the transient is determined only by L_{o} and C_{o}, as both diodes are in the blocking state. However, when the output voltage $v_{\mathrm{a*n}}$ either falls below $0\,\mathrm{V}$ or exceeds the DC-link voltage V_{DC}, the low-side or high-side diode starts to conduct and the voltage transient is dampened by R_{p} or R_{n}, respectively. Furthermore, by placing the capacitors C_{p} and C_{n} in parallel to R_{p} and R_{n}, the overshoot can be reduced at the cost of a prolonged discharge-time, cf. **Fig. 4(b.ii)**. Consequently, this concept offers a trade-off between these characteristics, without influencing the rise-time itself.

Passive dv/dt-filters have no effect on the semiconductor selection, i.e. the optimal chip area and the semiconductor losses remain unaffected. However, in both filter concepts, the filter output capacitor C_{o} has to be charged and discharged within each switching period T_{SW}, similar to the parasitic output capacitance of the switching MOSFET. Consequently, the additional energy loss caused by the passive filter is given with $E_{\mathrm{C}} = C_{\mathrm{o}} V_{\mathrm{DC}}^2$. The occurring capacitive losses $P_{\mathrm{C}} = f_{\mathrm{SW}} E_{\mathrm{C}}$ are independent of the output current

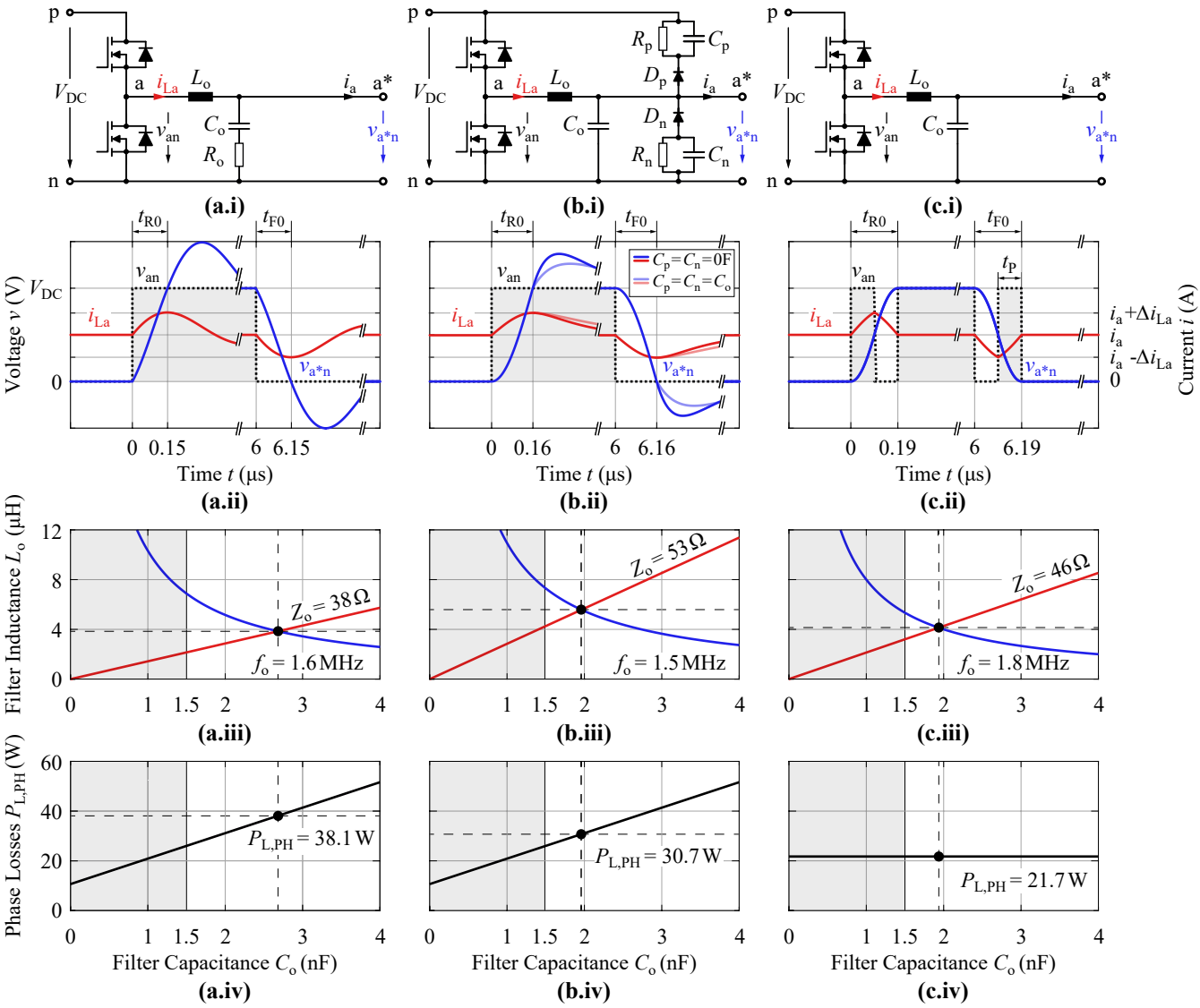

Fig. 4: **(i)** Circuit schematic and **(ii)** voltage and current waveforms including the inverter output voltage v_{an}, the machine terminal voltage v_{a^*n}, as well as the inductor current i_{La} during the switching transients of **(a)** the passive LCR-filter approach implemented using $L_o = 3.8\,\mu H$, $C_o = 2.7\,nF$ and $R_o = 19\,\Omega$, **(b)** the passive LC-filter with DRC damping implemented using $L_o = 5.6\,\mu H$ and $C_o = 2.0\,nF$ (dark blue and red for $C_p = C_n = 0\,F$ and $R_p = R_n = 26.6\,\Omega$ and light blue and red for $C_p = C_n = C_o$ and $R_p = R_n = 18.9\,\Omega$) and **(c)** the undamped LC-filter of the hybrid concept implemented using $L_o = 4.1\,\mu H$ and $C_o = 1.9\,nF$ with $t_P = 94\,ns$. All filter components are designed based on a design space consideration **(iii)** for $dv/dt = 6\,V/ns$ and a maximal current increase of $\Delta i_{La} = 15\,A$. The design space is constrained by $C_o > 1.5\,nF$ and $R_o < 25\,\Omega$ in order to eliminate the influence of the machine impedances; **(iv)** shows the resulting phase losses $P_{L,PH}$ for $\hat{i}_{a,opt}$ depending on the selected filter capacitance C_o.

and are increasing the phase losses $P_{L,PH} = P_{L,HB} + P_C$, reducing the peak efficiency and shifting the efficiency maximum to higher currents.

C. Hybrid dv/dt-Limitation Concept

The hybrid concept [26] combines an adapted switching pattern with an undamped LC-filter, in order to achieve a resonant voltage transition without any overshoot, cf. **Fig. 4(c)**. For example, the positive output voltage transition is initiated by turning-on the high-side switch and applying a short voltage pulse of duration t_P to the LC-filter, which excites a free oscillation. As a positive voltage is applied to the inductor, the inductor current i_{La} increases and the capacitor is charged by the additional current $i_{La} - i_a > 0\,A$. At time instant t_P, the capacitor voltage reaches half of the DC-link voltage, i.e. $v_C = V_{DC}/2$, and the voltage pulse is terminated by a second switching transient where the output current commutates from the high-side to the low-side switch. Consequently, now a negative voltage is applied to the inductor L_o and the inductor current decreases back to the actual output current i_a, but as the charging current flowing into the output capacitor C_o is still positive, $i_{La} - i_a > 0\,A$, the output voltage across C_o keeps increasing. Due to the symmetry of the transition, the transient finally reaches the steady state ($v_C = V_{DC}$, $i_{La} = i_a$) at $t_{R0} = 2t_P$, where, with a third switching transition, the high-side switch is finally turned-on during the remaining on-time. For the negative output voltage transition the same switching scheme is applied, where the high-side and low-side switches just swap their roles.

In contrast to the passive filter, the energy stored in the filter capacitor is not dissipated but can be recovered due to the resonant voltage transition, thus (ideally) no additional losses are generated by the LC-filter. However, as a result of the two additional transients, the switching losses are increased by a factor of three. Consequently, the optimal chip area has to be reduced to again balance the resulting switching and conduction losses, which according to (6) leads to $A_{SiC,opt} = 0.58 A^*_{SiC}$. Hence, a commercially available $32\,m\Omega$ device with the most suitable chip area is selected, which results in $P_{L,PH}\left(\hat{i}_{a,opt}, \alpha = 0.5\right) = 21.7\,W$ of semiconductor losses and a peak efficiency of 99.2%, cf. (7), neglecting any inductor losses. It should be noted that the losses are independent of the selected dv/dt.

III. Analytical Filter Design

This section describes the design procedure for the presented filter circuits. In order to provide a basis for a comparative evaluation, all

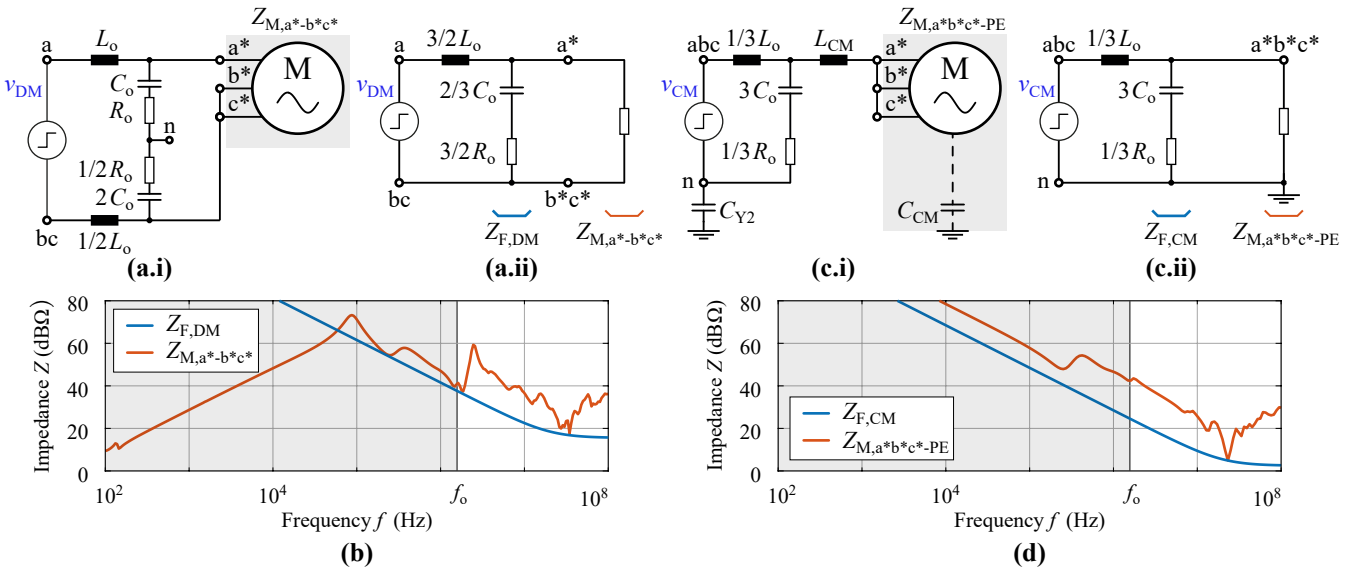

Fig. 5: Equivalent circuit of the dv/dt-filter with corresponding machine impedance measurement configurations for **(a)** the differential-mode (DM) voltage component v_{DM} and **(c)** common-mode (CM) voltage component v_{CM} of a switching transient. Comparison of **(b)** DM and **(d)** CM-characteristics between the measured machine impedances and the calculated filter output impedances with the minimum filter capacitance $C_{\mathrm{o}} = 2\,\mathrm{nF}$ and maximum damping resistance $R_{\mathrm{o}} = 4\,\Omega$ (L_{o} assumed to be infinite), resulting in a maximum deviation of 15% compared to the voltage overshoot or maximum current swing obtained for an unloaded dv/dt-filter.

filters are designed for a dv/dt $= 6\,\mathrm{V/ns}$ and a maximum current swing during the voltage transient of $\Delta i_{\mathrm{La}} = 15\,\mathrm{A}$. Furthermore, for the design of the filter it is considered that the VSD inverter system is arranged geometrically close to the motor, e.g. integrated into the machine housing, and therefore no long motor cables are required. However, the design space of the filter component values is still limited by the selected machine, and thus these constraints are elaborated in a first step.

A. Influence of the Machine Impedance

As the output terminals of the dv/dt-filters of the inverter bridge-legs are connected to the three-phase machine, the filter circuit basically cannot be assumed as unloaded. In fact, in the frequency range interesting for the dv/dt-filter design, i.e. the frequency range above the filter resonance frequency $f_{\mathrm{o}} \approx \frac{1}{2\pi t_{\mathrm{R0}}} = 1.5\,\mathrm{MHz}$, the machine typically shows a capacitive behavior, which means that its impedance decays with increasing frequency and accordingly can take influence on the resulting voltage transient.

Consequently, to minimize the influence of any machine impedance Z_{M}, the filter output impedance Z_{Fo} must be significantly smaller than Z_{M}, i.e. $Z_{\mathrm{Fo}} \ll Z_{\mathrm{M}}$, such that $Z_{\mathrm{Fo}} \approx Z_{\mathrm{Fo}} || Z_{\mathrm{M}}$ is valid. However, for a small machine impedance this means that large filter capacitor values C_{o} have to be provided, which result in unreasonably large filter losses. Furthermore, the damping resistor R_{o} would be restricted to small values and in turn would demand large inductances to limit the inductor current swing Δi_{La} below the defined value. Hence, in the following, Z_{Fo} should only be slightly smaller than or at least not larger than Z_{M}, such that the influence of the machine impedance stays below $20 - 30\%$ with respect to changes in voltage overshoot, voltage rise time or maximum current swing.

In order to verify whether this condition is met, the filter and machine impedances Z_{Fo} and Z_{M} seen from the inverter during a voltage transient have to be determined. There it must be considered that a voltage transition between two inverter switching states is composed of a differential-mode (DM) and a common-mode (CM) voltage transition v_{DM} and v_{CM}, which are both applied to the dv/dt-filter and to the machine. However, the filter and machine impedances Z_{Fo} and Z_{M} seen from the inverter switching stage output during a DM and CM excitation are not the same, which means that the above mentioned filter constraint must be examined for both excitation modes separately. If it can be shown that for both excitation modes the influence of the corresponding machine impedance is negligible, then also the influence on the overall voltage transient can be considered negligible.

For example, for the voltage transition from switching state (000) to (100), the inverter terminal voltage v_{an} changes from $0\,\mathrm{V}$ to V_{DC}, while the other terminal voltages v_{bn} and v_{cn} remain at $0\,\mathrm{V}$ (with reference to the negative DC-bus). Hence, the CM voltage step corresponds to $v_{\mathrm{CM}} = \frac{1}{3}(v_{\mathrm{an}} + v_{\mathrm{bn}} + v_{\mathrm{cn}}) = 1/3V_{\mathrm{DC}}$ and the DM voltage steps are $v_{\mathrm{DM,a}} = 2/3V_{\mathrm{DC}}$ for phase a and $v_{\mathrm{DM,b}} = v_{\mathrm{DM,c}} = -1/3V_{\mathrm{DC}}$ for the phases b and c, which together result in an overall DM voltage step of $v_{\mathrm{DM}} = v_{\mathrm{DM,a}} - v_{\mathrm{DM,b}} = V_{\mathrm{DC}}$ between phase terminal a and the two effectively shorted terminals b and c. In general, it is found that assuming a typical modulation scheme where only one bridge-leg is switched at a time, the same DM and CM voltage steps result for any other switching state changes.

Hence, based on the consideration made for the switching transient from (000) to (100), the three-phase equivalent DM output impedance of the dv/dt-filter $Z_{\mathrm{F,DMo}}$ and the machine input impedance $Z_{\mathrm{M,a^*\text{-}b^*c^*}}$ seen by the DM voltage transient v_{DM} are determined by the impedances measured between the terminal a^* and the two shorted terminals b^* and c^* (cf. **Fig. 5(a.i)**). $Z_{\mathrm{F,DMo}}$ can be further simplified to the circuit shown in **Fig. 5(a.ii)** with the lumped DM components: $3/2L_{\mathrm{o}}$, $2/3C_{\mathrm{o}}$ and $3/2R_{\mathrm{o}}$. Considering the worst case filter output impedance, where L_{o} is assumed to be infinite, $Z_{\mathrm{F,DMo}}$ simplifies to an RC-circuit with $Z_{\mathrm{F,DM}} = \left|\frac{1}{j\omega 2/3C_{\mathrm{o}}} + 3/2R_{\mathrm{o}}\right|$. **Fig. 5(b)** compares $Z_{\mathrm{F,DM}}$ - evaluated for $C_{\mathrm{o}} = 2\,\mathrm{nF}$ and $R_{\mathrm{o}} = 4\,\Omega$ - with the measured $Z_{\mathrm{M,a^*\text{-}b^*c^*}}$ and reveals that $Z_{\mathrm{F,DM}} < Z_{\mathrm{M,a^*\text{-}b^*c^*}}$.

On the other hand, the CM output impedance of the dv/dt-filter, $Z_{\mathrm{F,CMo}}$, and the machine input impedance $Z_{\mathrm{M,a^*b^*c^*\text{-}PE}}$ seen by the CM voltage transient v_{CM} is measured between the three shorted phase terminals and the protective earth (PE) connection (cf. **Fig. 5(c.i)**). For the worst case, where C_{Y2} is infinite, $Z_{\mathrm{M,a^*b^*c^*\text{-}PE}}$ corresponds directly to the load impedance of the dv/dt-filter for the CM voltage component. In reality, however, C_{Y2} would have to be considered in series to $Z_{\mathrm{M,a^*b^*c^*\text{-}PE}}$, which increases the effective load impedance and improves the relation between $Z_{\mathrm{F,CMo}}$ and $Z_{\mathrm{M,a^*b^*c^*\text{-}PE}}$ even further. According to $Z_{\mathrm{F,DMo}}$, the CM equivalent circuit of the dv/dt-filter for the CM voltage component v_{CM} can be derived as shown in **Fig. 5(c.ii)** with the effective CM components $1/3L_{\mathrm{o}}$, $3C_{\mathrm{o}}$ and $1/3R_{\mathrm{o}}$. Again, neglecting L_{o}, the filter output impedance simplifies to the RC-impedance $Z_{\mathrm{F,CM}} = \left|\frac{1}{j\omega 3C_{\mathrm{o}}} + 1/3R_{\mathrm{o}}\right|$, which for the previously selected values $C_{\mathrm{o}} = 2\,\mathrm{nF}$ and $R_{\mathrm{o}} = 4\,\Omega$ stays always below $Z_{\mathrm{M,a^*b^*c^*\text{-}PE}}$ as shown in **Fig. 5(d)**.

It should be noted, that both dv/dt-filter equivalent circuits have the same resonance frequency f_{o}, however, $Z_{\mathrm{F,DM}}$ is more than four times smaller than $Z_{\mathrm{F,CM}}$, which means that the DM equivalent

filter circuit reacts more sensitively to any loading by the machine impedance. Since in the considered case $Z_{\text{M,a*-b*c*}}$ is even slightly smaller than $Z_{\text{M,a*b*c*-PE}}$ and the excitation voltage v_{DM} is three times larger than v_{CM}, the overall influence of the machine impedance on the voltage transient is mainly defined by the DM component.

Numerical calculations considering the measured machine impedances and the minimum filter values of $C_{\text{o}} > 2\,\text{nF}$ and $R_{\text{o}} < 4\,\Omega$ revealed that for both excitation modes the error concerning overshoot and maximum current swing stays below 15% compared to the unloaded filter. Furthermore, if the maximum error is allowed to increase up to 30%, then even smaller filter component values of $C_{\text{o}} > 1.5\,\text{nF}$ and $R_{\text{o}} < 25\,\Omega$ are allowed.

B. Design Space Approach

In the following, a rough design guideline for the three presented dv/dt-filter approaches is given, which enables an initial comparison of their performances. The design goal is to limit the dv/dt to a maximum value, while the inductor current swing Δi_{La} as well as the voltage overshoot should stay below given boundaries.

The desired voltage slope dv/dt and the DC-link voltage V_{DC} define the resulting rise time t_{R} (from 10% to 90%) of the filtered voltage waveform:

$$t_{\text{R}} = t_{\text{F}} = \frac{0.8 V_{\text{DC}}}{\text{d}v/\text{d}t} = 107\,\text{ns}. \tag{11}$$

Furthermore, the ratio between the DC-link voltage V_{DC} and the maximal allowed current swing Δi_{La} determine the minimum effective filter impedance Z_{eff} as

$$Z_{\text{eff}} = \frac{V_{\text{DC}}}{\Delta i_{\text{La}}} = 53\,\Omega. \tag{12}$$

These two quantities can now be related to the filter resonance frequency f_{o} and the filter impedance Z_{o} according to

$$\omega_{\text{o}} = 2\pi f_{\text{o}} = \sqrt{\frac{1}{L_{\text{o}} C_{\text{o}}}} = \Omega \frac{1}{t_{\text{R}}}, \tag{13}$$

$$Z_{\text{o}} = \sqrt{\frac{L_{\text{o}}}{C_{\text{o}}}} = \gamma Z_{\text{eff}}, \tag{14}$$

which both are functions of L_{o} and C_{o}. For the LC-filter with DRC damping and the hybrid concept, the scaling parameters Ω and γ are specific and can be derived by analytical calculations. In case of the LCR-circuit, Ω and γ depend on the damping factor $Q = R_{\text{o}}/Z_{\text{o}}$, which also defines the overshoot, and thus are difficult to calculate. Alternatively, for all filter concepts Ω and γ can also be obtained from circuit simulations. The corresponding results are summarized in **Tab. II**, where for the LCR-circuit a voltage overshoot of 50% ($Q = 0.5$) is considered, as e.g. proposed in [7], [8].

With these values, for the LCR-filter a resonance frequency of $f_{\text{o}} = 1.6\,\text{MHz}$ and a filter impedance of $Z_{\text{o}} = 38\,\Omega$ are obtained, which both can be visualized in the $L_{\text{o}}C_{\text{o}}$ design space. As shown in **Fig. 4(a.iii)**, for the given resonance frequency f_{o}, the filter inductance is given as $L_{\text{o}} = 1/\omega_{\text{o}}^2 C_{\text{o}}$, and for the determined filter impedance Z_{o} the inductance is calculated as $L_{\text{o}} = Z_{\text{o}}^2 C_{\text{o}}$, depending on the selected capacitance value C_{o}. The intersection at $C_{\text{o}} = 1/Z_{\text{o}}\omega_{\text{o}}$ equals the targeted design and in case of the LCR-filter results in $L_{\text{o}} = 3.8\,\mu\text{H}$, $C_{\text{o}} = 2.7\,\text{nF}$ and $R_{\text{o}} = QZ_{\text{o}} = 19\,\Omega$. As shown in **Fig. 4(a.iv)**, the total losses per phase-leg comprising the semiconductor losses $P_{\text{L,HB}}$ and the losses P_{C} resulting due to the dissipated capacitor energy add up to $P_{\text{L,PH}} = 38.1\,\text{W}$ and would linearly increase if a larger capacitance value C_{o} would have to be selected.

In case of the LC-filter with DRC damping, the same specifications yield $f_{\text{o}} = 1.5\,\text{MHz}$ and $Z_{\text{o}} = 53\,\Omega$. Due to a similar scaling parameter Ω, the resonance frequency f_{o} remains almost identical but the impedance Z_{o} is larger than in the previous case, due to the smaller γ. Hence, the DRC-damped filter requires a larger inductance but a smaller capacitance, i.e. $L_{\text{o}} = 5.6\,\mu\text{H}$ and $C_{\text{o}} = 2.0\,\text{nF}$ (cf. **Fig. 4(b.iii)**). Advantageously, the smaller C_{o} results in 25% less capacitive filter losses and reduces the losses per phase-leg to $P_{\text{L,PH}} = 30.7\,\text{W}$, which is 20% lower with respect to the LCR-design (cf. **Fig. 4(b.iv)**). The filter losses are again defined by the energy stored in the filter capacitor C_{o} and increase therefore linearly with C_{o}. As already mentioned, the damping network consisting of C_{p}, C_{n}, R_{p} and R_{n} has no effect on the losses, but only influences the occurring overshoot. The values of the damping network are selected as $C_{\text{p}} = C_{\text{n}}$ and $R_{\text{p}} = R_{\text{n}}$, while R_{p} is given as $R_{\text{p}} = 0.5\sqrt{L_{\text{o}}/(C_{\text{p}} + C_{\text{o}})}$ in order to prevent ringing within the network. Considering $C_{\text{p}} = 0\,\text{F}$, i.e. using no capacitor C_{p}, corresponds to $R_{\text{p}} = 26.6\,\Omega$ and a voltage peak of 1100 V, while an increased capacitance of $C_{\text{p}} = C_{\text{o}}$ (with $R_{\text{p}} = 18.9\,\Omega$) would reduce the voltage peak by only 100 V.

Filter	$\Omega = t_{\text{R}}\omega_{\text{o}}$	$\gamma = Z_{\text{o}}/Z_{\text{eff}}$
Passive LCR-Filter ($Q = 0.5$)	1.05	0.71
Passive LC-Filter with DRC	1.02	1.00
Hybrid LC-Filter	1.19	0.87

TABLE II: Scaling parameters Ω and γ for the passive LCR-filter with an overshoot of 50% ($Q = 0.5$), the passive LC-filter with DRC damping and the hybrid filter.

Finally, the hybrid LC-filter is characterized by $f_{\text{o}} = 1.8\,\text{MHz}$ and $Z_{\text{o}} = 46\,\Omega$, leading to $L_{\text{o}} = 4.1\,\mu\text{H}$ and $C_{\text{o}} = 1.9\,\text{nF}$ (cf. **Fig. 4(c.iii)**). As this filter consists only of these two elements, there is no further degree of freedom and the pulse width is fixed to $t_{\text{P}} = \frac{1}{6 f_{\text{o}}} = 94\,\text{ns}$. The energy stored in the filter capacitor is always fully recovered in the subsequent transient, leading to a lossless filter with capacitance independent phase-leg losses $P_{\text{L,PH}} = 21.7\,\text{W}$ (cf. **Fig. 4(c.iv)**). Thus, the hybrid LC-filter is identified as the filter solution with the lowest losses among the considered cases including the active concept.

IV. Pareto Optimization

In addition to the straightforward design procedure and the initial performance comparison presented in the previous section, now the achievable performances of the different dv/dt-filter approaches are comprehensively evaluated with an $\eta\rho$-Pareto optimization with respect to achievable efficiency η and power density ρ. There, the resulting dv/dt, the maximum allowed voltage overshoot as well as the maximum allowed current swing are no more fixed to a defined value but are limited within a certain design space; for the dv/dt a range between $1\,\text{V/ns}$ and $12\,\text{V/ns}$ is considered, while the voltage overshoot is restricted to values below 50% [7], [8]. Furthermore, for the passive concepts, the maximum allowed current swing Δi_{La} is limited to the maximum current amplitude $\hat{i}_{\text{a,max}} = 25\,\text{A}$, while for the hybrid concept Δi_{La} is restricted to 8 A to prevent the need for correction pulses, at least at higher machine currents [26]. In addition, considering the impedance of the attached motor, the more conservative filter constraints of $C_{\text{o}} > 2\,\text{nF}$ and $R_{\text{o}} < 4\,\Omega$ are respected.

Based on these considerations, the filter component and the corresponding filter losses can be calculated. The semiconductor losses are determined with (5), where for the conduction losses also the temperature-dependent on-resistance R_{DS} of the MOSFET is considered [31], while at room temperature a worst case on-resistance of $R_{\text{DS}} = 20\,\text{m}\Omega$ is assumed to also account for device manufacturing tolerances [30]. To determine the junction temperature of the MOSFET, a thermal resistance between junction and heatsink of $R_{\text{th,J-HS}} = 1.2\,\text{K/W}$ is used, which includes the thermal resistances of the transistor and the thermal interface material. For the passive filter concepts, power resistors housed in a TO-247 package are employed, which are characterized by a thermal resistance of $2.3\,\text{K/W}$.

The system losses are assumed to be extracted by a heatsink with forced air flow and the corresponding thermal resistance $R_{\text{th,HS}}$ is calculated such that specified values for the maximum operating temperature of the SiC MOSFETs ($T_{\text{J,SiC}} = 125\,°\text{C}$), the power resistors ($T_{\text{J,R}} = 150\,°\text{C}$), and the heatsink surface ($T_{\text{HS}} = 85\,°\text{C}$) are not exceeded under all operating conditions, assuming an ambient temperature of $T_{\text{AMB}} = 45\,°\text{C}$. The corresponding heatsink volume Vol_{HS} is calculated following the Cooling System Performance Index (CSPI) approach [33] assuming a CSPI of $20\,\text{W/K L}$ as

$$\text{Vol}_{\text{HS}} = \frac{1}{R_{\text{th,HS}}\text{CSPI}}. \tag{15}$$

The inductor and capacitor volumes are determined from a pool of commercially available components, respecting the voltage and current ratings. The overall inverter power density is calculated as

$$\rho = \frac{P_{\text{M,max}}}{1.3\left(\text{Vol}_{\text{HS}} + \text{Vol}_{\text{L}} + \sum \text{Vol}_{\text{Ci}}\right)}, \tag{16}$$

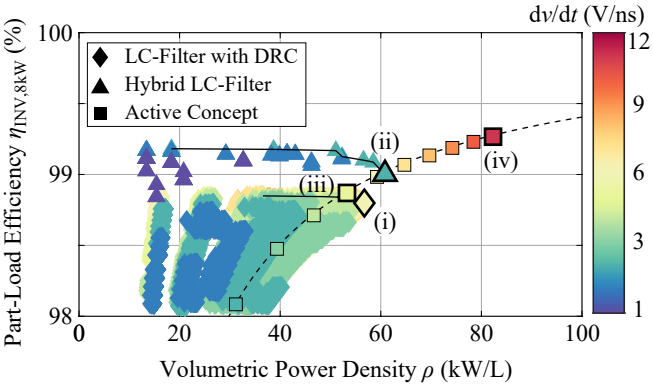

Fig. 6: $\eta_{\mathrm{INV,8kW}}$-ρ-Pareto optimization results comparing the presented concepts for the specified assumptions and restrictions, i.e. $C_{\mathrm{o}} > 2\,\mathrm{nF}$, $R_{\mathrm{o}} < 4\,\Omega$ and $1\,\mathrm{V/ns} < \mathrm{d}v/\mathrm{d}t < 12\,\mathrm{V/ns}$. For the passive LCR-filter no valid designs are found for the given design constraints. The performance of the passive LC-filter with DRC damping is limited by the dissipated filter capacitor energy and/or the losses occurring in the damping network and thus is outperformed by the hybrid filter concept. The active concept achieves a similar performance for low $\mathrm{d}v/\mathrm{d}t$-values and represents the best solution in case larger $\mathrm{d}v/\mathrm{d}t$-values can be tolerated. Promising designs are selected and are further compared in **Fig. 7** regarding their load-dependent efficiency: **(i)** Passive LC-filter with DRC damping for $7\,\mathrm{V/ns}$ with $L_{\mathrm{o}} = 4\,\mu\mathrm{H}$, $C_{\mathrm{o}} = 2\,\mathrm{nF}$ and a $16\,\mathrm{m\Omega}$ device: $\eta_{\mathrm{INV,8kW}} = 98.8\%$ and $\rho = 57\,\mathrm{kW/L}$; **(ii)** Hybrid concept for $3\,\mathrm{V/ns}$ with $L_{\mathrm{o}} = 16\,\mu\mathrm{H}$, $C_{\mathrm{o}} = 2.1\,\mathrm{nF}$ and a $32\,\mathrm{m\Omega}$ device: $\eta_{\mathrm{INV,8kW}} = 99.0\%$ and $\rho = 61\,\mathrm{kW/L}$; **(iii)** Active concept for $6\,\mathrm{V/ns}$ and a $16\,\mathrm{m\Omega}$ device: $\eta_{\mathrm{INV,8kW}} = 98.9\%$ and $\rho = 53\,\mathrm{kW/L}$; **(iv)** Active concept for $12\,\mathrm{V/ns}$ and a $16\,\mathrm{m\Omega}$ device: $\eta_{\mathrm{INV,8kW}} = 99.3\%$ and $\rho = 82\,\mathrm{kW/L}$.

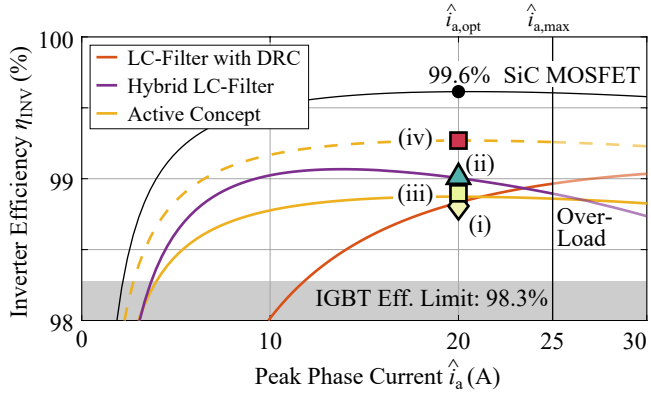

Fig. 7: Comparison of the load-dependent efficiency of the selected VSD inverter designs implementing the different filter concepts. The reference design has no $\mathrm{d}v/\mathrm{d}t$-limitation and represents an upper efficiency boundary for the other concepts. For a $\mathrm{d}v/\mathrm{d}t$-limit of $6\,\mathrm{V/ns}$ the hybrid concept achieves the highest peak efficiency of 98.8%, while for an output current above $24\,\mathrm{A}$ the passive concept performs best. Furthermore, the efficiency characteristic of the active concept ($12\,\mathrm{V/ns}$, dashed yellow line) and the efficiency limit of an IGBT inverter of 98.3% are shown.

where the factor 1.3 accounts for the difference between the sum of the boxed volumes of the components and the real system volume, i.e. the free space within the VSD inverter system.

The system efficiency is calculated with (7), where the three-phase losses are determined as $P_{\mathrm{L}} = 3\,(P_{\mathrm{L,HB}} + P_{\mathrm{C}} + P_{\mathrm{L,L}})$. There, $P_{\mathrm{L,L}}$ corresponds to the inductor losses, which can be approximated only by the low-frequency conduction losses, since the inductor current deviates from the machine current only during the switching transients, i.e. $i_{\mathrm{La,rms}} \approx i_{\mathrm{a,rms}}$.

In **Fig. 6**, the results of the $\eta\rho$-Pareto optimization for a part-load operation at $P_{\mathrm{M}} = 8\,\mathrm{kW}$ are shown. Beginning with the passive solutions, for the *LCR-filter concept* no designs are found for the given specifications, since for the specified damping resistance $R_{\mathrm{o}} < 4\,\Omega$ the 50% overshoot requirement cannot be met. On the other hand, the *LC-filter with DRC damping* achieves an inverter design efficiency of up to $\eta_{\mathrm{INV,8kW}} = 98.8\%$, which is limited by the dissipation of the energy stored in the filter capacitors, at a peak power density of $\rho_{\mathrm{max}} = 57\,\mathrm{kW/L}$ (cf. **Fig. 6(i)**). The considered design is implemented with $L_{\mathrm{o}} = 4\,\mu\mathrm{H}$, $C_{\mathrm{o}} = 2\,\mathrm{nF}$ and a $16\,\mathrm{m\Omega}$ device per switch and achieves a $\mathrm{d}v/\mathrm{d}t$-value of $\approx 7\,\mathrm{V/ns}$. The performance of the passive LC-filter with DRC damping cannot be further enhanced with higher $\mathrm{d}v/\mathrm{d}t$-values due to the given capacitance constraint of $C_{\mathrm{o}} \geq 2\,\mathrm{nF}$.

The *hybrid filter concept* overcomes the limitations of the passive approach. The Pareto optimal designs achieve a $\mathrm{d}v/\mathrm{d}t$-value in the range of $3\,\mathrm{V/ns}$. Higher $\mathrm{d}v/\mathrm{d}t$-values are not feasible as the peak current increases as a result of the capacitance limitation. The considered design with a maximum power density of $\rho_{\mathrm{max}} = 61\,\mathrm{kW/L}$ achieves an efficiency of $\eta_{\mathrm{INV,8kW}} = 99.0\%$, which corresponds to the highest efficiency among all concepts complying with the $\mathrm{d}v/\mathrm{d}t$-limit of $6\,\mathrm{V/ns}$ (cf. **Fig. 6(ii)**). It is implemented with $L_{\mathrm{o}} = 16\,\mu\mathrm{H}$, $C_{\mathrm{o}} = 2.1\,\mathrm{nF}$ and a $32\,\mathrm{m\Omega}$ device to account for the additional switching transitions.

The given $\mathrm{d}v/\mathrm{d}t$-value of $3\,\mathrm{V/ns}$ corresponds to a pulse-width of $t_{\mathrm{P}} \approx 370\,\mathrm{ns}$ and the required pulse pattern needs to be generated with a precision gate drive to prevent a timing error or a DRC damping network, similar to the one in **Fig. 4(b.i)**, needs to be added to dissipate the residual stored energy introduced by a possible timing mismatch. Circuit simulations revealed that a pulse-width error of 10%, e.g. a longer pulse-width of $t_{\mathrm{P}} = 410\,\mathrm{ns}$, leads to a considerable current error of almost $4\,\mathrm{A}$, however, with an installed DRC damping network of $C_{\mathrm{p}} = 10\,\mathrm{nF}$ and $R_{\mathrm{p}} = 18\,\Omega$ the energy loss is limited to $12\,\mu\mathrm{J}$, which results in only $190\,\mathrm{mW}$ of additional losses. Consequently, all components of the damping network can easily be implemented with SMD devices and neither the additional volume nor the increased losses of the damping network degrade the achieved performance of the hybrid filter concept.

The optimal *active concept* is implemented with a $16\,\mathrm{m\Omega}$ device and shows an efficiency of $\eta_{\mathrm{INV,8kW}} = 98.9\%$ at a maximum power density of $\rho_{\mathrm{max}} = 53\,\mathrm{kW/L}$, is similar in performance as the passive and hybrid concepts for low $\mathrm{d}v/\mathrm{d}t$-values below $6\,\mathrm{V/ns}$ (cf. **Fig. 6(iii)**). However, if higher $\mathrm{d}v/\mathrm{d}t$-values can be accepted, it clearly outperforms all other solutions as the switching losses continuously decrease with higher $\mathrm{d}v/\mathrm{d}t$. For example, for a voltage slope of $12\,\mathrm{V/ns}$, an inverter design efficiency of $\eta_{\mathrm{INV,8kW}} = 99.3\%$ at a power density of $\rho_{\mathrm{max}} = 82\,\mathrm{kW/L}$ is obtained (cf. **Fig. 6(iv)**).

Finally, in **Fig. 7**, the load-dependent efficiencies of the selected designs (cf. **Fig. 6**) are compared for part-load operation ($\hat{i}_{\mathrm{a}} < 25\,\mathrm{A}$), for nominal operation ($\hat{i}_{\mathrm{a}} = 25\,\mathrm{A}$) and for overload operation ($\hat{i}_{\mathrm{a}} > 25\,\mathrm{A}$), where e.g. the semiconductor heatsink and junction temperatures could increase above the specified limit. In addition, the load-dependent efficiency of an inverter without any $\mathrm{d}v/\mathrm{d}t$-limitation concept obtaining $\mathrm{d}v/\mathrm{d}t$-values up to $60\,\mathrm{V/ns}$ for the $16\,\mathrm{m\Omega}$ SiC MOSFET is given, which serves as an upper efficiency boundary for the analyzed $\mathrm{d}v/\mathrm{d}t$-filter concepts. This reference design achieves a peak efficiency of 99.6% at $\hat{i}_{\mathrm{a}} = 20\,\mathrm{A}$. Furthermore, the analyzed $\mathrm{d}v/\mathrm{d}t$-filter concepts are also compared to a state-of-the-art Si IGBT inverter, where a constant voltage drop of $2\,\mathrm{V}$ for both current directions, and a voltage/current overlap according to **Section II-A** for a $\mathrm{d}v/\mathrm{d}t$ of $6\,\mathrm{V/ns}$ is assumed. The resulting efficiency, which (for the assumptions made) is independent of the output current, is calculated as 98.3% and serves as a lower efficiency boundary.

As can be seen, the passive *LC-filter with DRC damping* is characterized by a poor part-load efficiency, which already for $\hat{i}_{\mathrm{a}} < 12\,\mathrm{A}$ falls below the Si IGBT inverter efficiency. However, at overload operation it features the highest efficiency of around 99% and even for $\hat{i}_{\mathrm{a}} = 30\,\mathrm{A}$ the junction temperature stays with $T_{\mathrm{J,SiC}} = 100\,^{\circ}\mathrm{C}$ well below the maximum allowed junction temperature.

In contrast, the SiC MOSFET inverter with either hybrid or active filter concept overcomes the state-of-the-art Si IGBT solution already for load currents above $5\,\mathrm{A}$ and thus even with the side condition of $\mathrm{d}v/\mathrm{d}t$-limited switching proves the possible performance gain of SiC MOSFETs in drive applications. The *hybrid concept* features the best part-load performance among all implementations at a $\mathrm{d}v/\mathrm{d}t$-value of $3\,\mathrm{V/ns}$, i.e. in fact with a two times slower voltage transient than the one assumed for the Si IGBT inverter. Only during overload operation, the efficiency of the hybrid concept drops below the efficiencies of the other concepts, as it shows a much stronger dependency of the switching losses on the output current, and consequently leads to the highest junction temperature of $T_{\mathrm{J,SiC}} = 130\,^{\circ}\mathrm{C}$. On the other hand, the efficiency of the *active concept* is much less load-dependent and is quasi constant around 98.85%. This is also reflected in the junction temperature, which for an overload condition of $\hat{i}_{\mathrm{a}} = 30\,\mathrm{A}$, just

stays below the specified $125\,^{\circ}\mathrm{C}$. As already mentioned, if higher $\mathrm{d}v/\mathrm{d}t$-values are tolerated, the efficiency of the active concept is further increased (up to 99.3%), but still keeps the same quasi load-independent characteristic and even for overload operation, a junction temperature of only $T_{\mathrm{J,SiC}} = 114\,^{\circ}\mathrm{C}$ results.

In conclusion, the hybrid approach is beneficially used in drive applications where low $\mathrm{d}v/\mathrm{d}t$-values are demanded and the drive system is mainly operated in the part-load range, while the active concept is the best choice, if the drive system is operated in a wide load range and higher $\mathrm{d}v/\mathrm{d}t$-values can be tolerated or the power component count should be minimized. For the sake of completeness it should be mentioned that in the performed Pareto optimization a large number of designs was discarded due to the minimum filter capacitance needed to minimize the influence of the machine impedances. To overcome this limitation, it is also possible to insert an additional CM-filter inductor or LCL-filter to better decouple the $\mathrm{d}v/\mathrm{d}t$-filter from the machine, or to even utilize the machine capacitance as part of the $\mathrm{d}v/\mathrm{d}t$-filter.

V. Conclusion

In this paper, different $\mathrm{d}v/\mathrm{d}t$-filter concepts are introduced and compared for a $10\,\mathrm{kW}$ three-phase SiC PWM inverter supplied from a $800\,\mathrm{V}$ DC-bus. The analyzed active filter concept can be realized using a simple Miller feedback capacitor and its efficiency reduction and/or losses are inversely proportional to the imposed $\mathrm{d}v/\mathrm{d}t$-limit. Passive filters are dissipating the energy stored in the filter capacitor, and are therefore only suitable for higher output currents. Alternatively, a hybrid concept employs an undamped LC-filter together with an adapted switching sequence and ensures a resonant output voltage transition without overshoot. Moreover, the filter itself is (ideally) lossless but the additional switching actions are increasing the semiconductor losses. Despite this, the hybrid filter concept achieves with 99.0% the highest part-load efficiency (at $8\,\mathrm{kW}$) of all analyzed options ensuring a $\mathrm{d}v/\mathrm{d}t$ below or equal to $6\,\mathrm{V}/\mathrm{ns}$. All filter structures, optimized regarding the bridge-leg semiconductor chip area, are ensuring a higher efficiency and power density than a Si IGBT reference design which underlies the possible performance gain associated with SiC MOSFETs in drive applications. In case of machine integrated inverter systems or machines with enhanced insulation systems, where higher $\mathrm{d}v/\mathrm{d}t$-ratings up to $12\,\mathrm{V}/\mathrm{ns}$ could be tolerated, the active filter concept enables a superior performance characterized in the considered case by an inverter maximum part-load efficiency of 99.3% and a power density above $80\,\mathrm{kW}/\mathrm{L}$.

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