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J. W. Kolar
T. Friedli
J. Rodriguez
P. W. Wheeler

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Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Review of Three-Phase PWM AC–AC Converter Topologies

Johann W. Kolar, *Fellow, IEEE*, Thomas Friedli, *Member, IEEE*,
Jose Rodriguez, *Fellow, IEEE*, and Patrick W. Wheeler, *Member, IEEE*

***Abstract*—This paper presents first an overview of the well-known voltage and current dc-link converter topologies used to implement a three-phase PWM ac–ac converter system. Starting from the voltage source inverter and the current source rectifier, the basics of space vector modulation are summarized. Based on that, the topology of the indirect matrix converter (IMC) and its modulation are gradually developed from a voltage dc-link back-to-back converter by omitting the dc-link capacitor. In the next step, the topology of the conventional (direct) matrix converter (CMC) is introduced, and the relationship between the IMC and the CMCs is discussed in a figurative manner by investigating the switching states. Subsequently, three-phase ac–ac buck-type chopper circuits are considered as a special case of matrix converters (MCs), and a summary of extended MC topologies is provided, including three-level and hybrid MCs. Therewith, a common knowledge basis of the individual converter topologies is established.**

***Index Terms*—AC–AC converter, current source converter, matrix converter (MC), voltage source converter.**

I. Introduction

CONVERTER systems with either a voltage or a current dc-link are mainly used nowadays for power conversion from a three-phase mains system to a three-phase load with an arbitrary voltage amplitude and frequency, as required, for example, for variable-speed drives. In the case of a converter with a voltage dc-link, the mains coupling can, in the simplest case, be implemented by a diode bridge. A pulse-controlled braking resistor must be placed across the dc-link, or an antiparallel thyristor bridge must be inserted on the mains side to enable generator (braking) operation of the load. The disadvantages are the relatively high mains distortion and high reactive power requirements.

A mains-friendly ac–ac converter with bidirectional power flow can be implemented by coupling the dc-link of a PWM rectifier and a PWM inverter. The dc-link quantity is then impressed by an energy storage element that is common to both stages: a capacitor C_{DC} for the voltage dc-link back-to-back converter [V-BBC; cf., Fig. 1(a)] or an inductor L_{DC} for the current dc-link back-to-back converter [C-BBC; cf., Fig. 1(b)]. The PWM rectifier is controlled in such a manner that a sinusoidal mains current is drawn, which is in-phase or antiphase with the corresponding mains line voltage. The implementation of the V-BBC and C-BBC requires 12 transistors (typically IGBTs) and 12 diodes or 12 reverse conduction IGBTs (RC-IGBTs) for the V-BBC and 12 reverse blocking IGBTs (RB-IGBTs) for the C-BBC.

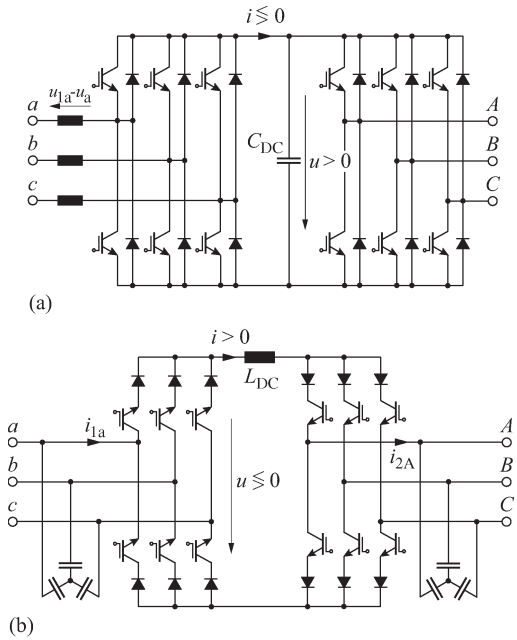

Fig. 1. Basic three-phase ac–ac converter topologies with dc-link energy storage. (a) V-BBC. (b) C-BBC.

Due to the dc-link energy storage element, there is an advantage that both converter stages are, to a large extent, decoupled regarding their control for a typical sizing of the energy storage. Furthermore, a constant mains-independent input quantity exists for the PWM inverter stage, which results in a high utilization of the converter's power capability. On the other hand, the dc-link energy storage element can have a relatively large physical volume compared with the total converter volume, and when electrolytic capacitors are used for the dc-link of the V-BBC, the service lifetime of the converter can potentially be reduced.

Aiming for high power densities, it is hence obvious to consider the so-called matrix converter (MC) concepts that enable three-phase ac–ac conversion without any intermediate

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J. W. Kolar and T. Friedli are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zurich, Switzerland (e-mail: kolar@lem.ee.ethz.ch; thomas.friedli@ieee.org).

J. Rodriguez is with the Department of Electronics Engineering, Universidad Tecnica Federico Santa Maria, Valparaiso 2390123, Chile (e-mail: jrp@usm.cl).

P. W. Wheeler is with the School of Electrical and Electronic Engineering, University of Nottingham, NG7 2RD Nottingham, U.K. (e-mail: pat.wheeler@nottingham.ac.uk).

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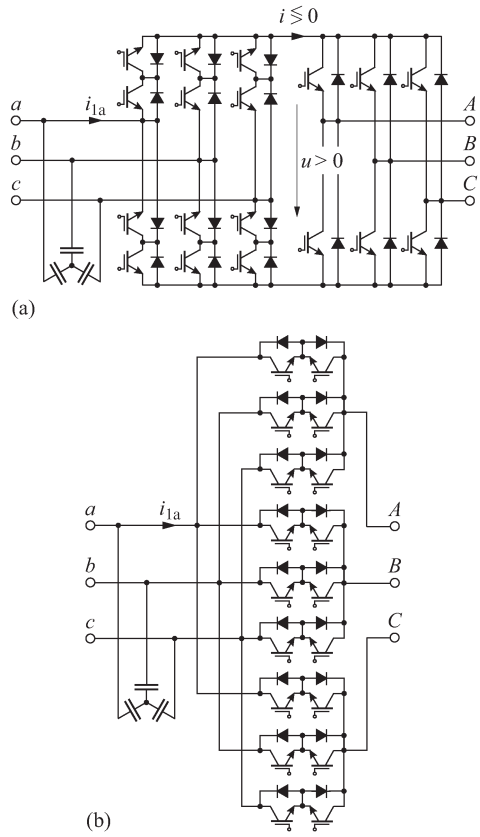

Fig. 2. Basic three-phase ac–ac MC topologies. (a) IMC. (b) CMC.

energy storage element. The physical basis of these systems is the constant instantaneous power provided by a symmetrical three-phase voltage–current system. Conventional (direct) MCs [CMCs; Fig. 2(b)] perform the voltage and current conversions in a single stage. Alternatively, the option of an indirect conversion by means of an indirect MC [IMC; Fig. 2(a)] exists. The IMC requires separate stages for the voltage and current conversions, in a similar way to the V-BBC and the C-BBC, but without an energy storage element in the intermediate link. The implementation of both MC topologies requires 18 IGBTs and 18 diodes, in the basic configuration, or 18 RB-IGBTs for the CMC or 12 RB-IGBTs and 6 RC-IGBTs for the IMC. Thus, the intermediate energy storage element is eliminated at the expense of more semiconductors.

MCs are frequently seen as a future converter concept for a wide area of applications ranging from mobile utility power supplies [32] to wind power generation systems [33], with a particular focus on bidirectional variable-speed drives. Despite intensive research over the last three decades, they have, until now, only achieved low market penetration. Excluding the technical aspects, the reasons for this could be the more complex modulation and dimensioning compared to converters with a dc-link and the high topological variations. A classification of the main forced commutated ac–ac converters presented in literature until now is shown in Fig. 3. Three subcategories are used: converters with dc-link energy storage, MCs, and intermediate category of hybrid MCs. A forced commutated ac–ac converter is considered as a MC if it does not require an intermediate energy storage in the power circuit as an essential functional element.

Starting with the well-known voltage and current dc-link converter topologies, Section II presents the three-phase PWM ac–ac converter systems with a dc-link energy storage element. Based on these converters and their space vector modulation, in Section III, the IMC is derived, and its basic modulation schemes are discussed. Next, in Section IV, the CMC is introduced, and the functional equivalence between the IMC and the CMC is investigated by comparing the switching states. In Section V, three-phase ac–ac buck converter topologies are presented as a subcategory of MCs with limited functionality compared to the CMC or IMC. Subsequently, in Section VI, a brief discussion of extended MC topologies is given, including three-level, hybrid, and cascaded MCs, which highlights the topological relations of the individual converter circuits. Finally, in Section VII, the basic ac–ac converter topologies, i.e., the V-BBC, C-BBC, IMC, and CMC, are compared based on easily quantifiable circuit properties, followed by a list of the main advantages and disadvantages of the MC compared to the industrially well-established V-BBC converter system. This review on ac–ac converter topologies concludes with a brief discussion of current trends and areas of concern in the research on MCs and highlights the need for a comprehensive comparison.

II. AC–AC Converters With DC-Link

In this section, the fundamentals of space vector modulation of PWM converters with a dc-link are briefly reviewed, and their functional equivalent circuit diagrams are shown. In the case of the V-BBC, the PWM inverter stage is considered, and for the C-BBC, the PWM rectifier stage is considered. This allows the development of the IMC topology by simply connecting the two subsystems and the modulation of the IMC by combination and coordination of the subsystems' modulation schemes.

A. Voltage DC-Link PWM Inverter

The PWM output stage (inverter) of the V-BBC, shown in Fig. 4(a), is made up of three bridge legs. Each exhibits the function of a switch that connects the output to either the positive or the negative dc-bus p and n. The switching state of the inverter is defined by (xxx) where x is either p or n; for example, (pnn) means that the output A is connected to p and that the outputs B and C are connected to n. The control of the switch is carried out in such a way that, over a pulse period T_P, an average voltage space vector $\bar{\vec{u}}_2 = \vec{u}_2^*$ is formed at the output of the inverter, where $\vec{u}_2^*$ is the output voltage reference value and "$\bar{}$" is the local average value of a pulse period.

In the simplest case, the two voltage space vectors closest to $\vec{u}_2^*$ and a freewheeling state must be utilized per pulse period to generate a sinusoidal symmetric three-phase voltage system at the converter output with an output voltage amplitude $\hat{U}_2^*$ and an output frequency ω_2^*

$$\vec{u}_2^* = \hat{U}_2^* e^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* e^{j\omega_2^* t}. \quad (1)$$

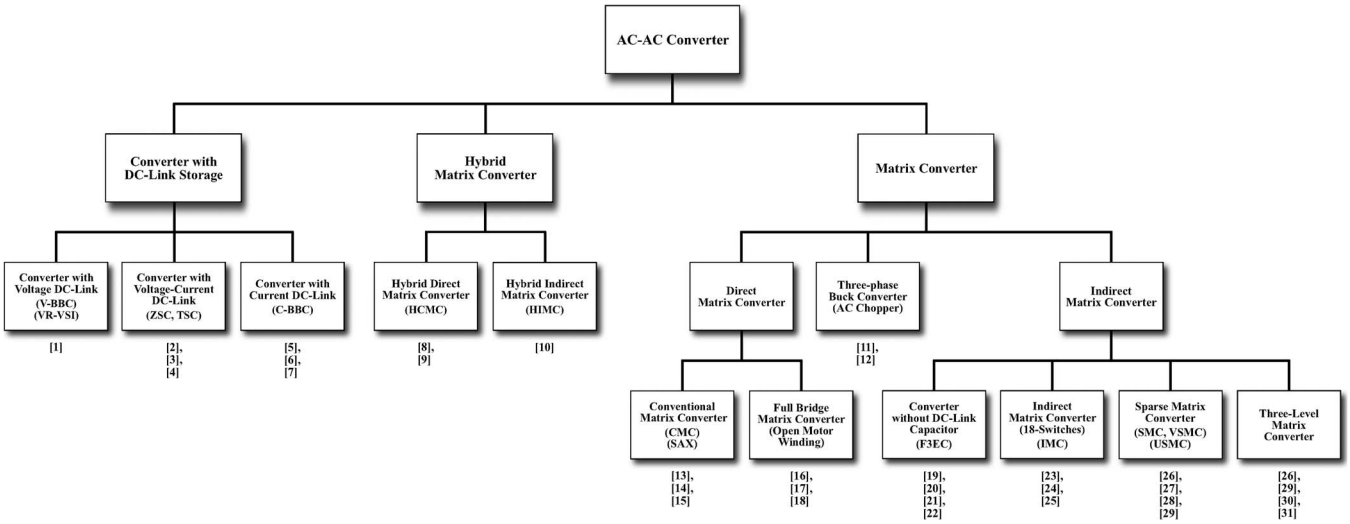

Fig. 3. Classification of three-phase ac–ac converter topologies with references to the technical literature.

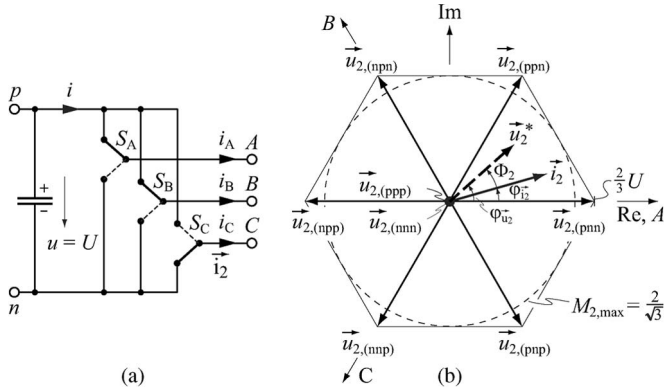

Fig. 4. (a) Idealized circuit representation and (b) voltage space vector diagram of the PWM output stage (inverter) of the V-BBC.

The following possible switching state sequences result to the phase angle range $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$ of $\vec{u}_2^*$ considered in Fig. 4(b)

$$\ldots \left| \begin{matrix} (\underline{p}nn)-(\underline{p}pn)-(\underline{p}pp) \\ t_\mu=0 \end{matrix} \right| \left| \begin{matrix} (\underline{p}pp)-(\underline{p}pn)-(\underline{p}nn) \\ t_\mu=T_P/2 \end{matrix} \right| \begin{matrix} \ldots \\ t_\mu=T_P \end{matrix} \tag{2}$$

$$\ldots \left| \begin{matrix} (pp\underline{n})-(pn\underline{n})-(nn\underline{n}) \\ t_\mu=0 \end{matrix} \right| \left| \begin{matrix} (nn\underline{n})-(pn\underline{n})-(pp\underline{n}) \\ t_\mu=T_P/2 \end{matrix} \right| \begin{matrix} \ldots \\ t_\mu=T_P \end{matrix} \tag{3}$$

in order to ensure

$$\begin{aligned} \bar{\vec{u}}_2 &= \frac{1}{T_P}\int_0^{T_P} \vec{u}_{2,j}\,dt_\mu = d_{(\mathrm{pnn})}\vec{u}_{2,(\mathrm{pnn})} + d_{(\mathrm{ppn})}\vec{u}_{2,(\mathrm{ppn})} \\ &= d_{(\mathrm{pnn})}\frac{2}{3}U + d_{(\mathrm{ppn})}\frac{2}{3}Ue^{j\pi/3} \\ &= \vec{u}_2^*. \end{aligned} \tag{4}$$

The dc-link current levels can be simply obtained by the projection of the output current space vector $\vec{i}_2$ onto the instantaneous active voltage space vector. The restriction of operation to a single freewheeling state per pulse period [cf., (2) and (3)] leaves one bridge leg clamped to p or n, and hence, there are no switching losses in that bridge leg. It is advantageous to change the clamping between the phases in such a way that the phase carrying the highest current is not switched. At an approximately ohmic load, e.g., a permanent magnet synchronous machine, therefore, for the phase angle $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$, phase A should be permanently connected to p, and for $\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$, phase C should be permanently connected to n. The corresponding switching state sequences with the dc-link current waveforms are shown in Fig. 5. Whichever switching state sequence is used, a fundamental amplitude of the output line voltage can be formed without overmodulation, where the modulation index M_2 is defined as

$$M_2 = \frac{\hat{U}_2^*}{U/2} = \left[0, \frac{2}{\sqrt{3}}\right]. \tag{5}$$

The current conversion of the converter from the output to the dc-link is determined not only by the switching states or the modulation index but also by the phase displacement angle Φ_2 between $\vec{i}_2$ and $\vec{u}_2^*$. The average dc-link current, which is formed from the line current blocks, is thus given by

$$\bar{i} = I = \frac{3}{4}M_2\hat{I}_2\cos(\Phi_2). \tag{6}$$

It decreases with increasing Φ_2 from its maximum value for $\Phi_2 = 0$ or $\Phi_2 = \pi$ to zero for $\Phi_2 = \pm\pi/2$. Thus, the output voltage $\hat{U}_2^*$ is directly formed from the dc-link voltage independent of the load. In contrast, the backward current conversion is determined not only by the load amplitude $\hat{I}_2$ resulting from $\hat{U}_2^*$ and ω_2^* but also by the phase displacement Φ_2 of the load.

Fig. 6 shows the characteristic input and output waveforms of the V-BBC [cf., Fig. 1(a)] for an inductive load.

B. Current DC-Link PWM Rectifier

The PWM input stage (rectifier) of the C-BBC, shown in Fig. 7(a), features the basic functionality of a diode bridge with

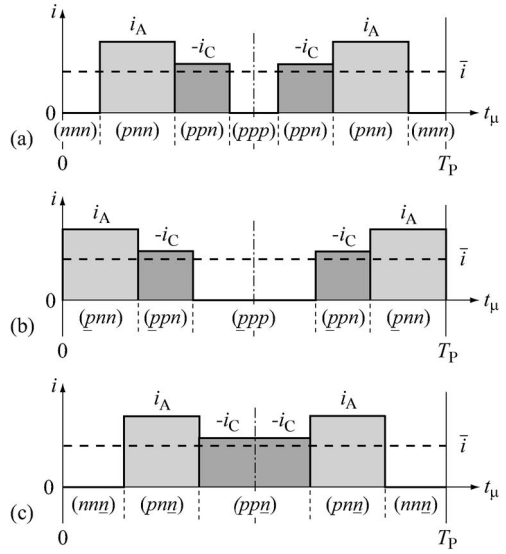

Fig. 5. DC-link current i waveform for one pulse period T_P. (a) Pulse pattern $(nnn) - (pnn) - (ppn) - (ppp)$. (b) Clamping pulse pattern $(\underline{p}nn) - (\underline{pp}n) - (\underline{ppp})$. (c) Clamping pulse pattern $(nn\underline{n}) - (pn\underline{n}) - (pp\underline{n})$.

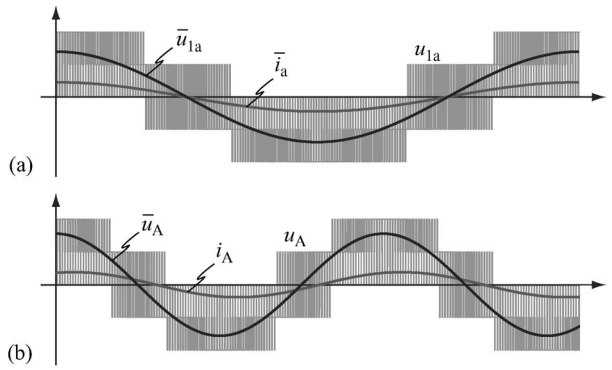

Fig. 6. Characteristic waveforms of the V-BBC for $\omega_1 < \omega_2$, $\Phi_1 \approx 0$, and $\Phi_2 = \pi/9$ (inductive load). (a) Input voltage u_{1a}, over T_P averaged input voltage $\bar{u}_{1a}$, and over T_P averaged input line current $\bar{i}_a$. (b) Output line voltage u_A, over T_P averaged output line voltage $\bar{u}_A$, and output line current i_A.

respect to the conducting state of the power transistors. The control of the power transistors must guarantee that a path for the impressed dc-link current is always available when no separate freewheeling diode is used across the dc-link. Therefore, at least one transistor of the positive and one transistor of the negative bridge-halves must always be held in the ON-state.

If a sinusoidal symmetric three-phase input current system $\bar{\vec{i}}_1 = \vec{i}_1^*$ is to be formed with an input current amplitude $\hat{I}_1$, a mains frequency ω_1, and a reference phase displacement angle Φ_1^* between $\vec{i}_1^*$ and $\vec{u}_1$

$$\bar{\vec{i}}_1 = \vec{i}_1^* = \hat{I}_1^* e^{j\varphi_{\vec{i}_1^*}} = \hat{I}_1^* e^{j\left(\omega_1 t - \Phi_1^*\right)} \tag{7}$$

then, in analogy to the considerations for the V-BBC, the switching states with the current space vectors closest to $\vec{i}_1^*$ must be selected. Thus, for the phase angle range $\varphi_{\vec{i}_1^*} \in [-\pi/6, +\pi/6]$, considered in Fig. 7(b), three possible switching

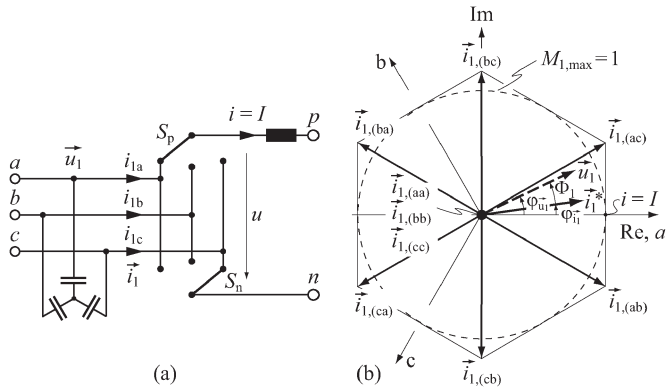

Fig. 7. (a) Idealized circuit representation and (b) current space vector diagram of the PWM input stage (rectifier) of the C-BBC.

state sequences may be employed

$$\ldots \left| \begin{matrix} (\underline{a}b) - (\underline{a}c) - (\underline{a}a) \\ t_\mu = 0 \end{matrix} \right| \left| \begin{matrix} (\underline{a}a) - (\underline{a}c) - (\underline{a}b) \\ t_\mu = T_P/2 \end{matrix} \right| \begin{matrix} \ldots \\ t_\mu = T_P \end{matrix} \tag{8}$$

$$\ldots \left| \begin{matrix} (\underline{a}c) - (\underline{a}b) - (\underline{a}a) \\ t_\mu = 0 \end{matrix} \right| \left| \begin{matrix} (\underline{a}a) - (\underline{a}b) - (\underline{a}c) \\ t_\mu = T_P/2 \end{matrix} \right| \begin{matrix} \ldots \\ t_\mu = T_P \end{matrix} \tag{9}$$

$$\ldots \left| \begin{matrix} (\underline{a}c) - (\underline{a}a) - (\underline{a}b) \\ t_\mu = 0 \end{matrix} \right| \left| \begin{matrix} (\underline{a}b) - (\underline{a}a) - (\underline{a}c) \\ t_\mu = T_P/2 \end{matrix} \right| \begin{matrix} \ldots \\ t_\mu = T_P \end{matrix} \tag{10}$$

which differ regarding the commutation voltages of the individual switching transitions. Therefore, for a given Φ_1^*, different switching losses result, which is investigated in detail in [6] and [7]. It is important to note that, in contrast to the converter with impressed dc-link voltage, the freewheeling state can now also be placed between two active switching states. Starting from one of the two active states, this can be achieved by changing the state of just a single switch. It can be derived from the converter modulation function that a line current amplitude equal to the magnitude of the dc-link current can be formed without overmodulation. The modulation index M_1 is defined as

$$M_1 = \frac{\hat{I}_1^*}{I} = [0, 1]. \tag{11}$$

The output voltage u of the input stage (voltage across the link) for the individual switching states for one pulse period is shown in Fig. 8. As can be seen, the individual voltage levels may be simply obtained by projecting the mains voltage space vector $\vec{u}_1$ onto the instantaneous active current space vector. The current on the input side, particularly the resulting current amplitude, is determined by the nature of the converter, and the output voltage formation is dependent on the (selectable) phase displacement angle Φ_1^* in order to fulfill the power balance requirement. The average output voltage decreases with increasing Φ_1^*.

$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos\left(\Phi_1^*\right). \tag{12}$$

Therefore, the instantaneous values of the mains line-to-line voltages become smaller and display positive and negative polarities until, for $|\Phi_1^*| = \pi/2$ (purely reactive input current), $\bar{u} = 0$ results. A further increase of Φ_1^* leads to the reversal of

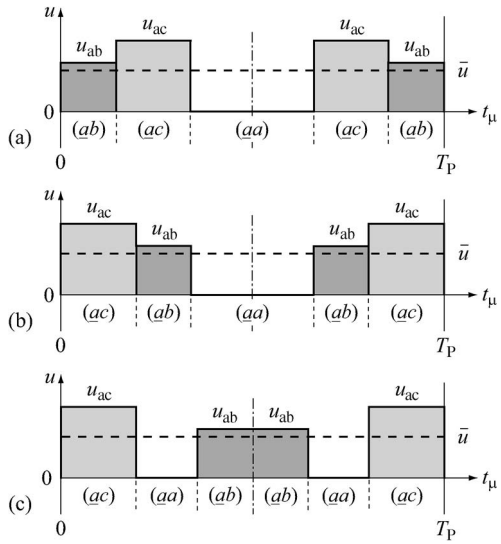

Fig. 8. DC-link voltage u waveform for one pulse period T_P. (a) Pulse pattern $(\underline{a}b) - (\underline{a}c) - (\underline{a}a)$. (b) Pulse pattern $(\underline{a}c) - (\underline{a}b) - (\underline{a}a)$. (c) Pulse pattern $(\underline{a}c) - (\underline{a}a) - (\underline{a}b)$.

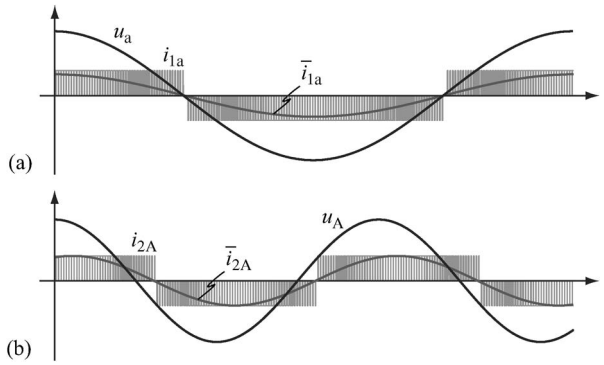

Fig. 9. Characteristic waveforms of the C-BBC for $\omega_1 < \omega_2$, $\Phi_1 \approx 0$, and $\Phi_2 = \pi/9$ (inductive load). (a) Input line voltage u_a, input current i_{1a}, and over T_P averaged input current $\bar{i}_{1a}$. (b) Output line voltage u_A, output current i_{2A}, and over T_P averaged output current $\bar{i}_{2A}$.

the polarity of the output voltage and the reversal of the power flow. The maximum value of the output voltage is obtained only for $\Phi_1^* = 0$.

Fig. 9 shows the characteristic input and output waveforms of the C-BBC [cf., Fig. 1(b)] for an inductive load.

III. IMC

The basis for the analysis of MC circuits is created by considering the basic functionality and modulation of the ac–dc converter with impressed output current (input stage of the C-BBC) and the dc–ac converter with impressed input voltage (output stage of the V-BBC). In the following, the topology of the IMC is developed, starting from the topology of the V-BBC.

A. AC–AC Converter With Voltage Link Without Intermediate Energy Storage (F3EC)

In order to derive an MC topology from the ac–ac converter with a dc-link capacitor, it is obvious to first consider that

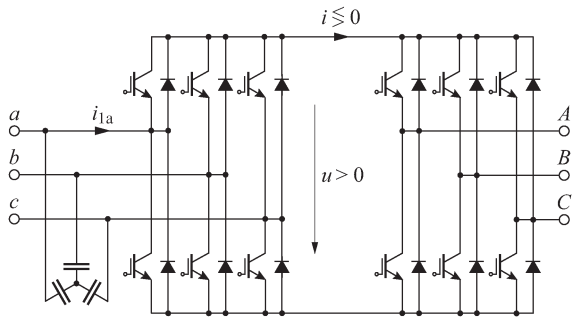

Fig. 10. Indirect ac–ac converter with an intermediate link without energy storage, also known as F3EC.

the topology of the V-BBC, where the dc-link capacitor is omitted, respectively, becomes the input filter capacitors, as shown in Fig. 10. Such a converter system was suggested in [19] and was investigated in more detail in [20]–[22], and it is in industrial use. The input filter capacitors are required to provide impressed voltages at the input due to the impressed load currents at the output.

The input stage of the converter system in Fig. 10 represents a synchronous three-phase rectifier. Its conductive state is directly defined by the mains voltage, and it cannot be influenced through the control. The load line current segments in the link, which are generated by the PWM output stage, are supplied by the input stage through the diodes with the highest instantaneous mains line-to-line voltage across them. In order to avoid a mains phase short circuit, only the power transistors that are connected in antiparallel to a conducting diode may be switched on. The transistors of the input stage thus have no influence on the formation of the link voltage for a positive link current $i > 0$ and only permit a reversal of the current flow direction. This is needed as negative components of the link current occur for $|\Phi_2| > \pi/6$ or during energy feedback into the mains, where a negative mean value of the link current exists. The switching frequency of the input stage transistors is equal to the mains frequency. It is for this reason that this topology is referred to as fundamental frequency frontend converter (F3EC). The switching state of the input stage can be changed at zero current within a freewheeling interval of the PWM output stage. Consequently, there are no switching losses of the input stage. Hence, the F3EC system enables higher energy conversion efficiency than the V-BBC and still allows bidirectional power flow. However, the variation of the link voltage at six times the mains frequency represents a fundamental disadvantage. As shown in Fig. 11, the minimum link voltage is equal to

$$u_{\min} = \frac{3}{2}\hat{U}_1 \tag{13}$$

and thus limits the amplitude of the output voltage to

$$\hat{U}_2^* \leq \frac{2}{\sqrt{3}}\frac{1}{2}u_{\min} = \frac{\sqrt{3}}{2}\hat{U}_1 \approx 0.86\,\hat{U}_1 \tag{14}$$

when operated without overmodulation. We shall find the same limitation of the output voltage later for the IMC and CMC. Furthermore, for a constant power of the load, a variation of the

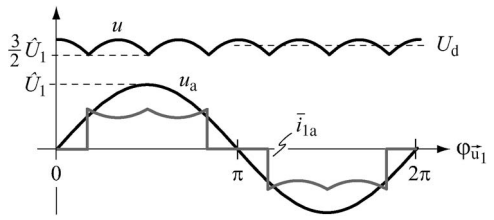

Fig. 11. Waveforms of the mains line voltage u_a, the over T_P averaged input line current $\bar{i}_{1a}$, and the link voltage u of the F3EC in Fig. 10.

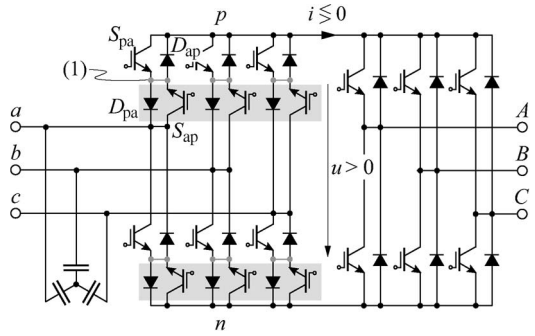

Fig. 12. Development of the topology of the IMC by extension of the F3EC with the components on gray backgrounds. (1) Optional connections.

local average value of the link current occurs, which is inversely proportional to the variation of the link voltage and appears in the two input phases of the conducting diodes. The system thus exhibits a relatively high power factor of $\lambda \approx 0.95$, but because of the $\pi/3$-wide gap in the input line currents, it also features relatively high harmonic current distortions. In order to obtain a sinusoidal input current, the circuit in Fig. 10 has to be extended in such a way that the conductive state of the input stage can be directly defined, which is independent of the mains voltage.

B. IMC

In order to be able to control the conductive state of the input stage, it is first necessary to place a power transistor in series with each diode, e.g., $S_{\rm ap}$ and $D_{\rm ap}$, in Fig. 12. However, when this series transistor blocks, a forward voltage can occur, which must not appear across the antiparallel transistor $S_{\rm pa}$ and which is used for the reverse power flow. This is achieved by adding the diode $D_{\rm pa}$ in series with $S_{\rm pa}$. The input stage now consists of two mutually antiparallel-connected current link PWM rectifier stages. Together with the PWM inverter output stage, they form the topology of the IMC. The power transistor and diode combinations between the input phases and the positive and negative buses form separately controllable four-quadrant switches, which could also be implemented by an antiparallel connection of RB-IGBTs.

A short circuit of two mains phases would result from simultaneously switching on of two four-quadrant switches of the upper or lower bridge-halves and must therefore be avoided. The basic function of the input stage can thus be abstracted in the same way as that for the input stage of the C-BBC and can be represented by means of two single-pole triple-throw

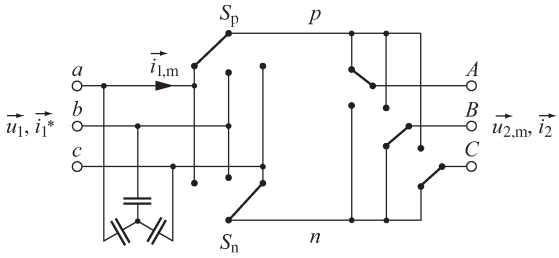

Fig. 13. Idealized circuit representation of the IMC. $\vec{i}_{1,m}$ and $\vec{u}_{2,m}$ denote the modulated input current and output voltage space vectors.

switches. With respect to the modulation, the IMC represents a combination of the input stage of the C-BBC, with the dc-link inductor moved to the load side, and the output stage of the V-BBC, with the dc-link capacitor moved to the mains side. The idealized circuit is shown in Fig. 13.

The modulation of the system is carried out such that, for a given input voltage $\vec{u}_1$, only positive line-to-line voltages are switched to the link, and the desired output voltage $\bar{\vec{u}}_2 = \vec{u}_2^*$ is formed along with a sinusoidal input current $\bar{\vec{i}}_1$ with a defined phase reference displacement angle Φ_1^*. On the input side, only the phase angle $\varphi_{\bar{\vec{i}}_1}^*$ can be predetermined but not the amplitude of the input current. The current amplitude adjusts itself through the load current segments, which reach the input through the link in such a way that the mains provide the real power required by the load.

Commencing, for instance, from $\varphi_{\vec{u}_1} \in [0, \pi/6]$ [cf., Fig. 14(a)] and projecting $\vec{u}_1$ onto the axes ab, ac, and bc lead to positive link voltages. Correspondingly, the switching states (ab), (ac), and (bc) of the input stage or the line-to-line voltages $u_{\rm ab}$, $u_{\rm ac}$, and $u_{\rm bc}$ are permissible within the particular segment of $\varphi_{\vec{u}_1}$. The output stage can form a space vector hexagon for each of these link voltages. A total of 18 different active voltage vectors and a zero vector are possible, with these being attainable by both the freewheeling states (nnn) and (ppp) of the output stage and by the freewheeling states (aa), (bb), and (cc) of the input stage [cf., Fig. 14(b)]. The IMC thus exhibits a variety of output voltage space vectors (similar to a three-level converter).

Regarding the current transfer from the load side to the input, the consideration is again limited to a $\pi/3$-wide interval, in this case, of the output period to $\varphi_{\vec{i}_2} \in [-\pi/6, +\pi/6]$, respectively, $i_A > 0$, $i_B < 0$, and $i_C < 0$. For the switching states (pnn), (ppn), and (pnp), instantaneous positive link currents $i_{(\rm pnn)} = i_A$, $i_{(\rm ppn)} = -i_C$, and $i_{(\rm pnp)} = -i_B$ occur. Link currents of the same absolute value but of inverse polarity $i_{(\rm npp)} = -i_A$, $i_{(\rm nnp)} = +i_C$, and $i_{(\rm npn)} = +i_B$ result to the inverse switching states (npp), (nnp), and (npn). The link currents are then translated into input current space vectors according to the switching state of the input stage. As stated previously, only the switching states (ab), (ac), and (bc) enable a positive link voltage, and hence, they are admissible.

If, for example, the input stage is in the switching state (ac), three input current space vectors are obtained, which point in the direction ac. They result from the instantaneous link current values of the three possible switching states (pnn), (ppn), and (pnp) of the output stage. Correspondingly, negative link

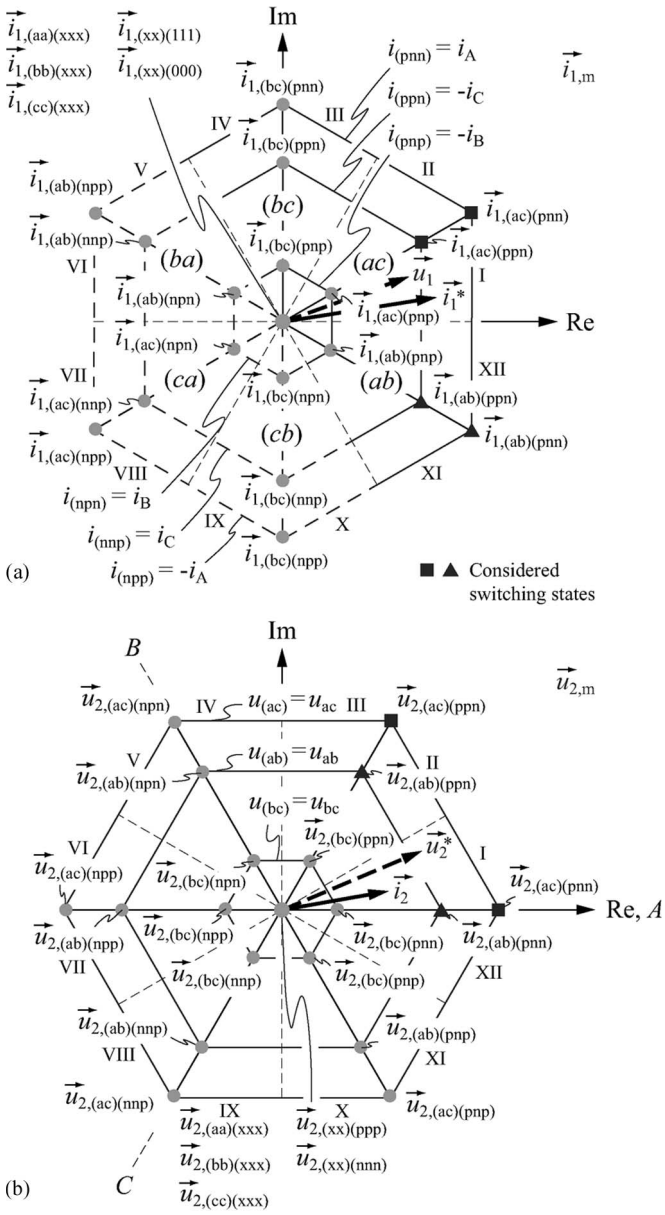

Fig. 14. (a) Current and (b) voltage conversions of the IMC for the input voltage and output current space vector $\vec{u}_1$ and $\vec{i}_2$. To maintain $u > 0$, input current space vectors in the direction of ca, ba, cb (dotted) can only be formed by inversion of the link current, i.e., inversion of the switching state of the output stage.

current values result to the inverse switching states of the output stage and lead to the input current space vectors $\vec{i}_{1,(\mathrm{ac})(\mathrm{npp})} = -\vec{i}_{1,(\mathrm{ac})(\mathrm{pnn})}$, $\vec{i}_{1,(\mathrm{ac})(\mathrm{nnp})} = -\vec{i}_{1,(\mathrm{ac})(\mathrm{ppn})}$, and $\vec{i}_{1,(\mathrm{ac})(\mathrm{npn})} = -\vec{i}_{1,(\mathrm{ac})(\mathrm{pnp})}$, oriented in the opposite direction to ac, which is in the direction ca. The input current space vectors of the mutually inverse switching states of the output stage have the same absolute values

$$\begin{aligned} |\vec{i}_{1,(\mathrm{ac})(\mathrm{pnn})}| &= |\vec{i}_{1,(\mathrm{ac})(\mathrm{npp})}| = i_A \\ |\vec{i}_{1,(\mathrm{ac})(\mathrm{ppn})}| &= |\vec{i}_{1,(\mathrm{ac})(\mathrm{nnp})}| = -i_C \\ |\vec{i}_{1,(\mathrm{ac})(\mathrm{pnp})}| &= |\vec{i}_{1,(\mathrm{ac})(\mathrm{npn})}| = -i_B. \end{aligned} \tag{15}$$

During the freewheeling states of the output stage [(nnn) or (ppp)], no link current occurs, and hence, no input current can be generated. The same applies for the freewheeling states (aa), (bb), and (cc) of the input stage, which close the link current path without inclusion of the mains input voltages. Correspondingly, no output voltage can be formed.

Through a suitable combination of switching states, a desired reference value of the output voltage $\vec{u}_2^*$ and, simultaneously, a desired phase angle $\varphi_{\vec{i}_1}^*$ of the input current $\vec{i}_1$ can be formed. $\varphi_{\vec{i}_1}^*$ is finally determined by the angular position $\varphi_{\vec{u}_1}$ of the input voltage space vector $\vec{u}_1$ and the desired phase shift Φ_1^* of $\vec{i}_1$ with reference to $\vec{u}_1$ ($\varphi_{\vec{i}_1}^* = \varphi_{\vec{u}_1} - \Phi_1^*$).

In order to maximize the output voltage control range, the input stage should always provide the largest instantaneous link voltage. Thus, for the whole pulse period, the modulation would be limited to the outermost voltage space vector hexagon [cf., Fig. 14(b)]. This corresponds to the switching state (ac) of the input stage or the link voltage $u_{(\mathrm{ac})} = u_{\mathrm{ac}}$ for the case under consideration. By inspection of the input current space vector diagram in Fig. 14(a), this would, however, not allow generation of the desired $\varphi_{\vec{i}_1}^*$ as only two input phases (a and c) are connected to the link. Consequently, over the entire pulse period, an input current space vector would be formed in the direction ac. The absolute value of the vector would be equal to the values $i_{1,(ac)(pnn)} = i_A$, $i_{1,(ac)(ppn)} = -i_C$, and $i_{1,(ac)(nnn)} = i_{1,(ac)(ppp)} = 0$. Within an entire mains period, the input current space vector would thus retain the direction of a line-to-line axis [cf., ac, bc, ba, etc., in Fig. 14(a)] within $\pi/3$-wide segments, which would lead to a block-shaped input current waveform, as for the F3EC topology in Fig. 11.

In order to always obtain the desired phase angle and a continuous rotation of the input current space vector $\vec{i}_1$ to ensure a sinusoidal input current, it is mandatory to include a second active switching state of the input stage (in this case (ab)) in the modulation scheme. This leads to a second link voltage level $u_{(\mathrm{ab})} = u_{\mathrm{ab}}$ and, hence, to a second output voltage space vector hexagon. For the modulation of the IMC, a switching state sequence must therefore be employed, which combines the active switching states $(ac)(ppn), (ac)(pnn), (ab)(ppn)$, and $(ab)(pnn)$ and the freewheeling states $(xx)(ppp)$ and $(xx)(nnn)$ or $(aa)(xxx)$, $(bb)(xxx)$, and $(cc)(xxx)$.

1) Modulation Scheme A—Zero Current Switching of the Input Stage: One method consists of leaving the input stage, at first, in the switching state (ac), while the output stage cycles through the switching state sequence $(pnn) - (ppn) - (ppp)$. In this way, voltage space vectors pointing to the corners of the triangular segment of the space vector plane, valid for $u = u_{ac}$, are generated. Thereby, the input current space vector in the direction ac is left in place. Next, the switching state of the input stage is changed to (ab). Consequently, only input current space vectors oriented in the direction ab are formed, while the output stage repeats the switching state sequence advantageously in reverse order $(ppp) - (ppn) - (pnn)$. However, the voltage space vector magnitudes are now equal to $u = u_{\mathrm{ab}}$. When the end of the first pulse half-period is reached, the sequence is then

immediately repeated in the opposite direction. The resulting switching state sequence may be written as

$$\begin{aligned}&\ldots|_{t_\mu=0}(ac)(pnn)-(ac)(ppn)-(ac)(ppp)\\&\quad-(ab)(ppp)-(ab)(ppn)-(ab)(pnn)|_{t_\mu=T_P/2}(ab)(pnn)\\&\quad-(ab)(ppn)-(ab)(ppp)-(ac)(ppp)-(ac)(ppn)\\&\quad-(ac)(pnn)|_{t_\mu=T_P}\ldots.\end{aligned}\tag{16}$$

The third possible switching state of the input stage [state (bc)] is omitted as the modulation can be limited in this case to those two switching states, which lead to the higher link voltages and, hence, to the maximum possible output voltage $(u_{\rm ac}>u_{\rm ab}>u_{\rm bc})$.

The switching cycle of the output stage is embedded in the switching cycle of the input stage for the switching state sequences, shown in (16). Thus, for a complete cycle of the current space vector triangle, the voltage space vector triangle is run through twice with different link voltages. The switching state sequence basically exhibits the form given in (10) for the current dc-link rectifier. The switching of the input stage occurs during the freewheeling state of the output stage for the modulation scheme presented. It thus has the advantage that the change of the input stage switching state takes place when the link current is equal to zero such that no switching losses occur in the input stage.

2) Modulation Scheme B—Zero Voltage Switching of the Output Stage: As an alternative to modulation scheme A, the switching state of the output stage is initially kept constant, e.g., (pnn) may be assumed at the start of the pulse period. The input stage then cycles through the switching state sequence $(ac)-(ab)-(aa)$ with a fixed output stage switching state. Thereby, a current space vector triangle at the input is run through. Subsequently, the switching state of the output stage is changed from (pnn) to (ppn), whereupon a new phase angle of the discrete output voltage space vector results. The switching state sequence of the input stage is then cycled through in reverse order $(aa)-(ab)-(ac)$, and the first pulse half-period ends. During the second half-period, the entire sequence is repeated in reverse order and leads to the switching state sequence

$$\begin{aligned}&\ldots|_{t_\mu=0}(ac)(pnn)-(ab)(pnn)-(aa)(pnn)\\&\quad-(aa)(pnn)-(ab)(pnn)-(ac)(pnn)|_{t_\mu=T_P/2}(ac)(ppn)\\&\quad-(ab)(ppn)-(aa)(ppn)-(aa)(ppn)-(ab)(ppn)\\&\quad-(ac)(ppn)|_{t_\mu=T_P}\ldots\end{aligned}\tag{17}$$

This modulation scheme is known, in principle, from the ac–ac converter with a current dc-link [cf., (9)], and for the IMC, it is described in more detail in [29]. The switching sequence of the input stage is embedded in the switching sequence of the output stage, and thus, the switching losses occur in the input stage. The change of the switching state of the input stage must be carried out at full link current for modulation scheme B. Hence, a relatively complex multistep commutation strategy must be applied to the CMC (cf., Section IV). In contrast, the implementation of modulation scheme A is comparatively simple. The four-quadrant switches of the input stage can be switched at zero current, and only a small safety time is required to avoid short circuiting the mains phases. Modulation scheme A is clearly preferable for practical purposes compared to modulation scheme B and is therefore taken as the basis for further considerations.

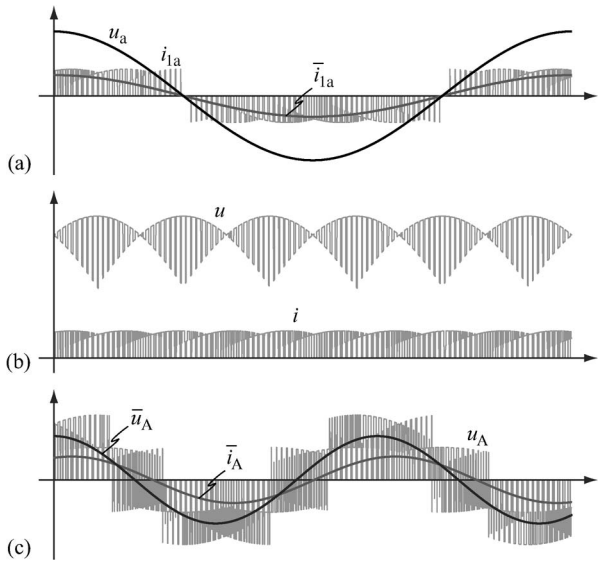

Fig. 15. Characteristic waveforms of the IMC for $\omega_1<\omega_2$, $\Phi_1\approx 0$, and $\Phi_2=\pi/9$ (inductive load). (a) Input line voltage u_a, input current i_{1a}, and over T_P averaged input current $\bar{i}_{1a}$. (b) Link voltage u and link current i. (c) Output line voltage u_A, over T_P averaged output line voltage $\bar{u}_A$ and output line current $\bar{i}_A$.

It should be noted that the maximum voltage transfer ratio of the IMC is independent of the selected modulation scheme and is limited, without overmodulation and for unity input power factor, to

$$\hat{U}^*_{2,\max}=\frac{\sqrt{3}}{2}\hat{U}_1\tag{18}$$

similar to the F3EC. For a general phase displacement angle at the input

$$\hat{U}^*_{2,\max}=\frac{\sqrt{3}}{2}\hat{U}_1\cos\left(\Phi^*_1\right)\tag{19}$$

applies. As discussed for the C-BBC, also for the IMC, the link voltage decreases with increasing Φ^*_1, which results in a reduction of the achievable maximum output voltage.

Fig. 15 shows the characteristic input, link, and output waveforms of the IMC [cf., Fig. 2(a)] for modulation scheme A and for an inductive load.

C. SMC

As shown in Fig. 12, the input stage of the IMC is implemented with six four-quadrant switches, and it could therefore also be operated with a negative link voltage $u<0$. On the other hand, for the PWM output stage, it is mandatory to maintain $u>0$ due to the diodes. It is hence obvious to consider a reduction in the number of switches by limiting the operating

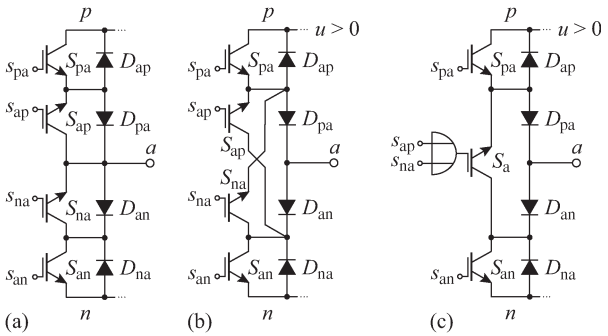

Fig. 16. Derivation of (c) the input stage bridge-leg topology of the SMC, starting from (a) the bridge-leg topology of the IMC.

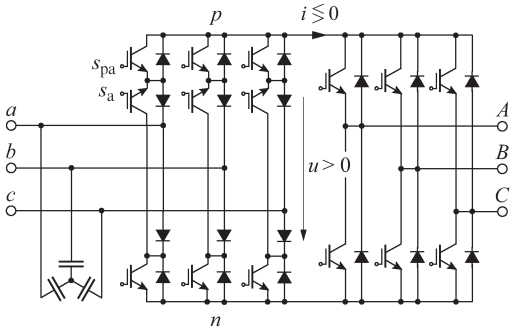

Fig. 17. Circuit topology of the SMC.

range of the PWM input stage to a unipolar link voltage that retains the option of bidirectional current flow.

The derivation of a simplified bridge-leg structure of the IMC is shown in Fig. 16. It is assumed, with reference to Fig. 16(a), that phase a of the IMC is connected bidirectionally with the positive link bus p. This means that $S_{\rm pa}$ and $S_{\rm ap}$ are switched on and $S_{\rm an}$ and $S_{\rm na}$ are switched off. The positive link voltage then always appears as a blocking voltage across $S_{\rm an}$. Thus, the function of $S_{\rm na}$ is limited to providing a current path from the negative link bus n via $D_{\rm na}$ to the input terminal a. No direct connection of the emitter of $S_{\rm na}$ with a is required for this purpose. The current return path can be provided through $S_{\rm na}$ and $D_{\rm pa}$. An analogous consideration for $S_{\rm ap}$ leads to the direct parallel connection of $S_{\rm na}$ and $S_{\rm ap}$, shown in Fig. 16(b). A further simplification may be achieved by replacing $S_{\rm na}$ and $S_{\rm ap}$ by a single switch S_a according to Fig. 16(c). The effort for the implementation of the IMC is thus reduced from 18 transistors and 18 diodes to 15 transistors and 18 diodes.

This circuit variant of an IMC, shown in Fig. 17, is referred to as sparse MC (SMC; [26], [28]). Although the SMC allows a reduction of the number of transistors compared with the IMC, this does not lead to a significant reduction of the installed semiconductor chip area as the average and rms currents of the transistors S_a, S_b, and S_c are twice as large as that for the transistors of the input stage of the IMC. In addition, the conduction losses of the input stage of the SMC depend on the direction of the link current i. The resultant conduction losses of the input stage of the SMC for a positive link current $(i > 0)$ are typically 40% higher compared to an equivalently designed IMC due to the higher number of semiconductor devices in the current path. The conduction losses of the input stage of the SMC and IMC are, however, similar for a negative link current $(i < 0)$.

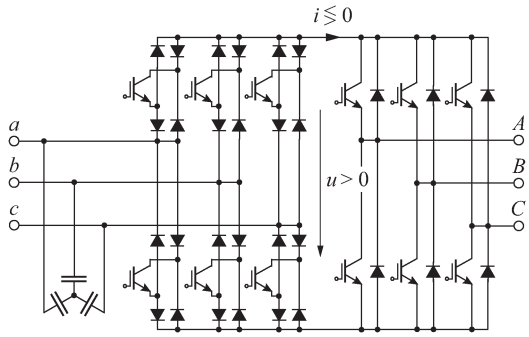

Fig. 18. Circuit topology of the VSMC.

Another fully bidirectional variant of the IMC, which is the very SMC (VSMC; [19], [26]), with only 12 transistors but with 30 diodes, is shown in Fig. 18. The reduction in the number of transistors of the input stage of the VSMC occurs at the cost of an increase in conduction losses due to the additional diodes and a loss in controllability with respect to the IMC. Its four-quadrant switches cannot be controlled separately depending on the current direction. However, this controllability is not required when using modulation scheme A for instance.

A more comprehensive simplification of the IMC circuit topology is possible by limiting the converter to unidirectional power flow. The transistors $S_{\rm pa}$ and $S_{\rm an}$ [cf., Fig. 16(c)] only conduct when current flows from the link into the mains $(i < 0)$ and can thus be omitted when connected to passive (and mostly ohmic) loads. The resulting topology is the ultra SMC (USMC), which is shown in Fig. 19. The operation of the converter is limited to

$$\Phi_1^* = \left[-\frac{\pi}{6}, +\frac{\pi}{6}\right] \quad \text{and} \quad \Phi_2 = \left[-\frac{\pi}{6}, +\frac{\pi}{6}\right] \tag{20}$$

and, consequently, not restricted to purely ohmic loads. This is explained by the absence of a connection between the mains star point, the link, and the load. Apart from the topology shown in Fig. 19(a), the USMC can also be implemented with six transistors in the input stage, as shown in Fig. 19(b). This circuit variant exhibits lower conduction losses but a greater implementation effort compared to the variant in Fig. 19(a) and is obtained by omitting the conducting power semiconductors of the input stage of the IMC (cf., Fig. 12) for $i < 0$.

The semiconductor losses of the output stages of all SMC topologies and the IMC are identical for an equivalent design.

IV. Direct MC

In contrast to the IMC, each of the input phases (a, b, and c) of the CMC, shown in Fig. 20, can be directly connected with each output phase (A, B, and C) by a four-quadrant switch. It can therefore be represented as a switching matrix according to Fig. 21(a). The four-quadrant switches must be implemented by an antiseries connection of transistors (typically IGBTs) with antiparallel freewheeling diodes as the input stage of the IMC. With respect to the conduction losses, an even better solution is to use an antiparallel connection of RB-IGBTs.

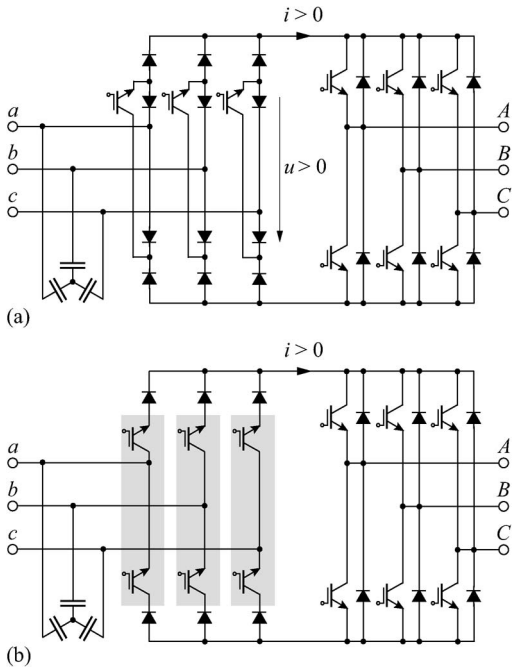

Fig. 19. (a) Circuit topology of the unidirectional USMC. (b) Circuit variant with low conduction losses, which allows the use of PWM inverter half-bridge modules (highlighted in gray).

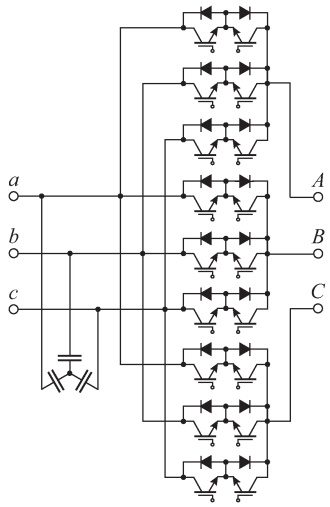

Fig. 20. Circuit topology of the CMC.

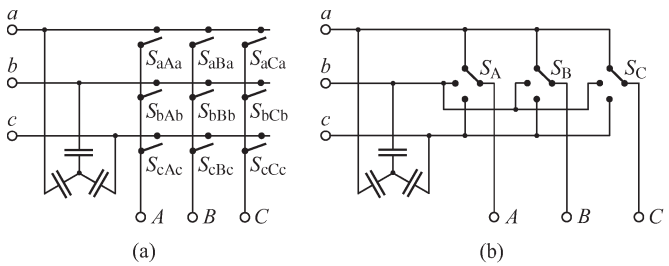

Fig. 21. Idealized representation of the CMC (a) as a switching matrix and (b) in the form of a three-level converter with variable voltage levels.

Assuming an inductive load, it is mandatory to place filter capacitors at the input of the CMC to enable free commutation of the current. To avoid a short circuit of the impressed input voltages, a simultaneous connection of two input phases to the same output phase must be strictly avoided. On the other hand, due to the impressed load currents, one output phase must, in any case, be connected to one input phase. Obviously, it is also permissible to connect all outputs to the same input. In a similar manner as that for the IMC, the input capacitors, together with additional filter inductors, help filter the current blocks on the input side in order to form sinusoidal mains currents.

The basic functionality of the MC can be represented by three single-pole triple-throw switches, as shown in Fig. 21(b). The resultant circuit topology clearly shows the similarity of the CMC to a three-level voltage dc-link PWM inverter. The change of the switching state of the CMC must be accomplished considering the impressed output current and input voltage. Suitable multistep commutation schemes were first described in [34] and [35]. The commutation is thereby carried out depending on the sign of the current in the output phase that is to be connected to another input phase or, as shown in Fig. 24, depending on the sign of the voltage difference of those input phases between which the commutation occurs. In the case under consideration, u_{ab} must be taken into account.

Fig. 22(a) shows a possible voltage-dependent multistep commutation strategy. The transistors on a gray background are in the ON-state, and those surrounded by a dashed line indicate that a change of the switching state has happened in the commutation step shown. Prior to a transistor turn-off, a transistor of the branch that is going to take over the current has to be switched on in order to always provide a current path. The transistor to be switched on is selected in such a manner that no input phase short circuit occurs for the given commutation voltage (u_{ab} in Fig. 22). This means that its series diode blocks. As a result, two possible current paths exist for one load current direction, and therefore, the remaining transistor of the branch handing over the current can be switched off.

As proposed in [36] and [37], the number of steps of the four-step commutation strategy [cf., Fig. 22(a)] can also be reduced, for instance, to two steps [cf., Fig. 22(b)]. As many transistors as possible are always held in the ON-state for this purpose, so that when a commutation is required, fewer steps have to be executed. It should be noted that the commutation of the CMC in all cases demands that the four-quadrant switches can be separately controlled for both current directions.

The CMC has a total of $3^3 = 27$ possible switching states, which may be subdivided into three groups according to Table I. All output phases are connected to the same input phase for group I, and for group II, two outputs in each case are connected to the same input. The third output is switched to one of the remaining inputs, whereby a total of 18 possibilities exist. Finally, with group III, six additional switching states are found, where each output phase is connected to a different input phase. This configuration leads to rotating output voltage and input current space vectors.

The use of rotating space vectors has been widely discussed when the concept of the CMC was first introduced [38], but it has lost considerable importance. The following considerations are hence limited to the switching states of groups I and II. This type of output and input connection is also known from the IMC. According to Fig. 2(a), each connection between the

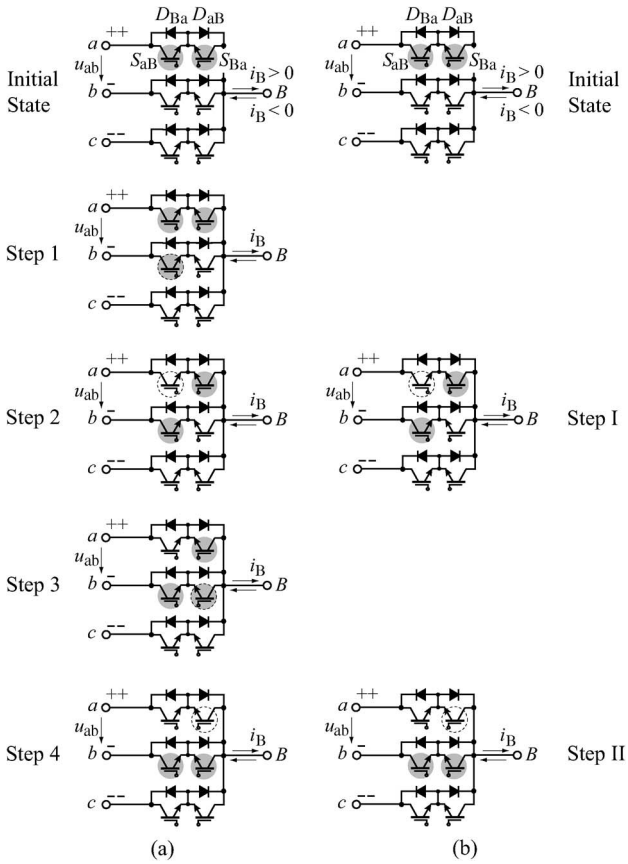

Fig. 22. Switching states of a branch of the CMC for a current commutation from $a-B$ to $b-B$. (a) Voltage-dependent four-step commutation (steps 1–4). (b) Voltage-dependent two-step commutation (steps I and II). For the input voltages $u_a > u_b > u_c$, $u_a > 0$, $u_b < 0$, and $u_c < 0$ are assumed.

TABLE I
CLASSIFICATION OF THE SWITCHING STATES OF THE CMC

Group I	(aaa)	(bbb)	(ccc)	
Group II	(cca)	(ccb)	(aab)	$u_{AB}=0$
	(aac)	(bbc)	(bba)	
	(acc)	(bcc)	(baa)	$u_{BC}=0$
	(caa)	(cbb)	(abb)	
	(cac)	(cbc)	(aba)	$u_{CA}=0$
	(aca)	(bcb)	(bab)	
Group III	(abc)	(cab)	(bca)	
	(acb)	(cba)	(bac)	

output and input phases is made via the link rails p and n, whereby only two choices exist for the outputs. The control of the CMC can then be considered simply with reference to a fictitious IMC (indirect space vector modulation). Thus, the switching states of the CMC can be obtained by recoding the switching states of the IMC, as shown in Fig. 23. The switching state $(ac)(pnn)$ of the IMC corresponds to the switching state (acc) of the CMC for instance. In both cases, the same output voltage and input current space vectors are generated

$$\vec{u}_{2,(\mathrm{acc})} = \vec{u}_{2,(\mathrm{ac})(\mathrm{pnn})} \tag{21}$$

$$\vec{i}_{1,(\mathrm{acc})} = \vec{i}_{1,(\mathrm{ac})(\mathrm{pnn})}. \tag{22}$$

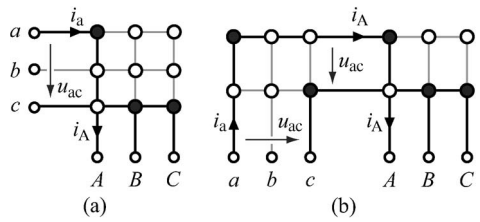

Fig. 23. (a) Conduction state of the CMC for the switching state (acc) and (b) associated switching state $(ac)(pnn)$ of the IMC.

The CMC and IMC show the same space vector diagrams (cf., Figs. 14 and 24) for the given input voltage and output current vectors $\vec{u}_1$ and $\vec{i}_2$. The switching state sequence of the IMC in (16) changes into the corresponding switching state sequence of the CMC

$$\begin{aligned}\ldots|_{t_\mu=0}&(\underline{a}cc)-(\underline{a}ac)-(\underline{a}aa)-(\underline{a}aa)-(\underline{a}ab)\\&-(\underline{a}bb)|_{t_\mu=T_P/2}(\underline{a}bb)-(\underline{a}ab)-(\underline{a}aa)-(\underline{a}aa)\\&-(\underline{a}ac)-(\underline{a}cc)|_{t_\mu=T_P}\ldots\end{aligned} \tag{23}$$

by considering the change in the coding of the switching states or by considering the space vector diagrams for the CMC. The clamping of phase C to n brings a greater reduction in the switching losses for the IMC in the angular range $\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$ than the clamping of phase A to p. This results in a modified switching state sequence for the IMC

$$\begin{aligned}\ldots|_{t_\mu=0}&(ac)(ppn)-(ac)(pnn)-(ac)(nnn)\\&-(ab)(nnn)-(ab)(pnn)-(ab)(ppn)|_{t_\mu=T_P/2}(ab)(ppn)\\&-(ab)(pnn)-(ab)(nnn)-(ac)(nnn)\\&-(ac)(pnn)-(ac)(ppn)|_{t_\mu=T_P}\ldots.\end{aligned} \tag{24}$$

Thus, the freewheeling state changes within a pulse half-period. The corresponding switching state sequence of the CMC is again determined by mapping the switching states and leads to

$$\begin{aligned}\ldots|_{t_\mu=0}&(aac)-(acc)-(ccc)-(bbb)-(abb)\\&-(aab)|_{t_\mu=T_P/2}(aab)-(abb)-(bbb)-(ccc)-(acc)\\&-(aac)|_{t_\mu=T_P}\ldots.\end{aligned} \tag{25}$$

As can be seen from (25), in each pulse half-period, there is a commutation of all output phases from input c to input b [cf., Fig. 25(b)]. In order to avoid such commutations with the CMC, a clamping of the input phase, which is not switched in the considered angular range, must be implemented. In the present case, the clamping to phase a or the freewheeling state (aaa) (corresponds to the freewheeling state (ppp) of the IMC) must be retained for $\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$. In consequence, the switching state sequence in Fig. 25(a) or (23) must be used within the entire angular interval $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$. Thereby, all

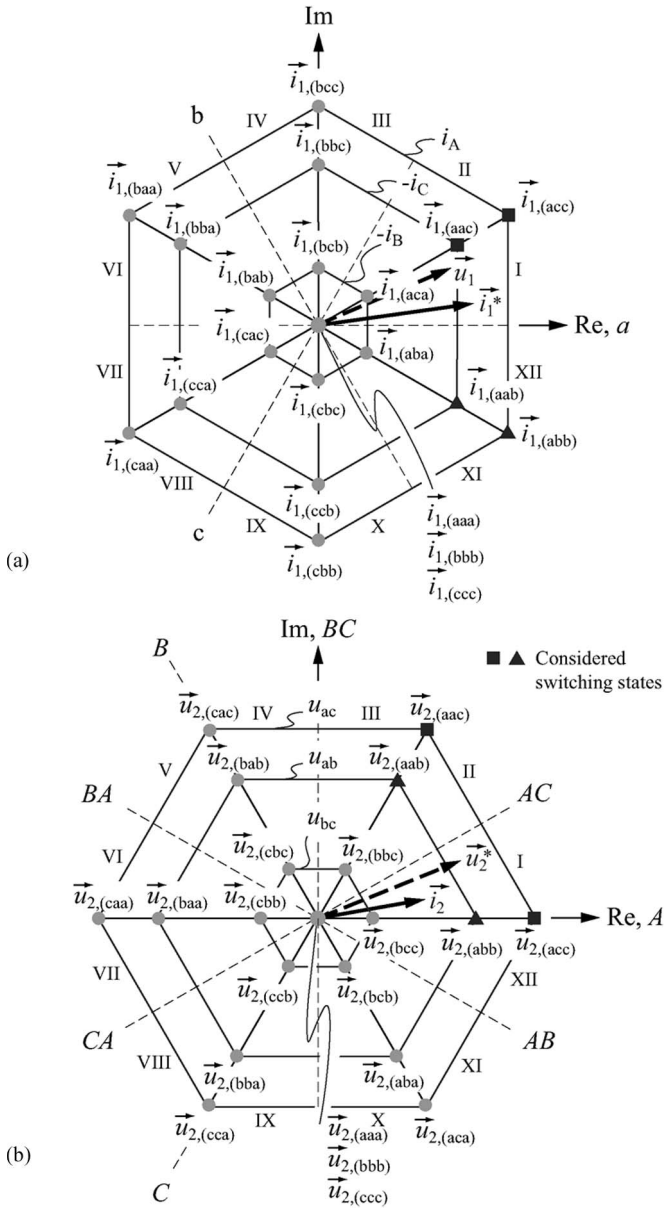

Fig. 24. (a) Current and (b) voltage conversions of the CMC for the switching states of groups I and II (cf., Table I), assuming the given input and output voltage and current space vectors.

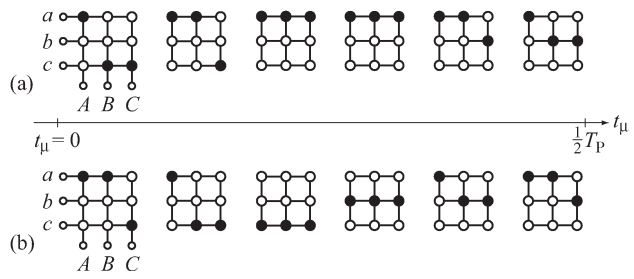

Fig. 25. Switching states of the CMC within a pulse half-period (a) for the sequence in (23) and (b) for the sequence in (25).

commutations always occur between input phases with a large voltage difference to assure high commutation reliability.

It is also beneficial for the IMC to retain the switching state sequence (16) over the entire angular range $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$.

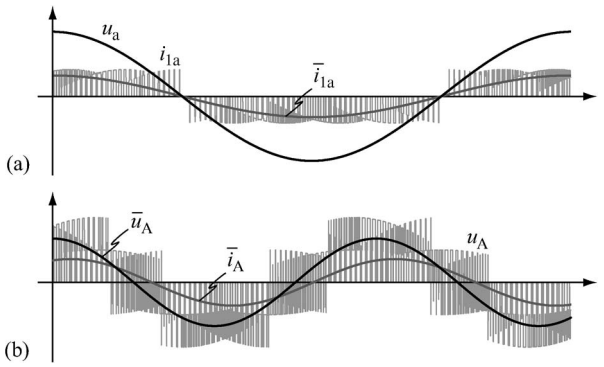

Fig. 26. Characteristic waveforms of the CMC for $\omega_1 < \omega_2$, $\Phi_1 \approx 0$, and $\Phi_2 = \pi/9$ (inductive load). (a) Input line voltage u_a, input current i_{1a}, and over T_P averaged input current $\bar{i}_{1a}$. (b) Output line voltage u_A, over T_P averaged output line voltage $\bar{u}_A$, and over T_P averaged output line current $\bar{i}_A$.

Hence, the bus of the link that is used in clamping the output stage remains permanently connected to an input terminal (via the input stage) during one pulse period. It can be shown that the freewheeling state used for the output stage is repeated with six times the mains frequency and not with six times the output frequency. In this way, at low output frequencies, a more even loading of the power semiconductors (inherently given by the CMC topology) of the output stage can be attained. This allows a higher stand-still torque when utilized for a variable-speed drive.

Fig. 26 shows the characteristic input and output waveforms of the CMC [cf., Fig. 2(b)] for the modulation scheme according to (16) and for an inductive load.

V. Three-Phase PWM AC–AC Buck Converters

Three-phase PWM ac–ac buck converters represent a subcategory of MCs. In a similar manner to the classical MC topologies (CMC and IMC), they enable an ac–ac power conversion without an intermediate energy storage. Three-phase ac–ac buck converters can be derived from the basic dc–dc converter topologies and are also known as buck-type ac–ac choppers. A review of various ac–ac chopper circuit topologies is provided in [39]. In contrast to MCs, three-phase ac–ac buck converters only enable control of the output voltage, whereas the stationary output frequency is equal to the mains frequency at the input. Three-phase buck converters are traditionally applied as soft-starters for induction motors or for saving energy by controlling the motor flux. Due to their capability of instantaneous control of the output voltage, they also allow compensation of unbalanced mains voltages, and thus, they can be utilized for power conditioning in power distribution systems. In the following, two typical three-phase PWM ac–ac buck converter topologies are briefly discussed.

Starting from the bidirectional dc–dc buck converter in Fig. 27(a), a three-phase buck converter can be derived, which requires only six transistors and six diodes. The resulting topology is shown in Fig. 27(b) and requires three series switches, providing a bidirectional current path between the input and

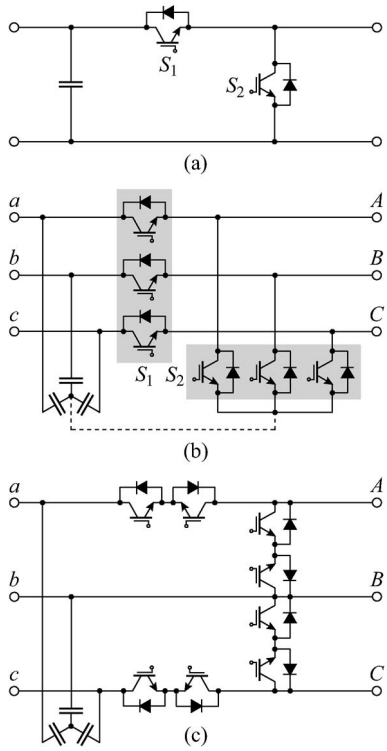

Fig. 27. (a) Bidirectional dc–dc buck converter. Three-phase ac–ac buck converter (b) with six switches and an optional connection between the input capacitors and the interphase switches and (c) with eight switches.

output phases [correspond to S_1 in Fig. 27(a)], and three interphase switches [correspond to S_2 in Fig. 27(a)], providing a bidirectional current path between the output phases. In order to enable a safe commutation, as described in [12], the series and interphase switches that are connected to the input phase with the smallest voltage are switched on, whereas the other four switches are modulated at a given duty cycle to generate the required output voltage. A simpler commutation is enabled if the star point of the input capacitors is connected with the star point of the interphase switches, as suggested in [11], which is represented by the dashed line in Fig. 27(b). Thus, all series switches and all interphase switches can be alternately switched on and off similar to a dc–dc converter.

An alternative topology with eight transistors and eight diodes is shown in Fig. 27(c). In this three-phase ac–ac buck converter, one input (phase b) is directly connected to one output (phase B). The resulting topology consists of a combination of two independently controllable, bidirectional, and bipolar dc–dc buck converters, which enables a simple modulation for compensating unbalanced input voltages.

VI. Extended MC Topologies

Numerous extensions of the basic MC topologies have been suggested over the last few years, which aim, for instance, at increasing the output voltage control range, lowering the switching frequency harmonics, reducing the switching losses, or minimizing the common-mode voltages at the output.

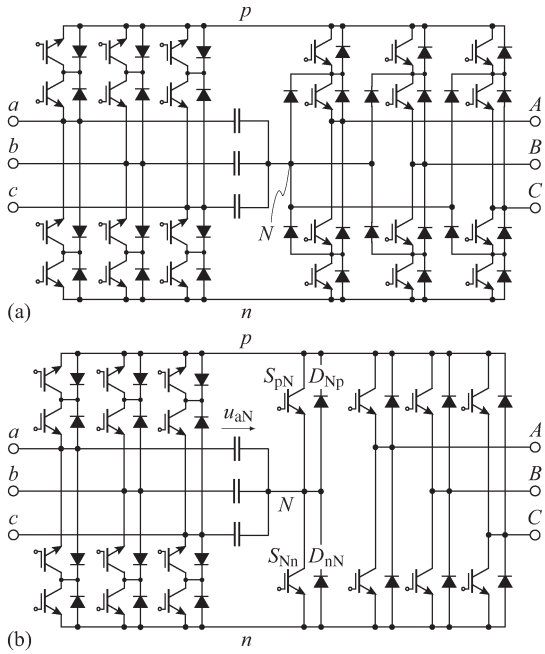

Fig. 28. (a) IMC with a three-level PWM output stage. (b) IMC with an additional bridge leg that allows the mains line voltages to be switched directly or inverted into the link, thus attaining the functionality of (a).

In the following, only the circuit topologies of the individual systems are presented, and the main characteristics are discussed. A detailed description of the functionality can be found in the provided references.

A. Indirect Three-Level MC

The output stage of the IMC is a two-level PWM inverter [cf., Fig. 2(a)]. It is thus obvious to employ an inverter stage with a three-level characteristic, as shown in Fig. 28(a), to reduce the switching frequency harmonics of the output voltage. Such a topology, in which the center point for the output stage is provided by the star point of the input filter capacitors, was proposed in [26]. It enables formation of the output voltage by the phase and line-to-line input voltages. As the input stage of an SMC can be used, this topology was later designated as three-level SMC (SMC3). The same functionality can be achieved with the topology shown in Fig. 28(b), which has the advantage of having a reduced number of switches [30]. The corresponding space vector modulation is described in [31] and [40].

A considerable simplification of the indirect three-level MC circuits is possible by restricting the systems to unidirectional power flow according to Fig. 29 and [29]. The input stage of this topology exhibits the structure of a Vienna rectifier (VR; [41]) and is, with respect to the complexity of the input stage, comparable to an USMC. This led to the abbreviation USMC3. It should be emphasized that, on the input side, the transistors are only switched with twice the mains frequency, which results in very low switching losses. By turning on a transistor of the input stage, the mains line voltage having the smallest absolute value is connected to the center point m of the three-level output stage.

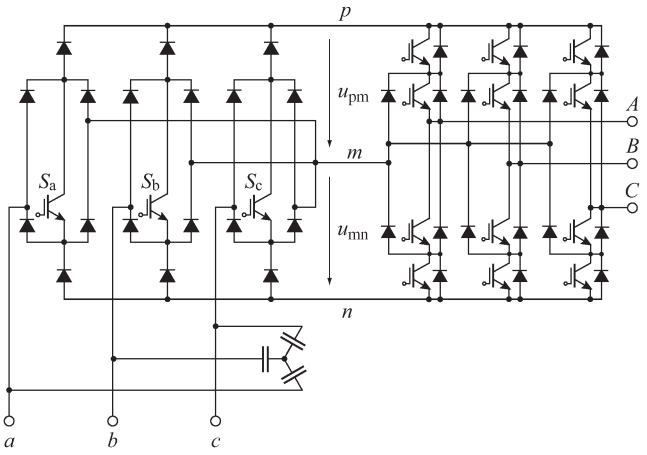

Fig. 29. Unidirectional IMC with a three-level input stage according to the concept of the VR and a three-level PWM output stage.

B. IMC With Links Separated According to Input Phases

In Section III-A, the F3EC is described as an example of a simple circuit topology of a bidirectional MC. Due to the lack of controllability of the input stage caused by the diodes, zero-current intervals and, thus, relatively high low-frequency harmonics of the mains current occur.

A sinusoidal shape of the mains current can be obtained with the circuit modification suggested in [42] by implementation of an explicit dc-link or by arrangement of a separate input stage for each input phase, as shown in Fig. 30. The converter system then requires 24 transistors and diodes and results in a higher component expenditure compared to the IMC with the same functionality. According to [42], however, a reduction of the switching stress of the power devices is achieved. Additionally, the power circuit can be implemented with commercially available semiconductor modules.

C. Full-Bridge MC

The CMC can be implemented with a half-bridge topology [cf., Fig. 2(b)] or, as is known from cycloconverters, with a full-bridge topology. The latter circuit variant is shown in Fig. 31 and requires 36 instead of 18 transistors and open motor windings compared to the half-bridge circuit topology. Aiming for a minimal component count, the half-bridge topology is often emphasized in publications. An exception is found in [18], where, for the full-bridge topology of the CMC, a control procedure is suggested, which enables a low stress on the insulation of the motor windings by minimizing the common-mode voltage at the output, a maximum output voltage of

$$\hat{U}_{2,\max} = \frac{3}{2}\hat{U}_1 \tag{26}$$

(instead of $\hat{U}_{2,\max} = \sqrt{3}/2\hat{U}_1$), and ohmic fundamental mains behavior. Consequently, the topology is of particular interest for high-power variable-speed drives. A reduction of the implementation effort of the full-bridge topology to 24 power

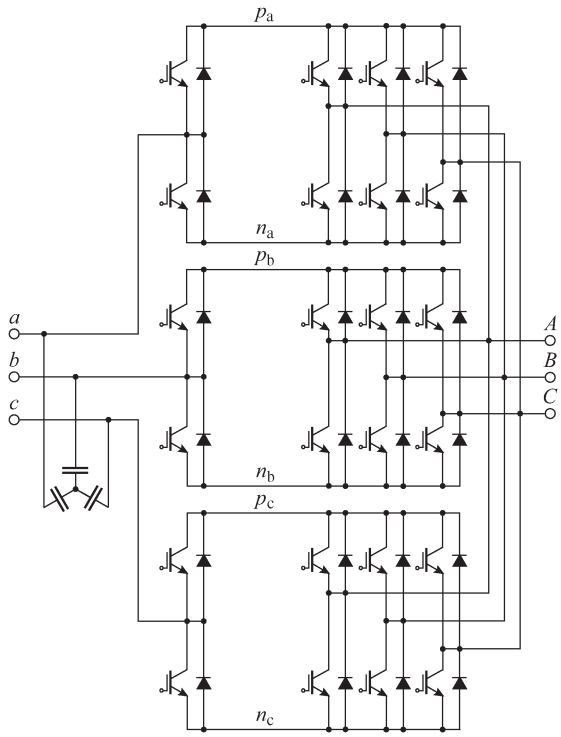

Fig. 30. IMC formed by separation of the input stage of a F3EC and separate arrangement of the individual input phases.

transistors is possible with the circuit variant shown in Fig. 32 by using two PWM output stages I and II in combination with an IMC input stage (cf., Fig. 15 in [18]). When the associated motor terminals are driven in opposition, then the maximum output voltage is equal to

$$\hat{U}_{2,\max} = 2\frac{\sqrt{3}}{2}\hat{U}_1 = \sqrt{3}\hat{U}_1. \tag{27}$$

D. Hybrid MC

The limited voltage control range of the basic MCs (CMC or IMC) is a significant disadvantage compared to converters with dc-link storage (C-BBC or V-BBC). Therefore, combinations of the basic MC topologies and the V-BBC, so-called hybrid MCs, were suggested, which overcome this limitation. However, these converter topologies again require energy storage elements (e.g., capacitors) and typically have a large component count.

If the four-quadrant switches in a CMC are replaced by cascaded H-bridge circuits with output capacitors (similar to PWM converters with cascaded bridge circuits), then the hybrid CMC topology (HCMC; [8]) results, as shown in Fig. 33. This modification enables step-up or step-down converter operation. No external supply of the switching cells is required with an adequate modulation scheme. In contrast to all previously discussed topologies, both the input and output currents for the HCMC are impressed and can be controlled according to [8] by the use of at least five half-bridges.

Transferring the concept of the HCMC to the hybrid IMC (HIMC) requires, in the simplest case, only one H-bridge in the link, as described in [10]. The resulting topology is shown in

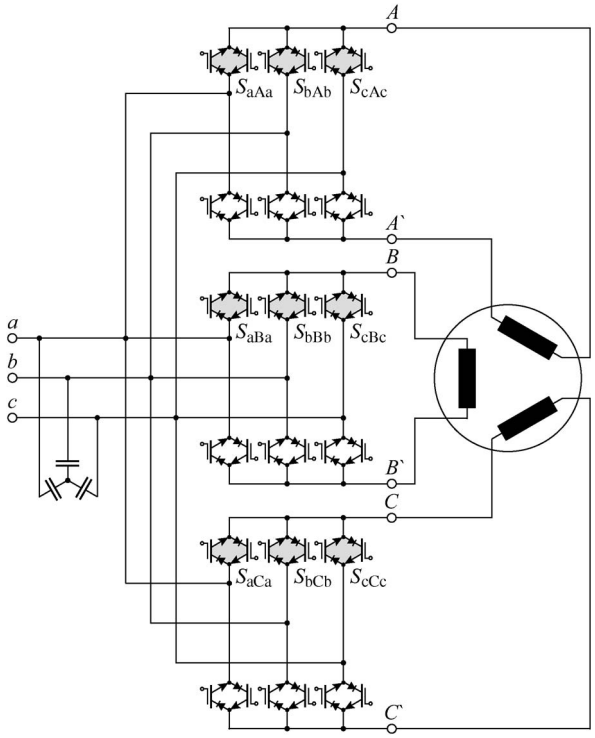

Fig. 31. Full-bridge CMC topology implemented with antiparallel-connected RB-IGBTs. The circuit is formed by two CMCs with a half-bridge topology (switches on gray and white background), which feed an ac motor with open windings.

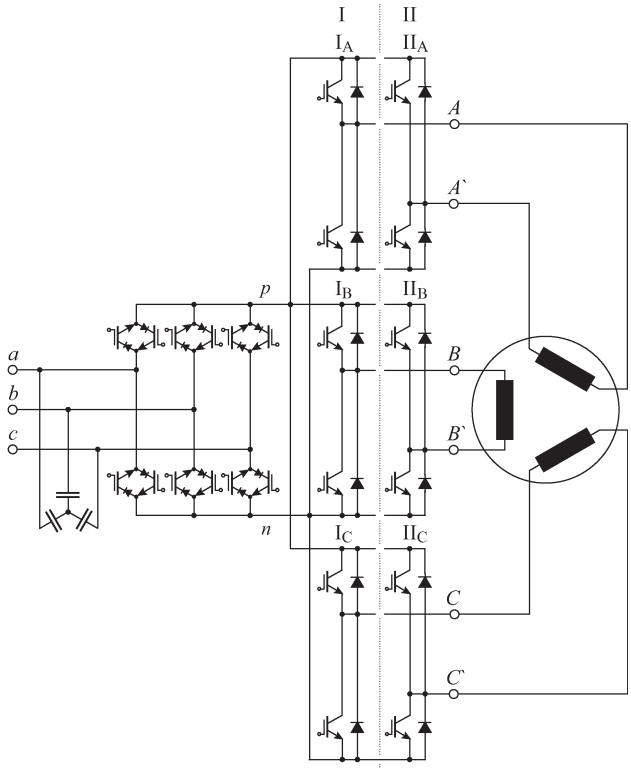

Fig. 32. IMC topology extended on the output side for supplying an ac motor with open windings.

Fig. 34. In the voltage step-up mode, when providing a voltage $u_{S,\mathrm{II-I}}$ with a positive mean value, an external supply of the capacitor C_H is necessary.

E. Modular MC With Multipulse Transformer

Another means of extending the output voltage range of an MC system is by a modular interconnection of multiple identical MCs that are connected to the mains by a common multipulse transformer. A possible circuit topology of such a converter system is shown in Fig. 35(a). This modular MC system consists of nine three-phase to two-phase direct MCs, according to Fig. 35(b), and are referred to as 3 × 2 MC. Each of the three output phases (A, B, and C), connected in a star format, is formed by a series connection of the outputs A_1 and A_2 of three 3 × 2 MCs. This enables the output line voltage of the modular MC system to be tripled in comparison with the output line voltage of a single 3 × 2 MC. The mains interface is provided in this case by an 18-pulse transformer with a three-phase winding, connected in star format, on the primary side and nine isolated three-phase windings on the secondary side that are connected in polygon or delta. In order to generate an 18-pulse voltage system on the secondary side of the transformer, the voltage vectors of the three topmost polygon windings lead the voltage vectors of the three delta windings in the middle by 20°, whereas the voltage vectors of the bottom three polygon windings lag the voltage vectors of the three delta windings in the middle by 20°. The 18-pulse transformer not only enables generation of the required isolated

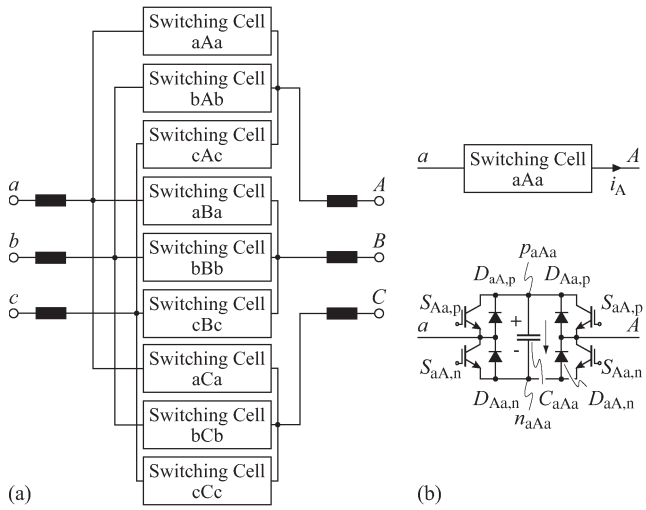

Fig. 33. (a) Circuit topology of the HCMC. A cascading of several H-bridges in each connection of an input and an output is also possible. (b) Implementation of a single switching cell.

multipulse voltage system for the 3 × 2 MCs but also, assuming a symmetrical loading, cancels the resulting current harmonics at the converter inputs (a, b, and c) up to the 17th order.

Over the last few years, modular MC has gained considerable attention. The first converter systems have been implemented by industry and are currently being investigated for high-power medium-voltage drive applications [43].

In summary, hybrid MCs enable an enlargement of the output voltage control range and can be advantageous when operated from unbalanced mains systems. These benefits, however, are

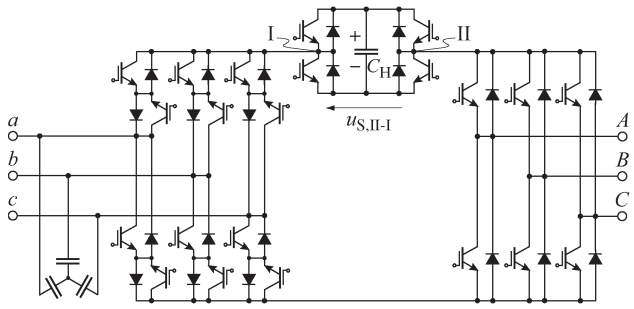

Fig. 34. Circuit topology of the HIMC with a series voltage source $u_{S,\mathrm{II}-\mathrm{I}}$ in the link.

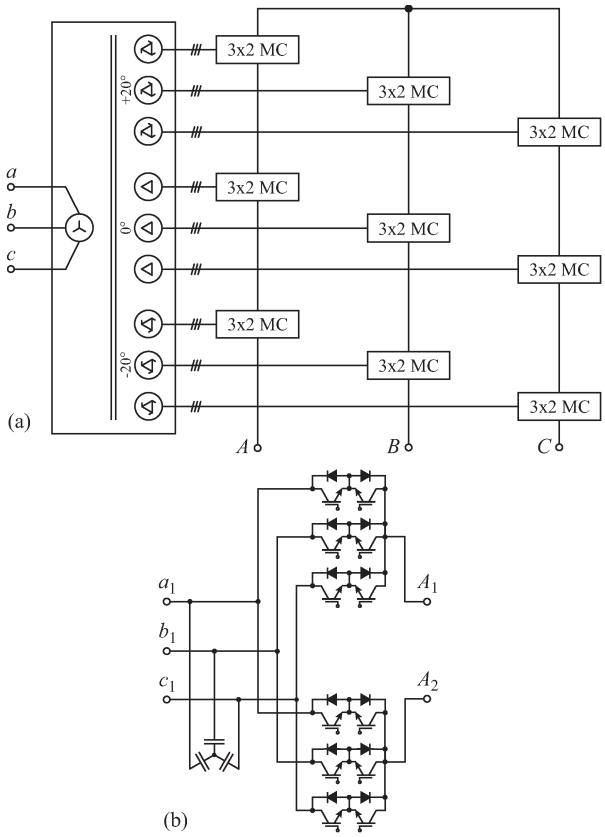

Fig. 35. (a) Modular MC system consisting of a 3 × 3 arrangement of nine three-phase to two-phase direct MCs that are interfaced to the mains by an 18-pulse transformer. (b) Circuit topology of the three-phase to two-phase direct MC (3 × 2 MC).

obtained at the expense of a higher complexity of the power circuits and a more intricate control.

VII. Conclusion

So far, the circuit topology of the IMC and CMC and their fundamental modulation and commutation schemes have been deduced step by step from the known topologies of V-BBC and C-BBC by combining the PWM input stage of the C-BBC with the PWM output stage of the V-BBC. The relationship between the IMC and CMC and the modulation scheme of the CMC has been discussed by mapping the switching states of the IMC to the CMC. In this manner, the often perceived complexity in the deduction and functional description of MCs has been eliminated, and a figurative knowledge basis of the operating principle of IMC and CMC has been established. Based on that, the main topological extensions of the CMC and IMC have been presented.

A brief comparison of the basic bidirectional ac–ac converter topologies, i.e., the V-BBC, C-BBC, IMC, and CMC, follows as the conclusion of this converter review. The key properties of these topologies, such as the number of transistors and diodes, the number of isolated gate driver supplies, or the required PWM signals, etc., are listed in Table II. In addition, Fig. 36 shows the dc–dc converter equivalents of the four basic topologies (without the EMI input filter and the load) to facilitate the subsequent considerations. The devices in a single circle represent semiconductor configurations in the corresponding ac–ac converter topologies that can provide

TABLE II
Key Properties of the Basic Converter Topologies

	V-BBC	C-BBC	IMC	CMC
# transistors	12	12	18	18
# diodes	12	12	18	18
# isolated gate driver supplies	8	8	9	9
# PWM signals	12	12	12	18
# devices in current path	4	8	6	4
Min. # current sensors	4	3	2	2
Min. # voltage sensors	4	6	3	3
Intermediate storage	C_{DC}	L_{DC}	no	no
Max. output voltage	$> \hat{U}_1$	$> \hat{U}_1$	$0.86\,\hat{U}_1$	$0.86\,\hat{U}_1$
Additional protection circuitry	no	yes	yes	yes

#: Number of

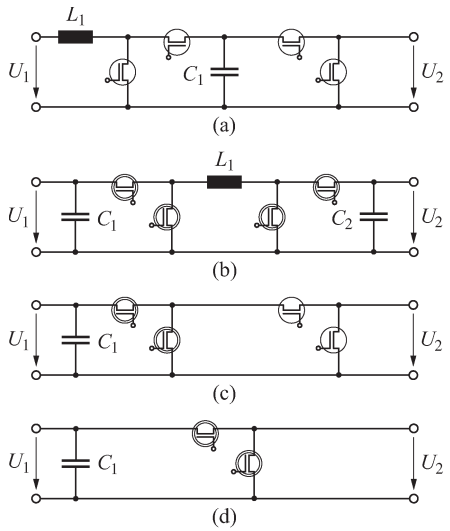

Fig. 36. DC–DC converter equivalents of the (a) V-BBC, (b) C-BBC, (c) IMC, and (d) CMC. L_1 represents the boost inductors of the V-BBC or the dc-link inductor(s) of the C-BBC. C_1 corresponds to the dc-link capacitor of the V-BBC or the input capacitors of the C-BBC, CMC, and IMC, whereas C_2 accounts for the output capacitor of the C-BBC. Single-encircled electronic switches represent semiconductor configurations in the corresponding ac–ac converter topologies that provide unidirectional voltage blocking, whereas double-encircled electronic switches represent semiconductor configurations that provide bipolar voltage blocking.

unipolar voltage blocking similar to a single transistor with an antiparallel freewheeling diode (cf., V-BBC or the output stage of IMC), whereas the devices in a double circle represent semiconductor configurations that can provide bipolar voltage blocking comparable to a series connection of a transistor and a diode (cf., C-BBC) or a four-quadrant switch (cf., CMC or the input stage of IMC).

As can be extracted from Table II, in the entire current path of the C-BBC between its input and output, there are eight semiconductor devices in total, leading to significantly higher conduction losses without providing definite advantages compared to the other three topologies. The C-BBC is excluded for that purpose from the following qualitative comparison between the two MC topologies (CMC and IMC) and the V-BCC, which is a standard industrial solution. The main advantages and disadvantages of MCs compared with the V-BBC regarding their fundamental converter properties can be summarized as follows.

1) The MC has a limited output voltage range (86.6% of the input voltage) compared with the V-BBC, which allows boost operation of the input stage. As can be seen from the equivalent circuits in Fig. 36, the MC exhibits a buck-type characteristic, whereas the V-BBC features a boost-buck-type operation.
2) As opposed to the V-BBC, the input currents of the MC cannot be controlled independently of the output currents which are impressed by the motor control. Thus, the control scheme of the V-BBC enables a higher degree of freedom and typically offers a more robust solution.
3) The input stage of the IMC can be switched at zero current, and the average commutation voltage of the CMC is only approximately two-third of the commutation voltage of a typical V-BBC. Consequently, with increasing switching frequency, the MC enables lower semiconductor losses compared with the V-BBC [44].
4) The volume of the passive components, including the EMI input filter and the heat sink (forced air cooling), of the MC is smaller compared with the V-BBC [45], e.g., by a factor of 2.5 at a switching frequency of 8 kHz. This difference mainly originates from the absence of the input (boost) inductors in the MC.

As can be seen from the previous argumentation, a general and simple statement regarding the benefits of MCs compared to the industrially widely applied voltage dc-link converter systems and possible application areas of MCs cannot be made. Both converter concepts can provide sinusoidal input currents, sinusoidal output currents, and bidirectional power transfer. The individual converter topologies thus differ not with regard to their basic functionality but with regard to the possible operating range, the behavior in characteristic operating points, or the implementation effort.

This fact is reflected in the research on MCs so far as MCs have been and are still being investigated for a wide range of applications and as numerous modulation and control strategies known from voltage and current source converters or even from other fields of research have been adapted and applied to MCs. A prominent example of such a cross-disciplinary topic area is model predictive control, which has been extensively investigated for MC [46]–[48] in recent years. Considerable research has also been devoted to the analysis and improvement of the operation of MCs under unbalanced input voltages [49]–[51], which is a critical operating mode of MCs due to the absence of an intermediate energy storage that could absorb the input voltage fluctuations and could allow generating a symmetrical voltage–current system at the converter output for the load. A further trend in recent research on MCs is the investigation of the MC topology for aircraft applications [52], [53], motivated by its potential for a compact and lightweight implementation. However, despite all these efforts, distinct application areas for MC systems, where they would enable both superior performance and a better benefit-to-cost ratio compared with existing industrial solutions, could not yet be quantified and should therefore be addressed in future research.

In order to identify possible benefits of MCs compared to established industrial converter systems, a systematic benchmarking procedure is required, which will ultimately enable us to determine key performance figures such as costs, volume, and energy efficiency of the analyzed converter topologies for a given application. Such a procedure should involve consideration of the required semiconductor chip area; the gate drivers; the cooling system; the passive components, including the (EMI) input filter; and the auxiliary and control hardware. The electrical, thermal, and mechanical converter properties and their relationship need to be carefully modeled for this purpose.

The results of such a comprehensive comparison of the CMC, IMC, and V-BBC are presented in [54], and they provide a quantitative basis in identifying the main advantageous application areas of MCs.

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Johann W. Kolar (M'89–SM'04–F'10) received the M.Sc. and Ph.D. degrees (*summa cum laude*/ promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Vienna, Austria.

Since 1984, he has been working as an independent international consultant in close collaboration with the University of Technology Vienna in the fields of power electronics, industrial electronics, and high-performance drives. He was appointed as a Professor and the Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, on February 1, 2001, which was awarded as the leading academic research institution in power electronics in Europe by the European Power Supplies Manufacturers Association in 2006. He initiated and/or he is the founder/cofounder of four spin-off companies targeting ultrahigh-speed drives, multidomain/level simulation, ultracompact/efficient converter systems, and pulsed power/electronic energy processing. He has proposed numerous novel PWM converter topologies and modulation and control concepts, e.g., the VIENNA rectifier, the SWISS rectifier, and the three-phase ac–ac sparse matrix converter. He has published over 350 scientific papers in international journals and conference proceedings and has filed more than 80 patents. The focus of his current research is on ac–ac and ac–dc converter topologies with low effects on the mains, e.g., for power supply of data centers, more electric aircraft, and distributed renewable energy systems. Further main areas of research are the realization of ultracompact and ultraefficient converter modules employing the latest power semiconductor technology (SiC and GaN), novel concepts for cooling and EMI filtering, multidomain/scale modeling/simulation and multiobjective optimization, physical-model-based lifetime prediction, pulsed power, and ultrahigh-speed and bearingless motors.

Dr. Kolar is a member of The Institute of Electrical Engineers of Japan (IEEJ) and international steering committees and technical program committees of numerous international conferences in the field (e.g., Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and the Chairman of the Education Chapter of the EPE Association. From 1997 to 2000, he was an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and since 2001, he has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. Since 2002, he has also been an Associate Editor of the *Journal of Power Electronics* of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the *IEEJ Transactions on Electrical and Electronic Engineering*. He received the Best Paper Award of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2005, the Best Paper Award of the ICPE in 2007, the 1st Prize Paper Award of the IEEE IAS IPCC in 2008, the IEEE IECON Best Paper Award of the IES PETC in 2009, the 2009 IEEE TRANSACTIONS ON POWER ELECTRONICS Prize Paper Award, and the 2010 Best Paper Award of the IEEE/ASME TRANSACTIONS ON MECHATRONICS. He also received an Erskine Fellowship from the University of Canterbury, Christchurch, New Zealand, in 2003.

Thomas Friedli (M'09) received the M.Sc. (with distinction) degree in electrical engineering and information technology and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2005 and 2010, respectively. His Ph.D. research from 2006 to 2009 was on the further development of current source and matrix converter topologies using silicon carbide JFETs and diodes (in collaboration with industry) and a comparative evaluation of three-phase ac–ac converter systems.

From 2003 to 2004, he was a trainee for Power-One in the R&D Center for Telecom Power Supplies.

Dr. Friedli received the 1st Prize Paper Award of the IEEE IAS IPCC in 2008 and the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS Prize Paper Award in 2009.

Jose Rodriguez (M'81–SM'94–F'10) received the Engineer degree in electrical engineering from the Universidad Tecnica Federico Santa Maria (UTFSM), Valparaiso, Chile, in 1977 and the Dr.-Ing. degree in electrical engineering from the University of Erlangen, Erlangen, Germany, in 1985.

He has been with the Department of Electronics Engineering, Universidad Tecnica Federico Santa Maria, since 1977, where he is currently a full Professor and the Rector. He has coauthored more than 250 journal and conference papers. His main research interests include multilevel inverters, new converter topologies, control of power converters, and adjustable-speed drives.

Dr. Rodriguez is a member of the Chilean Academy of Engineering. He has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS since 2002. He received the Best Paper Award from the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2007 and the Best Paper Award from the IEEE INDUSTRIAL ELECTRONICS MAGAZINE in 2008.

Patrick W. Wheeler (M'00) received the B.Eng. (Hons) degree and the Ph.D. degree in electrical engineering (for his work on matrix converters) from the University of Bristol, Bristol, U.K., in 1990 and 1994, respectively.

In 1993, he moved to the University of Nottingham, Nottingham, U.K., and worked as a Research Assistant with the Department of Electrical and Electronic Engineering. In 1996, he became a Lecturer with the Power Electronics, Machines and Control Group, University of Nottingham, where he has been a full Professor since January 2008. He has published over 250 papers in leading international conferences and journals. His research interests are in power conversion, energy, and more-electric-aircraft technology.