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***Abstract*—High power EV chargers connected to an AC power distribution bus are employing a three-phase AC/DC Power Factor Correction (PFC) front-end and a series-connected isolated DC/DC converter to efficiently regulate the traction battery voltage and supply the required charging current. In this paper, the component stresses and the design optimization of a novel two-stage three-phase bidirectional buck-boost current DC-link PFC rectifier system, realized solely with SiC power MOSFETs and conveniently requiring only a single magnetic component, are introduced. This topology offers a high efficiency in a wide operating range thanks to the synergetic operation of its two stages, the three-phase buck-type current source rectifier stage and the subsequent three-level boost-type DC/DC-stage, which makes it suitable for on-board as well as off-board charger applications. The calculated voltage and current component stresses of the proposed converter system, considering an output voltage range of 200 to 1000 V and up to 10 kW of output power, help to identify its operating boundaries, maximizing the utilization of the power semiconductors and of the DC-link inductor. The optimum values of the circuit parameters are selected after evaluating the converter average efficiency $\bar{\eta}$ and volumetric power density ρ in the Pareto performance space and analyzing its design space diversity, focusing on the semiconductor losses and on the characteristics of the inductor. Considering typical EV battery charging profiles, i.e. taking both full-load and part-load operation into account, a power converter realization featuring $\bar{\eta} = 98.5\,\%$ and $\rho = 13.9\,\mathrm{kW/dm^3}$ is achieved.**

***Index Terms*— Three-Phase Bidirectional Buck-Boost Current DC-Link PFC Rectifier System, Three-Phase Buck-Type Current Source Rectifier, Multi-Objective Pareto Optimization.**

I. Introduction

High power and high efficiency on-board and off-board battery chargers, which are enabling a fast recharging of electric vehicles (EVs), are of crucial importance for the fast growth of the EV market. Accordingly, charging voltage and power levels up to 1 kV and 400 kW, respectively, are proposed in the latest charging protocols, e.g. CHAdeMO [1]. Mainly two types of fast (or Level 3) EV charging architectures, i.e. systems supplied from a local three-phase (3-Φ) AC power distribution bus and DC-bus based systems, are discussed in literature [2]. Today, 3-Φ AC-bus based charging stations, benefiting from mature AC protection and metering technologies, are generally preferred and realized as cascaded system, comprising an AC/DC Power Factor Correction (PFC) front-end and an isolated DC/DC converter, as shown in **Fig. 1**. While ensuring 3-Φ sinusoidal input currents in phase with the 3-Φ sinusoidal AC-bus voltages and galvanic isolation between the AC-bus and the EV, the charging stations must cover a wide output voltage range to adapt to different battery voltages, e.g. 360 V [3] and 800 V [4]. The required voltage regulation can be performed by the AC/DC front-end or the isolated DC/DC converter, or shared between them. However, if the isolated DC/DC converter is realized as series resonant converter, offering high efficiency but limited output voltage controllability [5], the sole AC/DC front-end must provide the voltage adaption. Moreover, according to the developing vehicle-to-grid (V2G) trend, where EVs are planned to serve as distributed energy storage elements to support the grid operation, future EV chargers must allow bidirectional power conversion.

In this context, a 3-Φ bidirectional buck-boost (bB) current DC-link PFC rectifier system, formed by a 3-Φ buck-type current source rectifier (CSR)-stage [6] and a subsequent boost-type DC/DC-stage, offers several advantages compared to a conventional boost-type PFC rectifier approach, i.e. a reduced number of magnetic components, direct start-up capability, and a sinusoidally varying switched voltage of the CSR-stage potentially reducing the occurring switching losses [7]. Additionally, a variable DC-link current control strategy, which enables a further switching loss reduction of the current DC-link topology [8], [9], can be employed. Moreover, a 3-Φ bB current DC-link PFC rectifier system can also be applied in non-isolated on-board chargers protected by an on-board ground fault circuit interrupter [10]. In this case, the switches of the traction inverter and the stator coils of the motor, already present on-board of the EV, can be used as DC/DC-stage and DC-link inductor, respectively, aiming for a compact and low-cost realization [11]. Finally, a three-level (3-L) DC/DC-stage can be employed to extend the converter output voltage range and/or to reduce the occurring switching losses and minimize the size of the DC-link inductor.

These considerations motivate the comprehensive analysis of the 3-Φ bidirectional bB current DC-link PFC rectifier system illustrated in **Fig. 2**, which is presented in this paper. The operating principle of the proposed topology is briefly described in **Section II**. Afterwards, the voltage and current stresses experienced by the main power components, e.g. the power semiconductors, input capacitors, and the DC-link inductor, are evaluated in a wide output voltage range, i.e. for $200\,\mathrm{V} < V_{\mathrm{out}} < 1\,\mathrm{kV}$, to identify suitable operating boundaries, i.e. the converter output current and output power limits. Next, a multi-objective optimization, focusing on the average efficiency $\bar{\eta}$, i.e. considering typical EV battery charging profiles, and on the volumetric power density ρ, is performed in **Section III**. This includes an analysis of

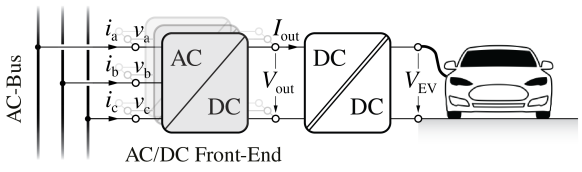


Fig. 1: Typical 3-Φ AC power distribution bus based Level 3 EV charging architecture, comprising an AC/DC PFC rectifier front-end and an isolated DC/DC converter for interfacing the 3-Φ AC-bus with the EV battery. Due to manufacturer specific EV battery voltages, off-board battery chargers must cover a wide output voltage range, i.e. provide a widely adjustable voltage conversion ratio between the 3-Φ sinusoidal AC-bus phase voltages v_a, v_b, and v_c and the battery voltage V_{EV}.

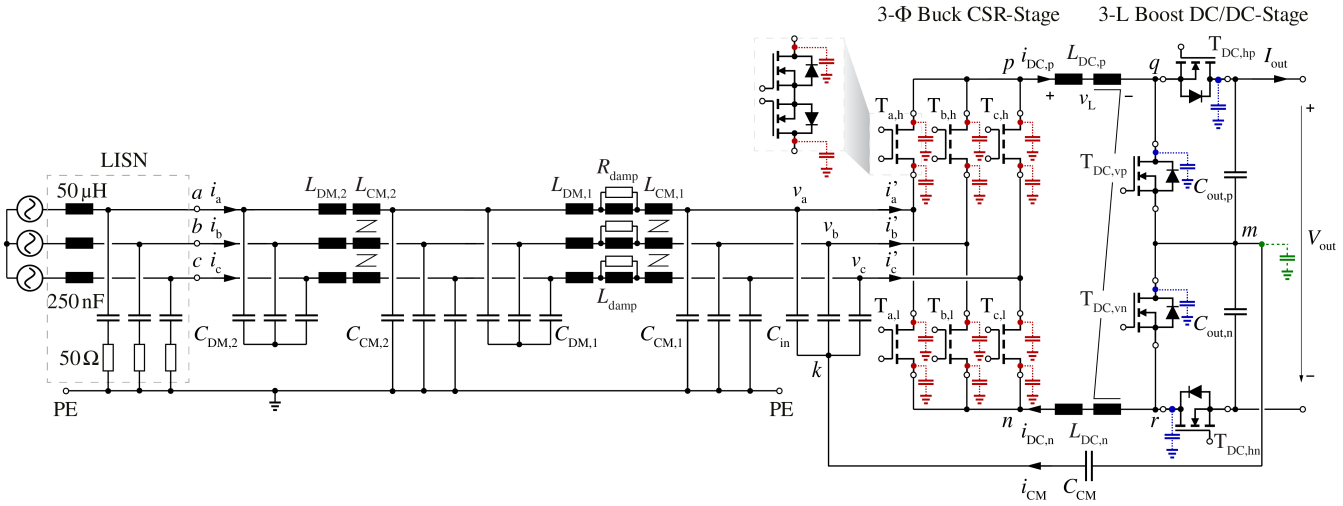


Fig. 2: Schematic of the proposed three-phase (3-Φ) bidirectional buck-boost (bB) current DC-link PFC rectifier system (EV battery charger 3-Φ AC/DC PFC front-end, cf. **Fig. 1**) including a two-stage EMI filter and employing a three-level (3-L) boost-type DC/DC-stage. To filter the common-mode (CM) noise at the output port, the artificial 3-Φ neutral point k and the DC voltage mid-point m are connected through a CM filter capacitor C_{CM}. The 3-Φ current source rectifier (CSR)-stage is realized with two anti-series common-source 1200 V silicon-carbide (SiC) power MOSFETs per switch (twelve in total), while the 3-L DC/DC-stage is realized by single 900 V SiC power MOSFETs. The parasitic capacitors most relevant for conducted CM noise emissions are additionally included in the schematic, e.g. from the drain nodes of the semiconductors in the CSR-stage (red) and in the DC/DC-stage (blue) to the grounded heat sink, and from the DC output rails and the DC mid-point to ground (green).

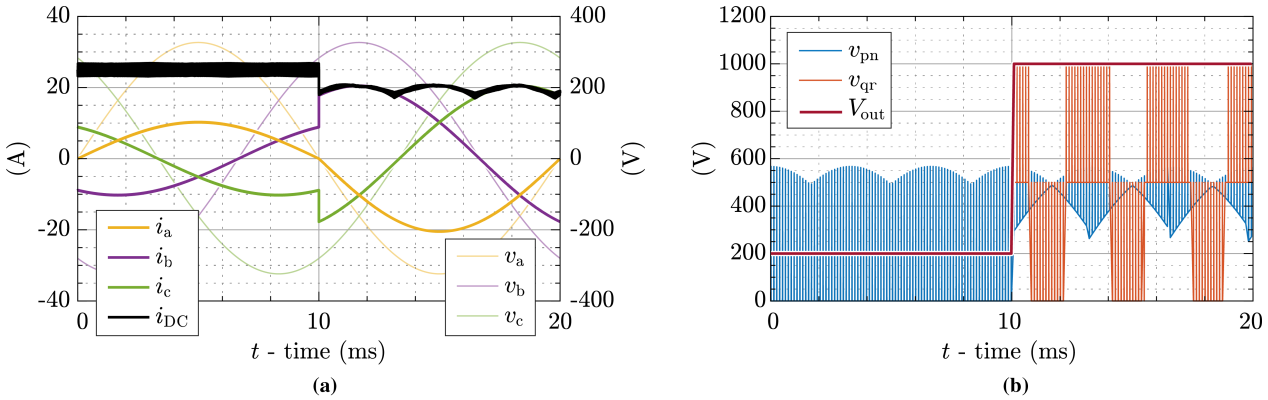


Fig. 3: Operating principle of the proposed 3-Φ bB current DC-link PFC rectifier system. In **(a)** the 3-Φ sinusoidal input currents i_a, i_b, and i_c, the DC-link current i_{DC}, and the 3-Φ sinusoidal AC-bus voltages v_a, v_b, and v_c are shown, and in **(b)** the switched voltages v_{pn} at the output of the CSR-stage and v_{qr} at the input of the DC/DC-stage, and the output voltage V_{out} are depicted. In order to highlight the dependency of the mode of operation on V_{out}, V_{out} is increased at time $t = 10\,\text{ms}$ from 200 V to 1000 V, hence the CSR-stage switches from 3/3-PWM (transistors of all three bridge-legs are switching within a switching period) to 2/3-PWM (switching state changes limited to two phases) operation, while the DC/DC-stage changes from clamping state (switches $T_{DC,hp}$ and $T_{DC,hn}$ permanently conducting) to 3-L operation.

the conduction and switching losses occurring in the two stages, which allows to identify the optimum number of parallel semiconductors and the required heat sink volume. Finally, optimum operating parameters and component values are determined resulting in a design featuring $\bar{\eta} = 98.5\,\%$ and $\rho = 13.9\,\text{kW/dm}^3$. **Section IV** summarizes the main findings and concludes the paper.

II. Operating Principle and Components Stresses

As first step of a brief analysis of the proposed topology, its operating range and operating principle, and the stresses on the main power components are discussed in this section.

A. Operating Principle

Three operating modes, i.e. the ***Buck-Mode*** ($\frac{3}{2}\hat{V}_{in} > V_{out}$), the ***Boost-Mode*** ($\sqrt{3}\hat{V}_{in} < V_{out}$) and the ***Transition-Mode*** ($\frac{3}{2}\hat{V}_{in} < V_{out} < \sqrt{3}\hat{V}_{in}$), can be defined [8].
In the ***Buck-Mode*** ($0 < t < 10\,\text{ms}$ in **Fig. 3**), i.e. for $V_{out} = 200\,\text{V} < \frac{3}{2}\hat{V}_{in} = 488\,\text{V}$, only the CSR-stage is switching, while the switches $T_{DC,hp}$ and $T_{DC,hn}$ of the DC/DC-stage are permanently conducting; hence, no switching losses are occurring in the DC/DC-stage. A constant DC-link current i_{DC} is controlled by the CSR-stage operated with 3/3-PWM [12], i.e. transistors of all three bridge-legs are switching within a switching period, and 3-Φ sinusoidal input currents i_a, i_b, and i_c are generated in phase with the 3-Φ sinusoidal AC-bus voltages v_a, v_b, and v_c. The voltage v_{pn} at the output of the CSR-stage is obtained switching between two line-to-line voltages and 0 V [8]. Furthermore, the CM emissions at the output port are minimized considering reduced CM 3/3-PWM, i.e. the zero state generating the minimum CM voltage is always preferred when $v_{pn} = 0\,\text{V}$ [12].

In the ***Boost-Mode*** ($10\,\text{ms} < t < 20\,\text{ms}$ in **Fig. 3**), i.e. for $V_{out} = 1\,\text{kV} > \sqrt{3}\hat{V}_{in} = 563\,\text{V}$, the CSR-stage is operated with 2/3-PWM, i.e. transistors of only two out of three bridge-legs are switching within a switching period, to reduce its switching losses [8], while i_{DC} is controlled to a six-pulse shape by the DC/DC-stage (synergetic control), which also reduces the total conduction losses. Only two line-to-line voltages are forming v_{pn}, while the DC/DC-stage generates a 3-L $\left(0\,\text{V},\ \frac{1}{2}V_{out},\ \text{and}\ V_{out}\right)$ voltage waveform v_{qr} at its input. Three sub-modes, characterized by different

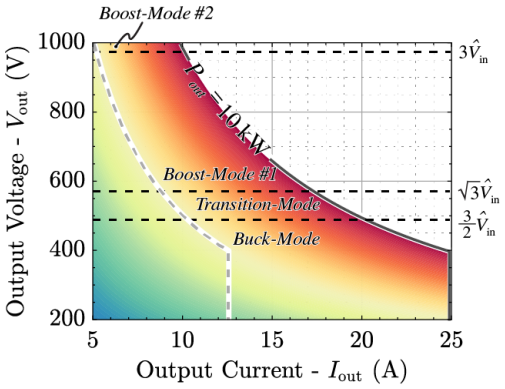


Fig. 4: Operating region of the proposed 3-Φ bB current DC-link PFC rectifier system. The three operating modes are highlighted. The dashed line indicates operating points for half maximum output power or output current.

modulation schemes of the DC/DC-stage, exist in the ***Boost-Mode*** depending on V_{out}, as shown in **Fig. 4** [12] (***Boost-Mode #3*** would be applied for $V_{out} > 2\sqrt{3}\hat{V}_{in} = 1126\,V$). Between ***Buck-Mode*** and ***Boost-Mode***, the system operates in the ***Transition-Mode*** ($\frac{3}{2}\hat{V}_{in} < V_{out} < \sqrt{3}\hat{V}_{in}$), where the converter is controlled as proposed in [13], automatically selecting the optimal operating mode with minimized conduction and switching losses, i.e. the CSR-stage alternates between 3/3-PWM and 2/3-PWM, and the DC/DC-stage is democratically activated only when its boost functionality is required.

The operating region of the proposed 3-Φ bB current DC-link PFC rectifier system (see **Fig. 4**) must cover a wide output voltage range, as required in EV battery charger applications. For the reasons clarified in the next section, the boundary of this region is divided in two sections, i.e. the constant output current section ($I_{out} = 25\,A$ for $200\,V < V_{out} < 400\,V$) and the constant output power section ($P_{out} = 10\,kW$ for $400\,V < V_{out} < 1\,kV$), as indicated with a grey solid line in **Fig. 4** [14]. There, a dashed line indicates operating points for half maximum output power or output current, and is considered in the calculation of $\bar{\eta}$ in **Section III**.

B. Component Stresses

The DC-link current i_{DC}, which determines the total conduction and switching losses, is considered first. Assuming zero high-frequency current ripple, the average and RMS values of i_{DC} showing a pulse-shape with six times the mains frequency in 2/3-PWM are

$$I_{DC,avg,2/3} = \frac{3}{\pi}\hat{I}_{in}, \tag{1}$$

$$I_{DC,rms,2/3} = \sqrt{\frac{1}{2} + \frac{3\sqrt{3}}{4\pi}}\hat{I}_{in}, \tag{2}$$

respectively. For a constant i_{DC} in 3/3-PWM, instead

$$I_{DC,avg,3/3} = I_{DC,rms,3/3} = \frac{1}{M}\hat{I}_{in} \tag{3}$$

holds, where $M = \frac{\hat{I}_{in}}{I_{out}}$ indicates the converter modulation index. $I_{DC,rms}$ is visualized in **Fig. 5** to justify the selected operating region of the converter system (cf. boundary marked in grey in **Fig. 4**). This is defined to fully utilize the main power components, e.g. the DC-link inductor, along the boundary of the operating region (the gray line in **Fig. 5(a)** follows an isoline of $I_{DC,rms}$).

The current stresses of the semiconductors in the CSR-stage are

$$I_{CSR,avg} = \frac{1}{3}I_{DC,avg}, \tag{4}$$

$$I_{CSR,rms} = \frac{1}{\sqrt{3}}I_{DC,rms}. \tag{5}$$

The RMS value of the switching frequency current in the input filter capacitors $I_{Cin,rms}$, which provides a preliminary indication for their voltage ripple and losses, and/or capacitance and volume, results as

$$I_{Cin,rms,2/3} = \sqrt{\frac{\sqrt{3}}{2\pi} - \frac{1}{6}}\hat{I}_{in}, \tag{6}$$

$$I_{Cin,rms,3/3} = \sqrt{\frac{2}{\pi}\frac{1}{M} - \frac{1}{2}}\hat{I}_{in}, \tag{7}$$

and is indicated in **Fig. 5(b)**.

The output capacitor C_{out} is selected to limit the peak-to-peak voltage ripple $V_{Cout,pp}$ (for each output capacitor), which is

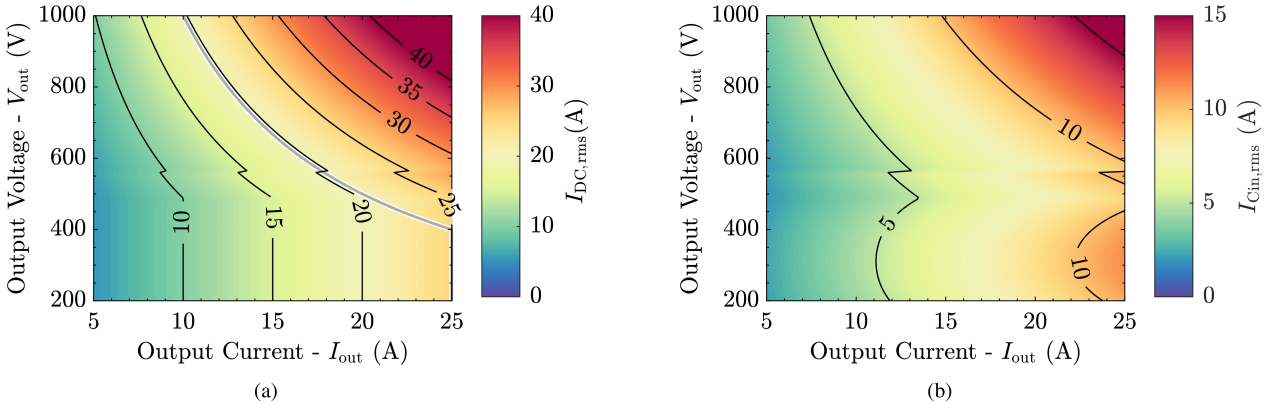
$$V_{Cout,pp,3/3} = \frac{1 - \frac{\sqrt{3}}{2}M}{8\,C_{out}\,f_{sw}^2}\frac{V_{out}}{L_{DC,CM}}, \tag{8}$$

$$V_{Cout,pp,2/3} = \frac{2}{C_{out}\,f_{sw}}\left(\frac{1}{M} - \frac{1}{M^2}\right)\hat{I}_{in}. \tag{9}$$

To conclude this section, the obtained analytical formulas (1) ∼ (9) are compared with the results of circuit simulations (for a system design according to **Section III.F**) in **Tab. I**, proving their accuracy.

III. Pareto Optimization

In order to identify the performance limits of the proposed topology, a multi-objective optimization is conducted in this section, following the flowchart depicted in **Fig. 6**. The design space, defined by the available components, operating



(a) (b)

Fig. 5: RMS value of **(a)** the DC-link current $I_{DC,rms}$ and of **(b)** the current flowing in each input filter capacitor $I_{Cin,rms}$ evaluated for $200\,V < V_{out} < 1\,kV$ to define the operating region of the proposed converter system. The modulation scheme is selected between 2/3-PWM and 3/3-PWM depending on the value of V_{out} for each operating point [8].

TABLE I: Comparison between analytical and simulation results of the expressions discussed in **Section II.B**. The system parameters of the design selected in **Section III.F** are assumed.

	200 V *Buck-Mode*		800 V *Boost-Mode*	
	Analyt.	**Sim.**	**Analyt.**	**Sim.**
$I_{\text{CSR,avg}}$	8.33 A	8.34 A	6.52 A	6.53 A
$I_{\text{CSR,rms}}$	14.43 A	14.44 A	11.30 A	11.31 A
$I_{\text{Cin,rms}}$	10.52 A	11.03 A	6.77 A	7.21 A
$V_{\text{Cout,pp}}$	0.60 V	0.61 V	9.75 V	10.20 V

parameters, electrical constraints, thermal limitations, etc., is mapped, through detailed loss and volume models of the individual components, into the $\bar{\eta}\rho$-Pareto performance space.

A. Optimization Inputs and Procedure

The input of the optimization procedure includes the system specifications, the design constraints, and the identified optimization variables. In particular, the number of parallel semiconductors N_{p} is selected as 1 or 2 in both stages (considering suitable SiC power MOSFETs according to **Section II.B**, after analyzing different semiconductors in the pre-design phase); the maximum peak-to-peak DC-link current ripple $\Delta I_{\text{DC,max}}$ is varied between 10 % and 25 % of the maximum I_{DC}; the switching frequency of the CSR-stage f_{CSR} is swept between 60 kHz and 220 kHz, while the one of the DC/DC-stage $f_{\text{DC/DC}}$ changes between $0.5 f_{\text{CSR}}$ and $2 f_{\text{CSR}}$ to ensure an exhaustive exploration of the design space.
After fixing the value of the optimization variables for each iteration, some component stresses, e.g. the voltage-time area across the DC-link inductors and the voltage ripple on the input and output capacitors, are calculated to select the most critical operating point for each component. Hence, e.g. the value of the DC-link DM inductor and of input and output capacitors, are defined accordingly and inserted into a script-based circuit simulation environment. The most significant waveforms characterizing the selected operating points along the full- and part-load operating boundaries, i.e. with $V_{\text{out}} = 200\,\text{V}, 300\,\text{V}$, and $400\,\text{V}$ in the constant output current section and $V_{\text{out}} = 500\,\text{V}, 600\,\text{V}, \ldots, 1\,\text{kV}$ in the constant output power section, are finally generated. These are at the basis of the AC side EMI filter design, the inductor and capacitor design and performance evaluation, and the semiconductor loss calculation and heat sink design, which are all performed according to the models and considerations presented in the following.

B. Semiconductor Losses

The semiconductor losses are calculated based on the results of experimentally derived loss maps. In particular, each switch of the CSR-stage is realized (for $N_{\text{p}} = 1$, cf. **Section III.A**) by two anti-series 1200 V 16 mΩ *C3M0016120K* SiC power MOSFETs [15]. These devices are characterized in a calorimetric switching loss measurement setup [16], obtaining the data and the polynomial fitting curves shown in **Fig. 7**. The considered fitting for hard-switching is

$$E_{\text{sw}}[\text{J}] = (k_1 I_{\text{sw}}^2 + k_2 I_{\text{sw}} + k_3) V_{\text{sw}} + (C_{\text{oss,Q}} + C_{\text{par}}) V_{\text{sw}}^2, \quad (10)$$

(I_{sw} in [A], V_{sw} in [V], C in [F]), and the coefficients are

$$k_1 = 85.1 \cdot 10^{-12},\ k_2 = 8.55 \cdot 10^{-9},\ k_3 = 27.6 \cdot 10^{-9}.$$

For soft-switching, the considered fitting is

$$E_{\text{sw}}[\text{J}] = k_4 I_{\text{sw}}^2 V_{\text{sw}}, \quad (11)$$

(I_{sw} in [A], V_{sw} in [V]) with

$$k_4 = 75.7 \cdot 10^{-12}.$$

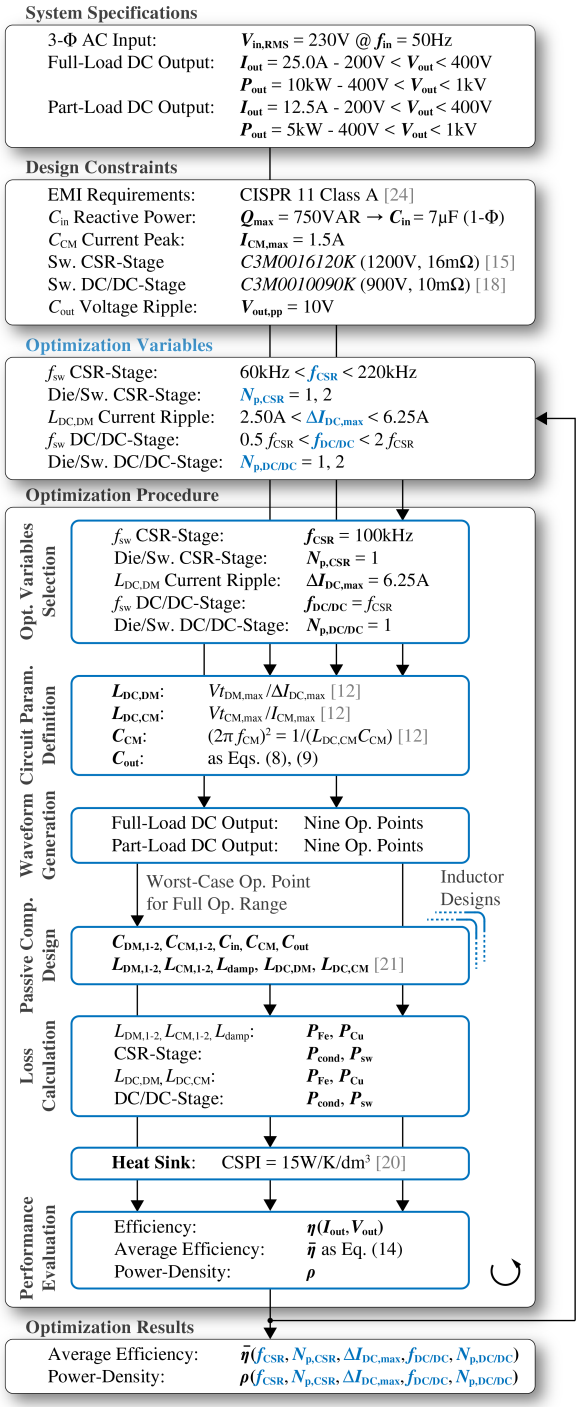


Fig. 6: Flowchart of the implemented optimization procedure for the proposed 3-Φ bB current DC-link PFC rectifier system.

The charge equivalent output capacitance $C_{\text{oss,Q}}$ in (10) is calculated from [15] and fitted as

$$C_{\text{oss,Q}}[\text{nF}] = \frac{k_{\text{c1}}}{k_{\text{c2}} + V_{\text{sw}}^{k_{\text{c3}}}} + k_{\text{c4}}, \quad (12)$$

(V_{sw} in [V]) with

$$k_{\text{c1}} = 42.8,\ k_{\text{c2}} = 7.38,\ k_{\text{c2}} = 0.77,\ k_{\text{c4}} = 0.17.$$

$C_{\text{par}} = 35\,\text{pF}$ in (10) is the additional parasitic capacitance introduced by the PCB and by the capacitive coupling of the power semiconductor package (TO 247-4) and the heat sink, which are separated by the thermal interface material (TIM, *BERGQUIST SIL-PAD 2000* [17]) used for isolation. Furthermore, the fitting of the measured temperature dependent on-state resistance is

$$R_{\text{ds,on}}[\text{m}\Omega] = 15.7 - 8 \cdot 10^{-3} \cdot T_{\text{j}} + 5 \cdot 10^{-4} \cdot T_{\text{j}}^2, \quad (13)$$

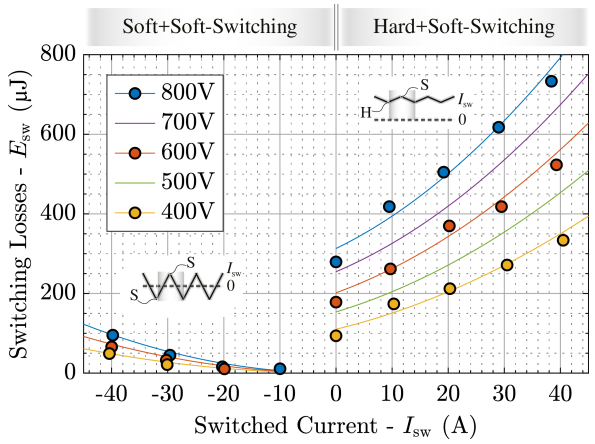


Fig. 7: Measured soft-switching and hard-switching losses of the considered 1200 V 16 mΩ *C3M0016120K* SiC power MOSFET for a full switching cycle at different switched voltage and current levels. The bridge-leg dead time is adjusted to ensure complete soft-switching transitions.

where T_j (in [°C]) is the junction temperature. In the final hardware realization, the same gate driver structure and power PCB layout of the measurement setup are used, thus comparable switching and conduction properties and thermal performance are expected, ensuring accurate loss estimations during the design phase.

Differently, each switch of the 3-L DC/DC-stage is realized (for N_p = 1) by a single 900 V 10 mΩ *C3M0010090K* SiC power MOSFET, achieving an output voltage of 1 kV with enough margin on the device blocking voltage rating [18]. The semiconductor losses are estimated from the results of calorimetric measurements presented in [19].

In both cases, the required heat sink volume is determined from the semiconductor losses, assuming an ambient temperature of 30 °C and a typical cooling system performance index (CSPI, [20]), i.e. thermal conductance normalized to the heat sink volume, of 15 $W/K/dm^3$. The total semiconductor losses over the wide output voltage and output current range (cf. **Fig. 4**) are evaluated first; hence, an aluminium heat sink is designed to maintain its temperature at 80 °C when the maximum losses occur.

C. DC-Link Inductor

The DC-link DM inductor $L_{DC,DM}$ is designed for the most critical operating point, i.e. the operating point where the largest area product is required to achieve the desired inductance value [12], considering different core materials (ferrite and iron powder), core geometries (E cores with dimensions from 13/7/4 to 80/38/20 and U cores with dimensions from 10/8/3 to 141/78/30, including the option of stacking multiple cores) and wire types (round and litz wires) [21]. Forced air cooling is assumed with an air speed of 2 m/s. The designs are evaluated at different operating points over the whole operating region (cf. **Fig. 4**). Only the realizations which fulfill defined thermal requirements ($T_{hot\text{-}spot} < 125$ °C) in all operating points are stored for the following system performance calculation.

The design of the DC-link CM inductor follows the same procedure. In other words, an optimization sub-routine for both DC-link inductors is integrated in the main procedure for the whole converter system. Hence, several inductor designs are considered for each converter design, and the optimal solutions are selected only in combination.

D. Capacitors

Ceramic capacitors are considered for the AC-side filter and at the converter output. The input capacitors (including EMI DM capacitors) are designed to filter the switched

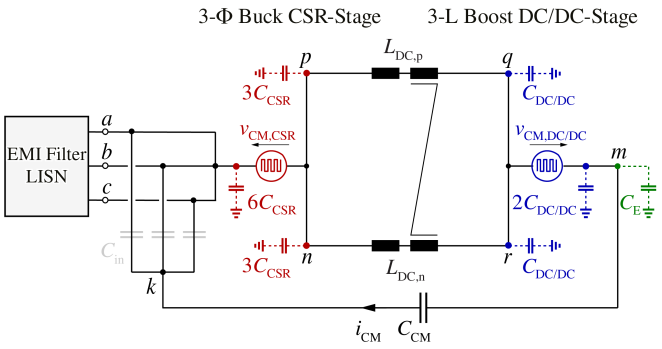


Fig. 8: High-frequency CM equivalent circuit of the proposed 3-Φ bB current DC-link PFC rectifier system obtained according to the procedure described in [22]. C_{CSR} and $C_{DC/DC}$ represent the parasitic capacitors of the semiconductors in the CSR-stage and in the DC/DC-stage, i.e. the capacitive coupling of the drain nodes and the grounded heat sink, estimated as 35 pF per package. C_E models the parasitic capacitance from the DC output rails and the DC mid-point to ground, assumed to be 140 pF according to [23]. The parasitic capacitive couplings of the DC-link inductor are neglected.

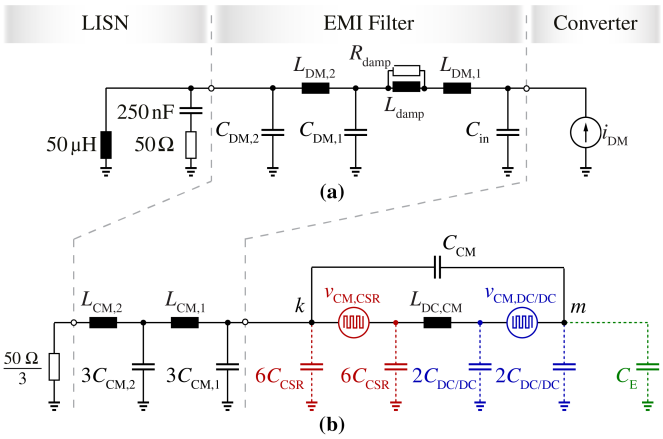


Fig. 9: High-frequency **(a)** single-phase DM and **(b)** CM equivalent circuit of the proposed 3-Φ bB current DC-link PFC rectifier system. The DM (CM) capacitors and inductors are neglected in the CM (DM) equivalent circuit.

current waveforms. The maximum allowed capacitance value is $C_{in} = 15\,\mu F$ per phase, such that the total reactive power is less than 7.5% of the rated output power (including EMI DM filter capacitors). The output capacitors are designed to limit the voltage ripple on each capacitor to 1% of the maximum output voltage. The integrated filter capacitor C_{CM} is selected to achieve the required natural frequency as in [12].

E. EMI Filter

A two-stage damped EMI filter is designed based on the calculated waveforms to provide sufficient attenuation, i.e. the maximum required attenuation over the wide output voltage and output current range (cf. **Fig. 4**), to meet the requirements of CISPR 11 class A [24]. To support this analysis, first, a high-frequency CM equivalent circuit of the converter system, featuring equivalent voltage noise sources, is obtained (see **Fig. 8**), where $v_{CM,CSR} = \frac{1}{2}(v_{pk} + v_{nk})$ and $v_{CM,DC/DC} = \frac{1}{2}(v_{qm} + v_{rm})$. After simplification, DM and CM equivalent circuits including the EMI filter are derived and shown in **Fig. 9** (i_{DM} denominating the HF component of the CSR-stage input phase current, e.g. i'_a, cf. **Fig. 2**). A passive damping concept, i.e. a damping resistor in parallel with a bypass inductor for the mains frequency current, is applied in each phase as in [25].

F. Design Analysis and Selection

Once the system design is completed, i.e. all circuit parameters are defined and all components are designed/selected,

and the converter performance in each operating point is calculated, a weighted average efficiency $\bar{\eta}$ is defined as

$$\bar{\eta} = \frac{k_\mathrm{f}}{N}\sum_{i=1}^{N}\eta_{i,\mathrm{f}} + \frac{k_\mathrm{p}}{N}\sum_{i=1}^{N}\eta_{i,\mathrm{p}} \tag{14}$$

(cf. **Fig. 6**) to estimate the converter system performance in a realistic battery charging scenario [26]. $k_\mathrm{f} = 0.8$ is the weight of full-load operation (assuming the converter delivers full power, solid line in **Fig. 4**, during 80 % of the operating time), $k_\mathrm{p} = 0.2$ is the weight of part-load operation, and $N = 9$ (since nine operating points, with $V_\mathrm{out} = 200\,\mathrm{V}, 300\,\mathrm{V}$, and $400\,\mathrm{V}$ in the constant output current section and $V_\mathrm{out} = 500\,\mathrm{V}, 600\,\mathrm{V}, \ldots, 1\,\mathrm{kV}$ in the constant output power section, are selected along the operating boundaries). The derived $\bar{\eta}\rho$-Pareto performance space is finally shown in **Fig. 9**, and highlights f_CSR (the axis variable) and $f_\mathrm{DC/DC}$ (the color bar variable). The performance space is the combination of several $\bar{\eta}\rho$-Pareto planes, each of them corresponding to one value of f_CSR.

The $\bar{\eta}\rho$-Pareto performance space is further analyzed considering the parallel coordinate plots shown in **Fig. 10**. Parallel coordinate plots allow to compare the characteristics of single designs with comparable performance, and to obtain a deep insight into the derived performance space [27].

The Pareto fronts associated to designs with different values of f_CSR, which determines the major fraction of switching losses and the first harmonic entering the regulated EMI frequency band ($150\,\mathrm{kHz} \sim 30\,\mathrm{MHz}$), are first compared in **Fig. 10(a.i)**. The designs with $f_\mathrm{CSR} = f_\mathrm{DC/DC}$ in the highlighted area around the Pareto front are analyzed in the parallel coordinate plot shown in **Fig. 10(a.ii)**. This highlights how the semiconductor losses are strongly influenced by the switching frequency and how the CSR-stage generates more losses than the DC/DC-stage, due to the higher number of semiconductors conducting i_DC and the higher number of switching transitions per period. By comparing the volume of the semiconductors heat sink with the one of the DC-link inductor, i.e. V_HS with $V_\mathrm{L,DC,CM}$, the characteristic power

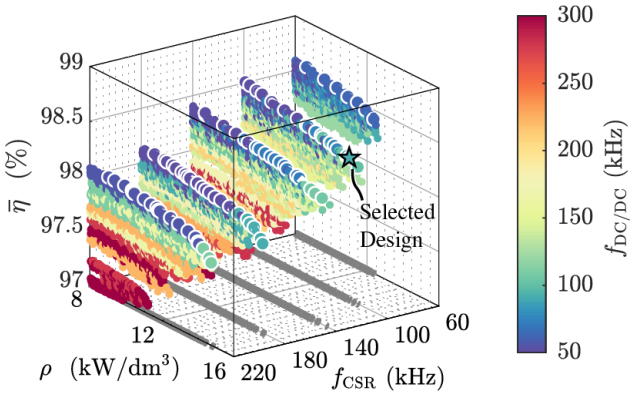


Fig. 9: Performance space of the proposed 3-Φ bB current DC-link PFC rectifier system considering the average efficiency $\bar{\eta}$, the volumetric power density ρ (calculated with reference to 10 kW and based on the sum of the boxed volumes of the power components), the switching frequency of the CSR-stage f_CSR, and the switching frequency of each bridge-leg of the DC/DC-stage $f_\mathrm{DC/DC}$. 3/3-PWM is assumed in all operating points, leading to increased switching losses in the ***Boost-Mode*** and to a larger heat sink design, but allowing the experimental verification of the loss reduction introduced by 2/3-PWM. Only designs fulfilling the system specifications in the entire operating region are shown.

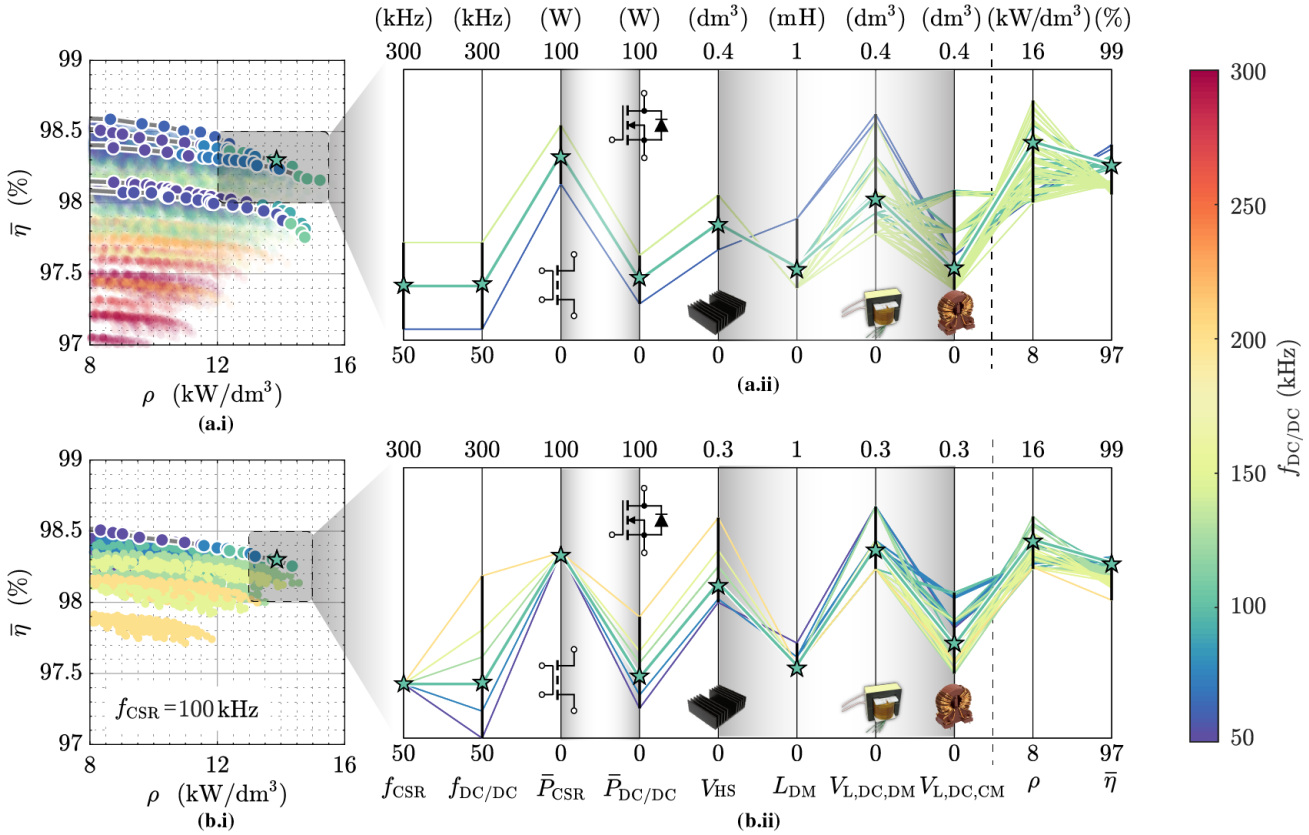


Fig. 10: Performance of the proposed 3-Φ bB current DC-link PFC rectifier system considering the average efficiency $\bar{\eta}$ and the volumetric power density ρ (calculated with reference to 10 kW). Specifically, **(a.i)** highlights the Pareto fronts associated to designs with different values of f_CSR and different values of $f_\mathrm{DC/DC}$ (2D representation of **Fig. 9**), while **(b.i)** is the $\bar{\eta}\rho$-Pareto plane corresponding to $f_\mathrm{CSR} = 100\,\mathrm{kHz}$. Moreover, **(a.ii)** provides, by means of a parallel coordinate plot, detailed information about the designs belonging to the highlighted area of the $\bar{\eta}\rho$-Pareto planes and featuring the same switching frequency for both stages ($f_\mathrm{CSR} = f_\mathrm{DC/DC}$), while **(b.ii)** considers designs with $f_\mathrm{CSR} = 100\,\mathrm{kHz}$, but different values of $f_\mathrm{DC/DC}$.

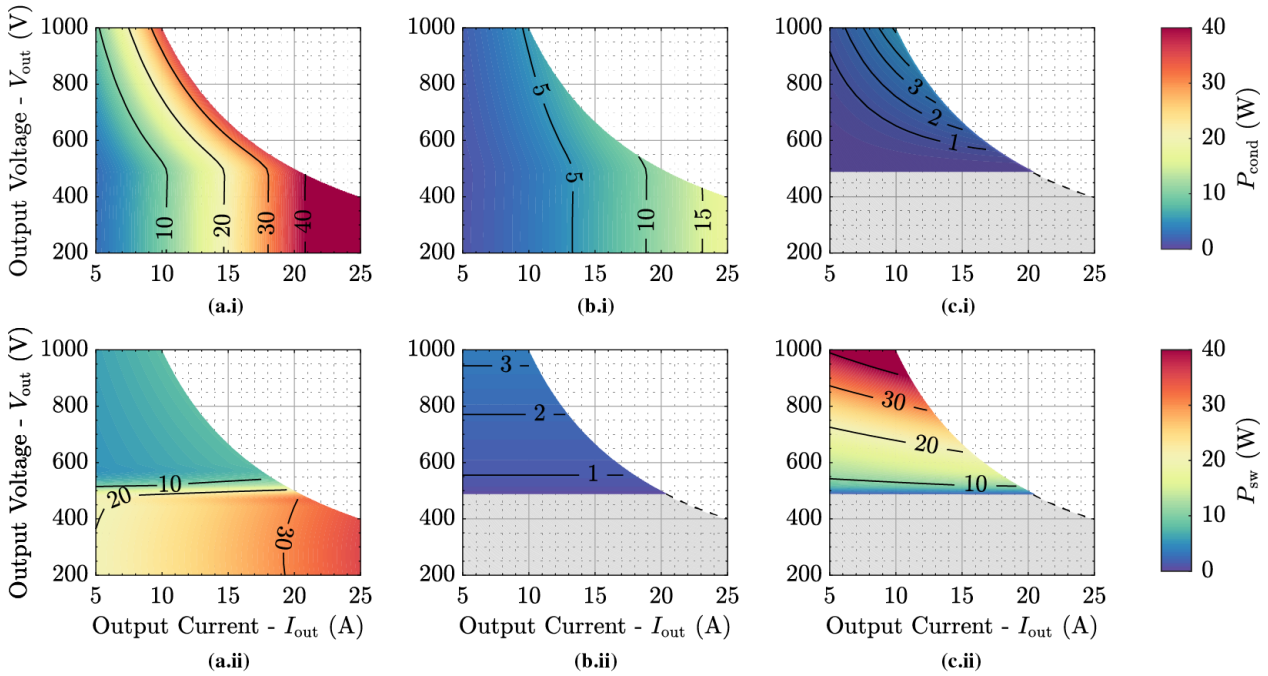


Fig. 11: Semiconductor losses of the selected 3-Φ bB current DC-link PFC rectifier system over the whole operating region. In particular, **(a.i)** total conduction losses and **(a.ii)** total switching losses occurring in the CSR-stage, **(b.i)** conduction losses and **(b.ii)** sum of the switching losses of the switches $T_{dc,hp}$ and $T_{dc,hn}$ of the DC/DC-stage, and **(c.i)** conduction losses and **(c.ii)** sum of the switching losses of the switches $T_{dc,vp}$ and $T_{dc,vn}$ of the DC/DC-stage. The grey shaded area indicates that no losses occur, since the DC/DC-stage remains clamped in the ***Buck-Mode*** operation. The system parameters listed in **Tab. II** are assumed.

density trade-off is visible: a converter operated at a higher switching frequency generates higher switching losses, hence requires a larger heat sink, but enables a downsizing of the magnetic components. Moreover, it can be observed that only few magnetic cores, which mainly determine $V_{L,DC,DM}$, are always used for the optimal designs in the highlighted area, regardless of the switching frequencies. This stresses the importance of a discrete multi-objective optimization based on off-the-shelf components, in contrast to a continuous optimization procedure which would provide designs with any core dimension.

The designs with $f_{CSR} = 100\,\text{kHz}$, but different values of $f_{DC/DC}$ are analyzed in **Fig. 10(b.i)**, and the details of the design space are provided in **Fig. 10(b.ii)**. Designs with higher $f_{DC/DC}$ lead to increased losses in the DC/DC-stage and thus larger V_{HS}. However, the required $L_{DC,DM}$ is not reduced, since the critical operating point with the maximum DC-link current ripple is in the ***Buck-Mode***, where the DC/DC-stage is clamped [12]. Additionally, the designs of the DC-link CM inductor $L_{DC,CM}$ are thermally limited, thus its volume is not affected by $f_{DC/DC}$. Hence, increasing $f_{DC/DC}$ leads to reduced power density and efficiency at the same time. A decreased $f_{DC/DC}$ generates less switching losses, and is responsible for only a slight increase of $L_{DC,DM}$. However, the increased voltage-time area leads to a larger $L_{DC,CM}$ and therefore to a lower ρ.

The analysis of the design space diversity additionally allows to identify the most advantageous designs among the ones with similar $\bar{\eta}\rho$-performance, e.g. introducing the maximum temperature or the peak flux density of the DC-link inductors as further design selection criteria.

The design with the parameters and components listed in **Tab. II** is finally selected, achieving an average efficiency $\bar{\eta} = 98.5\%$ and a volumetric power density $\rho = 13.9\,\text{kW/dm}^3$ (calculated as sum of the boxed volumes of the power components) at a switching frequency $f_{sw} = 100\,\text{kHz}$ for both stages ($f_{CSR} = f_{DC/DC}$).

TABLE II: Parameters of the selected design.

	Description	Value
f_{CSR}	CSR-stage switching freq.	100 kHz
$f_{DC/DC}$	DC/DC-stage switching freq.	100 kHz
T_{CSR}	CSR-stage semiconductor	*C3M0016120K*, N_p = 1 (1200 V, 16 mΩ)
$T_{DC/DC}$	DC/DC-stage semiconductor	*C3M0010090K*, N_p = 1 (900 V, 10 mΩ)
$L_{DC,DM}$	DC-link DM inductor	270 µH (5×N87 E42/21/20, 18 turns)
$L_{DC,CM}$	DC-link CM inductor	23 mH (2×VAC 45/30/15, 14 turns)
C_{in}	Input filter capacitor	3×7 µF
$C_{out,p} = C_{out,n}$	Output filter capacitor	2×10 µF
C_{CM}	Integrated filter capacitor	48 nF
$L_{DM,1} = L_{DM,2}$	EMI DM inductor	4.8 µH (KoolMu E18/08, 10 turns)
$C_{DM,1} = C_{DM,2}$	EMI DM capacitor	4 µF
$L_{CM,1} = L_{CM,2}$	EMI CM inductor	780 µH (2×VAC 16/10/6, 8 turns)
$C_{CM,1} = C_{CM,2}$	EMI CM capacitor	17 nF
ρ	Volumetric power density	13.9 kW/dm³
$\bar{\eta}$	Average efficiency	98.5 % (2/3-PWM) 98.3 % (3/3-PWM)

Detailed information on the semiconductor (conduction and switching) losses occurring in the CSR-stage and in the DC/DC-stage of the selected design are presented in **Fig. 11**. Due to the phase symmetrical operation of the CSR-stage, the conduction losses (see **Fig. 11(a.i)**) are distributed equally between the twelve switches. **Fig. 11(a.ii)**, instead, highlights how the switching losses in the CSR-stage are more significant in the ***Buck-Mode*** (3/3-PWM) than in the ***Boost-Mode***, where 2/3-PWM is applied [8]. The DC/DC-stage is clamped in the ***Buck-Mode***, hence no switching losses occur (see **Fig. 11(b.ii)** and **(c.ii)**), and conduction losses are present only

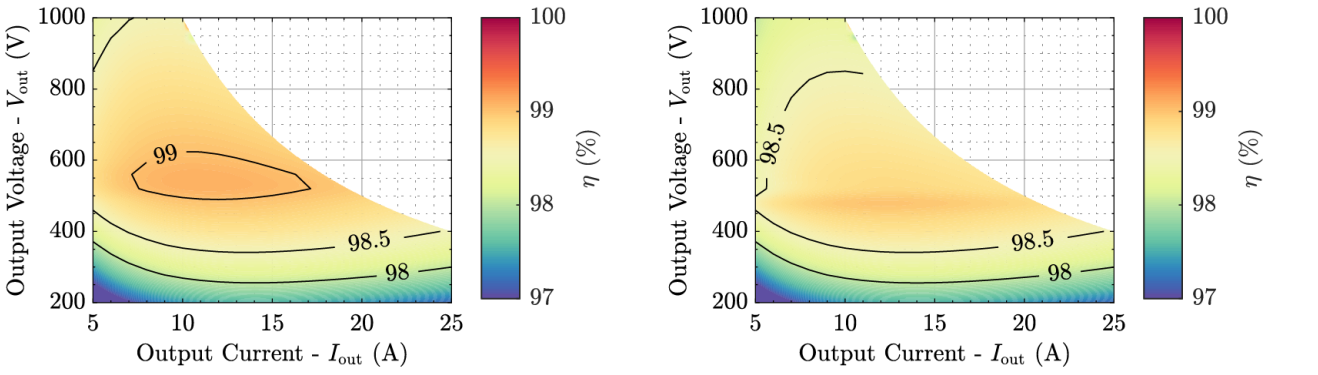


Fig. 12: Efficiency η of the selected $\bar{\eta}\rho$-Pareto optimum 3-Φ bB current DC-link PFC rectifier system design according to **Tab. II** over the whole operating region, in case of operation **(a)** with or **(b)** without 2/3-PWM.

in $\mathrm{T}_{\mathrm{dc,hp}}$ and $\mathrm{T}_{\mathrm{dc,hn}}$, which are conducting I_{out} (cf. **Fig. 11(b.i)** and **(c.i)**). Hard switching losses occur in $\mathrm{T}_{\mathrm{dc,vp}}$ and $\mathrm{T}_{\mathrm{dc,vn}}$ in the ***Boost-Mode***, as highlighted in **Fig. 11(c.ii)**. This detailed approach facilitates the selection of an optimal number of parallel devices and ensures a reliable semiconductor heat sink design.

To conclude, the efficiency η calculated for the selected design (see **Tab. II**) over the whole operating region is shown in **Fig. 12(a)**. In **Fig. 12(b)**, the efficiency of the same converter operated only with 3/3-PWM is depicted. In the ***Buck-Mode*** (cf. **Fig. 4**), the same η is achieved because 3/3-PWM operation is mandatory. In the ***Boost-Mode***, instead, the peak efficiency of the converter employing 2/3-PWM reaches $99.0\,\%$, which constitutes an up to $0.4\,\%$ improvement (cf. **Fig. 12(b)**).

IV. Conclusion

A high efficiency, reliable and geographically distributed battery charging infrastructure would accelerate the widespread adoption of EVs. Hence, a three-level three-phase bidirectional buck-boost current DC-link PFC rectifier system, suitable to perform AC/DC energy conversion in AC power distribution bus based fast EV charging architectures, is proposed in this paper. To cope with widely different EV battery voltages, the proposed converter features a wide output voltage range, i.e. $200\,\mathrm{V} < V_{\mathrm{out}} < 1\,\mathrm{kV}$, and is designed for an output power of $P_{\mathrm{out}} = 10\,\mathrm{kW}$, thus constituting a building block for a modular charging station. The operating principle of the converter system is briefly discussed and a suitable operating region is defined, after the analysis of voltage and current stresses experienced by the main power components, in order to maximize their utilization. Furthermore, a multi-objective optimization based on an average efficiency $\bar{\eta}$ and a volumetric power density ρ is conducted, considering typical EV battery charging profiles. The final design achieves $\bar{\eta} = 98.5\,\%$ and $\rho = 13.9\,\mathrm{kW/dm^3}$, and is selected after a careful investigation of the design space diversity, which is performed in parallel coordinate plots, indicating the main dependencies on the operating parameters, and component losses and volumes.

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