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***Abstract*—This paper presents a galvanic isolated multi-level dc-dc converter using different modulation strategies for wide voltage range operation. The dc gain of the converter can be changed in three steps by the proposed modulation schemes and thus achieve the change in output voltage among V_{out}, $0.5\times V_{out}$ and $0.25\times V_{out}$. The operating frequency of the resonant tank is the same in all three cases. Therefore, the converter can be designed to operate at the optimal operating point to maintain high efficiency for a wide voltage range operation. The output voltage can then be adjusted within the three output voltages depending on the application by either varying the switching frequency of the converter or cascading a second stage dc-dc converter. The operating principle and the dc characteristics of the proposed modulation scheme are discussed and demonstrated with a 17kW five-level half-bridge LLC resonant dc-dc converter prototype operating at 150 kHz. The input and output voltage of the converters are 750V voltage and, 650V, 325V and 163V output voltages, respectively. The experimental results are closely matched with the theoretical predictions.**

Keywords: multi-level dc-dc converter, resonant converter, modulation strategies, power electronic transformer

I. INTRODUCTION

Power electronic converters are becoming an important element for the future development of critical applications and are entering more and more in technologies, which traditionally belongs to different engineering disciplines as e.g. power distribution [1] [2] and universal power supplies [3]. Therefore, the power electronic converter technology has not only to meet characteristics demanded by the load, but also be able to process energy with high efficiency, high reliability, high power density and low cost. Furthermore, the possibility of having power converters which not only optimize performance and minimize the size of magnetic elements, but also allows the stabilization and improvement on the grid is of great benefit. The use of resonant converters is an attractive option to reach the aforementioned high requirements [4] [5]. However, for wide output/input voltage variation, the converter must operate with a wide range of switching frequency, which complicates the optimization of the converter [6] - [8]. In order to operate in wide voltage range, it is nearly impossible to process the energy with a single stage solution as presented in [9]. There, a combination of frequency modulation and using two different modulation strategies in order to change the DC gain of the converter is compared with a single stage solution. It shows that the converter efficiency decreases when the switching frequency is deviating from the optimal operating point, which is defined by the resonant frequency because the semiconductor turn-off losses as well as conduction losses are increasing. The change in the modulation strategy leads to higher efficiency and can therefore maintain constant high converter efficiency over wide voltage range operation. However, if the voltage range for certain application is even wider, two modulation strategies are not any more the best solution. Therefore, this paper proposes a method to reduce the impact of wide output/input voltage range in the performance of dc-dc isolated converter for high-input voltage applications. The approach combines the use of a five-level structure with proposed modulation strategies allowing two-level, three-level and five-level mode operation according to the output voltage range. Therefore, the required extreme output voltage variations of the converter can be achieved without penalizing the performance of the converter. As a result, the derating of efficiency encountered by the previous approaches can be avoided.

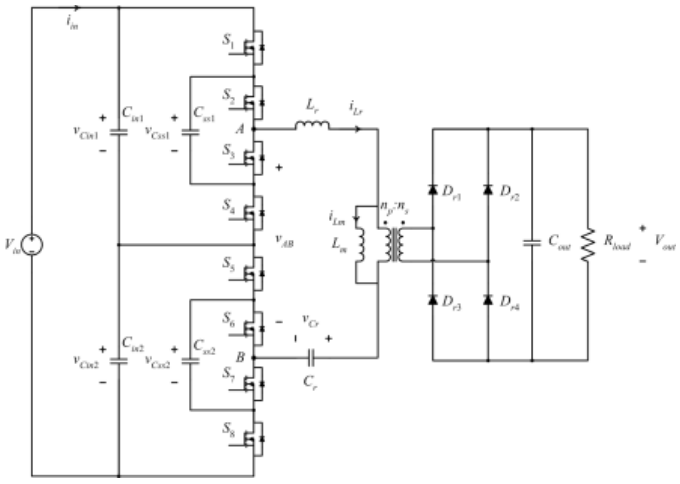

Figure 1: Schematic of the proposed five-level resonant converter.

II. CHARACTERISTIC OF THE PROPOSED FIVE-LEVEL RESONANT CONVERTER

Figure 1 shows the topology of the proposed 5-level LLC resonant converter. By the 5-level configuration, the voltage across the switches, S_1 to S_8, is only a quarter of the input voltage V_{in}. The power processing is realized in a resonant mode where ZVS is achieved at turn-on and reduced turn-off losses result for S_1 to S_8. The resonant inductor, L_r, can be implemented by using the inherent leakage inductance of the trans-

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former. Thus, the power density of the converter can be increased. The switching frequency of the converter is designed to be lower than the resonant frequency of the resonant tank. The magnetizing current is used to achieve the ZVS condition. Furthermore, the converter is operated in the region where the DC gain is insensitive to the load variations. As a result, the converter operates in an open loop manner which allows the optimization of the transformer and converter design. It is important to mention that this operation mode will require an additional conversion stage which will take care of the characteristics demanded by the load. Due to the LLC resonant tank characteristics, the diodes on the secondary side, D_{r1} to D_{r4}, operate under ZCS condition. Thus, the reverse recovery losses are minimized. Due to this reason, standard ultra-fast Si diodes can be used. The converter is operated with a two-level, three-level or five-level modulation strategy without penalizing the performance. The converter behaves as a power electronic transformer with a variable turns ratio. Figure 2, Figure 4 and Figure 5 show the gate signals and the key waveforms for the proposed modulation strategies. In order to guarantee the same DC gain despite of the input/output voltage variations, the conduction time of the switches S_1, S_2, S_5 and S_7 has to be equal and constant in all given modulation strategies. In order to meet this requirement, the switching frequency in each modulation strategy is different. In this case, the switching frequency will be f_s for the two-level modulation, $0.5\times f_s$ for three-level modulation and $0.25\times f_s$ for five-level modulation. Therefore, an equal equivalent frequency across the resonant tank and transformer are achieved despite of the modulation strategies. The combination of the five-level structure with the LLC resonant tank allows high frequency operation with high efficiency. In this way, the power density of the DC-DC converter is increased when compared with the state of the art ZVS PWM converters in wide voltage range operation.

III. Operating Principle

This section presents the operation principle of the proposed solution. As mentioned, for voltage conversion from e.g. a fixed input to a wide output voltage range, it can be realized by a single stage resonant converter. However, due to the wide operating range, the converter design, and thus the converter's efficiency and performance, can only be optimized at a single operating point. In order to keep a good performance throughout the operating range, a two stage solution with a front stage five-level LLC series resonant converter cascaded by a buck type converter is proposed. This configuration can maintain the efficiency nearly constant throughout the operating range and simplified the filter requirements of the buck type converter as the duty cycle is confined to a narrower range. In addition, the rms current in the converter is also minimized. The following description will be focused on the voltage conversion from a fixed input to a wide output range. The operation mode for a voltage conversion with the opposite characteristic, wide input voltage range to a fixed output voltage, is the same.

The five-level resonant converter can provide three different output voltage levels according to the modulation strategies. As mentioned before, the converter is designed to work with fixed switching frequency and the DC gain is close to unity. Therefore, the output voltage of the converter can be described as follow,

$$V_{out} = \frac{N_s V_{AB}}{2N_p(l-1)}. \quad (1)$$

Whereas V_{out} is the output voltage of the five-level resonant converter, N_p and N_s are the number of turns of primary and secondary winding of the transformer and l is the number of levels of the modulation strategies. Therefore, the output voltages of the resonant converter are V_{out}, $0.5\times V_{out}$ and $0.25\times V_{out}$ with respect to two-level, three-level and five-level modulation strategies.

A. Two-level Modulation

Figure 2 shows the timing diagram of two-level modulation. The operation is similar to the typical two-level resonant converter by applying a square waveform to the resonant tank, v_{AB}, with a peak value equals to V_{in}.

In the positive half cycle, S_1, S_2, S_7 and S_8 are closed. v_{AB} equals to V_{in}. D_{r1} and D_{r4} are conducting in this mode. The resonant tank is excited by the input voltage and the resonant tank current, i_{Lr}, is flowing in the positive direction.

In the negative half cycle, S_3, S_4, S_5 and S_6 are closed. v_{AB} equals to zero. D_{r2} and D_{r3} are conducting in this mode. The resonant tank is excited by the resonant capacitor voltage, v_{Cr}, which contains a DC component, and i_{Lr} flows in the negative direction.

In the two-level modulation, four of the switches have to share the full dc link voltage. S_1, S_2, S_7 and S_8 for the positive half cycle and S_3 to S_6 for the negative half cycle. Theoretically, four of them are switching at the same time in order to evenly share the dc link voltage. However, the voltage balancing between the MOSFETs is not guaranteed because of the tolerance of the parasitic drain-source capacitances, C_{ds}, and the timing of the gate signals. Moreover, C_{ds} is very sensitive to drain-source voltage and behave highly non-linear. This makes difficult that the drain-source voltage of MOSFETs is naturally

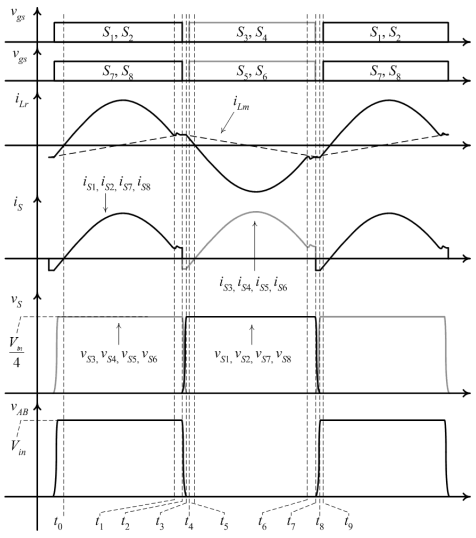


Figure 2: Timing diagram of the two-level modulation strategy.

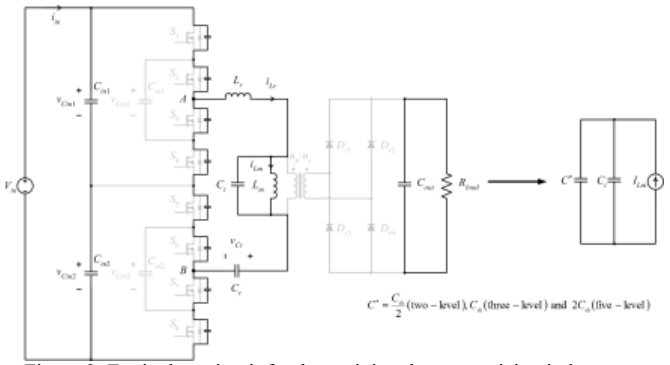


Figure 3: Equivalent circuit for determining the magnetizing inductance.

balanced. In order to tackle the problem, an additional linear capacitor is added to each of the drain-source terminals of the MOSFETs to diminish the non-linear effect of C_{ds}. This helps to share the voltages between the MOSFETs comparatively uniform. The detail operation within half of a switching cycle will be explained with the example of two-level modulation and the analysis can be extended to three-level and five-level modulation strategies as well. In those cases the magnitude of v_{AB} has to be changed to $0.5\times V_{out}$ and $0.25\times V_{out}$ for three-level and five-level modulation strategies.

Figure 3 shows the equivalent circuit to determine the minimum magnetizing current for fully charge and discharge all the capacitors during the switching transient for the three modulation strategies. The minimum magnetizing current can be determined as follow and summarized into Table I.

$$I_{Lm,\min} = \frac{\Delta V_{ds} C_{ds\_eqv}}{\Delta t} \tag{2}$$

From Table I, the required $I_{Lm,min}$ for the five-level modulation is the maximum and thus the design of the magnetizing inductance of the transformer has to be based on this modulation strategy also. The description of the five-level resonant converter working in two-level modulation is given below with the assistance of the timing diagram which is shown in Figure 2.

During the period $t_0 < t < t_1$, S_1, S_2, S_7 and S_8 are closed, the other switches are open and v_{AB} equals to V_{in}. Energy is transferring from the primary side to the secondary side through the excitation of the resonant tank by the voltage difference between v_{AB} and the sum of v_{Cr} and the voltage on the primary winding of the transformer, v_{pri} which is equal to the secondary voltage reflected to the primary side, nV_{out} when the output diodes are conducted. The output rectifiers D_{r1} and D_{r4} are conducting in this mode. C_{ds} of S_3 to S_6 are already fully charged

Table I. Minimum required magnetizing current for fully charged and discharged the C_{ds} for the three modulation strategies.

	Two-level	**Three-level**	**Five-level**
C_{eqv}	$0.5(C_{ds}+2C_t)$	$C_{ds}+2C_t$	$2C_{ds}+C_t$
Δv_{Cds}	V_{in}	$0.5V_{in}$	$0.25V_{in}$
$I_{Lm,min}$	$\frac{(C_{ds}+2C_t)V_{in}}{2\Delta t}$	$\frac{(C_{ds}+C_t)V_{in}}{2\Delta t}$	$\frac{(C_{ds}+0.5C_t)V_{in}}{2\Delta t}$
v_{Lm}	V_{in}	$0.5V_{in}$	$0.25V_{in}$
V_{ab}	V_{in}	$0.5V_{in}$	$0.25V_{in}$

before mode 1 and the drain-source voltage of S_3 to S_6 is equal to a quarter of V_{in} respectively. The resonant tank current, i_{Lr}, flows in the positive direction.

$$v_{Cr}(t) = V_{AB} - nV_{out} + [nV_{out} + v_{Cr}(t_0) - V_{AB}]\cos\omega_0(t-t_0) \tag{3}$$

$$i_{Lr}(t) = \frac{1}{Z_0}[V_{AB} - nV_{out} + v_{Cr}(t_0)]\sin\omega_0(t-t_0) \tag{4}$$

This mode ends when i_{Lr} equals to the magnetizing current i_{Lm}.

During $t_1 < t < t_2$, S_1, S_2, S_7 and S_8 are still closed. v_{AB} is still equal to V_{in}. The output rectifiers D_{r1} and D_{r4} turn-off softly under the resonant process, no high *di/dt* exists and thus the reverse recovery current is limited. As a result, no energy can be transferred to the secondary side as the resonant tank current is smaller than and limited to i_{Lm}. The converter enters to the circulating stage. i_{Lr} equals to i_{Lm} and the rate of change of i_{Lm} depends on the voltage on v_{pri} and the magnetizing inductance of the transformer. This stage should keep short in order to minimize the conduction losses.

$$i_{Lr}(t) = i_{Lm}(t) = \frac{nV_{out}(t-t_1)}{L_m} + i_{Lm}(t_1) \tag{5}$$

$$v_{Cr}(t) = \frac{nV_{out}(t-t_1)^2}{2L_mC_r} + \frac{i_{Lm}(t_1)(t-t_1)}{C_r} + v_{Cr}(t_1) \tag{6}$$

This mode ends when the gate signal of S_1, S_2, S_7 and S_8 are turned-off.

During $t_2 < t < t_3$, all the switches are open in this operating mode, the C_{ds} of S_1, S_2, S_7 and S_8 is charged and the output capacitance of S_3 to S_6 is discharged by i_{Lm}. Therefore, the duration of this mode depends on the magnitude of the i_{Lm} and the equivalent capacitance of the loop. The equivalent circuit of this mode is shown in Figure 3 where C_t is the parasitic terminal capacitor of the transformer. This mode ends when v_{S1}, v_{S2}, v_{S7} and v_{S8} equal to a quarter of V_{in} and v_{S3} to v_{S6} equal to zero. The converter is still in a circulating stage and thus no energy is transferred to the secondary side. In order to simplify the calculation, i_{Lm} is considered unchanged as the change in i_{Lm} is very small and the duration of this mode is very short.

$$i_{Lr}(t) = i_{Lm}(t) = I_{Lm} \tag{7}$$

I_{Lm} is defined in Table I.

$$v_{Cr}(t) = \frac{I_{Lm}(t-t_2)}{C_r} + v_{Cr}(t_2) \tag{8}$$

During $t_3 < t < t_4$, when v_{S3} to v_{S6} equal to zero and i_{Lm} is still flowing in the positive direction, the body diodes of S_3 to S_6 conduct and clamp the drain-source voltages to zero. As v_{S3} to v_{S6} equal to zero, v_{S1}, v_{S2}, v_{S7} and v_{S8} are clamped to a quarter of V_{in}. The resonant tank is excited by v_{Cr} and started a resonant process. As v_{S3} to v_{S6} are clamped to zero, gate signals of S_3 to S_6 should be applied to turn-on the switches in zero-voltage condition before the current direction of i_{Lr} reverses polarity. The output rectifiers D_{r2} and D_{r3} are conducting and this mode ends when the gate signals of S_3 to S_6 are applied. As v_{AB}

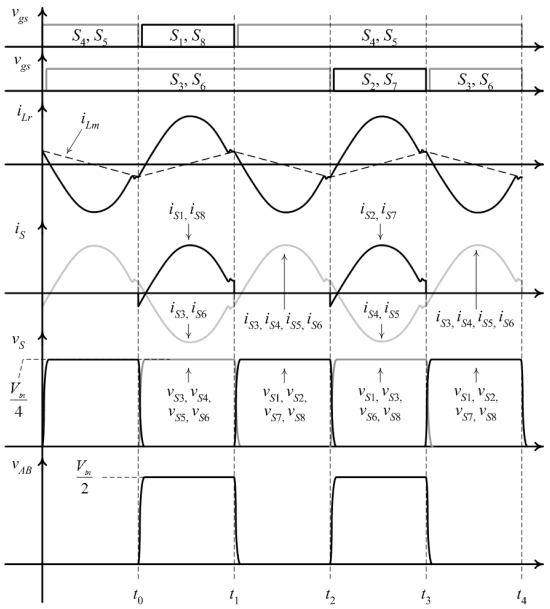


Figure 4: Key waveforms of three-level modulation strategy.

equals to zero, the resonance is triggered by the voltage difference between v_{Cr} and v_{pri}.

$$v_{Cr}(t) = nV_{out} + \left[v_{Cr}(t_3) - nV_{out}\right]\cos\omega_0(t-t_3) + i_{Lr}(t_3)Z_0\sin\omega_0(t-t_3) \quad (9)$$

$$i_{Lr}(t) = \frac{nV_{out} - v_{Cr}(t_3)}{Z_0}\sin\omega_0(t-t_3) + i_{Lr}(t_3)\cos\omega_0(t-t_3) \quad (10)$$

These are the operation modes for the positive half switching cycle and the operation of the negative half switching cycle is the same but opposite in polarity.

B. Five-level Modulation

Figure 5 and Figure 6 show the key waveforms and operating modes of the converter with the proposed five-level modulation. As mentioned before the operation is similar to the two-level modulation but the voltage level of v_{AB} is only a quarter of V_{in}. This can be realized by utilizing the input and flying capacitors, C_{in} and C_{ss}, together with the switching strategy. Therefore, the voltage balancing between the MOSFETs is not sensitive to the tolerances of the C_{ds} under the aid of C_{in} and C_{ss}.

In mode 1 [$t_0 - t_1$], Figure 6 (a), the first positive half cycle, S_1, S_3, S_5 and S_6 are closed and the other devices are open. v_{AB} is equal to the difference between v_{Cin1} and v_{Css1}. Since v_{Cin1} is equal to half of V_{in} and v_{Css1} is equal to a quarter of V_{in}, v_{AB} is equal to a quarter of V_{in}. During this period, C_{in} is providing the energy and C_{ss1} is been charged at the same time. D_{r1} and D_{r4} conduct in this mode since i_{Lr} is in the positive direction.

In mode 2 [$t_1 - t_2$], Figure 6 (b), the negative half cycle, S_3, S_4, S_5 and S_6 are closed and the other devices are open. The resonant capacitor voltage, v_{Cr}, becomes the source of the resonance process. The DC value of the v_{Cr} equals to half of v_{AB}. i_{Lr} is in the negative direction. D_{r2} and D_{r3} are conducting in this mode.

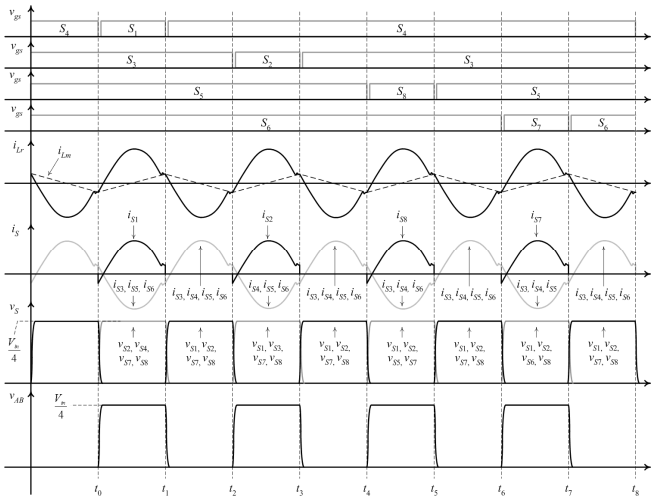


Figure 5: Key waveforms of five-level modulation strategy.

In mode 3 [$t_2 - t_3$], Figure 6 (c), the second positive half cycle takes place. The operation is equal to mode 1 but v_{AB} is supplied by v_{Css1}.

The operation of mode 4, [$t_3 - t_4$], mode 6, [$t_5 - t_6$], and mode 8, [$t_7 - t_8$], are equal to mode 2, Figure 6 (b).

In mode 5 [$t_4 - t_5$], Figure 6 (d), a third positive resonant half cycle occurs. S_3, S_4, S_6 and S_8 are closed and the rest of the devices are open. v_{AB} is equal to the difference between v_{Cin2} and v_{Css2}. Since v_{Cin2} is equal to half of V_{in} and v_{Css2} is equal to a quarter of V_{in}, v_{AB} is equal to a quarter of V_{in}. C_{in} is discharged and C_{ss2} is charged. D_{r1} and D_{r4} conduct in this mode. i_{Lr} is in the positive direction.

In mode 7 [$t_6 - t_7$], Figure 6 (e), the final positive half cycle of the complete switching cycle takes place. The operation is equal to mode 5 but v_{AB} is supplied by v_{Css2}.

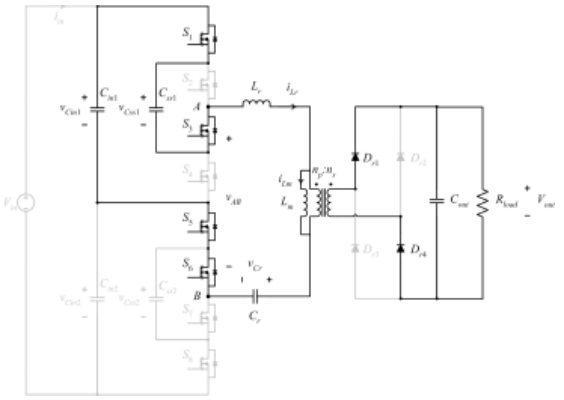
IV. Simplified Design Guidelines for the Proposed Five-level Resonant Converter

- Determination of the switching frequency, f_s:

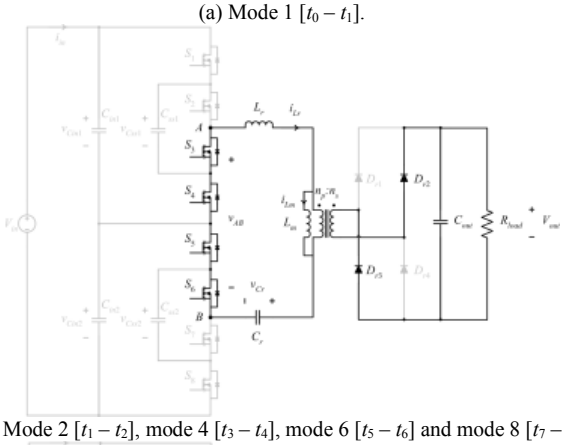
The switching frequency of the converter is determined based on the total losses of the switches and the transformer. In general, a higher switching frequency selection results in a lower magnetic flux, thus the core size, as well as the core loss, can be reduced. However, higher the switching frequency also results in higher AC loss on the winding of the transformer and turn-off loss on the switches which penalizes the converter efficiency. As a result, the selection of the switching frequency is a compromise of these two effects. Those depend on the power rating, semiconductor type and operating range of the converter.

- Determination of the resonant tank frequency:

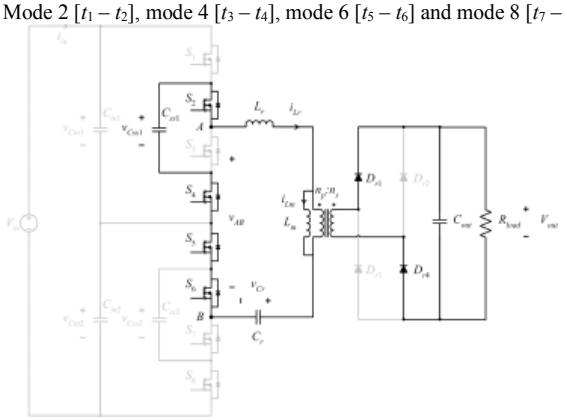
In order to minimize the resistive losses, the duration of the circulating stages, mode 2 – mode 3, shown in Figure 2, should



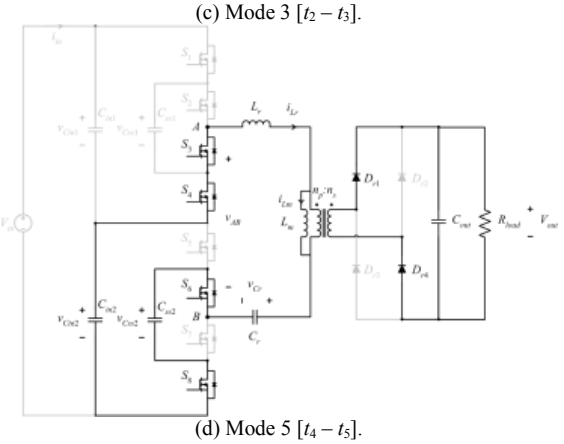
(a) Mode 1 [$t_0 - t_1$].



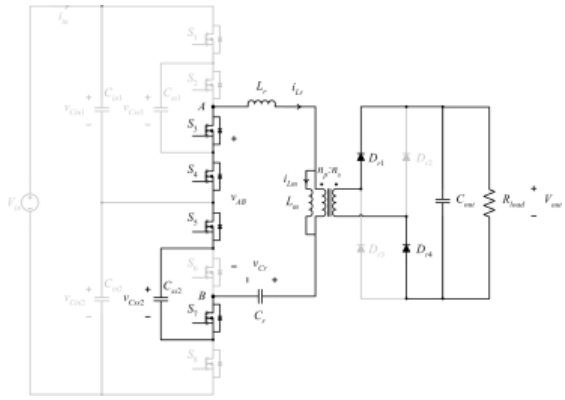
(b) Mode 2 [$t_1 - t_2$], mode 4 [$t_3 - t_4$], mode 6 [$t_5 - t_6$] and mode 8 [$t_7 - t_8$].



(c) Mode 3 [$t_2 - t_3$].



(d) Mode 5 [$t_4 - t_5$].



(e) Mode 7 [$t_6 - t_7$].

Figure 6: Operating modes of the five-level modulation strategy.

be minimized. This can be achieved setting the frequency ratio, f_n, of the switching frequency, f_s, to the resonant frequency of the resonant tank, f_r, smaller than but close to unity.

$$f_n = \frac{f_s}{f_r} < 1 \tag{11}$$

- Determination of the transformer's turns ratio

As the converter is designed to operate in open loop and in an operating point insensitive to load variations, the turns ratio of the transformer will be defined by the critical output and input voltages defined by the given specifications. For this paper, the critical conditions are minimum input voltage and maximum output voltage.

$$n = \frac{N_p}{N_s} = \frac{V_{in}}{2V_{out}} \tag{12}$$

- Determination of the minimum magnetizing current, $I_{\mathrm{Lm,min}}$, and magnetizing inductance of the transformer, L_{m}:

The maximum magnetizing current is determined based on the need to fully charge and discharge the parasitic C_{ds} of the MOSFETs and the transformer equivalent capacitance during the time $t_2 < t < t_3$ as shown in Figure 2. By using Table I, one can conclude that the magnetizing current for five-level modulation is the most demanding. It is reproduced here for convenience.

$$I_{Lm,\min} = \frac{T_s}{8} \frac{\Delta t}{2C_{ds} + C_t} \tag{13}$$

- Determination of the Q factor:

In order to minimize the circulating energy and rms current a small quality factor value, Q for rated power should be set. Q = 0.2 is a desired value [10].

- Determination of the resonant tank, L_{r} and C_{r}:

With the information of turns ratio and L_{m}, the transformer can be built. In order to increase the power density of the converter, the leakage inductance of the transformer is utilized as

the resonant inductor, L_r, rather than using an additional inductor. Therefore, the resonant capacitor, C_r, can be determined by the measured value of L_r and (8),

$$C_r = \frac{1}{4\pi^2 f_r^2 L_r} \tag{14}$$

- Determination of the flying capacitors, C_{ss}:

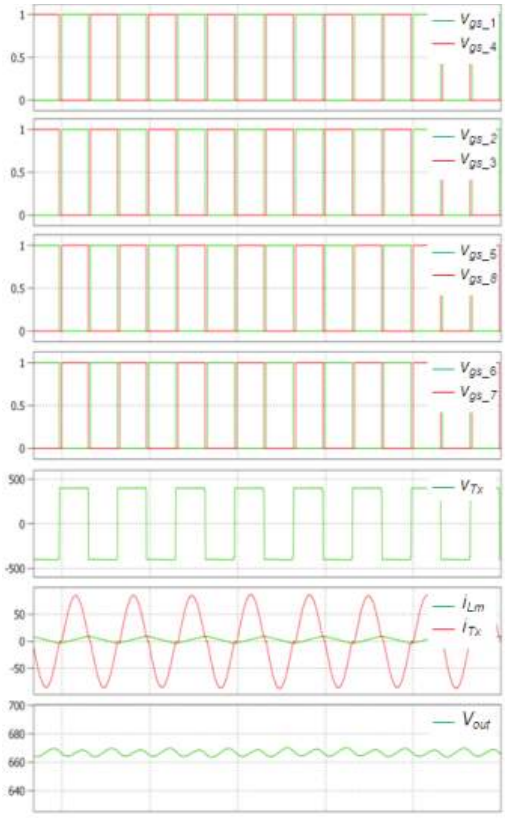
C_{ss} is part of the energy source for the resonant for three-level and five-level modulations. The voltage variation on C_{ss} will be reflected on the drain-source voltage of the switches in those modulation modes. Therefore, by setting allowable voltage variation across the capacitor, Δv_{Css}, the capacitance of C_{ss} can be determined as follow:

$$C_{ss} \geq \frac{2\sqrt{2}}{kR_{ac}\omega_r}, \tag{15}$$

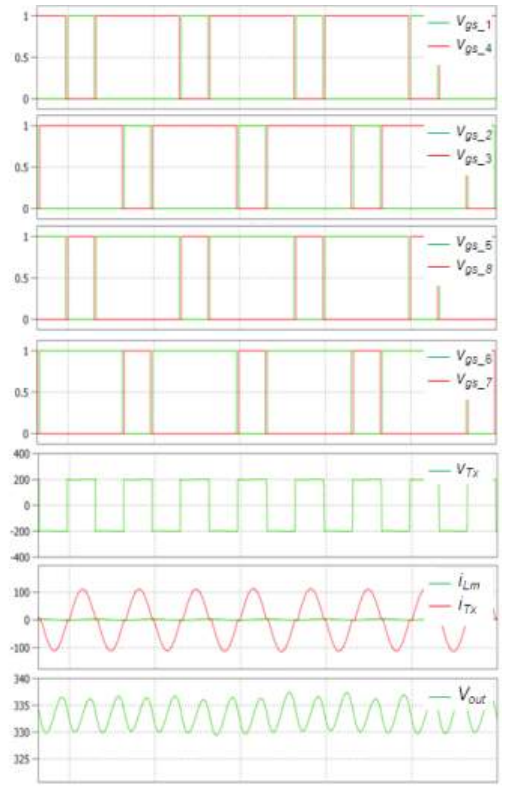
where k is the allowable percentage of voltage variation on v_{Css}.

V. Simulation and Experimental Verification

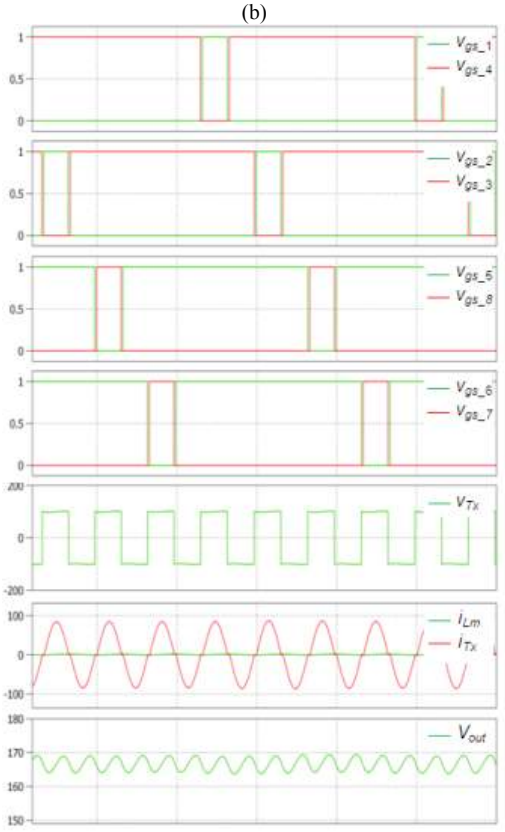
The proposed converter and modulation scheme are theoretically verified by simulation using Matlab and Plecs. Figure 7 shows the simulation results of the key waveforms of the proposed converter at an operating condition of 17kW and 150kHz resonant frequency. The switching pattern of the gate signals is modified according to the modulation scheme. It is important to observe that the operating frequency of the resonant tank remains unchanged. The output voltage is set to 665V, 333V and 165V for the two-level, three-level and five-



(a)



(b)



(c)

Figure 7: Simulation results of the key waveforms for the three modulations (a) two-level, (b) three-level and (c) five-level modulations.

Table II. Design parameters and resulting component values for the resonant converter prototype.

Items	Value	Items	Value
f_s	150kHz	C_{ds}	2.04nF
n	0.58	C_t	120pF
f_n	0.95	Δt	600ns
f_r	158kHz	L_m	100µH
C_r	1.65µF	L_r	0.62µH
C_{ss1} and C_{ss2} (with k = 0.1)			32µF
$S_1 - S_8$	4 x IRFP4768PbF	$D_{r1} - D_{r4}$	APT2x101DQ120J

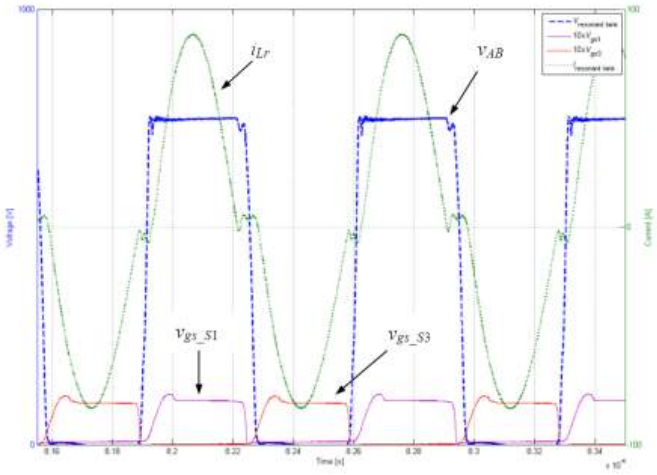


Figure 8: Experimental key waveforms with the proposed two-level modulation.

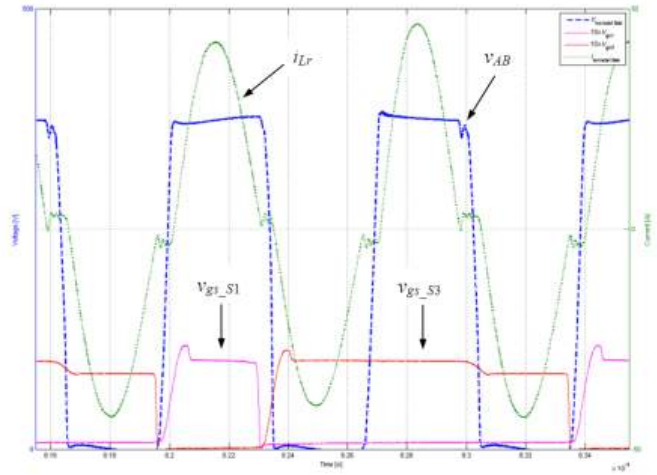


Figure 9: Experimental key waveforms with the proposed three-level modulation.

level modulations respectively and is closely matched with the theoretical prediction of equation (1).

A 17kW, 750V input voltage, 80V to 650V output voltage converter has been built to verify the theoretical prediction. The converter consists of two stages; the front stage is the 150kHz five-level half-bridge LLC resonant dc-dc converter; and the second stage is a buck type converter. The front stage converter can deliver three different output voltages according to the modulation strategies; these are 650V, 325V and 163V.

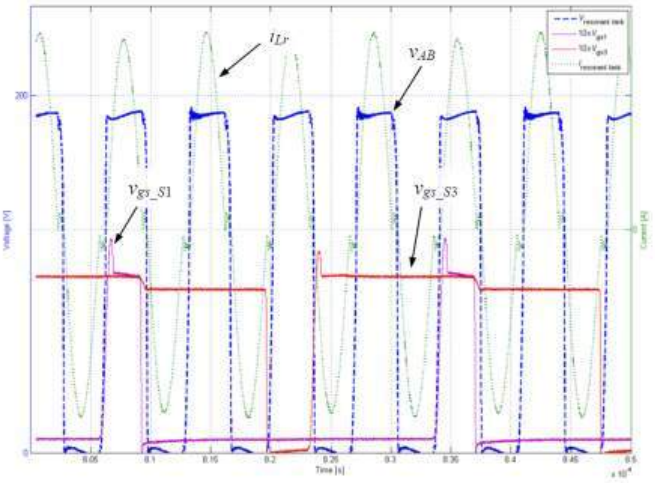


Figure 10: Experimental key waveforms with the proposed five-level modulation.

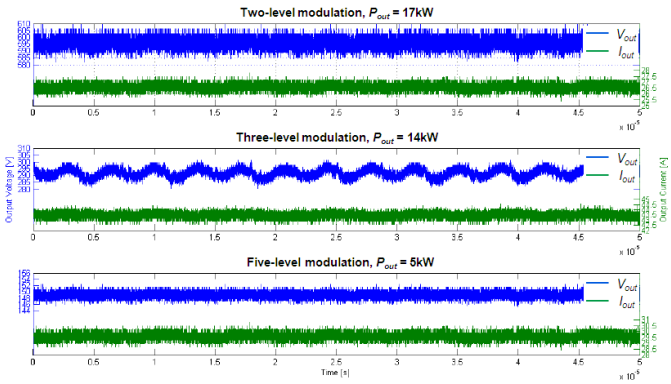


Figure 11: Experimental output voltage and current waveforms of two-level (top), three-level (middle) and five-level (bottom) modulations.

Therefore, the second stage buck type converter is only responsible to regulate the output voltages between 80V to 150V for 163V input, 150V to 300V for 325V input and 300V to 600V for 650V input. Taking in account that the input/output voltage ratios for the buck type converter are almost the same for the three operating ranges; the duty ratios, as well as the output current ripple, are almost the same for the three cases. This feature helps to simply the design of the buck type converter as the operating range and condition are limited and similar in the three cases. The component values for the resonant converter are determined based on the design guidelines given in Section IV and summarized in Table II.

Figure 8, Figure 9 and Figure 10 show the experimental key waveforms and the output voltage and current waveforms of resonant converter with two-, three- and five-level modulation strategies. Figure 10 shows that the voltage level of V_{AB} is around 750V, 375V and 188V respectively. The experimental measurement is closely matched with the theoretical prediction which is summarized in Table I. Similarly, Figure 11 shows that the output voltage is about 600V, 295V and 150V for the three modulation strategies. Figure 12 shows the efficiency of the proposed power electronic converter.

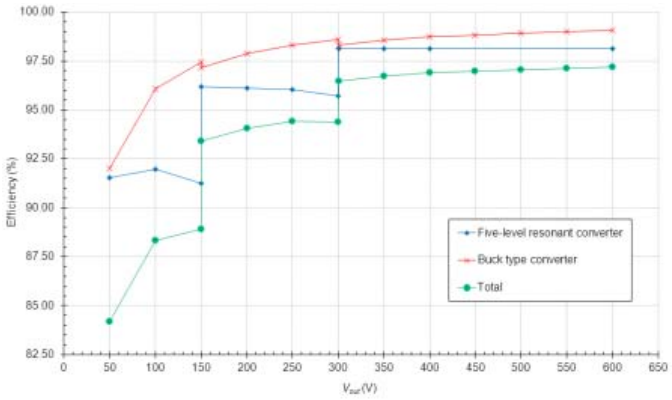


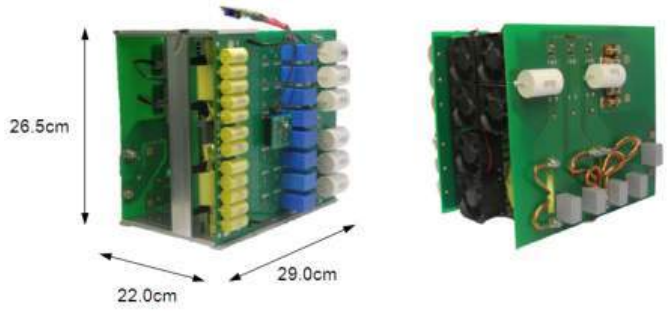
Figure 12: Efficiency curves of the proposed five-level resonant converter with the proposed modulation strategies.

It is important to mention that the design of the resonant converter is simple as it only operates at the optimal operating point. In this way, the circulating and rms current in the converter are minimized allowing a positive impact in the design of the transformer. As mentioned, the voltage steps feature provided by the resonant converter also result in a simplification in the design of the second stage converter. As a result, the overall system will present high efficiency as shown in Figure 12, and power density despite of the sever output voltage variations.

Finally, Figure 13 shows the experimental prototype. Figure 13 (a) shows the primary side of the proposed five-level resonant converter and Figure 13 (b) shows the secondary side of the output rectification and output capacitor and the second stage buck type converter. The buck type is not described as it is out of the scope of the paper. The power density of the overall converter is 1kW/dm^3.

VI. CONCLUSIONS

A converter and modulation scheme which can maintain high efficiency and power density for wide input/output voltage range have been proposed. The proposed converter consists of two stages which includes a five-level half-bridge LLC series resonant converter cascaded by a second stage buck type converter. The buck type converter benefits from the five-level resonant converter because the operating range is reduced. As a result, the efficiency and power density of the proposed converter are higher than the ordinary single stage resonant converter with frequency control. A 17kW, 750V input, 80V to 600V output converter has been built and evaluated. The



(a) (b)

Figure 13: Photos of the experimental prototype (a) the proposed 5-level resonant converter and (b) buck derived converter.

operations of the converter are in good agreement with theoretical prediction.

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