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***Abstract*—This paper introduces a novel unidirectional unity power factor single-to-three-phase Z-source Buck+Boost AC/AC Converter (*123ZBBC*) topology to supply three-phase AC machines with widely varying rated voltage directly from the single-phase mains. Due to the integration of the boost circuit into the inverter stage, the proposed circuit benefits from a reduced realization effort and an increased robustness. Furthermore, the insertion of a front-end buck-stage allows to select an intermediate voltage which is lower than the peak mains voltage and on the other hand enables to achieve a sinusoidal input current within the entire mains period. The paper gives a detailed analysis of the proposed converter including the different conduction states, the modulation schemes in order to implement the power factor correction and the inverter functionality, as well as the corresponding closed-loop control enabling sinusoidal input current and output voltages. Furthermore, the converter operation is verified by circuit simulations and the stresses on the main components are analyzed and compared to a conventional single-to-three-phase Z-source based AC/AC converter system.**

I. Introduction

In industry applications, electrical drive systems with a power level of $5\,\mathrm{kW}$ to $10\,\mathrm{kW}$ are often supplied from the single-phase mains in order to keep the grid interface as simple as possible. This involves e.g. drive systems for fans, blowers, pumps and local automation systems. Furthermore, since in industrial three-phase networks a connection to the neutral conductor N is commonly not available, the single-phase front-end of the electrical drive system has to be connected between two phases [1], [2]. This means that the line-to-line voltage of the three-phase mains is applied to the front-end and thus a relatively wide input voltage range with voltages up to $400\,\mathrm{V_{rms}}$ or $480\,\mathrm{V_{rms}}$ has to be covered. Furthermore, the single-phase front-end has to provide active power factor correction, i.e. a sinusoidal input current in phase with the input voltage, to keep the harmonic distortion and reactive power in the grid at a minimum. Finally, in order to cover a wide area of applications, compatibility to three-phase machines with different rated voltages has to be ensured.

All these requirements e.g. can be fulfilled with a buck-boost PFC rectifier [3]–[5] followed by a voltage source PWM inverter (VSI) [6]. Due to the buck-boost functionality of the PFC rectifier [7], [8], the intermediate DC link voltage can be selected independent from the mains input voltage, which advantageously allows to flexibly adapt the DC link voltage to the required (rated) machine voltage. In contrast, for a conventional boost PFC rectifier, the DC link voltage level would be limited to voltages above the peak value of the mains voltage. For applications with low nominal machine voltages this would mean that the inverter stage would have to be operated with a low modulation index and consequently would have to be designed for high peak currents (and voltages) in order to provide the required machine power. However, the mentioned two-stage system, comprising a two-switch buck-boost PFC rectifier and a three-phase VSI, comes with a relatively high realization effort and therefore the question of a topological simplification, for example by integration of the boost function into the inverter stage by means of a Z-source inverter [9]–[12], arises.

The basic Z-source inverter topology only employs an impedance-source (Z-source) network followed by a three-phase inverter (cf. **Fig. 1**) [13], where the boost operation is realized with a short-circuit interval of one inverter bridge leg, the so-called shoot-through interval, which enables an intermediate voltage $\bar{v}_{\mathrm{PN}} = v_{\mathrm{C}}$ that is higher than the input voltage v_{AB}. As a result, the Z-source inverter also features an enhanced robustness and reliability compared to the VSI, where a short-circuit of one inverter bridge leg could lead to the destruction of the converter system. Hence, due to this integrated boost functionality, the Z-source inverter constitutes an interesting alternative for applications with a wide input voltage range, e.g. for fuel or solar cell applications [9], [14]. However, in order to prevent a current flowing back to the DC-voltage source v_{DC}, a series diode $\mathrm{D_Z}$ is required at the input as shown in **Fig. 1(a)**. Advantageously, this series diode can be replaced by a diode rectifier $\mathrm{D_1} - \mathrm{D_4}$, since due to the wide input voltage range capability, the Z-source inverter can be directly connected to the single-phase mains and be operated as a single-stage single-to-three phase AC/AC converter (cf. **Fig. 1(b)**) [15], [16]. Unfortunately, with this high level of integration also certain degrees of freedom concerning controllability are lost, which means that e.g. in the vicinity of the input voltage zero crossings the grid current i_{G} can no longer be controlled to be sinusoidal, since the Z-source inverter draws at least a minimal input current $\bar{i}_{\mathrm{A,min}}$, as will be shown later. A further limitation of the system is that due to the inherent boost functionality, the intermediate voltage $\bar{v}_{\mathrm{PN}}$ has to be larger than the peak value of the input voltage v_{G}, which results in a high voltage stress on the semiconductor devices and the passive components.

These drawbacks can be resolved by adding a half-bridge directly behind the bridge rectifier, which in combination with the already existing Z-source network features a simple buck-stage (cf. **Fig. 1(c)**). Consequently, with the proposed *single-to-three-phase Z-source Buck+Boost Converter* (*123ZBBC*, cf. **Fig. 6**), on the one hand the input voltage v_{G} can be stepped down, which enables to reduce the intermediate voltage $\bar{v}_{\mathrm{PN}}$ below the peak input voltage and therefore also reduces the voltage stress on the Z-source network and the semiconductor devices of the inverter stage. On the other hand, the input current i_{G} can be controlled to be sinusoidal within the entire mains period, even though the Z-source input current shows a value equal or higher than $\bar{i}_{\mathrm{A,min}}$. Hence, since the *123ZBBC* features the same functionality as the conventional buck-boost PFC rectifier with a subsequent VSI, and due to the high

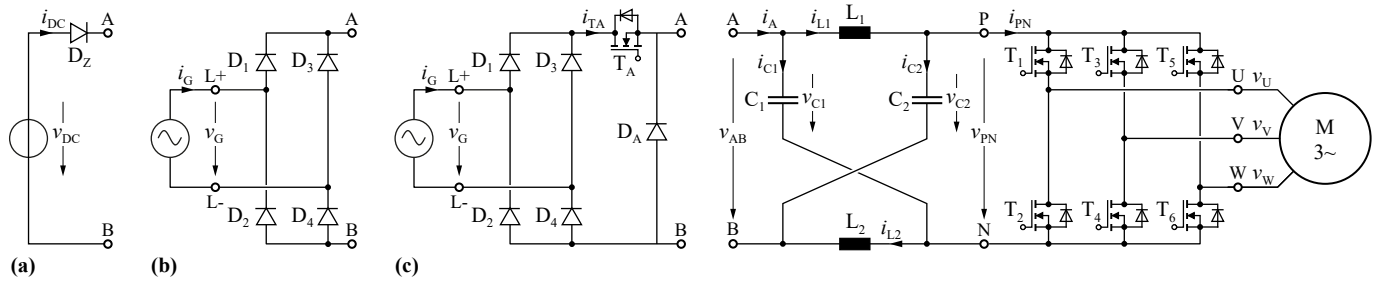

Fig. 1. Basic Z-source inverter topology consisting of an impedance-source network (Z-source) and a conventional three-phase inverter stage, which features an inherent boost functionality and can be directly supplied from **(a)** a wide range DC-voltage source v_{DC}, e.g. fuel cell or solar cell, via a series diode $\mathrm{D_Z}$ [13], **(b)** a single-phase supply connected to a diode bridge rectifier, or **(c)**, as proposed in this paper, a single-phase supply followed by a bridge rectifier and a half-bridge.

level of integration also a high power density is expected. In this paper the operation principle, the control as well as the modulation scheme of the *123ZBBC* is analyzed in detail. In **Section II**, the different conduction states and the most suitable PFC modulation strategy are presented. Afterwards in **Section III**, the corresponding control structure for the intermediate voltage $\overline{v}_{\mathrm{PN}}$, the sinusoidal input current i_{G} and the machine speed is derived, which is then verified by means of a circuit simulation. Furthermore, due to the fact that the instantaneous intermediate voltage v_{PN} changes depending on the conduction state, special attention has to be paid on the modulation scheme of the inverter, particularly on the distribution of the shoot-through interval within one switching period. An analysis of the stresses on the main components and a comparison to the conventional Z-source based single-to-three phase topology is performed in **Section IV**. Finally, **Section V** summarizes the findings of the work and gives an outlook to future research.

II. Conduction States and PFC Modulation Strategy

Similar to conventional buck-boost PFC rectifiers, the proposed *123ZBBC* is operated in a buck (BU) mode when the grid voltage v_{G} is higher than the intermediate voltage $\overline{v}_{\mathrm{PN}}$, and in a boost (BO) mode when v_{G} is lower than $\overline{v}_{\mathrm{PN}}$. As will be shown later, however, in the vicinity of the zero-crossing of the input voltage,

$$v_{\mathrm{G}} = \hat{V}_{\mathrm{G}} \cdot \cos \omega_{\mathrm{G}} t, \tag{1}$$

the converter has to be operated in a buck-boost (BB) mode in order to be able to draw a sinusoidal current

$$i_{\mathrm{G}} = G_{\mathrm{C}} \cdot v_{\mathrm{G}} = \frac{2P_{\mathrm{M}}}{\hat{V}_{\mathrm{G}}^2} \cdot v_{\mathrm{G}} \tag{2}$$

within the entire mains period from the grid.

Hence, the buck and the integrated boost stage are controlled by means of the buck duty cycle d_{A}, which defines the effective on-time of the buck transistor $\mathrm{T_A}$, i.e. the time when $\mathrm{T_A}$ is turned on *and* one of the upper/lower diodes of the input diode bridge is conducting, and the boost duty cycle d_{B}, which corresponds to the Z-source specific relative shoot-through time of one of the inverter bridge legs [13]. Consequently, for the inverter stage this means that during a shoot-through interval no voltage is applied to the machine terminals, thus the formation of the three output voltages v_{U}, v_{V}, and v_{W} has to occur during the remaining non shoot-through interval, whose duration depends on the mentioned duty cycles d_{A} and d_{B} of the PFC rectifier. Due to the dependency of the inverter's modulation scheme on the rectifier's duty cycles d_{A} and d_{B}, the control strategy to achieve a sinusoidal input current is examined first. For this purpose, the proposed circuit topology is simplified and the conduction states of the resulting circuit are analyzed. Afterwards, the modulation strategy to achieve the desired PFC functionality is derived.

A. Derivation of the Equivalent Circuit

The traditional Z-source inverter [13] consists of a symmetrical impedance network with $C = C_1 = C_2$ and $L = L_1 = L_2$, which also implies symmetric operation conditions: $v_{\mathrm{C}} = v_{\mathrm{C1}} = v_{\mathrm{C2}}$, $i_{\mathrm{C}} = i_{\mathrm{C1}} = i_{\mathrm{C2}}$, $i_{\mathrm{L}} = i_{\mathrm{L1}} = i_{\mathrm{L2}}$ and $v_{\mathrm{L}} = v_{\mathrm{L1}} = v_{\mathrm{L2}}$.

In order to simplify the analysis of the basic converter operation, the grid voltage, the EMI-filter and the bridge rectifier of the actual converter topology (cf. Fig. 6) are replaced by a voltage source $v_{\mathrm{Q}} = |v_{\mathrm{G}}|$ and a series diode $\mathrm{D_R}$, which models the unidirectional power flow (cf. **Fig. 2(a)**). Furthermore, the three-phase inverter and the machine are substituted by a shoot-through/boost transistor $\mathrm{T_B}$ in parallel to a current source

$$i_{\mathrm{Q}} = \frac{1}{2}\left[i_{\mathrm{U}}\left(\mathrm{S_1} - \mathrm{S_2}\right) + i_{\mathrm{V}}\left(\mathrm{S_3} - \mathrm{S_4}\right) + i_{\mathrm{W}}\left(\mathrm{S_5} - \mathrm{S_6}\right)\right], \tag{3}$$

where $S_{\mathrm{i}} \in [0, 1]$ is the switching state of the transistor $\mathrm{T_i}$. The resulting equivalent circuit, which models the behaviour of the Z-source based buck-boost rectifier stage, is presented in **Fig. 2**.

B. Conduction States

The two transistors $\mathrm{T_A}$ and $\mathrm{T_B}$ are operated with the switching frequency $f_{\mathrm{SW}} = \frac{1}{T_{\mathrm{SW}}}$, thus four different switching or conduction states would be found. However, as will shown in the following, when $\mathrm{T_B}$ is turned on, $\mathrm{T_A}$ can be either turned on or turned off without any effect on the current paths; hence, only three states exist. For the analysis of these states, the energy related quantities v_{C} and i_{L} are assumed to be impressed, i.e constant.

State 1 (Active State): The first conduction state with the duration $t_{\mathrm{A}} = d_{\mathrm{A}} T_{\mathrm{SW}}$ equals the active state (energy is directly transferred from the input to the output) and is defined by $S_{\mathrm{A}} = 1$ and $S_{\mathrm{B}} = 0$, which means that $\mathrm{T_A}$ is turned on and $\mathrm{T_B}$ is turned off (cf. **Fig. 2(a)**). It should be mentioned again that t_{A} corresponds to the *effective* on-time of $\mathrm{T_A}$ meaning that $\mathrm{T_A}$ is not only turned on, but also conducts a current, which e.g. is not the case in state 3 even if $\mathrm{T_A}$ is in the on-state. Hence, in state 1 a positive buck-stage input current $i_{\mathrm{TA,1}}$ ($i_{\mathrm{TA,1}} > 0\,\mathrm{A}$) must be assumed, such that the diode $\mathrm{D_R}$ and the buck switch $\mathrm{T_A}$ are conducting. Consequently, a positive input voltage v_{Q} is applied to the buck diode $\mathrm{D_A}$,

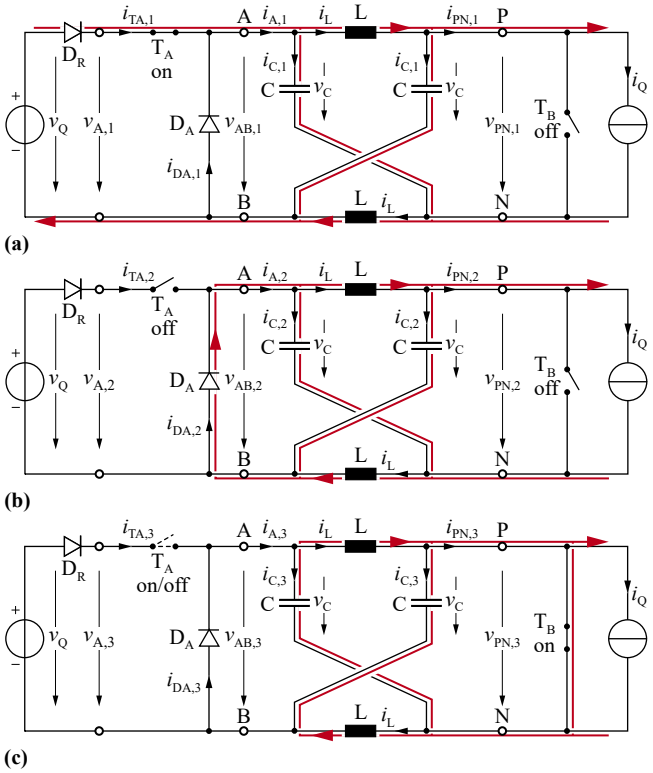

Fig. 2. Equivalent circuit of the proposed Z-source-based buck-boost AC/AC converter, where a symmetric impedance network is assumed. The grid voltage and the bridge rectifier are replaced by a voltage source v_Q and a series diode $\mathrm{D_R}$. The inverter and the machine are substituted by a parallel connection of a shoot-through/boost transistor $\mathrm{T_B}$ and a current source i_Q. In **(a)-(c)** the three conduction states and the corresponding current paths are shown.

which means that this diode has to block and the current $i_{\mathrm{TA},1}$ is defined by the two impedance network currents i_L and $i_{\mathrm{C},1}$ ($i_{\mathrm{TA},1} = i_{\mathrm{A},1} = i_\mathrm{L} + i_{\mathrm{C},1}$), which in turn are determined by the current source i_Q ($i_\mathrm{Q} = i_\mathrm{L} - i_{\mathrm{C},1}$). Based on these two equations it can be found that the inductor current i_L must always be larger than half of the peak inverter output current $\hat{I}_\mathrm{Q}$, which actually equals the peak phase current of the machine $\hat{I}_\mathrm{M}$ ($= \hat{I}_\mathrm{U} = \hat{I}_\mathrm{V} = \hat{I}_\mathrm{W}$), in order to keep the current through $\mathrm{D_R}$ and $\mathrm{T_A}$ positive, i.e. $i_{\mathrm{TA},1} > 0\,\mathrm{A}$,

$$i_\mathrm{L} \geq i_{\mathrm{L,min}} = \frac{1}{2} \cdot \hat{I}_\mathrm{M}. \tag{4}$$

The instantaneous value of the intermediate voltage, i.e. the inverter input voltage $v_{\mathrm{PN},1}$, can be calculated based on the two voltage equations $|v_\mathrm{G}| = v_\mathrm{C} + v_{\mathrm{L},1}$ and $v_{\mathrm{PN},1} = v_\mathrm{C} - v_{\mathrm{L},1}$, which results in $v_{\mathrm{PN},1} = 2v_\mathrm{C} - |v_\mathrm{G}|$. Furthermore, the voltage applied to the inductor can be found as $v_{\mathrm{L},1} = |v_\mathrm{G}| - v_\mathrm{C}$. Consequently, since due to the antiparallel body diodes of the inverter stage switches the voltage $v_{\mathrm{PN},1}$ cannot fall below zero ($v_{\mathrm{PN},1} > 0\,\mathrm{V}$), it reveals that even in buck operation the capacitor voltage v_C cannot be reduced below half of the peak input voltage $\hat{V}_\mathrm{G}$,

$$v_\mathrm{C} \geq v_{\mathrm{C,min}} = \frac{1}{2} \cdot \hat{V}_\mathrm{G}. \tag{5}$$

State 2 (Buck State): In the second state with duration $t_0 = d_0 T_\mathrm{SW}$, which is only used during buck operation, $\mathrm{T_A}$ is turned off ($S_\mathrm{A} = 0$, $S_\mathrm{B} = 0$ and $i_{\mathrm{TA},2} = 0\,\mathrm{A}$) and the current commutates from switch $\mathrm{T_A}$ to the diode $\mathrm{D_A}$ (cf. **Fig. 2(b)**). Consequently, since the remaining current paths do not change (impressed by the inductor current and the load current), the diode current $i_{\mathrm{DA},2}$ can be expressed by the same equations as used in state 1, i.e. $i_{\mathrm{DA},2} = i_{\mathrm{A},2} = i_\mathrm{L} + i_{\mathrm{C},2}$ and $i_\mathrm{Q} = i_\mathrm{L} - i_{\mathrm{C},2}$. In order to keep $\mathrm{D_A}$ conducting, i.e. $i_{\mathrm{DA},2} > 0\,\mathrm{A}$, the same condition (4) as for state 1 is found. Furthermore, also the intermediate voltage can be derived by the same equations, however, due to the conducting diode $\mathrm{D_A}$, the voltage equation simplifies to $v_{\mathrm{PN},2} = 2v_\mathrm{C}$. As can be noticed, the voltage stress on the semiconductors is twice the capacitor voltage v_C and therefore a reduction of v_C by an additional buck-stage is encouraged. In addition, the inductor voltage changes to $v_{\mathrm{L},2} = -v_\mathrm{C}$, which means that the full capacitor voltage is applied in negative direction to the inductor.

State 3 (Boost State): The third state is defined by $S_\mathrm{B} = 1$, which means that the shoot-through transistor $\mathrm{T_B}$ is closed during the interval $t_\mathrm{B} = d_\mathrm{B} T_\mathrm{SW}$ and the converter is operated in the boost mode (cf. **Fig. 2(c)**). Consequently, due to the shoot-through, the inverter input voltage is zero ($v_{\mathrm{PN},3} = 0\,\mathrm{V}$) and no voltage is applied to the machine terminals. Furthermore, the full capacitor voltage v_C is applied to each inductor L in positive direction, i.e. $v_{\mathrm{L},3} = v_\mathrm{C}$. Based on the already described voltage equation it reveals that the sum of both capacitor voltages is applied to the diode $\mathrm{D_A}$ ($v_{\mathrm{DA},3} = v_{\mathrm{AB},3} = 2v_\mathrm{C}$), hence $\mathrm{D_A}$ has to block. On the other hand, the diode $\mathrm{D_R}$ blocks the voltage $2v_\mathrm{C} - |v_\mathrm{G}|$ as long as (5) is fulfilled, hence $\mathrm{T_A}$ can be either turned on or off without any effect, and the only remaining current path is given through the Z-source network.

For the different operation modes either all or only a subset of the described conduction states are used during one switching cycle T_SW. For example, the buck (BU) operation only utilizes the states 1 and 2, which leads to the relative durations $d_\mathrm{A} + d_0 = 1$ ($d_\mathrm{B} = 0$), while the boost (BO) operation uses the states 1 and 3, which equals $d_\mathrm{A} + d_\mathrm{B} = 1$ ($d_0 = 0$). Consequently, all three states are only required during buck-boost (BB) operation, i.e. $d_\mathrm{A} + d_0 + d_\mathrm{B} = 1$. It has to be noted again that the instantaneous inverter voltage $\bar{v}_\mathrm{PN}$ changes depending on the actual conduction state (cf. **Fig. 3**), which has to be considered later for the duty cycle calculation of the inverter switches. However, for the duty cycle calculation of the rectifier the averaged values are needed first.

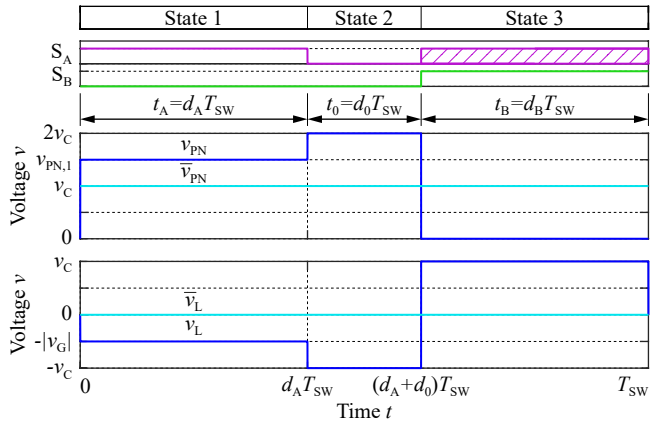

Fig. 3. PFC rectifier switching signals S_A and S_B, the corresponding conduction state, the time-dependent intermediate voltage v_PN, the inductor voltage v_L, and the switching frequency averaged quantities $\bar{v}_\mathrm{PN}$ and $\bar{v}_\mathrm{L}$ are shown over one switching period T_SW.

Based on a steady state analysis over one switching period T_SW, the averaged intermediate voltage $\bar{v}_\mathrm{PN}$ is calculated as $\bar{v}_\mathrm{PN} = d_\mathrm{A} v_{\mathrm{PN},1} + d_0 v_{\mathrm{PN},2} + d_\mathrm{B} v_{\mathrm{PN},3}$, whereby the interval

d_0 is replaced by $d_0 = 1 - d_\mathrm{A} - d_\mathrm{B}$. Similarly, the averaged inductor voltage $\bar{v}_\mathrm{L}$ and the averaged input current $\bar{i}_\mathrm{TA}$ are derived, which together with the equivalent load current $\bar{i}_\mathrm{Q}$ results in

$$\bar{v}_\mathrm{PN} = 2v_\mathrm{C} \cdot (1 - d_\mathrm{B}) - |v_\mathrm{G}| \cdot d_\mathrm{A}, \tag{6}$$

$$\bar{v}_\mathrm{L} = |v_\mathrm{G}| \cdot d_\mathrm{A} - v_\mathrm{C} \cdot (1 - 2 \cdot d_\mathrm{B}), \tag{7}$$

$$\bar{i}_\mathrm{Q} = \frac{P_\mathrm{M}}{\bar{v}_\mathrm{PN}}, \tag{8}$$

$$\bar{i}_\mathrm{TA} = |i_\mathrm{G}| = (2 \cdot i_\mathrm{L} - \bar{i}_\mathrm{Q}) \cdot d_\mathrm{A}. \tag{9}$$

C. PFC Modulation Strategy

In the following, each duty cycle d_x ($x \in \{A, B\}$) is split into a steady state duty cycle D_x and a duty cycle variation $\tilde{d}_\mathrm{x}$ provided from the circuit controller

$$d_\mathrm{A} = D_\mathrm{A} + \tilde{d}_\mathrm{A}, \tag{10}$$

$$d_\mathrm{B} = D_\mathrm{B} + \tilde{d}_\mathrm{B}. \tag{11}$$

This allows to first determine the needed duty cycles D_A and D_B from (6)-(9) in steady state, which means that the averaged inductor voltage is zero ($\bar{v}_\mathrm{L} = 0\,\mathrm{V}$) and in turn also the duty cycles $\tilde{d}_\mathrm{A}$ and $\tilde{d}_\mathrm{B}$ derived from the controller are zero. Consequently, the right side of (7) can be set to zero, resulting in the average capacitor voltage

$$V_\mathrm{C} = \bar{v}_\mathrm{PN} = |v_\mathrm{G}| \cdot \frac{D_\mathrm{A}}{1 - 2 \cdot D_\mathrm{B}} \geq \frac{1}{2} \cdot \hat{V}_\mathrm{G}, \tag{12}$$

which based on (5) has to be larger than half the peak input voltage $\hat{V}_\mathrm{G}$. Furthermore, applying (12) in (6) reveals that v_C has to equal the averaged inverter voltage $\bar{v}_\mathrm{PN}$ and due to a large capacitance C can be assumed to be nearly constant. From (12), the modulation index m is calculated as the ratio of the grid voltage $|v_\mathrm{G}|$ and the intermediate voltage $\bar{v}_\mathrm{PN}$,

$$m = \frac{|v_\mathrm{G}|}{\bar{v}_\mathrm{PN}} = \frac{1 - 2 \cdot D_\mathrm{B}}{D_\mathrm{A}} \in [0, 2]. \tag{13}$$

As can be noticed, due to the absolute value of v_G, m is limited to positive values and due to (5), m is restricted to values equal or below 2. Furthermore, a modulation index $m \in [0, 1]$ means boost (BO) operation and for $m \in [1, 2]$ the system is operated in buck (BU) mode (cf. **Fig. 4**). As already mentioned, in buck operation $D_\mathrm{B,BU}$ is zero, which means that $D_\mathrm{A,BU} = 1/m$ for $m \in [1, 2]$ (cf. **Fig. 4**). On the other hand, in boost-operation it follows that $D_\mathrm{B,BO} = 1 - D_\mathrm{A,BO}$ and thus from (13) it is found that $D_\mathrm{A,BO} = 1/(2 - m)$ for $m =\in [0, 1]$. Consequently, as can be noticed from **Fig. 4**, the steady state duty cycle $D_\mathrm{A,BU/BO}$ valid for boost and buck operation is always found by taking the minimum of the two mentioned duty cycles $D_\mathrm{A,BU}$ and $D_\mathrm{A,BO}$, which is

$$D_\mathrm{A,BU/BO} = \min\left(\frac{1}{m}, \frac{1}{2 - m}\right). \tag{14}$$

With this modulation strategy, the switching losses and the inductor current i_L can be kept minimal, thus typically the highest converter efficiency can be achieved. However, in order to guarantee proper converter operation, based on (4) the inductor current i_L has to be larger than a certain minimum value $i_\mathrm{L,min}$, which with pure buck or boost operation is always undercut around the input voltage zero crossings. Fortunately, from (13) it can be noted that a certain modulation index m also can be achieved with other sets of duty cycles

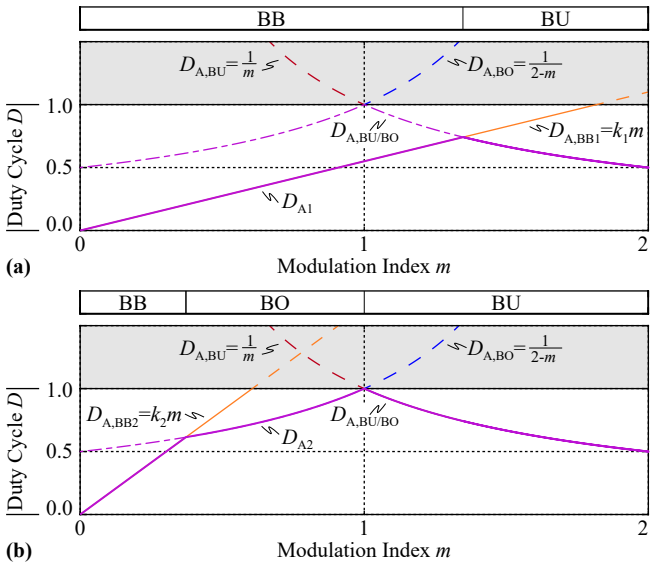

Fig. 4. The optimal steady state buck duty cycle D_A is given with the minimum of $D_\mathrm{A,BU/BO}$ and $D_\mathrm{A,BB}$. Thereby, $D_\mathrm{A,BB}$ is proportional to the modulation index m by the factor k and ensures an inductor current i_L above the minimum value $i_\mathrm{L,min}$. The steady state duty cycle $D_\mathrm{A,BU/BO}$ is valid for boost and buck operation and results from the minimum of the buck $D_\mathrm{A,BU}$ and the boost $D_\mathrm{A,BO}$ operation related buck duty cycle. The employed operation modes depend on the factor k, **(a)** in case $k = k_1 < 1$ only the buck-boost (BB) and the buck (BU) operation are present, while **(b)** in case $k = k_2 > 1$ all three operation modes BB, BO and BU occur.

D_A and D_B, i.e. when the system is operated in buck-boost (BB) mode. Even though this operation is not preferred, with the adaptation of the duty cycles D_A and D_B the inductor current i_L can be kept above $i_\mathrm{L,min}$. Hence, the maximum allowed duty cycle $D_\mathrm{A,BB}$ can be derived from (9), while for i_L the relation given in (4) is used,

$$D_\mathrm{A,BB} = \frac{|i_\mathrm{G}|}{\hat{I}_\mathrm{M} - \bar{i}_\mathrm{Q}}. \tag{15}$$

In order to obtain for $D_\mathrm{A,BB}$ a dependency on m, the currents $|i_\mathrm{G}|$ and $\bar{i}_\mathrm{Q}$ are substituted considering (2) and (3), respectively. The machine current $\hat{I}_\mathrm{M}$ can be expressed by the machine power $P_\mathrm{M} = 3/2\hat{V}_\mathrm{M}\hat{I}_\mathrm{M}\cos(\varphi)$ and the modulation index of the inverter stage $M = 2\hat{V}_\mathrm{M}/V_\mathrm{C}$, which after some rearrangements results in

$$D_\mathrm{A,BB} = \frac{6M\cos\varphi}{4 - 3M\cos\varphi}\left(\frac{V_\mathrm{C}}{\hat{V}_\mathrm{G}}\right)^2 \cdot m = k \cdot m, \tag{16}$$

where $M < M_\mathrm{max} = \frac{2}{\sqrt{3}}$ and $\cos\varphi \leq 1$. Consequently, the optimal and also maximum allowed duty cycle D_A is found by selecting the minimum value out of $D_\mathrm{A,BU/BO}$ and $D_\mathrm{A,BB}$, which is

$$D_\mathrm{A} = \min\left(D_\mathrm{A,BU/BO}, D_\mathrm{A,BB}\right). \tag{17}$$

The corresponding D_B is found by solving (13) to

$$D_\mathrm{B} = \frac{1}{2}\left(1 - m \cdot D_\mathrm{A}\right). \tag{18}$$

In **Fig. 4**, $D_\mathrm{A,BB}$ is shown for two different load conditions. As can be noticed, depending on the slope of $D_\mathrm{A,BB}$, within one mains half cycle - where m changes sinusoidally from zero to a certain maximum - either the buck (BU) operation directly follows after the buck-boost (BB) operation (cf. **Fig. 4(a)**) or all three operation modes (BB,BO,BU) are present (cf. **Fig. 4(b)**). The resulting PFC rectifier waveforms for the latter case are shown in **Fig. 5** over one grid period T_G.

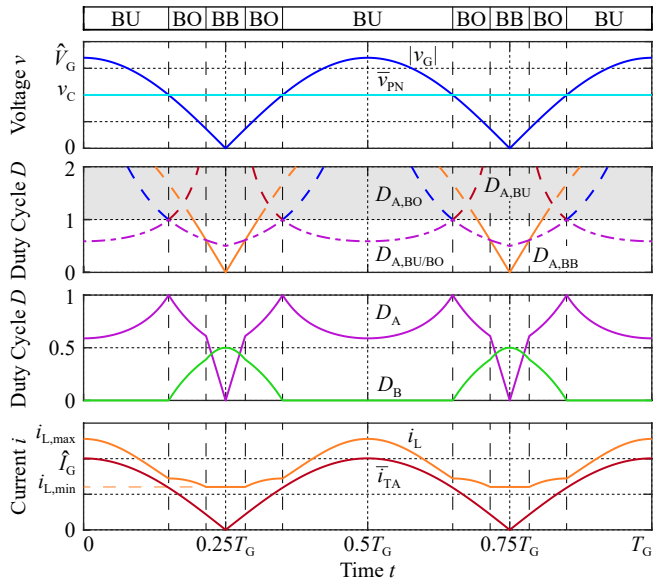

Fig. 5. Calculated waveforms for the inductor current minimal PFC modulation strategy showing the operation modes, the rectified grid voltage $|v_\mathrm{G}|$ and intermediate voltage $\bar{v}_\mathrm{PN}$, the steady state buck duty cycles $D_\mathrm{A,BU}$, $D_\mathrm{A,BO}$, $D_\mathrm{A,BU/BO}$ and $D_\mathrm{A,BB}$, the optimal steady state duty cycles D_A and D_B, the rectified grid current $\bar{i}_\mathrm{TA}$ and the inductor current i_L over one grid period T_G for $\bar{v}_\mathrm{L} = 0\,\mathrm{V}$ and a constant capacitor voltage v_C.

III. Control Structure

The described PFC modulation strategy already allows to operate the PFC rectifier in an open loop fashion. However, due to disturbances, nonlinearities or simplified models, typically the capacitor voltage and the input current deviate from their reference values. Therefore, a cascaded *PFC rectifier control* consisting of an inner *input/inductor current control* loop and an outer *capacitor voltage control* loop is needed, that provides the two controller duty cycles $\tilde{d}_\mathrm{A}$ and $\tilde{d}_\mathrm{B}$ as outputs, which are afterwards added to the steady state duty cycles D_A and D_B (cf. Section II-C) in order to achieve a sinusoidal input current and a controlled capacitor voltage (cf. **Fig. 6**). In addition, for the inverter stage an *inverter/machine control* [17] is used, which has to generate the duty cycles d_U, d_V and d_W of the inverter in such a way that the machine speed reference ω^* can be properly tracked. However, the calculated duty cycles of both stages cannot directly be assigned to a certain switch T_A or $T_1 - T_6$, which means that the corresponding switching signals S_A and $S_1 - S_6$ first have to be derived in the *switching signal generation* block depending on the output voltage sector, as will be shown in the following.

A. PFC Rectifier Control

The outer *capacitor voltage control* has to regulate the measured and averaged capacitor voltage $\bar{v}_\mathrm{C}$ according the reference $\bar{v}_\mathrm{C}^* = V_\mathrm{PN}^*$. Hence, dependent on the voltage error $\Delta\bar{v}_\mathrm{C}$, the voltage controller $\mathrm{R_V}$ determines the needed capacitor current $\bar{i}_\mathrm{C}^*$ - and with the reference capacitor voltage $\bar{v}_\mathrm{C}^*$ the needed average capacitor power $\bar{p}_\mathrm{C}^*$ - to keep the capacitor voltage at its nominal value.

Based on $\bar{p}_\mathrm{C}^*$, now the input current reference i_G^* for the *input/inductor current control* can be calculated in order to provide the needed power to the capacitor. However, the PFC rectifier not only has to cover the power $\bar{p}_\mathrm{C}^*$, but has to provide in addition the load power to the machine. Therefore, $\bar{p}_\mathrm{M}$ derived from the *inverter/machine control* is added to $\bar{p}_\mathrm{C}^*$.

With (9), the inner *input/inductor current control* now translates i_G^* into the inductor current reference i_L^*, which together with the measured inductor current i_L is then processed by the current controller $\mathrm{R_I}$. The current controller, implemented as multiple parallel PR-controllers [18], finally provides the reference inductor voltage $\tilde{v}_\mathrm{L}$ to adjust the current i_L to the desired value. The inductor voltage variation $\tilde{v}_\mathrm{L}$ can be achieved by either a duty cycle variation $\tilde{d}_\mathrm{A}$ or a duty cycle variation $\tilde{d}_\mathrm{B}$, (cf. (7)),

$$\tilde{v}_\mathrm{L} = |v_\mathrm{G}| \cdot \tilde{d}_\mathrm{A} + 2v_\mathrm{C} \cdot \tilde{d}_\mathrm{B}. \tag{19}$$

This advantage can be optimally exploited for the different operating mode. For example, in buck (BU) operation, the shoot-through duty cycle d_B is zero ($d_\mathrm{B} = 0$), hence also $\tilde{d}_\mathrm{B} = 0$. In boost (BO) operation $d_0 = 0$, which means that $d_\mathrm{A} + d_\mathrm{B} = 1$ and therefore $\tilde{d}_\mathrm{A} = -\tilde{d}_\mathrm{B}$ is found. In the remaining buck-boost (BB) operation, where the duty cycle d_A is defined by the minimum inductor current $i_\mathrm{L,min}$, it is clear that an increase of this duty cycle by $\tilde{d}_\mathrm{A}$ is not allowed, and consequently only $\tilde{d}_\mathrm{B}$ can be changed, while $\tilde{d}_\mathrm{A} = 0$

$$\tilde{d}_\mathrm{A}, \tilde{d}_\mathrm{B} = \begin{cases} \frac{\tilde{v}_\mathrm{L}}{|v_\mathrm{G}|}, & 0 \quad \text{if BU} \\ \frac{\tilde{v}_\mathrm{L}}{|v_\mathrm{G}| - 2v_\mathrm{C}}, & -\tilde{d}_\mathrm{A} \quad \text{if BO} \\ 0, & \frac{\tilde{v}_\mathrm{L}}{2v_\mathrm{C}} \quad \text{if BB} \end{cases}. \tag{20}$$

B. Machine Control

The *inverter/machine control* has to regulate the rotational speed ω with respect to its reference value ω^*, which can be implemented with a conventional inverter control for variable speed drives [17]. There, the inverter duty cycles d_U, d_V and d_W are derived based on the speed error $\Delta\omega$, the rotor position ε, the capacitor voltage v_C, and the phase currents i_U, i_V and i_W. Furthermore, as already mentioned, the averaged machine power $\bar{p}_\mathrm{M}$ and the phase peak current $\hat{I}_\mathrm{M}$ are used by the PFC rectifier control as a feedforward and on the other hand are used to calculate $D_\mathrm{A,BB}$ based on (15). Alternatively, this calculation would also be possible with (16), where the modulation index of the inverter M and the power factor $\cos(\varphi)$ would have to be known.

C. Switching Signal Generation

The switching signal generation block has to translate the PFC rectifier duty cycles d_A and d_B as well as the inverter duty cycles d_U, d_V and d_W to the actual transistor switching signals S_A and $S_1 - S_6$, since these duty cycles cannot directly be assigned to a certain switch. Therefore, first the transistor duty cycles $d_1 - d_6$ of the switches $S_1 - S_6$ are derived, and then the corresponding switching patterns for the different operation modes are discussed.

Starting from a conventional VSI with constant DC-link voltage v_DC, the switching signals and the corresponding phase voltage waveform within one switching period T_SW can be easily derived by comparing the symmetrical triangular carrier with the inverter duty cycles d_U, d_V and d_W, i.e. conventional PWM as shown in **Fig. 7** for the phase voltage v_UN between phase output U and the negative DC-rail N. There, the phase voltage is equal to the DC-link voltage in case the carrier signal is smaller than the duty cycle d_U, and within the remaining interval the phase voltage is zero, which means that the duty cycle d_U actually defines the average phase voltage $\bar{v}_\mathrm{UN} = v_\mathrm{DC} \cdot d_\mathrm{U}$ which is applied to the machine over one switching period.

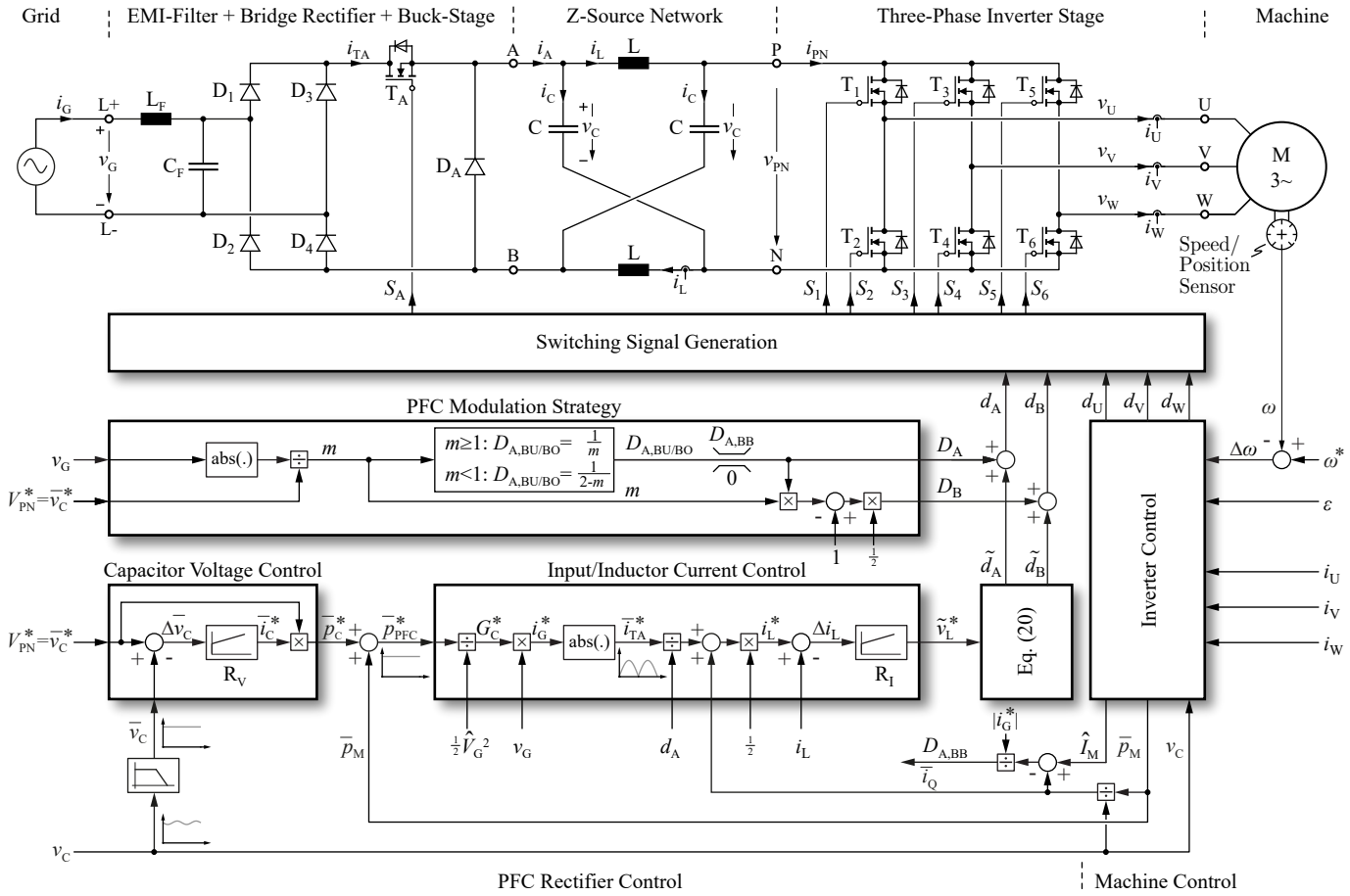

Fig. 6. Proposed Z-source-based buck-boost AC/AC converter: The corresponding control structure consists of a *PFC rectifier control*, which derives the buck duty cycle d_A and the shoot-through duty cycle d_B, and a conventional *machine control*, which provides the inverter duty cycles d_U, d_V and d_W. The *switching signal generation* block generates the transistor switching signals $S_1 - S_6$, based on the already determined PFC rectifier and the inverter duty cycles.

Hence, the same averaged output voltage $\bar{v}_\mathrm{UN}$ should also result from the duty cycles d_U, d_V and d_W calculated by the *inverter control* block of the *123ZBBC*. However, there the instantaneous intermediate voltage v_PN, i.e. the input voltage of the inverter stage, changes depending on the present conduction state of the PFC rectifier (cf. Section II). In case of a shoot-through state, for example, v_PN is zero and therefore, the needed averaged output voltage $\bar{v}_\mathrm{UN}$ can only be formed during the active state ($v_\mathrm{PN,1} = 2v_\mathrm{C} - |v_\mathrm{G}|$) and the buck state ($v_\mathrm{PN,2} = 2v_\mathrm{C}$). One possibility is to modify the PWM carrier signal to an asymmetrical triangular carrier, which rises within the active state $t_\mathrm{A} = d_\mathrm{A} T_\mathrm{SW}$ from zero to one, falls again during the buck state $t_0 = d_0 T_\mathrm{SW}$ down to zero and stays at zero within the remaining shoot-through interval $t_\mathrm{B} = d_\mathrm{B} T_\mathrm{SW}$ (cf. **Fig. 7**). With this assumption, on the one hand the zero voltage interval, which in addition to the shoot-through interval is needed to generate the correct averaged phase voltage v_PN, is proportionally distributed between the active state interval $d_\mathrm{A} T_\mathrm{SW}$ and the buck stage interval $d_0 T_\mathrm{SW}$, and on the other hand it is beneficially achieved that the same duty cycles d_U, d_V and d_W as for the conventional VSI can be used. With $t_\mathrm{U,A} = d_\mathrm{U} \cdot t_\mathrm{A} = d_\mathrm{U} \cdot d_\mathrm{A} \cdot T_\mathrm{SW}$, $t_\mathrm{U,B} = d_\mathrm{U} \cdot t_0 = d_\mathrm{U} \cdot d_0 \cdot T_\mathrm{SW}$ and (6), the correct calculation of the averaged phase voltage $\bar{v}_\mathrm{UN}$ can be verified,

$$\begin{aligned}\bar{v}_\mathrm{UN} &= v_\mathrm{PN,1} \cdot \frac{t_\mathrm{U,A}}{T_\mathrm{SW}} + v_\mathrm{PN,2} \cdot \frac{t_\mathrm{U,0}}{T_\mathrm{SW}} \\ &= (2v_\mathrm{C} - |v_\mathrm{G}|) \cdot d_\mathrm{A} d_\mathrm{U} + 2v_\mathrm{C} \cdot d_0 d_\mathrm{U} = \bar{v}_\mathrm{PN} \cdot d_\mathrm{U}. \quad (21)\end{aligned}$$

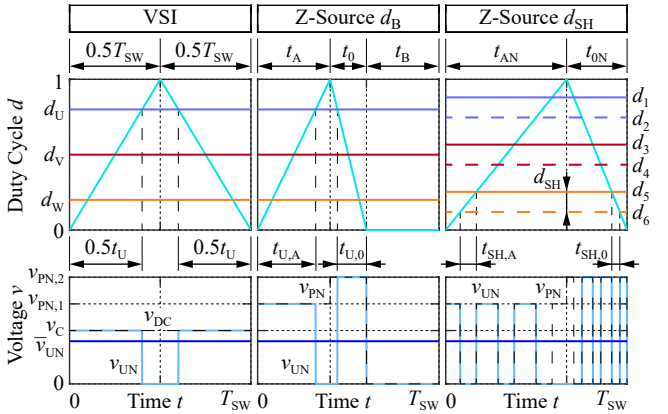

Fig. 7. PWM modulation scheme and the resulting phase voltage v_UN for a conventional three-phase VSI, the proposed converter structure with a single shoot-through interval t_B and with the distributed shoot-through intervals $t_\mathrm{SH,A}$ and $t_\mathrm{SH,0}$.

In order to reduce the current ripple in the Z-source inductance L, another possibility is to distribute and integrate the shoot-through interval $d_\mathrm{B} T_\mathrm{SW}$ into the inverter switching transitions as also proposed in [13]. In contrast to the conventional switching procedure, where first one switch of a half-bridge is turned off before the other switch is turned on, i.e. the switching signals are separated by a certain interlocking time where both transistors are kept off, now

the sequence is reversed, which means that both switches are turned on during a certain shoot-through time t_{SH}. Hence, since this actually corresponds to a negative interlocking time, where only the switching sequence of the upper and lower switch are changed, it becomes clear that with the integration of the shoot-through interval into a switching transition the number of switching transitions within one switching cycle is not increased. However, it has to be mentioned that in a conventional switching transition the interlocking delay is typically short compared to the on- and off-times of the switches. Therefore, in a half-bridge for the high-side and low-side switches the same duty cycle $d_{\mathrm{H}} = d_{\mathrm{L}}$ is calculated, whereas the interlocking delay is then e.g. generated by the PWM unit of the microcontroller. However, if now the shoot-through interval t_{SH} is integrated into the switching transient, the negative interlocking time can reach values which are similar to the on- and off-times of the switches. Hence, for the switches in a half-bridge individual duty cycles d_{H} and d_{L}, where $d_{\mathrm{H}} = d_{\mathrm{L}} + d_{\mathrm{SH}}$, have to be used. Similarly to the first approach, the shoot-through interval $t_{\mathrm{B}} = d_{\mathrm{B}} T_{\mathrm{SW}}$ is now proportionally distributed between the active state and buck state interval, i.e. $t_{\mathrm{B,A}} = d_{\mathrm{B,A}} T_{\mathrm{SW}} = d_{\mathrm{B}} d_{\mathrm{A}} / (d_{\mathrm{A}} + d_0) T_{\mathrm{SW}}$ and $t_{\mathrm{B},0} = d_{\mathrm{B},0} T_{\mathrm{SW}} = d_{\mathrm{B}} d_0 / (d_{\mathrm{A}} + d_0) T_{\mathrm{SW}}$, which results in the two extended intervals $t_{\mathrm{AN}} = d_{\mathrm{AN}} T_{\mathrm{SW}} = (d_{\mathrm{A}} + d_{\mathrm{B,A}}) T_{\mathrm{SW}}$ and $t_{0\mathrm{N}} = d_{0\mathrm{N}} T_{\mathrm{SW}} = (d_0 + d_{\mathrm{B},0}) T_{\mathrm{SW}}$, where $d_{\mathrm{AN}} + d_{0\mathrm{N}} = 1$ must be satisfied (cf. **Fig. 7**),

$$d_{\mathrm{AN}} = d_{\mathrm{A}} + \frac{t_{\mathrm{B,A}}}{T_{\mathrm{SW}}} = \frac{d_{\mathrm{A}}}{1 - d_{\mathrm{B}}}, \tag{22}$$

$$d_{0\mathrm{N}} = d_0 + \frac{t_{\mathrm{B},0}}{T_{\mathrm{SW}}} = \frac{d_0}{1 - d_{\mathrm{B}}}. \tag{23}$$

Since during the active interval and the buck state interval a switching transition occurs in each output phase both shoot-through intervals $t_{\mathrm{B,A}}$ and $t_{\mathrm{B},0}$ have to be divided by three, in order to get the needed shoot-through times $t_{\mathrm{SH,A}} = 1/3 \cdot t_{\mathrm{B,A}}$ and $t_{\mathrm{SH},0} = 1/3 \cdot t_{\mathrm{B},0}$, i.e. the negative interlocking delays for the switching transitions in each state. If now, according to the first approach, again an asymmetrical PWM carrier signal is used, which rises within $d_{\mathrm{AN}} T_{\mathrm{SW}}$ from zero to one and falls again during $d_{0\mathrm{N}} T_{\mathrm{SW}}$ down to zero, from geometrical considerations, both (horizontal) shoot-through times $t_{\mathrm{SH,A}}$ and $t_{\mathrm{SH},0}$ result in the same (vertical) duty cycle difference $d_{\mathrm{SH}} = 1/3 \cdot d_{\mathrm{B}}$ between the duty cycle of the upper switch, $d_{\mathrm{x,H}}$, and of the lower switch, $d_{\mathrm{x,L}}$, for each half-bridge $x \in \{a, b, c\}$ [12] (cf. **Fig. 7**),

$$d_{\mathrm{x,H}} = d_{\mathrm{x,L}} + 1/3 \cdot d_{\mathrm{B}}, \quad x \in \{a, b, c\}, \tag{24}$$

whereby, a represents the half-bridge with the lowest duty cycle, i.e. $d_{\mathrm{a}} = \min(d_{\mathrm{U}}, d_{\mathrm{V}}, d_{\mathrm{W}})$, c the half-bridge with the highest duty cycle, i.e. $d_{\mathrm{c}} = \max(d_{\mathrm{U}}, d_{\mathrm{V}}, d_{\mathrm{W}})$, and b the remaining half-bridge, i.e. $d_{\mathrm{b}} = \mathrm{mid}(d_{\mathrm{U}}, d_{\mathrm{V}}, d_{\mathrm{W}})$. For the calculation of the duty cycles $d_{\mathrm{x,H}}$ and $d_{\mathrm{x,L}}$ it has to be considered that a shoot-through interval in one phase can influence the effective on-time of another phase, since in a shoot-through interval the inverter input voltage is shorted and thus also the voltage of the other phases is zero, even if in these phases a voltage should be applied. However, this is not true for the phase with the lowest duty cycles ($d_{\mathrm{a,H}}$ and $d_{\mathrm{a,L}}$), because the shoot-through of the other phases occur during the off-time of this phase, i.e. when the low-side switch is turned on and anyway no voltage is applied to this phase. Hence, for $d_{\mathrm{a,L}}$ the smallest duty cycle of d_{U}, d_{V} and d_{W} has to be used, i.e. d_{a}, which due to the integration of the shoot-through

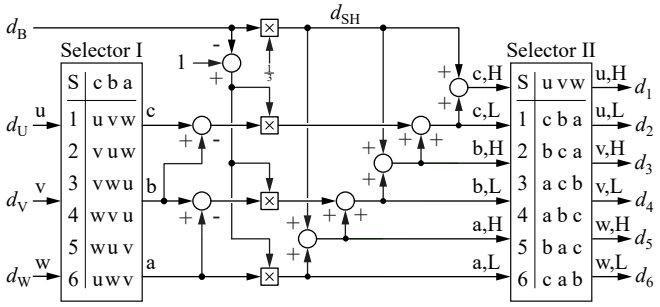

Fig. 8. Implementation of the transistor duty cycle calculation. The selectors I and II provide the signal paths to calculate the transistor duty cycles $d_1 - d_6$, which achieve the correct phase voltages in all six sectors of the three-phase system. Sector 1: $d_{\mathrm{U}} > d_{\mathrm{V}} > d_{\mathrm{W}}$, Sector 2: $d_{\mathrm{V}} > d_{\mathrm{U}} > d_{\mathrm{W}}$, Sector 3: $d_{\mathrm{V}} > d_{\mathrm{W}} > d_{\mathrm{U}}$, Sector 4: $d_{\mathrm{W}} > d_{\mathrm{V}} > d_{\mathrm{U}}$, Sector 5: $d_{\mathrm{W}} > d_{\mathrm{U}} > d_{\mathrm{V}}$, Sector 6: $d_{\mathrm{U}} > d_{\mathrm{W}} > d_{\mathrm{V}}$.

interval has to be scaled by the factor $d_{\mathrm{A}}/d_{\mathrm{AN}} = 1 - d_{\mathrm{B}}$. Consequently, the high-side duty cycle $d_{\mathrm{a,H}}$ is found with (24). For the second phase with $d_{\mathrm{b,H}}$ and $d_{\mathrm{b,L}}$, however, the shoot-through time of the first phase has to be considered because it occurs during the on-time of phase b; and for phase c with $d_{\mathrm{c,H}}$ and $d_{\mathrm{c,L}}$ the shoot-through times of both phases a and b have to be considered. Hence, depending on the values of the duty cycles d_{U}, d_{V} and d_{W}, i.e. the voltage sector in a three-phase system, the low-side duty cycles have to be calculated recursively from bottom to top, whereas the corresponding high-side duty cycles are calculated with (24),

$$d_{\mathrm{a,L}} = (1 - d_{\mathrm{B}}) \cdot d_{\mathrm{a}}, \tag{25}$$

$$d_{\mathrm{b,L}} = d_{\mathrm{a,H}} + (1 - d_{\mathrm{B}}) \cdot (d_{\mathrm{b}} - d_{\mathrm{a}}), \tag{26}$$

$$d_{\mathrm{c,L}} = d_{\mathrm{b,H}} + (1 - d_{\mathrm{B}}) \cdot (d_{\mathrm{c}} - d_{\mathrm{b}}). \tag{27}$$

However, the resulting low- and high-side duty cycles of the half-bridges a, b and c have to be assigned to the corresponding transistor duty cycles $d_1 - d_6$. Thereby, the high and the low-side duty cycles of phase a, i.e. $d_{\mathrm{a,H}}$ and $d_{\mathrm{a,L}}$, are assigned to the upper and the lower switch of the half-bridge with the lowest inverter duty cycle, e.g. in sector 1 results $d_5 = d_{\mathrm{a,H}}$ and $d_6 = d_{\mathrm{a,L}}$. The remaining transistor duty cycles $d_1 - d_4$ follow the same scheme, which is also shown in **Fig. 8**.

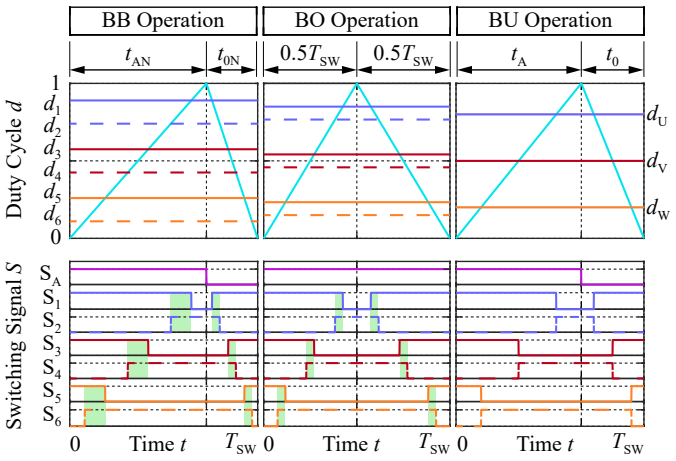

Fig. 9. Modulation scheme, including the PWM carrier and the transistor duty cycles $d_1 - d_6$, together with the switching signals of the inverter switches $S_1 - S_6$ and the buck transistor S_{A}, for the buck-boost (BB), the boost (BO) and the (BU) buck operation, whereby the shoot-through intervals are indicated.

Finally, the buck transistor $\mathrm{T_A}$ is operated accordingly to the actual conduction state, which means that during d_{AN} the buck transistor $\mathrm{T_A}$ is turned on and during $d_{0\mathrm{N}}$ is turned off. In **Fig. 9**, the switching signals of the inverter switches and of the buck transistor for all operation modes are shown. In buck-boost (BB) operation, the shoot-through interval d_{B} is integrated into the switching transitions as previously described. In buck (BU) operation, the duty cycle d_{B} is zero and therefore no shoot-through intervals exist. In boost (BO) operation, where $d_0 = 0$, the asymmetrical PWM carrier would lead to a sawtooth carrier, which is undesired, since in this case all transistors would switch at the same time instant. Therefore, again a symmetrical triangular carrier is used, which leads to the conventional Z-source inverter operation described in [13].

D. Verification

The proper operation of the proposed topology is verified by circuit simulations. The considered variable speed drive system is rated for an output power of 7.5 kW and is supplied from a single-phase mains with $480\,\mathrm{V_{rms}}/50\,\mathrm{Hz}$. The overall system specifications are summarized in **Tab. I**. For a better visualisation, in the simulation a peak-to-peak capacitor voltage ripple of 3% and a peak-to-peak inductor current ripple of 15% is assumed. Furthermore, a machine frequency close to the mains frequency is chosen. The resulting circuit parameters are also listed in Tab. I. However, it has to be mentioned that for a real circuit design the values of the passive components as well as the switching frequency would have to be optimized concerning efficiency and/or power density.

TABLE I
SUMMARY OF THE CONVERTER SPECIFICATIONS AND THE CIRCUIT PARAMETERS.

Grid voltage $V_{\mathrm{G,rms}}$	480 V
Angular grid frequency ω_{G}	$2\pi \cdot 50$ Hz
Nominal intermediate voltage V_{PN}	400 V/700 V
Machine phase voltage $V_{\mathrm{M,rms}}$	160 V
Electrical machine frequency ω_{M}	$2\pi \cdot 67$ Hz
Nominal mechanical power $P_{\mathrm{M,N}}$	7.5 kW
Z-source inductance L	300 µH
Z-source capacitance C	2 mF
Switching frequency f_{SW}	140 kHz

With the given machine voltage $V_{\mathrm{M,rms}}$, the minimum intermediate voltage is given with $V_{\mathrm{PN}} = 400\,\mathrm{V}$, which thanks to the buck-stage can be set below the peak grid voltage, i.e. $\hat{V}_{\mathrm{G}} = 679\,\mathrm{V}$. In **Fig. 10(a)** the corresponding waveforms at the nominal operating point are shown. It can be noticed that the capacitor voltage $v_{\mathrm{C}} = V_{\mathrm{PN}}$ is constant and the inductor current i_{L} nicely tracks its reference (dashed line), which with the buck-boost operation in the vicinity of the voltage zero crossings can be kept at the minimum required value $i_{\mathrm{L,min}}$. Furthermore, the converter operation smoothly transitions between the different operation modes (BU), (BO) and (BB), which leads to a sinusoidal grid current i_{G} with a low current THD of 1.1%. Finally, with the proposed modulation concept, three purely sinusoidal phase voltages and phase currents i_{U}, i_{V} and i_{W} can be achieved.

In the following, the benefits gained from the additional buck-stage should be highlighted. As already mentioned, the Z-source inverter can also be directly connected to the single-phase mains via a diode rectifier. In this case, the buck functionality is lost and the intermediate voltage has to be larger than the peak grid voltage, e.g. $V_{\mathrm{PN}} = 700\,\mathrm{V}$, and thus the voltage stress on the semiconductor elements increases considerably. Further on, in the vicinity of the zero crossings, the input current can no longer be sinusoidally controlled. The resulting waveforms are shown in **Fig. 10(b)**. In addition, it can be noticed, that this input current distortion also leads to slight distortions in the output phase currents i_{U}, i_{V} and i_{W}.

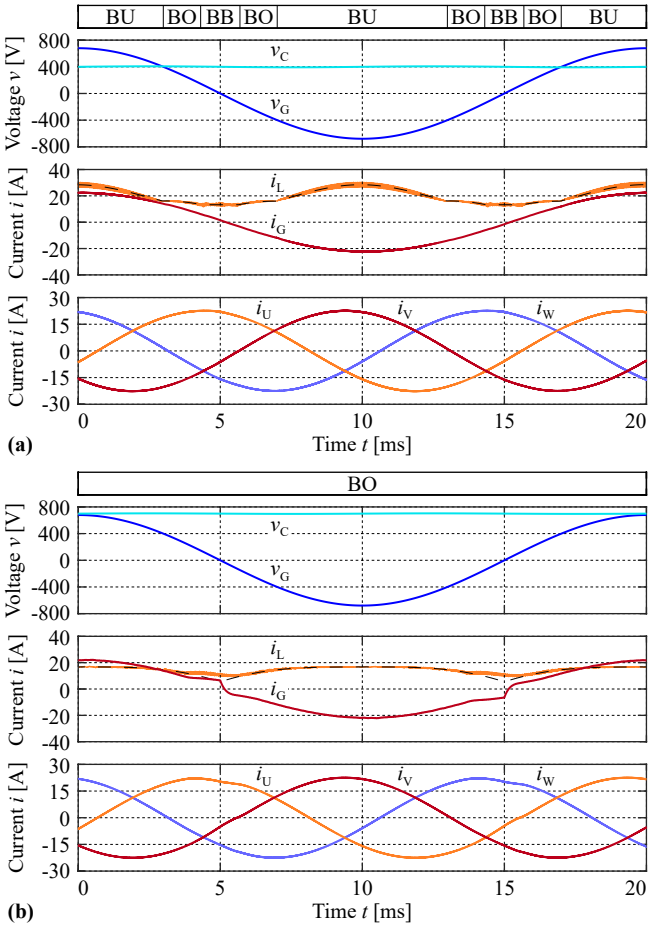

Fig. 10. Simulation results at nominal operating conditions of the grid voltage v_{G}, the capacitor voltage v_{C}, the grid current i_{G}, the inductor current i_{L} with its reference (dashed line) as well as the three phase currents i_{U}, i_{V} and i_{W} over one grid period T_{G} for **(a)** the proposed and **(b)** the Z-source-based single-to-three phase boost topology. In both cases, the machine is modelled by a symmetrical RL-load.

IV. COMPONENT STRESS ANALYSIS AND COMPARISON

With the additional buck-stage, the proposed *123ZBBC* not only leads to a better input and output current quality, but also to a lower component stress as analyzed in the following for the already presented application (cf. Tab. I). Thereby, the voltage stresses are calculated analytically, while the current stresses are derived from the circuit simulations.

The capacitor voltage V_{C} is equal to the average intermediate voltage $\bar{v}_{\mathrm{PN}}$ and consequently, for the *123ZBBC* the capacitor voltage stress is only $V_{\mathrm{C}} = 400\,\mathrm{V}$ compared to $V_{\mathrm{C}} = 700\,\mathrm{V}$, as it is the case for the Z-source topology without buck-stage. However, due to the buck operation now the inductor current increases from $I_{\mathrm{L,rms}} = 14.8\,\mathrm{A}$ for the boost topology to $I_{\mathrm{L,rms}} = 20.8\,\mathrm{A}$ in case of the *123ZBBC*. Furthermore, additional current stresses appear in the buck-stage ($I_{\mathrm{DA,avg/rms}} = 5.8\,\mathrm{A}/13.8\,\mathrm{A}$ and $I_{\mathrm{TA,rms}} = 19.9\,\mathrm{A}$), which for the boost Z-source do not exist (cf. **Tab. II**). The maximum voltage applied to the inverter transistors is given by the maximum intermediate voltage v_{PN}, which either occurs during the active state, when $v_{\mathrm{G}} = 0\,\mathrm{V}$, or

during the buck state and equals twice the capacitor voltage $V_{\mathrm{Ti,max}} = v_{\mathrm{PN}} = 2V_{\mathrm{C}}$. Hence, for the proposed topology the minimum blocking voltage of the inverter switches is $800\,\mathrm{V}$, whereas without buck-stage the minimum blocking voltage increases to $1.4\,\mathrm{kV}$ (cf. **Tab. II**). The same is also true for the voltage stress on the bridge rectifier diodes as well as the buck diode. The buck transistor, however, only has to block the maximum grid voltage during buck state, which in this case is $V_{\mathrm{TA,max}} = \hat{V}_{\mathrm{G}} = 687\,\mathrm{V}$.

Therefore, in the *123ZBBC* for all switches and diodes $1.2\,\mathrm{kV}$ semiconductor devices, e.g. SiC MOSFETs, can be employed, whereas for the boost-only Z-source converter, semiconductor components with a blocking voltage of at least $1.7\,\mathrm{kV}$, e.g. $1.7\,\mathrm{kV}$ SiC MOSFETs (with higher on-state resistance than $1.2\,\mathrm{kV}$ devices), are needed. Hence, the benefit gained from the change of semiconductor technology, i.e. improved conduction and switching performance [19], overcompensate the additional conduction losses caused by the inserted buck-stage, which additionally allows to achieve a purely sinusoidal input current.

TABLE II
COMPONENT STRESS COMPARISON BETWEEN THE PROPOSED BUCK-BOOST Z-SOURCE-BASED AC/AC CONVERTER AND THE CONVENTIONAL Z-SOURCE CONVERTER DIRECTLY SUPPLIED FROM THE SINGLE-PHASE MAINS VIA A DIODE BRIDGE RECTIFIER.

Component	Z-Buck-Boost	Conv. Z-Boost
V_{PN}	400 V	700 V
$I_{\mathrm{L,rms}}$	20.8 A	14.8 A
$I_{\mathrm{C,rms}}$	8.9 A	11.8 A
$V_{\mathrm{Di,max}}$	800 V	1400 V
$I_{\mathrm{Di,avg}}$	7.1 A	7.3 A
$I_{\mathrm{Di,rms}}$	14.1 A	13.7 A
$V_{\mathrm{DA,max}}$	800 V	-
$I_{\mathrm{DA,avg}}$	5.8 A	-
$I_{\mathrm{DA,rms}}$	13.8 A	-
$V_{\mathrm{TA,max}}$	687 V	-
$I_{\mathrm{TA,avg}}$	19.9 A	-
$V_{\mathrm{Ti,max}}$	800 V	1400 V
$I_{\mathrm{Ti,rms}}$	11.7 A	11.8 A

V. CONCLUSION

This paper proposes a novel unidirectional single-to-three-phase Z-source buck-boost AC/AC converter (*123ZBBC*), which integrates the boost function into the inverter stage, resulting in a reduced realization effort. The included buck-stage enables a sinusoidal input current and reduces the overall component voltage stress, compared to the single-to-three phase Z-source boost topology.

The analysis provided in this paper reveals the basic operation principle, including the conduction states, and presents the PFC modulation strategy achieving the minimal inductor current. The proposed closed-loop control enables a sinusoidal input current, controles the required intermediate voltage and provides a three-phase voltage system to the load. Additionally, the modulation scheme of the inverter, and particularly the distribution of the shoot-through interval, is analyzed in detail. All these findings are verified by means of circuit simulations. The component stresses are derived and the conducted comparison to a Z-source boost topology reveals a lower blocking voltage of the semiconductor devices and enables the employment of $1.2\,\mathrm{kV}$ SiC MOSFETS instead of $1.7\,\mathrm{kV}$ devices for the presented application. Due to the change in the semiconductor technology, the system performance is improved, i.e. the additional losses of the buck-stage are overcompensated, which leads to an overall higher efficiency.

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