Power Electronic Systems
Laboratory

IEEE Transactions on Power Electronics, Vol. 28, No. 9, pp. 4422-4430, September 2013

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Modeling and Pareto Optimization of Microfabricated Inductors for Power Supply on Chip

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***Abstract*—Microfabricated inductors experience increasing interest and research activity because of their high potential in buck converters for power supply in package and power supply on chip applications. This paper details the modeling and optimization of microfabricated racetrack inductors. The analytical expressions derived characterize inductance, efficiency, and power density based on geometrical parameters, inductor current, and switching frequency. An accurate analysis of the inductor current that includes the impact of losses is performed to determine the switching frequency, the ac copper losses, and the core losses. The presented model is compared to finite element method simulations and reported results of three microfabricated inductors. Finally, the optimum tradeoff between efficiency and power density is identified using the Pareto front, which results from the evaluation of a large number of microfabricated inductors in the design space defined by the application.**

***Index Terms*—Modeling, optimization methods, thin film inductors.**

I. Introduction

THE use of microfabricated inductors in power converters for voltage regulator module (VRM) applications is a key enabler for power supply on chip (PwrSoC) systems, whereas for power supply in package (PSiP) systems, the utilization of microfabricated inductors may lead to a higher power density compared to what can be obtained using readily available discrete inductors [1]–[3]. These systems exhibit a high level of power supply integration where switches, passive components, and control drivers are copackaged in one package (PSiP) or manufactured on the same integrated circuit die (PwrSoC). The power supply specifications depend on the application and semiconductor technology, but typical value ranges are input voltage: 1.8–3.6 V, output voltage: 0.9–1.5 V, and output power: 0.1–1 W [4]–[8]. The buck converter is a popular topology choice since it performs the step-down conversion required by these specifications. It is furthermore a widely used and well-known converter topology for VRM applications.

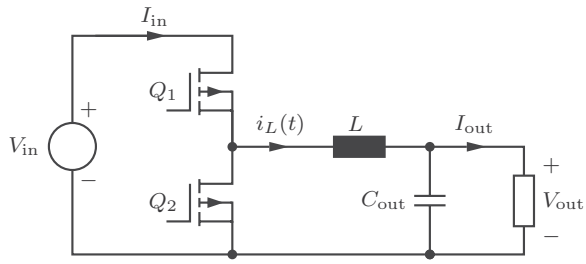

Fig. 1. Synchronous buck converter implemented with two switches Q_1 and Q_2 controlled by the duty cycle D. The output filter consists of the microfabricated inductor L and the output capacitor C, which is in parallel with the load.

Design and optimization of the buck converter depicted in Fig. 1 for PSiP or PwrSoC systems have proven a major challenge [1], [2], [9]–[11]. Discussing the optimization potential of the individual buck converter components, first the transistors Q_1 and Q_2 need to withstand the input voltage, which may be close to the transistor breakdown voltage of the chosen semiconductor technology. The optimum transistor area is usually determined as a tradeoff between ON-state resistance, gate charge, and drain–source capacitance. The required output filter capacitance is simply determined from voltage ripple requirements, and it may be reduced using a multiphase design [12]. However, the microfabricated inductor has several degrees of freedom in magnetic material and geometry. It is, therefore, the buck converter component with the highest potential for optimization.

Microfabricated inductors are implemented either with or without magnetic core material. Air core inductors benefit from having no core losses, but the resulting required switching frequency is very high (e.g., several hundreds of megahertz [8], [10]) due to the relatively low inductance value obtainable. To increase the specific inductance, and thereby lower the switching frequency, a magnetic material forming a closed-loop path for the magnetic flux is implemented. The ferrite MnZn is commonly used for frequencies below 1 MHz, whereas thin-film permalloy like NiFe and nanogranular film like CoZrO are used for frequencies in the megahertz range, thereby being suitable for PSiP and PwrSoC systems levels of integration [9].

The microfabricated racetrack inductor is an effective geometry for PSiP and PwrSoC systems due to the simpler manufacturability of magnetic material around straight conductors rather than rounded conductors; example designs include a 94.0%

Manuscript received June 12, 2012; revised September 9, 2012; accepted October 24, 2012. Date of current version February 15, 2013. Recommended for publication by Associate Editor Y.-F. Liu.

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Digital Object Identifier 10.1109/TPEL.2012.2227815

efficiency cored racetrack inductor with 0.25- W/mm^2 power density [13]. Wang *et al*. [6] design and fabricate a 92% efficiency cored racetrack inductor with 0.05- W/mm^2 power density, and Meere *et al*. [4] consider the performance of the cored racetrack inductor in a buck converter operated over a wide load range. They achieve converter efficiencies above 72% for a 1.12-V output voltage at a variable output current of 30–100 mA; the switching frequency of that converter design ranges from 20 to 100 MHz.

This paper details a thorough analysis and Pareto optimization of cored racetrack inductors for PSiP and PwrSoC systems. Section II discusses the buck converter operating modes and their related inductor current. To accurately determine losses, an analysis of the inductor current that captures the impact of losses on duty cycle and switching frequency is performed. Section III presents the analytical cored racetrack inductor model, which predicts the inductance, the copper losses, and the core losses of the inductor. Three-dimensional finite element method (FEM) simulations are used to verify the results obtained from the analytical model. Section IV compares the calculated, simulated, and reported performance of three manufactured cored racetrack inductors. Section V utilizes the analytical model in an optimization procedure that maps the calculated performances of a large number of different cored racetrack inductor designs to the $\eta - \alpha$ plane, where η is the efficiency and α the power density (in W/mm^2). The envelope resulting from the highest efficiency at each power density value is the $\eta - \alpha$ Pareto front [14], which is the outcome of the optimization procedure.

II. Buck Converter Operation—Inductor Current Analysis

The microfabricated inductor losses, which are modeled in the next section, depend on the inductor current. Therefore, an analysis that accurately predicts the impact of the losses on the inductor current is carried out.

The buck converter is specified by the input voltage $V_{\rm in}$, the output voltage $V_{\rm out}$, the output current $I_{\rm out}$, and the peak inductor current $I_{\rm pk}$. With these specifications, the inductor current is characterized by the duty cycle D, the switching period $T_{\rm s}$, and the operating mode of the buck converter as analyzed in the following.

A. Buck Converter Operating Modes

The buck converter in Fig. 1 has three steady-state operating modes: continuous conduction mode with solely positive inductor current (CCM1), continuous conduction mode where the inductor current is negative during parts of the switching period (CCM2), and boundary conduction mode (BCM) where the inductor current is exactly zero after each switching cycle. The discontinuous conduction mode is not considered since the synchronous rectification is implemented with a bidirectional switch. Operation in BCM and CCM2 is of particular interest since these modes enable very low switching losses. Furthermore, BCM results in the lowest stored energy in the inductor [10].

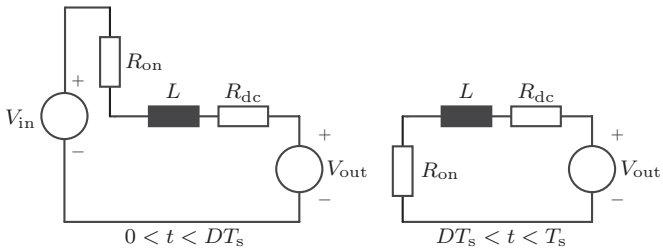

Fig. 2. Simplified dc buck converter schematic used to determine the duty cycle and switching frequency based on the specifications. Switching phase one is valid for $0 < t < DT_{\rm s}$ and switching phase two is valid for $DT_{\rm s} < t < T_{\rm s}$. $R_{\rm eq} = R_{\rm on} + R_{\rm dc}$ is the total equivalent series resistance of the inductor in both switching phases.

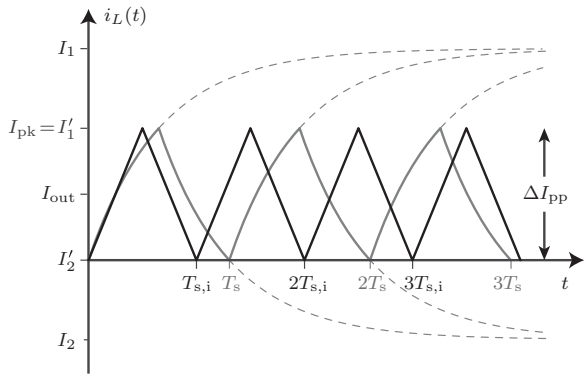

Fig. 3. Idealized (black) and accurate (gray) steady-state inductor current $i_L(t)$ shown in BCM. Including the losses results in an exponential inductor current, which effectively changes the switching frequency from $T_{\rm s,i}$ in the ideal case to $T_{\rm s}$ in the accurate case for the same buck converter operating mode. For high-efficiency inductor designs, the deviation of the exponential inductor current compared to the ideal triangular current becomes small, but it is nonetheless included throughout the analysis for completeness.

We introduce the peak-to-average ratio (PAR) as a means to describe the buck converter operating mode

$$\mathrm{PAR} = \frac{I_{\rm pk}}{I_{\rm out}}. \tag{1}$$

For a buck converter specified by $V_{\rm in}$, $V_{\rm out}$, $I_{\rm out}$, $I_{\rm pk}$, and given an inductance with an equivalent series resistance, PAR can be used to determine the switching period $T_{\rm s}$.

B. Accurate Inductor Current Analysis

The accurate inductor current analysis is based on the simplified buck converter circuit shown in each of its two switching phases in Fig. 2. Switches Q_1 and Q_2 are assumed to be ideal except for identical ON-state resistances $R_{\rm on}$. The output capacitance is assumed to be infinite leading to a constant dc output voltage. Hence, including $R_{\rm on}$ and the inductor dc resistance $R_{\rm dc}$, the equivalent inductor series resistance, $R_{\rm eq} = R_{\rm on} + R_{\rm dc}$, is independent of the switching phase. With these assumptions, the duty cycle becomes

$$D = \frac{V_{\rm out} + I_{\rm out}(R_{\rm on} + R_{\rm dc})}{V_{\rm in}} = \frac{V_{\rm out} + I_{\rm out}R_{\rm eq}}{V_{\rm in}}. \tag{2}$$

To accurately determine the switching frequency $f_{\rm s} = 1/T_{\rm s}$, the exponential nature of the inductor current depicted in Fig. 3 is

analyzed. The inductor current increases or decreases toward I_1 and I_2, respectively; I_1' and I_2' are the maximum and minimum inductor currents during each switching phase, respectively. It follows from Fig. 2 that

$$I_1 = \frac{V_{\rm in} - V_{\rm out}}{R_{\rm eq}} \tag{3}$$

$$I_2 = \frac{-V_{\rm out}}{R_{\rm eq}}. \tag{4}$$

The inductor current in each switching phase is calculated using Fig. 3 as

$$i_{L1}(t) = I_1 + (I_2' - I_1)e^{-t/\tau}, \qquad \text{for } 0 < t < DT_{\rm s} \tag{5}$$

$$i_{L2}(t) = I_2 + (I_1' - I_2)e^{-(t-DT_{\rm s})/\tau}, \text{ for } DT_{\rm s} < t < T_{\rm s} \tag{6}$$

where $\tau = L/R_{\rm eq}$ is the inductor time constant.

Using (3) and (4) in (5) and (6), the maximum and minimum currents $I_1' = i_{L1}(DT_{\rm s})$ and $I_2' = i_{L2}(T_{\rm s})$, respectively, are attained as

$$I_{\rm pk} = I_1' = \frac{V_{\rm in}\left(e^{-DT_{\rm s}/\tau} - 1\right) + V_{\rm out}\left(1 - e^{-T_{\rm s}/\tau}\right)}{R_{\rm eq}\left(e^{-T_{\rm s}/\tau} - 1\right)} \tag{7}$$

$$I_2' = \frac{V_{\rm in}e^{-T_{\rm s}/\tau}\left(1 - e^{DT_{\rm s}/\tau}\right) + V_{\rm out}\left(1 - e^{-T_{\rm s}/\tau}\right)}{R_{\rm eq}\left(e^{-T_{\rm s}/\tau} - 1\right)}. \tag{8}$$

This leads to a peak–peak inductor current of

$$\Delta I_{\rm pp} = I_1' - I_2' = \frac{V_{\rm in}}{R_{\rm eq}} \frac{e^{-DT_{\rm s}/\tau} + e^{-(1-D)T_{\rm s}/\tau} - e^{-T_{\rm s}/\tau} - 1}{e^{-T_{\rm s}/\tau} - 1}. \tag{9}$$

The expression for $I_{\rm pk}$ in (7) together with D from (2) can be evaluated for a specific value of PAR in (1) to determine the switching period $T_{\rm s}$. However, no closed-form solution for $T_{\rm s}$ exists, so a numerical approach must be used for accurate calculations.

The PAR value that corresponds to BCM can be (numerically) calculated. Hence, when the switching period fulfills $I_2' = 0$, then

$$\mathrm{PAR}_{\rm BCM} = \left.\frac{I_{\rm pk}}{I_{\rm out}}\right|_{I_2'=0} \tag{10}$$

and CCM1 applies for $1 < \mathrm{PAR} < \mathrm{PAR}_{\rm BCM}$ while CCM2 applies for $\mathrm{PAR} > \mathrm{PAR}_{\rm BCM}$.

A closed-form approximate expression for $T_{\rm s}$ can be derived assuming a constant inductor current slope of $di_{L1}(t)/dt \approx (V_{\rm in} - V_{\rm out} - I_{\rm out}R_{\rm eq})/L$ as in [15]. The peak inductor current may then be described as $I_{\rm pk} \approx I_{\rm out} + \Delta I_{\rm pp}/2$, and the switching period becomes[1]

$$\Delta I_{\rm pp} \approx \frac{V_{\rm in} - V_{\rm out} - I_{\rm out}R_{\rm eq}}{L} DT_{\rm s}$$

$$\Leftrightarrow T_{\rm s} \approx \frac{2LI_{\rm out}(\mathrm{PAR} - 1)}{V_{\rm in}D(1-D)}. \tag{11}$$

[1]This expression can also be derived from a first-order Taylor series expansion of $\Delta I_{\rm pp}$ in (9).

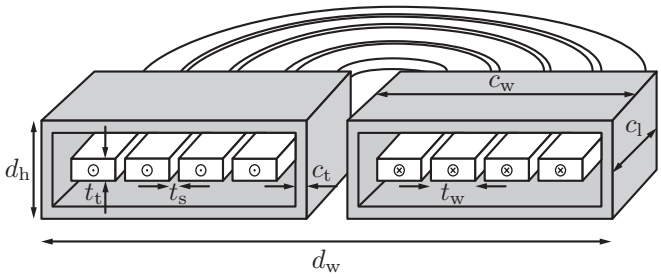

Fig. 4. Cross-sectional view of the cored racetrack inductor with noncored half-spiral end turns.

With these assumptions, BCM occurs for

$$\mathrm{PAR}_{\rm BCM} \approx 2. \tag{12}$$

C. Limits of $R_{\rm eq}$ and PAR

The equivalent series resistance $R_{\rm eq} = R_{\rm on} + R_{\rm dc}$ has an upper limit stemming from the criteria $D < 1$. Using (2), the limit for which the buck converter is realizable is

$$R_{\rm eq} < \frac{V_{\rm in} - V_{\rm out}}{I_{\rm out}}. \tag{13}$$

The maximum value of PAR for a given inductor design can be determined from (7) as the switching period approaches infinity; hence, from (1), we have

$$1 < \mathrm{PAR} < \lim_{T_{\rm s}\to\infty} \frac{I_{\rm pk}}{I_{\rm out}} = \frac{V_{\rm in} - V_{\rm out}}{I_{\rm out}R_{\rm eq}}. \tag{14}$$

D. Inductor Current Fourier Analysis

To estimate the losses at the switching frequency and its harmonics, the inductor current amplitude at each switching frequency harmonic is calculated. The absolute value of the kth complex Fourier coefficient c_k describing the periodic waveform in Fig. 3 represents the inductor current amplitude I_k at the kth switching frequency harmonic [16]

$$I_k = 2|c_k| = \frac{2}{T_{\rm s}}\left|\int_0^{DT_{\rm s}} i_{L1}(t)e^{-2j\pi kt/T_{\rm s}}\,dt + \int_{DT_{\rm s}}^{T_{\rm s}} i_{L2}(t)e^{-2j\pi kt/T_{\rm s}}\,dt\right| \tag{15}$$

where j is the imaginary unit. However, since a very long expression results from (15), a simplified yet useful expression for I_k assuming constant inductor current slope yields

$$I_k \approx \Delta I_{\rm pp}\frac{\sin(D\pi k)}{(\pi k)^2 D(1-D)}. \tag{16}$$

III. Modeling of Cored Racetrack Inductors

An analytical model, which utilizes the accurate inductor current analysis, is developed to evaluate the inductance and the losses of cored racetrack inductors. The cross section of the cored racetrack inductor is depicted in Fig. 4, and the appertaining geometrical parameters used in the following analysis are listed in Table I.

TABLE 1
GEOMETRICAL PARAMETERS DESCRIBING THE CORED RACETRACK INDUCTOR

Symbol	Description
N	Number of turns
t_w	Winding width
t_t	Winding thickness
t_s	Winding spacing
c_w	Core width
c_t	Core thickness
c_l	Core length
d_h	Device height
d_w	Device width
d_l	Device length

A. Inductance Estimation

The inductance estimation of the cored racetrack inductor partitions the inductor into 1) the core; 2) the winding parts covered by the core; and 3) the noncored end turns.

The core cross-sectional area using Fig. 4 is $A_\mathrm{c} = c_\mathrm{t} c_\mathrm{l}$ and the magnetic path length is $l_\mathrm{m} = 2(c_\mathrm{w} + d_\mathrm{h})$; hence, the inductance contribution from the two cores can be estimated as

$$L_\mathrm{core} = 2\frac{\mu_0 \mu_\mathrm{c} N^2 A_\mathrm{c}}{l_\mathrm{m}} = \frac{\mu_0 \mu_\mathrm{c} N^2 c_\mathrm{t} c_\mathrm{l}}{c_\mathrm{w} + d_\mathrm{h}} \tag{17}$$

where $\mu_0 = 4\pi 10^{-7}$ H/m is the permeability of free air and μ_c is the relative permeability of the core material.

The winding inductance contribution of the cored part is estimated considering the self-inductance of each wire and the mutual inductances of the adjacent wires. The self-inductance (in μH) of a straight wire with rectangular cross section using [17] is

$$L_\mathrm{t,self} \approx 0.2 c_\mathrm{l} \left[\ln\left(\frac{2c_\mathrm{l}}{t_\mathrm{w} + t_\mathrm{t}} \right) + \frac{1}{2} \right] \tag{18}$$

and the total mutual inductance (in μH) for $N > 1$ between the adjacent straight wires in the cored part is

$$L_\mathrm{t,mutual} \approx \sum_{i=1}^{N-1} \sum_{j=i+1}^{N} 0.2 c_\mathrm{l} \left[\ln\left(\frac{2c_\mathrm{l}}{(j-1)(t_\mathrm{w} + t_\mathrm{s})} \right) - 1 + \frac{(j-i)(t_\mathrm{w} + t_\mathrm{s})}{c_\mathrm{l}} - \left(\frac{(j-i)(t_\mathrm{w} + t_\mathrm{s})}{2c_\mathrm{l}} \right)^2 \right]. \tag{19}$$

The previous two equations neglect tabulated correction terms that were found to have negligible influence on the calculated inductances. The winding inductance of the two cored parts is

$$L_\mathrm{t,core} = 2(N L_\mathrm{t,self} + L_\mathrm{t,mutual}). \tag{20}$$

The inductance contributions of the two noncored end windings are assumed to equal the inductance of a single circular planar spiral inductor with outer and inner diameters d_o and d_i, respectively:

$$L_\mathrm{t,spiral} \approx \frac{u_0 N^2 d_\mathrm{avg}}{2} \left[\ln\left(\frac{2.46}{p} \right) + 0.2 p^2 \right] \tag{21}$$

where $d_\mathrm{avg} = (d_\mathrm{o} + d_\mathrm{i})/2$ is the average diameter, $p = (d_\mathrm{o} - d_\mathrm{i})/(d_\mathrm{o} + d_\mathrm{i})$ the fill factor, and the empirical constants stem from curve fitting of measured circular planar spiral inductors [18].

Finally, the total dc inductance of cored racetrack inductors may be estimated as

$$L = L_\mathrm{core} + L_\mathrm{t,core} + L_\mathrm{t,spiral}. \tag{22}$$

B. Copper Loss Analysis

Assuming the length of each winding to be $2c_\mathrm{l}$ plus the circumference of the nth winding circle that accounts for the end turns, the dc winding resistance may be estimated as

$$R_\mathrm{dc} = \frac{\rho_\mathrm{t}}{t_\mathrm{w} t_\mathrm{t}} \left(2N c_\mathrm{l} + 2\pi \sum_{n=1}^{N} r_n \right) \tag{23}$$

where ρ_t is the resistivity of the winding material and $r_n = d_\mathrm{o}/2 - n(t_\mathrm{w} + t_\mathrm{s})$ is the radius of the nth end winding circle.

The Dowell's analysis [19] for ac resistance factor calculations utilizes a 1-D modeling approach assuming horizontal field direction in the winding window. Although this assumption may yield limited accuracy for microfabricated inductors [13], [20], it is included here to indicate the effect of switching frequency on copper losses. Assuming the effective number of layers for the Dowell analysis is $h = 0.5$ as in [13], the ac resistance factor at the kth switching frequency harmonic becomes

$$F_k = \theta_k \left[\frac{\sinh(2\theta_k) + \sin(2\theta_k)}{\cosh(2\theta_k) - \cos(2\theta_k)} + \frac{2(h^2 - 1)}{3} \frac{\sinh(\theta_k) - \sin(\theta_k)}{\cosh(\theta_k) + \cos(\theta_k)} \right] \tag{24}$$

where $\theta_k = t_\mathrm{t}/\delta_k = t_\mathrm{t}/\sqrt{\rho_\mathrm{t}/(\mu_0 \mu_\mathrm{t} \pi k f_\mathrm{s})}$ is the winding thickness to skin depth ratio at the kth switching frequency harmonic with μ_t being the relative permeability copper. Hence, the ac winding resistance at the kth switching frequency harmonic is

$$R_{\mathrm{ac},k} \approx F_k R_\mathrm{dc}. \tag{25}$$

The total copper losses are estimated using (15), (23), and (25) as

$$P_\mathrm{t} = R_\mathrm{dc} I_\mathrm{out}^2 + \sum_{k}^{k_\mathrm{max}} R_{\mathrm{ac},k} \frac{I_k^2}{2} \tag{26}$$

where k_max is the maximum switching frequency harmonic considered.

C. Core Loss Analysis

The following core loss analysis is based on the assumption that the magnetic field, and thereby the flux density, is constant throughout the entire core material. The dc magnetic field and flux density are

$$H_\mathrm{dc} = \oint \boldsymbol{H} \cdot \mathbf{d}\boldsymbol{l}_\mathbf{m} = \frac{N I_\mathrm{out}}{2(c_\mathrm{w} + d_\mathrm{h})} \tag{27}$$

$$B_\mathrm{dc} = \mu_0 \mu_\mathrm{c} H_\mathrm{dc} = \frac{\mu_0 \mu_\mathrm{c} N I_\mathrm{out}}{2(c_\mathrm{w} + d_\mathrm{h})}. \tag{28}$$

To derive analytical calculations of core losses is a tedious task because of the nonlinear loss mechanisms in magnetic materials [21], [22]. For that reason, core losses are most commonly determined with the Steinmetz equation [15], which is an empirical curve fit to measured core loss data

$$P_{\mathrm{steinmetz}} = K f_{\mathrm{s}}^{\alpha} \left(\frac{\Delta B_{\mathrm{pp}}}{2} \right)^{\beta} V_{\mathrm{c}} \tag{29}$$

where K, α, and β are the material-dependent Steinmetz parameters and the peak–peak flux density is calculated using $\Delta B_{\mathrm{pp}}/B_{\mathrm{dc}} = \Delta I_{\mathrm{pp}}/I_{\mathrm{dc}}$.

If the Steinmetz parameters are unknown, the core losses can be determined by considering hysteresis losses and induced eddy current losses individually.

The hysteresis losses, which are due to the hysteretic change in flux density versus magnetic field over a switching period, are approximately proportional to switching frequency and can be described in the following form:

$$P_{\mathrm{h}} = K_{\mathrm{h}} f_{\mathrm{s}} \left(\frac{\Delta B_{\mathrm{pp}}}{2} \right)^{b} V_{\mathrm{c}} \tag{30}$$

where K_{h} and b are material-dependent parameters [15].

The proximity effect of the generated magnetic field gives rise to induced eddy currents in the core material. To estimate the eddy current losses, the core is considered to be composed of four bus bars of equal thickness: one bus bar for each top and bottom section, and one bus bar for each side wall section. The magnetic field inside each bus bar is assumed to be homogeneous and therefore the expression for proximity losses in a bus bar [23] can be applied to determine the eddy current losses in the two cores:

$$P_{\mathrm{e}} = 2 \frac{\rho_{\mathrm{c}} 2(c_{\mathrm{w}} + d_{\mathrm{h}}) c_{\mathrm{l}}}{c_{\mathrm{t}}} \sum_{k}^{k_{\mathrm{max}}} \nu_k \frac{\sinh(\nu_k) - \sin(\nu_k)}{\cosh(\nu_k) + \cos(\nu_k)} H_k^2 \tag{31}$$

where $\nu_k = c_{\mathrm{t}}/\delta_{\mathrm{c},k} = c_{\mathrm{t}}/\sqrt{\rho_{\mathrm{c}}/(\mu_0 \mu_{\mathrm{c}} \pi k f_{\mathrm{s}})}$ is the core thickness to skin depth ratio at the kth switching frequency harmonic with ρ_{c} being the resistivity of the core material. The magnetic field amplitude at the kth switching frequency harmonic is calculated using $H_k/H_{\mathrm{dc}} = I_k/I_{\mathrm{dc}}$.

The efficiency of the cored racetrack inductor is

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss}}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{t}} + P_{\mathrm{h}} + P_{\mathrm{e}}} \tag{32}$$

with $P_{\mathrm{out}} = V_{\mathrm{out}} I_{\mathrm{out}}$, and the power density is

$$\alpha = \frac{P_{\mathrm{out}}}{A} \tag{33}$$

where $A = d_{\mathrm{l}} d_{\mathrm{w}}$ is the area of the cored racetrack inductor.

IV. Experimental Verification

In this section, reported results of three microfabricated racetrack inductors are compared against the analytical model from Section III and 3-D FEM simulation results. Manufacturing steps and further details of the microfabricated inductors, of which one is shown in Fig. 5, can be found in [4]–[6]. Fig. 6 shows the FEM simulator setup in Ansoft Maxwell of the cored racetrack inductor. For the analytical calculations and FEM simulations, the dc inductance and dc resistance are used to evaluate the inductor current according to Section II to determine the switching frequency, where we for a qualitative inductor comparison neglect the ON-state resistances of the switches, i.e., $R_{\mathrm{on}} = 0\ \Omega$.

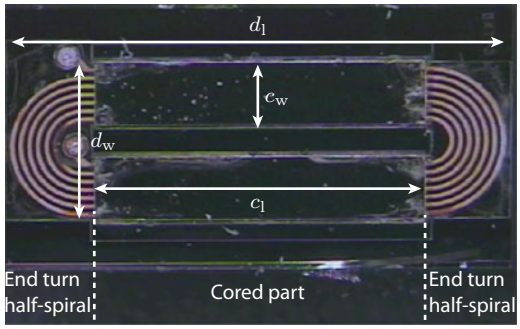

Fig. 5. Photograph of a microfabricated racetrack inductor (see inductor 3 from [6]) used for comparison with the analytical model and the 3-D FEM simulations.

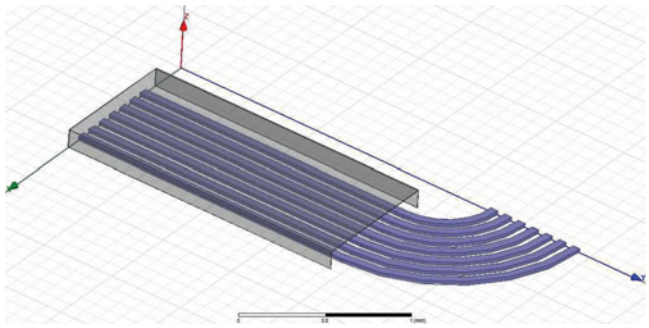

Fig. 6. Three-dimensional FEM simulation setup of the inductor shown in Fig. 5. Three symmetrical planes—one for each axis pair—are inserted to reduce the computational effort by a factor of 8 compared to a full simulation setup without symmetrical planes.

All three inductors use the soft magnetic thin-film permalloy $\mathrm{Ni_{45}Fe_{55}}$ as core material. This material has resistivity $\rho_{\mathrm{c}} = 45\,\mu\Omega \cdot \mathrm{cm}$ and relative permeability $\mu_{\mathrm{c}} = 280$ for inductors 1 and 2 whereas $\mu_{\mathrm{c}} = 250$ for inductor 3. The difference in μ_{c} is due to the shape anisotropy effect, which influences the relative permeability as a function of the aspect ratio $c_{\mathrm{l}}/c_{\mathrm{w}}$. The parameters describing the hysteresis losses are $K_{\mathrm{h}} = 300$ and $b = 1.73$, and they include excess losses in the magnetic material. The saturation flux density is $B_{\mathrm{sat}} = 1.6\,\mathrm{T}$.

Table II lists the buck converter specifications and geometrical parameters with which each inductor has been designed, and it presents the calculated, simulated, and reported results. As can be seen, the analytical inductance calculations from (22) fit the simulated and reported values well. The calculated dc resistances using (23) fit the simulated values well; however, the reported dc resistances for inductors 2 and 3 deviate slightly from the calculations and simulations. The ac winding resistance calculations from (25) are seen to deviate from the simulated resistances since the 1-D field approximation inside the winding window yields limited accuracy. The dc copper loss dominates over the ac copper loss in all three inductors considered and thus

TABLE II
COMPARISON OF CALCULATED, SIMULATED, AND REPORTED RESULTS FOR THREE MICROFABRICATED RACETRACK INDUCTORS

Specifications		**Unit**	**Inductor 1**			**Inductor 2**			**Inductor 3**		
$V_{\rm in}$	Input voltage	V		1.8			3.0			3.6	
$V_{\rm out}$	Output voltage	V		1.12			1.5			1.2	
$I_{\rm out}$	Output current	mA		70			125			250	
$P_{\rm out}$	Output power	mW		78.4			188			300	
PAR	Peak-to-average ratio	–		1.9			1.6			1.3	
N	Number of turns	–		5			5			7	
$t_{\rm w}$	Winding width	µm		80			52			50	
$t_{\rm t}$	Winding thickness	µm		50			28			50	
$t_{\rm s}$	Winding spacing	µm		50			10			50	
$c_{\rm w}$	Core width	µm		750			335			850	
$c_{\rm t}$	Core thickness	µm		4.2			4.2			4.2	
$c_{\rm l}$	Core length	µm		2300			1400			3850	
$d_{\rm h}$	Device height	µm		170			100			100	
$d_{\rm w}$	Device width	µm		1800			800			2000	
$d_{\rm l}$	Device length	µm		4130			3120			5760	
A	Inductor area	$\rm mm^2$		7.4			2.4			11.7	
α	Power density	$\rm mW/mm^2$		10.5			78.3			25.6	
Performance		**Unit**	**Calc.**	**Sim.**	**[4]**	**Calc.**	**Sim.**	**[5]**	**Calc.**	**Sim.**	**[6]**
$L_{\rm core}$	Inductance of cored part	nH	92	97	–	102	112	–	262	253	–
$L_{\rm t,core}$	Winding inductance of cored part	nH	28	30	–	19	19	–	63	69	–
$L_{\rm spiral}$	Winding inductance of end turns	nH	47	48	–	30	32	–	169	159	–
L	Total inductance	nH	167	175	160	151	163	150	494	481	440
$R_{\rm dc}$	DC winding resistance	mΩ	169	180	191	279	297	400	529	576	500
$f_{\rm s}$	Switching frequency	MHz	20	19	20	30	31	30	17	17	20
$R_{\rm ac}$	AC winding resistance	mΩ	249	344	–	315	538	–	765	882	–
$P_{\rm t}$	Total copper losses	mW	1.1	1.3	1.7	4.8	5.6	9.8	33.8	36.7	31.8
$P_{\rm h}$	Core hysteresis losses	mW	1.7	1.1	1.7	3.5	2.3	4.3	2.4	1.5	4.0
$P_{\rm e}$	Core eddy current losses	mW	2.1	1.8	2.5	8.3	7.2	7.6	2.3	2.3	4.0
$P_{\rm loss}$	Total inductor losses	mW	4.9	4.2	5.9	16.6	15.1	22.1	38.5	40.5	39.8
η	Efficiency	%	94.1	94.9	93	91.9	92.6	89.5	88.6	88.1	88.3

the deviation in $R_{\rm ac}$ has minor effect on the overall efficiency estimation. Inspection of the 3-D FEM simulation results shows that the current density in the core resembles the current density in a bus bar as assumed in (31). Thus, the calculated eddy current losses match the simulated and reported values well.

V. CORED RACETRACK INDUCTOR PARETO OPTIMIZATION

An optimization procedure of cored racetrack inductors is developed. It outputs the efficiency and power density Pareto front using the accurate inductor current analysis from Section II and the analytical cored racetrack inductor model from Section III. The presented optimization procedure is a further development of [10], and it includes magnetic material for cored racetrack inductors. A flowchart describing the procedure setup and processing steps is shown in Fig. 7. The optimization procedure inputs are the buck converter specifications and the design space $\boldsymbol{X}$ containing m cored racetrack inductors. Each set $x_i \in \boldsymbol{X}$, where $i = \{1, 2, \ldots, m\}$, contains the geometrical parameters of the ith racetrack inductor design defined in Table I. Efficiency and power density for each set are determined, and the Pareto front is plotted when all sets in the design space have been processed.

The optimization procedure has been implemented in a MATLAB script, which, within a much shorter time than using a 3-D FEM simulator, accurately estimates the efficiency and power density of a large number of inductor designs. This can be used to select the best inductor design for given buck converter specifications based on an optimum tradeoff between efficiency and power density. The selected optimum inductor design may thereafter be implemented in an FEM simulator for fine tuning of the geometrical parameters.

A. Case Study

The optimization procedure is exemplified in a case study, where Table III outlines the buck converter specifications and geometrical parameters that define the design space.

The distance from the winding to the core side wall is assumed to equal $t_{\rm s}$; hence, the core width using Fig. 4 is obtained using $c_{\rm w} = Nt_{\rm w} + (N+1)t_{\rm s} + 2c_{\rm t}$. Designs where $c_{\rm w} > 1500\,\mu$m are omitted. The distance between the two cores is assumed to equal $2(t_{\rm w} + t_{\rm s})$ for this case study; hence, $d_{\rm w} = 2(c_{\rm w} + t_{\rm w} + t_{\rm s})$ and $d_{\rm l} = c_{\rm l} + d_{\rm w} - 2(t_{\rm s} + c_{\rm t})$. The vertical distance between the winding and core is assumed to be $t_{\rm s}$; hence, the device height is obtained using $d_{\rm h} = 2(t_{\rm s} + c_{\rm t})$. The winding thickness maximum limit of $60\,\mu$m is due to the maximum plating mold thickness that can be reliably formed using photo resist while providing reasonable process yield. An inductor set in the design space is omitted if $t_{\rm w} < t_{\rm t}/2.5$ or $t_{\rm s} < t_{\rm t}/2.5$ due to yield issues in the fabrication process.

The magnetic core material is $\rm Ni_{45}Fe_{55}$ described in Section IV, where anisotropic effects are neglected, and the relative permeability is $\mu_{\rm c} = 280$ regardless of the inductor aspect ratio. Transistor switching losses are not included in the model, since the buck converter is operated in BCM where switching

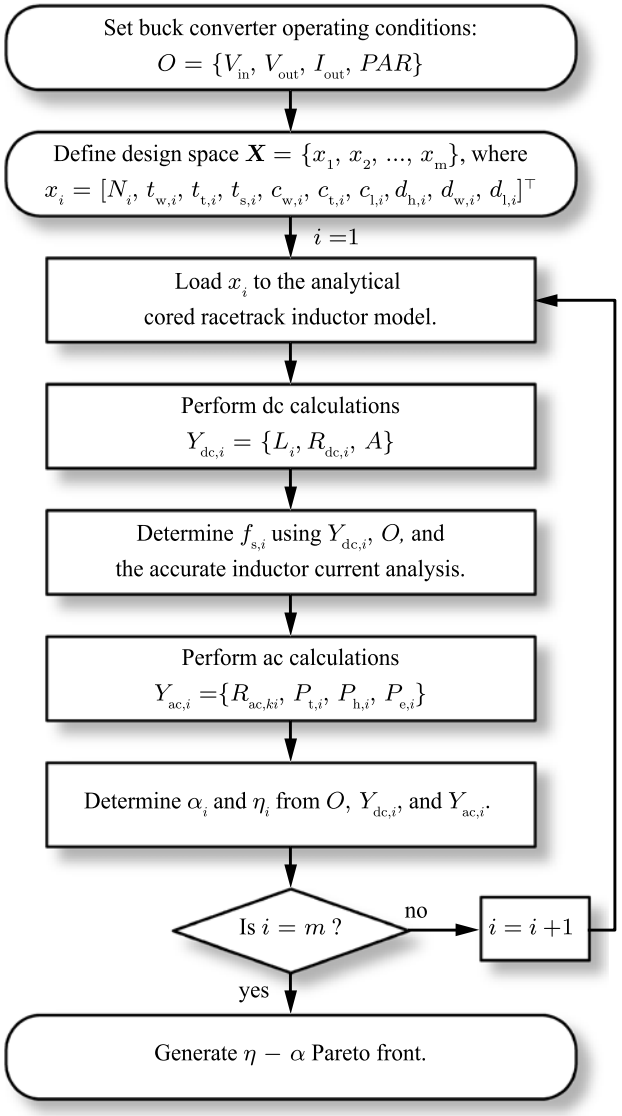

Fig. 7. Flowchart of the cored racetrack inductor optimization procedure, which outputs the $\eta - \alpha$ Pareto front.

TABLE III
BUCK CONVERTER SPECIFICATIONS AND GEOMETRICAL PARAMETER RANGES DEFINING THE CORED RACETRACK INDUCTOR DESIGN SPACE FOR THE CASE STUDY

Specifications	Unit	Value	
V_{in}	V	1.8	
V_{out}	V	0.9	
I_{out}	mA	250	
PAR	–	PAR_{BCM}	
Geometrical parameter	**Unit**	**Minimum**	**Maximum**
N	–	1	8
t_w	µm	10	1500
t_s	µm	10	100
t_t	µm	10	60
c_l	µm	1000	9000
c_t	µm	1	9

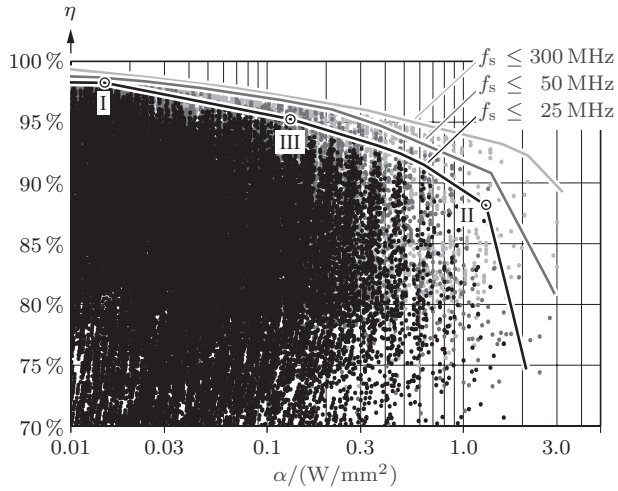

Fig. 8. Resulting Pareto fronts for three different switching frequency limits from the optimization procedure applied on the cored racetrack inductor design space of the case study.

losses are low. Hence, for each cored racetrack inductor design, the switching frequency is calculated numerically using (10). An inductor design is omitted if the resulting $\mathrm{PAR_{BCM}}$ violates (14) or if $B_{pk} > B_{sat}$.

The evaluated efficiencies and power densities of the cored racetrack inductors in the case study design space are mapped to the $\eta - \alpha$ plane as shown in Fig. 8. The Pareto front is constructed from the designs that achieve the highest efficiencies for a given power density. Three Pareto fronts with different switching frequency limits are shown in grayscale highlighting the inductor's efficiency and power density improvement achieved by increasing the switching frequency.

Three different cored racetrack inductor designs on the Pareto front for $f_s < 25$ MHz are highlighted in Fig. 8, and their geometrical parameters and evaluated performances are listed in Table IV. The very high efficiency design on the Pareto front ([I]: $\eta = 98.3\%$, $\alpha = 14$ mW/mm^2) exhibits the lowest power density value considered; the core width is at the maximum limit resulting in wide windings that reduce the copper losses at the cost of increased area. The minimum core thickness and core length facilitate low core losses.

The very high power density design ([II]: $\eta = 88.2\%$, $\alpha = 876$ mW/mm^2) exhibits the lowest efficiency of the designs on the Pareto front; the number of turns and the winding dimensions are low resulting in low area at the cost of increased copper losses. The core thickness of 3 μm increases the inductance to ensure a switching frequency below 25 MHz at the cost of increased eddy current losses. The power loss density is $\alpha_{loss} = 117$ mW/mm^2. This is less than typical power loss densities of advanced microprocessor systems, which can be more than 500 mW/mm^2. Thus, the realization of the highest power density design is feasible.

The third highlighted design on the Pareto front ([III]: $\eta = 95.2\%$, $\alpha = 107$ mW/mm^2) is included to exemplify a tradeoff between the very high efficiency design and the very high power density design.

TABLE IV
GEOMETRICAL PARAMETERS AND EVALUATED PERFORMANCES OF THE THREE HIGHLIGHTED CORED RACETRACK INDUCTOR DESIGNS ON THE PARETO FRONT FOR SWITCHING FREQUENCIES BELOW 25 MHZ

Geometrical parameter	Value	Output parameter	Calculated value
[I] – Very high efficiency Pareto design:			
N	4	L	41.7 nH
t_w	300 μm	f_s	21.6 MHz
t_t	60 μm	P_t	3.0 mW
t_s	40 μm	$P_\mathrm{h} + P_\mathrm{e}$	0.9 mW + 0.1 mW
c_l	1000 μm	η	98.3%
c_t	1 μm	α	14 mW/mm^2
[II] – Very high power density Pareto design:			
N	2	L	40.5 nH
t_w	20 μm	f_s	22.2 MHz
t_t	20 μm	P_t	16.6 mW
t_s	10 μm	$P_\mathrm{h} + P_\mathrm{e}$	5.5 mW + 8.0 mW
c_l	1000 μm	η	88.2%
c_t	3 μm	α	876 mW/mm^2
[III] – High efficiency and high power density Pareto design:			
N	3	L	38.6 nH
t_w	50 μm	f_s	23.3 MHz
t_t	70 μm	P_t	7.5 mW
t_s	20 μm	$P_\mathrm{h} + P_\mathrm{e}$	3.3 mW + 0.5 mW
c_l	2000 μm	η	95.2%
c_t	1 μm	α	107 mW/mm^2

VI. CONCLUSION

The analytical model of microfabricated racetrack inductors presented in this paper facilitates a thorough inductor Pareto optimization with respect to efficiency and/or power density. The analytical model estimates the inductance, the copper losses, and the core losses of cored racetrack inductors, and the impact of the losses on inductor current is taken into account to improve the accuracy of the predicted efficiency. The model can be used to accurately characterize the efficiency and power density of a given microfabricated inductor design to be used in buck converters for PSiP and PwrSoC systems, and it features high evaluation speed compared to FEM simulations. The analytical model is verified using 3-D FEM simulations, and a comparison of calculated, simulated, and reported results of three manufactured cored racetrack inductors is carried out showing good agreement between predicted and reported performance.

The $\eta - \alpha$ Pareto front, which shows the efficiency and power density limits of realizable inductors, is obtained by evaluating a large number of inductor designs. The resulting Pareto front facilitates the selection of the two most suitable inductor designs: either an inductor with high efficiency ($\eta = 98.3\%$, $\alpha = 14$ mW/mm^2) or an inductor with high power density ($\eta = 88.2\%, \alpha = 876$ mW/mm^2) for a maximum switching frequency of 25 MHz.

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