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Analytical Loss Model for Three-Phase 1200V SiC MOSFET Inverter Drive System Utilizing Miller Capacitor-Based dv/dt-Limitation

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ABSTRACT Next-generation Variable Speed Drive (VSD) systems utilize SiC MOSFETs to achieve both high efficiency through reduced bridge-leg losses and high power density through an order-of-magnitude increase in switching frequency or reduction of the DC-link capacitance. These systems, however, must contend with the high voltage slew rate ($\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$) of these next-generation power semiconductors, especially in the context of protecting the motor from partial discharge phenomena, surge voltages from cable reflections, and unequal distribution of the voltage across motor windings. We assess the attractiveness of an external Miller capacitor across the bridge-leg power semiconductors to limit the maximum voltage slew rate in a system. To evaluate this technique, we propose a maximum $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ model, finding that the maximum turn-on slew rate occurs at Zero-Current Switching (ZCS) with an increase in $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ as the device junction temperature increases. During the turn-off transition, the applied $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ saturates at a particular current. We then find a switching loss model, arriving at a piecewise-linear dependence of bridge-leg switching losses on current under $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$-limited conditions, a finding that runs counter to the widely-utilized quadratic current dependence. The proposed models are validated on a SiC MOSFET bridge-leg designed for a 10 kW 800 V DC-link Variable Speed Drive (VSD) system with a switching frequency of 16 kHz, where the Miller capacitor-based technique achieves lower losses (for the same maximum $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$) than a gate resistor-only $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ limiting approach. This SiC MOSFET bridge-leg achieves peak calculated bridge-leg efficiencies of 99.2 % for a $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ limitation of 10 V/ns and 99.4 % for a limit of 15 V/ns.

INDEX TERMS Power MOSFET, wide band gap semiconductors, silicon carbide, variable speed drives.

I. INTRODUCTION

Variable Speed Drive (VSD) inverter systems are critical for the efficient electrification of the mobility, manufacturing, and logistics sectors, with VSD-driven industrial motors projected for over 30 % of electricity growth to 2040 [1]. More broadly, VSD-driven motors are rapidly replacing single-speed motors for higher efficiency, better control, and lower operating costs.

For the switching power semiconductor devices, state-of-the-art VSD inverters use Insulated Gate Bipolar Transistors (IGBTs), often with a blocking voltage of 1200 V, accompanied by anti-parallel freewheeling diodes. IGBTs incur high switching losses due to the bipolar on-state carriers, and these switching losses limit the switching frequency of industrial drives that utilize IGBTs to 4 kHz to 16 kHz, typically.

With the most recent commercialization and adoption of Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), these switching frequencies can be extended by nearly an order-of-magnitude, enabling full sine-wave filtering [2], [3] and higher performance on both power density and efficiency (including at partial load [4]), simultaneously. Relative to IGBTs with the same blocking voltage, SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) incur significantly lower switching losses due to the unipolar carrier characteristic, lower conduction

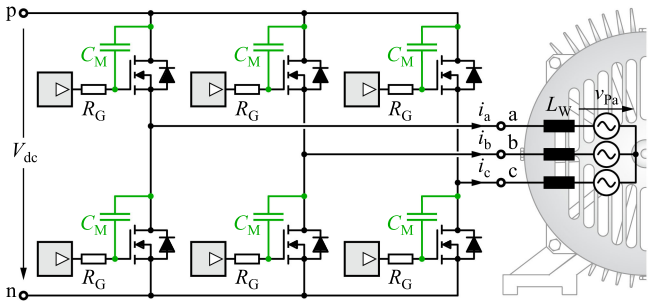

FIGURE 1. Three-phase Variable Speed Drive (VSD) PWM inverter system employing SiC MOSFETs with gate control — in this case, a gate driver with gate resistor R_G and explicit Miller feedback capacitor C_M — to limit the voltage slew rate applied to the motor terminals *a*, *b*, *c* and prevent partial discharge phenomena and/or progressive insulation aging.

losses due to fundamental material improvements [5], [6] and the lack of an on-state voltage drop in forward or reverse conduction, and support synchronous rectification. Further, the internal body diode of the MOSFETs eliminates the need for external freewheeling diodes. Overall, SiC MOSFETs support smaller overall chip areas, lower conduction and switching losses, and higher switching frequencies for smaller high-frequency motor losses and lower DC-link capacitance for given switching frequency voltage ripple.

These next-generation VSD systems (like the three-phase VSD shown in Fig. 1) must contend, though, with new complications introduced by the faster switching speeds of SiC MOSFETs. High slew rate voltages, or dv/dt values, at the output of the VSD can lead to partial discharge phenomena and progressive insulation aging of the motor [7], [8], unequal distribution of the voltage across the motor windings, and/or surge voltages from reflections in long motor cables. VSD systems must meet critical standards that protect industrial motors from these deleterious effects [9], [10]. One method of dv/dt-limiting is to implement a full sine-wave LC-filter to limit the dv/dt applied to the motor, but this approach carries the familiar drawbacks of additional high-power passive components: volume, design and realization effort, and cost [11]. Alternatively, the voltage slope applied to the motor can be limited directly through other techniques, but with industrial IGBTs feature switching speeds of only 1 V/ns to 5 V/ns [12] while SiC MOSFETs can achieve slew rates of up to 100 V/ns, a deeper exploration of dv/dt-limiting concepts is required.

The most straightforward approach to limit the dv/dt applied to the motor is with a dv/dt-filter, where an LC-filter with a resonant frequency above the switching frequency is implemented between the switching stage and the motor terminals (or the cable). Different passive filter implementations to limit dv/dt applied to the motor include a damped LCR-filter [13] or an undamped LC-filter with Diode-Resistor-Capacitor (DRC) damping [14], which utilizes a pair of diodes but does not require active control. Combined Differential-Mode (DM) and Common-Mode (CM) filters, further, feature capacitors connected to the DC-link rails [15], [16] and limit both bearing currents [17] and radiated electromagnetic emissions [18]. Finally, as a combination of a passive filter and an active control scheme, an undamped LC-filter can be combined with an adaptive switching cycle to enforce resonant transitions without overshoot [19], [20]. Each of these concepts reduces the filter requirements relative to a bulky full sine-wave filter, but still require the design, implementation, and realization of multiple passive components that diminish the benefits of the adoption of SiC MOSFETs in VSD systems.

Alternatively, the dv/dt applied to the motor can be limited through gate drive control of the MOSFET directly. The simplest approach is to increase the resistance of the gate resistor to increase the gate time constant [21] (including with multiple discrete gate resistance values [22]), leading to slower switching transients and higher switching losses but lower dv/dt slew rates. An improvement to this approach, as shown in Fig. 1, is to implement a conventional gate driver with gate resistor and an additional Miller feedback capacitor connected between the gate and drain of each MOSFET [23], [24]. The additional Miller capacitor influences the transient of the switch-node voltage but, unlike an oversized gate resistor, does not have a meaningful effect on the gate time constant. A larger Miller capacitance prevents, *a priori*, fast voltage transients instead of filtering them out, linearizes the gate voltage (especially valuable for Gallium Nitride (GaN) [24]), and is small in both capacitance value and size. Further, unlike alternative gate drive modifications that require additional active circuits [25], [26] or closed-loop concepts to control dv/dt [27]–[29], the Miller capacitor concept is simple, compact, and straightforward to implement.

Despite the performance promised by the Miller capacitor concept for next-generation VSD systems, there is limited literature on the optimal Miller capacitor configuration for SiC MOSFETs [25], with more for GaN-based systems [24], [26], [30]. None of this prior work, however, includes *(a)* accurate modeling and analysis for SiC MOSFETs or *(b)* the effect of the Miller capacitor on overall system performance beyond dv/dt, most notably on switching losses and the shorter dead-time (and lower diode conduction losses) supported by the faster gate time constant.

Motor-integrated VSD systems support dv/dt values as high as 10 V/ns to 15 V/ns, as no cable reflections need to be considered with direct motor integration. In [31], we analyzed a number of approaches to meet these dv/dt requirements in an $V_{dc} = 800$ V VSD system, and found the Miller capacitor solution promised the best analytical performance. In this paper, we extend this work into a complete switching loss model for SiC MOSFETs with an external Miller capacitor, first revisiting the switching behavior of a bridge-leg and experimentally validating the effect of the Miller capacitor on the switching transient (Section II). From there, we find a parametric gate drive model to enable the selection of a gate resistor and Miller capacitor combination to achieve the desired voltage slew rate during turn-on and turn-off, and propose and validate a loss model for the switching losses

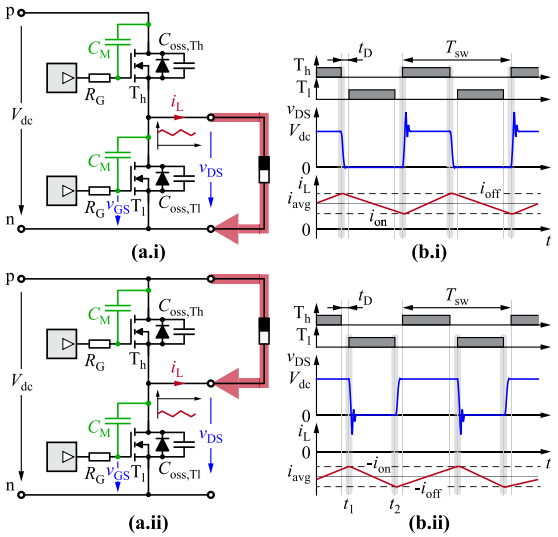

FIGURE 2. (a) Half-bridge power semiconductor bridge-leg comprising a high-side T_h and a low-side transistor T_l with individual gate drives and external Miller feedback capacitors C_M. (b) Characteristic bridge-leg waveforms: gate drive signals, switch-node voltage v_{DS}, and load current i_L. (i) Strictly positive load current i_L and (ii) a strictly negative load current i_L, both of which occur during a fundamental period.

across these voltage slew rates that unifies turn-on and turn-off switching loss models under soft- and hard-switching conditions (Section III). In Section IV, these switching losses are validated on a 10 kW VSD, where the inverter losses are derived for sinusoidal current and then verified by measurements with both an external Miller capacitor and under conventional operation, achieving a peak bridge-leg efficiency of 99.4 % at a 15 V/ns slew rate limitation. In Section V, we provide a design approach for implementing $\mathrm{d}v/\mathrm{d}t$-limited VSD systems. Section VI concludes the paper and points to further improvements for Wide-Bandgap (WBG)-enabled, motor-integrated, next-generation VSD systems.

II. SWITCHING BEHAVIOR WITH AN EXTERNAL MILLER CAPACITOR

A. SWITCHING BEHAVIOR EXPLANATION

To understand the external Miller capacitor (C_M) approach under investigation, we first must analyze the effect of C_M on the switching transient. To investigate this switching behavior, we consider a half-bridge configuration with a high-side T_h and a low-side transistor T_l connected to a DC-link with the voltage V_{dc} and driving an ohmic-inductive load with both positive and negative load currents i_L (such that either a strictly positive or strictly negative current is seen during a switching cycle). In Fig. 2, the half-bridge power semiconductors are each shown with a gate driver and an explicit Miller feedback capacitor C_M.

For a positive load (and switched) current, the load is connected to the negative DC-link rail, as shown in Fig. 2(a.i). When T_h is conducting, the load current i_L is increasing (under $v_{DS} = V_{dc}$) until the switching transition occurs, at which time T_h is turned-off and $i_L = i_{off}$ (Fig. 2(b.i)). This triggers a Zero-Voltage Switching (ZVS) turn-on transition [32] for the low-side switch T_l and a ZVS turn-off transition for the high-side switch T_h, where the effective switch-node capacitance is the combination of the output capacitances of the high-side $C_{oss,Th}$ and low-side transistor $C_{oss,Tl}$ and *both* Miller capacitors C_M (as both switches are off). This switch-node capacitance defines the slope as the switch-node voltage v_{DS} discharges from V_{dc} to zero, at which point the voltage transient ends and the load current flows through the low-side diode.

After the enforced dead-time t_D, the low-side transistor is turned-on and the load current commutates from the diode to the MOSFET channel (note that the low-side transistor, under a strictly positive current condition, cannot trigger any transitions and only enables synchronous rectification). While the low-side switch is on, the current decreases ($v_{DS} = 0$ V) until T_l is turned-off again at $i_L \approx i_{on} > 0$ A and the current commutates back from the channel to the low-side diode. Again, after an enforced dead-time t_D, T_h is turned on and a hard-switching event occurs $i_L = i_{on}$. This hard-switching event discharges $C_{oss,Th}$ and the high-side C_M while charging $C_{oss,Tl}$ and the low-side C_M to bring the switch-node voltage v_{DS} from zero to V_{dc}, and this fast transient typically causes a voltage overshoot caused by an oscillation between the equivalent output capacitance and the commutation loop inductance.

Under a negative load current, where the load is equivalently connected to the positive DC-link rail (Fig. 2(a.ii)), the behavior of T_h and T_l are reversed, with the high-side device transistor turned-on under ZVS and the low-side transistor hard-switched at turn-on, as shown in Fig. 2(b.ii).

B. EXPERIMENTAL VALIDATION

To validate our understanding of the effect of the external Miller capacitance on the switching transition, we construct a half-bridge using two next-generation low-$R_{DS,on}$ SiC MOSFETs (*C3M0016120K* [33]) and a gate driver with an output clamp variant (for enhanced noise immunity) [34] that drives the transistors at the maximum positive ($V_{G,on} = 15$ V) and minimum negative ($V_{G,off} = -4$ V) gate drive voltages. The Miller capacitor is implemented with a Mica capacitor [35], which has low dissipation factor, linear capacitance, and is rated for transients up to 20 V/ns [35]. Turn-on and turn-off behavior for the half-bridge is measured under Double-Pulse Test (DPT) conditions, and we define the rise time t_r and fall time t_f of v_{DS} as the time interval between 10 % and 90 % (or 90 % and 10 %) of the DC-link voltage V_{dc} with a resulting voltage slope $\mathrm{d}v_{DS}/\mathrm{d}t = 0.8\,V_{dc}/t_r$ or $\mathrm{d}v_{DS}/\mathrm{d}t = 0.8\,V_{dc}/t_f$ for $V_{dc} = 800$ V.

Firstly, we measure and analyze the behavior for $R_G = 0\,\Omega$ without a Miller capacitor ($C_M = 0$ pF), as reported in Fig. 3. The turn-on transition occurs under Zero-Current Switching (ZCS) conditions ($I_{on} = 0$ A) and the measured slew rate is $\mathrm{d}v_{DS}/\mathrm{d}t = 60$ V/ns, with the turn-off transitions at $I_{off} = 5$ A and $I_{off} = 40$ A achieving voltage slew rates of 6.1 V/ns and

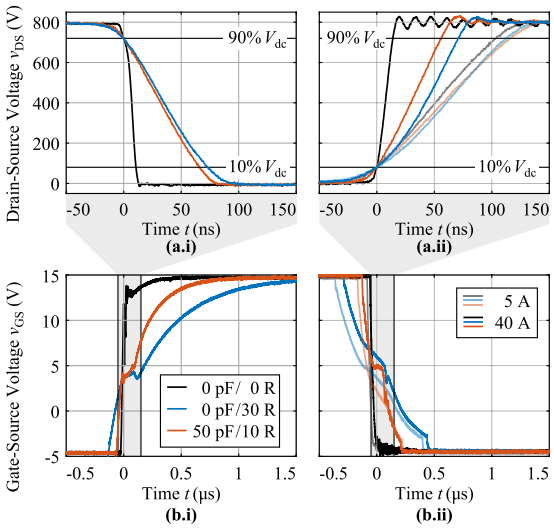

FIGURE 3. **(a) Measured drain-source voltage v_{DS} and (b) measured gate-source voltage v_{GS} of a *C3M0016120K* low-side transistor T_1 (see Fig. 2(a)), during (i) turn-on at zero current (t_1 in Fig. 2(a)) and (ii) turn-off at 5 A (faded lines) and at 40 A (t_2 in Fig. 2(a)) for different gate drive parameter combinations R_G and C_M. The change of the drain-source voltage is nearly linear between 10 % and 90 % (or 90 % and 10 %) of V_{dc} and is further linearized with the external Miller capacitor C_M. The turn-on voltage slew rate at zero current results with 8.8 V/ns for both gate drive parameter combinations of $R_G = 30\,\Omega$, $C_M = 0$ pF, and $R_G = 10\,\Omega$, $C_M = 50$ pF. In contrast, the turn-off voltage slew rate at $I_{off} = 40$ A differs for the two cases and results with 9.0 V/ns for $R_G = 30\,\Omega$, $C_M = 0$ pF and 11.5 V/ns for $R_G = 10\,\Omega$, $C_M = 50$ pF. The Miller plateau becomes visible at reduced voltage slopes, with non-zero values of R_G and C_M.**

45 V/ns, respectively. We might expect the voltage slew rate to increase by a factor of 8 with an 8× increase in current; instead, we find an increase of 7.4 and encounter the saturation of $\mathrm{d}v_{DS}/\mathrm{d}t$ under high-current switching conditions that was reported in [36]. For all of the measured turn-on and turn-off transitions in Fig. 3, the drain-source voltage transitions nearly linearly between 10 % and 90 % (or 90 % and 10 %), justifying the previously-introduced derivation of voltage slope based on the rise (or fall) time.

The power loop inductance can be estimated from the oscillation frequency of the commutation loop, which is measured at 71 MHz in Fig. 3(a.ii) and corresponds to 20 nH, which originates primarily from the parasitic inductances of the two TO-247 packages. Even with a current slew rate of 2 A/ns, a reasonable value for the gate resistors considered here, the inductive voltage drop is only 40 V — less than 5 % of V_{dc}, and safely neglected in the subsequent analysis.

Next, the gate resistor is increased to $R_G = 30\,\Omega$ while maintaining zero Miller capacitance ($C_M = 0$ pF), which slows the turn-on voltage slew rate significantly to 8.8 V/ns. We find, perhaps unexpectedly, a negligible effect on the turn-off slew rate at 5 A (measured at 5.7 V/ns), but the high-current turn-off transient slew is reduced from 45 V/ns to 9.0 V/ns. The gate transient, as we see in Fig. 3(b), is also much slower relative to the reference case with $R_G = 0\,\Omega$.

Finally, an arbitrary Miller capacitance of $C_M = 50$ pF is added to the half-bridge, and a much-lower gate resistance

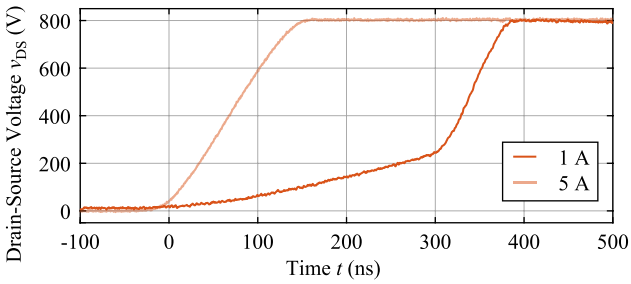

FIGURE 4. **Measured drain-source voltage v_{DS} for a turn-off current of $I_{off} = 1$ A, causing an incomplete ZVS transition, and a turn-off current of 5 A with a complete ZVS transition. Both configurations have $R_G = 10\,\Omega$ and $C_M = 50$ pF. After the dead time $t_D = 400$ ns has passed, the complementary transistor turns on and enforces a rapid voltage transient similar to ZCS conditions at a reduced voltage difference. This case is inherently included in the selected half-bridge configuration and the $\mathrm{d}v_{DS}/\mathrm{d}t$ limitation is still met.**

of $R_G = 10\,\Omega$ is selected to achieve the $\mathrm{d}v_{DS}/\mathrm{d}t$ at turn-on as for the $R_G = 30\,\Omega$ case (Fig. 3(a.i)). The gate transient is now faster than for the large gate resistance case (although still slower than for the $R_G = 0\,\Omega$, $C_M = 0$ pF case, as expected), and we again find little effect on the turn-off transition at 5 A (measured at 5.6 V/ns) but a large influence on the high-current transition (slew measured at 11.5 V/ns at 40 A).

At low current levels during turn-off, the rise time may become longer than the dead time t_D, which is selected to minimize the diode conduction losses. Under these conditions, a partial hard turn-on event occurs, causing an incomplete ZVS transition (see [32] for a more complete discussion). During this turn-off transition, the gate-source voltage decays to a negative voltage during the dead time, and, when the second transistor turns on after the dead time (but before the transition is complete), a ZCS-like transition occurs for the remaining voltage difference, with a fast $\mathrm{d}v_{DS}/\mathrm{d}t$ transient. A measured waveform for this event is shown in Fig. 4 (for $R_G = 10\,\Omega$, $C_M = 50$ pF) at a turn-off current of 1 A and a dead time of 400 ns. Because the low current (which must be the case to cause this condition) causes a slow transition during the dead-time, the slew rate limitation is still met under these conditions.

We see, then, that the Miller capacitor slows the voltage transient, as desired, and that the Miller capacitor can achieve different turn-on and turn-off voltage slew rates with the same gate resistor. For the same drain-source voltage slope, the Miller capacitance solution has a faster gate transition than a gate resistor alone, which could be beneficial. Most importantly, though, we find a significant dependence of the voltage slew rates $\mathrm{d}v_{DS}/\mathrm{d}t$ on the switched current, an influence beyond the gate drive parameters R_G and C_M alone, and this warrants a deeper investigation.

C. VOLTAGE SLEW RATE MEASUREMENTS ACROSS SWITCHED CURRENT

To understand the current dependence of the slew rate, the voltage slew rate $\mathrm{d}v_{DS}/\mathrm{d}t$ is measured across switched current with and without the Miller capacitor. We sweep the

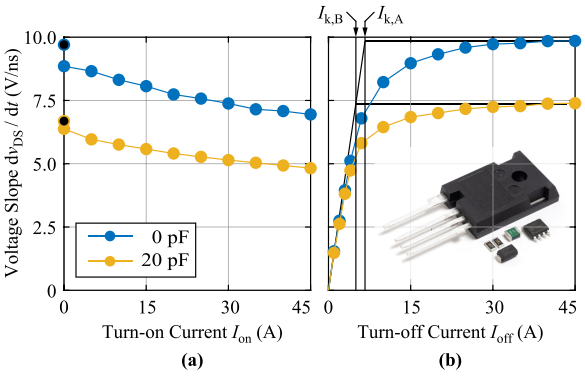

FIGURE 5. dv_{DS}/dt **measurements from Double-Pulse Test (DPT) experiments on a *C3M0016120K* bridge-leg over switched current from 0 A to 45 A for (a) turn-on and (b) turn-off, with $R_{G,on} = 30.1\,\Omega$, $R_{G,off} = 24.3\,\Omega$ and two different Miller capacitors C_M. The black dots indicate continuous Zero-Current Switching (ZCS) measurements at 100 °C. In (b), the size of the Miller capacitor (green) is compared to the gate drive components (gate driver, turn-on resistor, second resistor with an additional diode to achieve an independent turn-off resistance) and the SiC MOSFET to show the compactness of this solution.**

DPT measurements with switched currents from 0 A to 45 A for *both* turn-on and turn-off currents with gate resistors $R_{G,on} = 30.1\,\Omega$ and $R_{G,off} = 24.3\,\Omega$ and a Miller capacitance, when used, of 20 pF. The results are shown in Fig. 5, alongside an image showing the relative volume contribution of the Miller capacitor, which is negligible compared to the SiC MOSFET and other gate drive components.

At turn-on, we find that dv_{DS}/dt reduces with higher switched turn-on currents I_{on}, with the maximum slope occurring at ZCS ($dv_{DS}/dt|_0$). This aligns with conventional theory with a transconductance g_m, where the Miller voltage increases at higher currents as $v_M = v_{th} + I_{on}/g_m$ and the slew rate goes as $dv_{DS}/dt|_{on} \propto V_{G,on} - v_M$. We also find a temperature dependence by applying continuous switching under ZCS (rather than the DPT) at around 100 °C junction temperature, which is indicated by the black dots in Fig. 5 and achieves higher a dv_{DS}/dt than ZCS under DPT conditions (with a junction temperature near room temperature). The maximum measured voltage slope under turn-on (at the elevated junction temperature) is $dv_{DS}/dt|_0 = 9.8\,V/ns$ without the Miller capacitor and 7.4 V/ns with $C_M = 20\,pF$.

At low turn-off currents and under ZVS, the voltage slew rate dv_{DS}/dt scales with the switched turn-off current I_{off}. At higher switched currents, though, the voltage slope dv_{DS}/dt saturates, replicating the "kink current" I_k behavior found in [36]. The kink current is:

$$I_k = C_{eff} \left.\frac{dv_{DS}}{dt}\right|_0, \tag{1}$$

with $C_{eff} = 2C_{dQ,oss} + 2C_M + C_{par}$ and $C_{dQ,oss}$ as the charge-equivalent capacitance [32] of the transistor between 10 % and 90 % of the DC-link voltage. Without an external Miller capacitance, and considering C_M and any parasitic capacitance C_{par} as negligible compared to $C_{dQ,oss}$, the effective capacitance is $C_{eff} \approx 2C_{dQ,oss} = 666\,pF$ and the kink current is $I_{k,A} = 6.5\,A$. With $C_M = 20\,pF$, the kink current is $I_{k,B} = 4.9\,A$ as a result of the reduced $dv_{DS}/dt|_0$, with these values labeled in Fig. 5 (although the kink current transition from rising slope to saturated is relatively smooth here).

In sum, then, the external Miller capacitance C_M maintains the behavior of the voltage slew rates across current, but reduces dv_{DS}/dt overall and can be used with a gate resistor to achieve the desired voltage slope. That said, the important saturation current characteristic mandates a deeper investigation of the switching behavior during a transition, leading to an analytical model for both dv_{DS}/dt and switching losses for any gate resistance and Miller capacitor combination.

III. DV/DT AND LOSS MODELS

In this Section, we derive a dv_{DS}/dt model to find suitable gate drive configurations (for an arbitrary power semiconductor device) to achieve a desired dv_{DS}/dt and a related switching loss model for determining turn-on and turn-off losses. First, we return to a deeper investigation of the half-bridge during a switching transition to better understand the detailed models derived here.

A. DV/DT MODEL

Fig. 6(a) shows the equivalent half-bridge circuit present during the turn-off and turn-on transition of the low-side switch (T_l in Fig. 2(a)), with the corresponding waveforms shown in Fig. 6(b). Here, we limit our focus to the switch-node voltage transient, with the broader gate and bridge-leg waveforms detailed in [22], [25]. The switching current I_{sw} is assumed positive (hard-switching T_l at turn-on), constant during the switching transition, and with a magnitude greater than the kink current as $I_{sw} > I_k$. The waveforms use a straight-line approximation and C_{DS} represents the charge equivalent output capacitance between the drain and source, including the drain-source capacitance of T_l, the output capacitance of T_h (indicated in the figure only with a free-wheeling diode to which I_{sw} commutates) and any additional parasitic capacitances, such that $C_{DS} = C_{oss,Th} + C_{ds,Tl} + C_{par}$.

1) TURN-OFF TRANSITION

At turn-off (Fig. 6(a.i) and Fig. 6(b.i)), the initial condition is with T_l turned on, such that the gate is charged to $V_{G,on}$. The gate driver applies $V_{G,off}$, and the internal gate-source voltage is reduced and clamped at the Miller voltage $v_{GS,i} = v_M = v_{th} + I_{sw}/g_m$. We assume a strict Miller plateau, such that $v_{GS,i} = v_M$ is strictly true and therefore no current flows to C_{GS}. Through KVL, we can then find $v_M - V_{G,off} = [R_{G,off}(C_M + C_{GD}) + R_{int}C_{GD}]\frac{dv_{DS}}{dt} + R_{G,off}R_{int}C_MC_{GD}\frac{d^2v_{DS}}{dt^2}$. Using the straight-line approximation such that $\frac{d^2v_{DS}}{dt^2} = 0\ V^2/s^2$, we find our model for dv_{DS}/dt during the turn-off transition:

$$\left.\frac{dv_{DS}}{dt}\right|_{off} = \frac{v_M - V_{G,off}}{R_{G,off}C_M + R_{G,off}C_{GD} + R_{int}C_{GD} + \tau_{off}}, \tag{2}$$

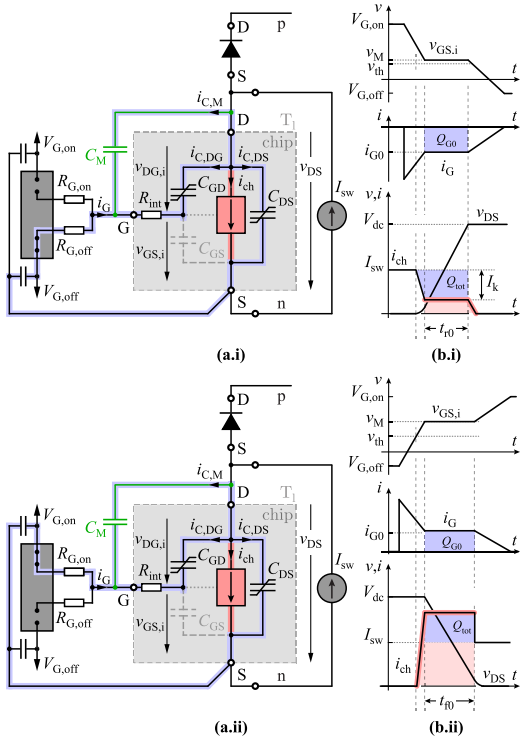

FIGURE 6. **(a) Equivalent circuit of the bridge-leg of Fig. 2(a) during the (i) turn-off and (ii) turn-on switching transitions of T_l for switched current greater than the kink current, or $I_{sw} > I_k$. The upper power transistor is only visualized as the body diode and the shown drain-source capacitance C_{DS} includes the parasitic capacitances $C_{ds,Tl}$, $C_{oss,Th}$, and C_{par}. (b) shows the corresponding time waveforms. The switched current I_{sw} is taken as constant during the turn-off transition (low ripple approximation) and the time behavior of the inner gate-source voltage ($v_{GS,i}$) of T_l is based on a straight-line approximation.**

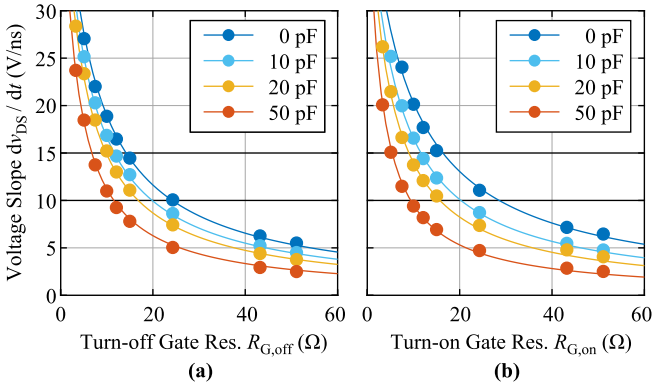

FIGURE 7. **Measured voltage slope for different Miller capacitors and gate resistors for (a) turn-off at 40 A and (b) turn-on at zero current. The proposed model of (2) and (3) is shown overlaid as the solid lines, where we find excellent matching between the model and the measurement. Maximum considered voltage slew rates of 10 V/ns and 15 V/ns are highlighted.**

TABLE 1 **Required Gate Resistors $R_{G,on}$ and $R_{G,off}$ for Different Voltage Slopes and External Miller Capacitor Values**

Gate Resistors $R_{G,on}$, $R_{G,off}$	$\frac{dv_{DS}}{dt}\big\|_0 = 10\,V/ns$	$\frac{dv_{DS}}{dt}\big\|_0 = 15\,V/ns$
$C_M = 0\,pF$	30.1 Ω, 24.3 Ω	15.0 Ω, 15.0 Ω
$C_M = 20\,pF$	16.2 Ω, 16.2 Ω	8.6 Ω, 10.0 Ω
$C_M = 50\,pF$	9.5 Ω, 11.0 Ω	5.2 Ω, 6.8 Ω

with an additional fitting time constant τ_{off} to account for further delays, perhaps inside the semiconductor or the semiconductor package. With no external gate resistor ($R_{G,off} = 0\,\Omega$), the internal gate resistance R_{int} limits the voltage slew rate.

2) TURN-ON TRANSITION

At turn-on (Fig. 6(a.ii) and Fig. 6(b.ii)), T_l is turned off and the gate is therefore charged to $V_{G,off}$. The gate driver applies $V_{G,on}$, and we can follow the same analysis as for the turn-off model — with the important exception that $v_{GS,i} = v_{th}$ because the device is turned-on under ZCS to consider the worst-case dv_{DS}/dt (Fig. 6(b.ii) shows the behavior for a current value I_{sw} different from zero). During turn-on, the voltage slew rate is:

$$\left.\frac{dv_{DS}}{dt}\right|_{on} = \frac{V_{G,on} - v_{th}}{R_{G,on}C_M + R_{G,on}C_{GD} + R_{int}C_{GD} + \tau_{on}}. \quad (3)$$

C_{GD} corresponds to the charge-equivalent gate-drain capacitance. Although the local value (c_{GD}) is voltage-dependent and non-linear, the external Miller capacitor linearizes or even dominates the total gate-drain capacitance. The drain-source voltage change is therefore more linear, and we emphasize again that the Miller capacitor primarily influences the drain-source voltage transient without significant affecting the gate transient.

3) EXPERIMENTAL VALIDATION

We validate the proposed dv_{DS}/dt models in the same half-bridge configuration with four Miller capacitance values ($C_M = [0, 10, 20, 50]$ pF) and several turn-on and turn-off resistors. Turn-off transitions are measured with DPT conditions at 40 A switched current and turn-on transitions are measured with continuous ZCS with a junction temperature of 100 °C.

The results are reported in Fig. 7, with the modeled voltage slope shown as lines and the measured slope as dots. The turn-on model is fit to the measurements with $v_{th} = 6.0\,V$, $C_{GD} = 24.5\,pF$, $R_{int} = 2.2\,\Omega$ and $\tau_{on} = 143\,ps$, and the turn-off model is fit with $v_M = 8.7\,V$, $C_{GD} = 45.7\,pF$, $R_{int} = 2.5\,\Omega$ and $\tau_{off} = 151\,ps$. These parameters are quite similar, as desired, with the large deviation for C_{GD} assumed to originate in the different contribution of C_{GS} between turn-on and turn-off since the Miller plateau is not perfectly flat [37], [38].

The proposal models match the measurements across gate driver circuit values, supporting the selection of suitable gate resistor-Miller capacitor combinations to achieve the desired voltage slew rate in any application. In Fig. 7, our targets of $dv_{DS}/dt|_0 = 10\,V/ns$ and $dv_{DS}/dt|_0 = 15\,V/ns$ are highlighted, with the Miller capacitance and gate resistor values that result in those maximum slew rates summarized in Table 1.

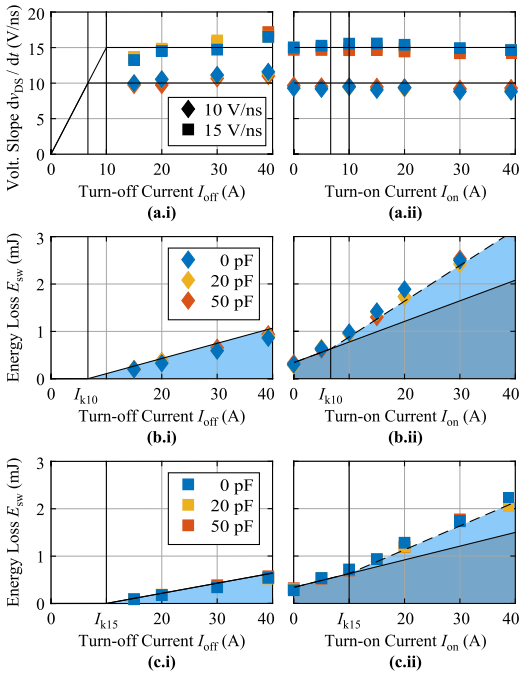

FIGURE 8. (a) Measured voltage slopes dv_{DS}/dt and switching losses for (b) $dv_{DS}/dt|_0 = 10\,V/ns$ and (c) $dv_{DS}/dt|_0 = 15\,V/ns$ at (i) turn-off and (ii) turn-on, verifying the proposed models. Diamonds indicate a maximum slope of $dv_{DS}/dt|_0$ of 10 V/ns (♦) and squares indicate a maximum slope of 15 V/ns (■). In (b.i) and (c.i), turn-off losses (light blue) are directly measured and, subsequently, turn-on losses (dark blue) are extracted from a total loss measurement of (b.ii) and (c.ii) with the turn-off losses known (shown in light blue).

B. DV/DT RELATED LOSS MODEL

1) LOSS MEASUREMENTS

We see in Table 1, then, that different gate drive parameter combinations can achieve the same maximum voltage slew rate, but recall from Fig. 3 that the time-domain behavior can be quite distinct among them. Here, we explore if this degree of freedom can be used to minimize switching losses, and derive a suitable — and novel, for turn-on losses — model for switching losses.

We use the thermal transient measurement method [39] to conduct ZCS-only, turn-off-only, and turn-on and turn-off loss measurements for all six sets of gate drive parameters that achieve our maximum voltage slew rates in Table 1. These results are given in Fig. 8 across turn-on and turn-off currents, where we report the loss measurements alongside the measured dv_{DS}/dt for a single transition (Fig. 8(a)) under continuous half-bridge operation (Fig. 8(b) and Fig. 8(c)). We see, upon a quick examination, that the losses depend, to first order, upon dv_{DS}/dt but that the tradeoff between gate resistor and Miller capacitor value has almost no influence, and we move to find a suitable loss model that explains this behavior.

2) TURN-OFF LOSS MODEL

A detailed turn-off loss model is given in [36], and only a short summary is given here.

For currents below the kink current, only the resonant charging-discharging C_{oss}-losses [40] occur during turn-off, denoted as E_0. Above the kink current, the voltage slew rate dv_{DS}/dt saturates and a portion of the load current flows through the channel, resulting in losses of $E_0 + k_{off}(I_{off} - I_k)$, with $k_{off} = \frac{1}{2} V_{dc}^2 / \frac{dv_{DS}}{dt}|_0$. Turn-off switching losses are, then:

$$\left.\frac{dv_{DS}}{dt}\right|_{off} = \begin{cases} \frac{I_{off}}{I_k}\left.\frac{dv_{DS}}{dt}\right|_0 & \text{if} \quad I_{off} < I_k \\ \left.\frac{dv_{DS}}{dt}\right|_0 & \text{if} \quad I_{off} \geq I_k \end{cases} \tag{4}$$

$$E_{sw,off}(I_{off}) = \begin{cases} E_0 & \text{if} \quad I_{off} < I_k \\ E_0 + k_{off}(I_{off} - I_k) & \text{if} \quad I_{off} \geq I_k \end{cases} \tag{5}$$

with $I_{off} > 0\,A$. Note that the gate current flows as $i_G = -i_{C,M} - i_{C,DG}$ (with the gate charge related to the Miller plateau $Q_{G0} = i_{G0} t_{r0}$), which corresponds to the charge requirements of C_M and C_{GD} and must be absorbed by the gate driver itself. For our application here, we apply (1) and find $I_{k10} = 6.6\,A$ for $dv_{DS}/dt|_0 = 10\,V/ns$ and $I_{k15} = 10\,A$ for $15\,V/ns$.

3) TURN-ON LOSS MODEL

During the turn-on transition, the charge corresponding to the total capacitance $Q_{tot} = Q_{oss}(V_{dc}) + (C_M + C_{par}/2)V_{dc}$ is charged/discharged via the channel, resulting in ZCS losses of $V_{dc}Q_{tot}$. If dv_{DS}/dt is assumed as independent of load-current, a reasonable approximation from our findings in Section II (see Fig. 5), then the current-dependent losses increase linearly with the current as $k_{on}I_{on}$ and can be considered the losses associated with dv_{DS}/dt-overlap. The turn-on losses, then, can be described as $E_{sw,on}(I_{on}) = V_{dc}Q_{tot} + k_{on}I_{on}$, or:

$$\left.\frac{dv_{DS}}{dt}\right|_{on} = \left.\frac{dv_{DS}}{dt}\right|_0 \tag{6}$$

$$E_{sw,on}(I_{on}) = V_{dc}Q_{tot} + k_{on}I_{on}. \tag{7}$$

For turn-on losses, our model utilizes the values $Q_{oss}(V_{dc}) = 344\,nC$, $C_{par} = 100\,pF$ (PCB), and a neglected charge contribution from the Miller capacitor for $Q_{tot} = 384\,nC$. We fit $k_{on} = \frac{1.35}{2} V_{dc}^2 / \frac{dv_{DS}}{dt}|_0$, with the factor of 1.35 interpreted as a waveform correction factor for the turn-on losses.

4) UNIFIED LOSS MODEL

Finally, we can unify the two loss models, finding a linear piecewise function for half-bridge losses that is distinct, and novel, from the typical assumption of a quadratic loss model that is dependent on current.

With a simple summation, and neglecting E_0 which is always small fraction of $V_{dc}Q_{tot}$ [40], the half-bridge switching losses $E_{sw}(I_{sw}) = E_{sw,on}(I_{on}) + E_{sw,off}(I_{off})$ at a low current ripple (i.e. $I_{sw} \approx I_{on} \approx I_{off}$) result in a piecewise linear function:

$$E_{sw}(I_{sw}) = \begin{cases} V_{dc}Q_{tot} + k_{on}I_{sw} & \text{if} \quad I_{sw} < I_k \\ V_{dc}Q_{tot} + k_{on}I_{sw} + k_{off}(I_{sw} - I_k) & \text{if} \quad I_{sw} \geq I_k. \end{cases} \tag{8}$$

TABLE 2 Derived Loss Parameters for Different Voltage Slope Limitations

Parameter	$\frac{dv_{DS}}{dt}\big\vert_0 = 10\,V/ns$	$\frac{dv_{DS}}{dt}\big\vert_0 = 15\,V/ns$
Q_{tot} (nC)	384	384
I_k (A)	6.6	10
k_{on} (µJ/A)	43	29
k_{off} (µJ/A)	32	21

These linear functions intersect at the value of the kink current I_k, which is dependent — along with k_{on} and k_{off} — on the selected maximum voltage slew rate $dv_{DS}/dt|_0$. Critically, half-bridge switching losses are actually *piecewise-linear* on I_{sw}, rather than quadratic [39], with the kink current I_k playing a critical role as the intersection of these functions and the switched current value after which switching losses start increasing more rapidly. This arises because of the lack of dependence — in either turn-on or turn-off losses — on di/dt, as mentioned previously [22], [25].

The proposed model is validated in Fig. 8(b) and Fig. 8(c), with the turn-off losses measured directly and with tight matching (cf. Fig. 8(i)). Turn-on losses cannot be measured directly easily, so we instead measure half-bridge losses with a small current ripple, which are comprised of one turn-on and one turn-off transition, and report the total measured losses (cf. Fig. 8(ii)). The obtained parameters for the switching loss model are reported in Table 2.

IV. CASE STUDY: 10 KW MOTOR DRIVE SYSTEM

The derived dv_{DS}/dt and loss models are validated by measuring the losses (thermally [39]) of a single *C3M0016120K* bridge-leg of a VSD system for an electric motor, as shown in Fig. 1. The specifications for this motor drive are $V_{dc} = 800\,V$, $P_M = 10\,kW$, $\hat{i}_{nom} = 25\,A_{pk}$, $\hat{i}_{opt} = 20\,A_{pk}$, $M = 0.8$, $M\cos\phi = 0.68$ [31] with a switching frequency $f_{sw} = 16\,kHz$ to remain outside the audible range [41].

With large motor inductances, the output phase current is sinusoidal under Continuous Current Mode (CCM) with a low ripple. For a sinusoidal phase current $i(\epsilon) = \hat{i}\sin(\epsilon)$, the output power is $P_{INV} = \frac{3}{4}\hat{i}V_{dc}M\cos\phi$. The half-bridge losses will include both conduction and switching losses as $P_{HB} = P_{cond} + P_{sw}$, with conduction losses as $P_{cond} = \frac{1}{2}R_{DS,on}\hat{i}^2$ (with current ripple neglected) and the switching losses $P_{sw} = f_{sw}\frac{1}{2\pi}\int_0^{2\pi} E_{sw}(i(\epsilon))d\epsilon$. Using the derived loss model of (8) for the switching losses, the total half-bridge losses are:

$$P_{HB} = \frac{1}{2}R_{DS,on}\hat{i}^2 + f_{sw}\left(V_{dc}Q_{tot} + \frac{2}{\pi}k_{on}\hat{i}\right) + \begin{cases} 0 & \text{if } \hat{i} < I_k \\ f_{sw}\frac{2}{\pi}k_{off}\left[\hat{i}\sqrt{1-\left(\frac{I_k}{\hat{i}}\right)^2} - I_k\arccos\left(\frac{I_k}{\hat{i}}\right)\right] & \text{if } \hat{i} \geq I_k \end{cases} \quad (9)$$

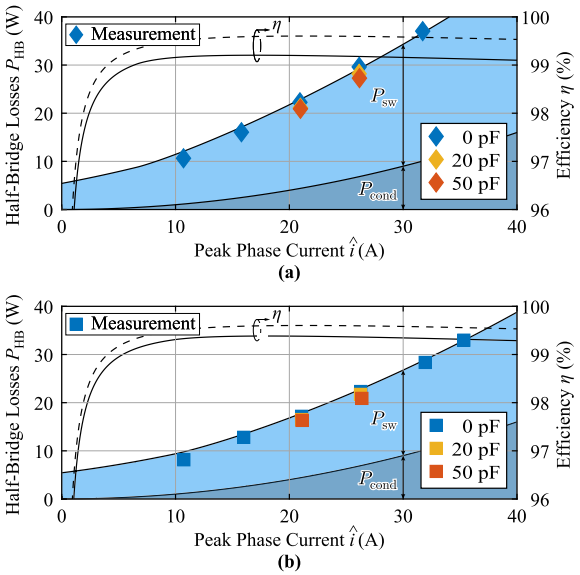

FIGURE 9. Measured semiconductor bridge-leg losses and the corresponding calculated bridge-leg efficiency over peak phase current $\hat{i}$ for (a) $dv_{DS}/dt|_0 = 10\,V/ns$ (♦) and (b) $dv_{DS}/dt|_0 = 15\,V/ns$ (■). Measurements are conducted across several load currents and gate drive circuit parameters (gate resistor and Miller capacitor values) to validate the proposed model. The efficiency without a dv_{DS}/dt-limitation is calculated based on [31] and shown for comparison as the dashed line.

and the bridge-leg efficiency is:

$$\eta = \frac{P_{INV}}{P_{INV} + 3P_{HB}} \approx 1 - \frac{P_{HB}(\hat{i})}{\frac{1}{4}\hat{i}V_{dc}M\cos\phi}. \quad (10)$$

The power semiconductor losses and bridge-leg efficiency are measured with the gate driver circuit parameters of Table 2 under the maximum voltage slew rates of 10 V/ns and 15 V/ns, with the results shown in Fig. 9. The modeled conduction losses use an on-resistance value of $R_{DS,on} = 20\,m\Omega$, which corresponds to a junction temperature of 100 °C. The die area of the selected *C3M0016120K* SiC MOSFETs is optimal for a phase current of $20\,A_{pk}$ [31], which we denote as $\hat{i}_{opt}$.

The loss measurements match neatly with the total loss predicted by the proposed loss model across maximum slew rate $dv_{DS}/dt|_0$ limits, phase current, and combinations of gate resistance and Miller capacitance. With the 10 V/ns maximum slew rate constraint, the measured bridge-leg losses are $P_{HB} = 22.3\,W$ for $\hat{i}_{opt} = 20\,A_{pk}$ without the Miller capacitor and improve to 20.9 W with $C_M = 50\,pF$. Similarly, with the same 10 V/ns maximum slew rate but at $\hat{i}_{nom}$, the measured bridge-leg losses are $P_{HB} = 29.9\,W$ without the Miller capacitor and improve to 27.3 W with $C_M = 50\,pF$. With a higher slew rate limitation of 15 V/ns, the measured bridge-leg losses are reduced relative to the 10 V/ns case, as expected, from 17.2 W ($C_M = 0\,pF$) to 16.3 W ($C_M = 50\,pF$) at $\hat{i}_{opt}$ and from 22.3 W ($C_M = 0\,pF$) to 20.9 W ($C_M = 50\,pF$) at $\hat{i}_{nom}$.

For the slew rate limit of 10 V/ns, the maximum calculated bridge-leg efficiency reaches 99.2 % at $17.0\,A_{pk}$ and for the maximum slew rate of 15 V/ns, the maximum calculated

bridge-leg efficiency reaches 99.4 % at 18.1 A_{pk}. Without the slew rate limitation (0 Ω gate resistance, which reaches a slew rate of 60 V/ns, as reported in Section II), the peak bridge-leg efficiency is 99.6 % (calculated based on [31]), as shown with the dotted line in each plot in Fig. 9.

For the slew rate limit of 10 V/ns, the maximum calculated bridge-leg efficiency reaches 99.2 % at 17.0 A_{pk} and for the maximum slew rate of 15 V/ns, the maximum calculated bridge-leg efficiency reaches 99.4 % at 18.1 A_{pk}.

A. PERFORMANCE COMPARISON TO A dv/dt-FILTER-BASED SLEW RATE LIMITATION

To evaluate the performance of the proposed Miller-capacitor-based approach, we compare the system volume and losses with a conventional dv/dt-LC-filter-based approach [14] to meet the same slew rate limitation. We derive a simple volume model and use the filter loss model from [31] for the comparison.

The volume of the power stage is primarily driven by the volume of the heatsink. We assume a maximum hestsink temperature of $T_{HS} = 85\,°C$ and an ambient temperature of $T_{amb} = 45\,°C$, and use the Cooling System Performance Index (CSPI) approach [42] with a typical CSPI of 20 W/KL to calculate the heatsink volume Vol_{HS}. The design equations for the heatsink volume are:

$$R_{HS} = \frac{T_{HS} - T_{amb}}{3P_{HB}(\hat{i}_{nom})} \tag{11}$$

$$Vol_{HS} = \frac{1}{CSPI\, R_{HS}}. \tag{12}$$

For a three-phase inverter at nominal operation ($\hat{i}_{nom} = 25\,A_{pk}$) and a slew rate limit of 15 V/ns ensured by the discussed gate drive modifications, the inverter heatsink volume is $Vol_{HS} = 81\,cm^3$ (for maximum semiconductor losses of 64.6 W at $\hat{i}_{nom} = 25\,A_{pk}$) with total losses of 50.5 W at $\hat{i}_{opt} = 20\,A_{pk}$. Without the slew rate limitation (0 Ω gate resistance, which reaches a slew rate of 60 V/ns, as reported in Section II), the peak bridge-leg efficiency is 99.6 % at 21.3 A_{pk} and the *power stage* heatsink volume is reduced by almost 40 % to 51 cm^3 (for maximum semiconductor losses of only 41 W at $\hat{i}_{nom} = 25\,A_{pk}$).

Without the bridge-leg slew rate limitation, the dv/dt-LC-filter is now required to protect the motor winding system. We use, as a reference, an LC-filter with DRC damping branches (connected between the filter output and the positive and negative DC bus, [14]) this is designed for the same application scenario with 15 V/ns. If we consider the Permanent-Magnet Synchronous Motor (PMSM) 1FT7084 from Siemens [43], the dv/dt-filter capacitor of a phase needs to be at least $C_o = 1.5\,nF$ [31], which can be implemented with a Mica capacitor [35] for a volume of only 0.1 cm^3 per phase. While this small capacitor volume can be easily neglected, the filter capacitors introduce additional capacitive switching losses, resulting in additional losses of $P_C = 3 f_{sw} C_o V_{dc}^2 = 46\,W$ that are dissipated in the damping resistors. An additional heatsink for these resistors (which we allow to reach $T_{HS,R} = 125\,°C$, as power resistors can be operated at high temperatures) requires a volume of $Vol_{HS,R} = 28.8\,cm^3$.

According to [31], in each phase a filter inductor with $L_o = 1.2\,\mu H$ is required which causes a current swing of 28 A, thus the inductor must be designed to saturate above 58 A. This filter inductor can be implemented with the HCI Inductor from Würth Elektronik [44] for only 3 cm^3 of additional volume per phase.

In sum, then, a dv/dt-limiting passive LC-filter with DRC damping (in each phase) achieves a system volume of 89.4 cm^3 and system losses at $\hat{i}_{opt}$ of 79 W, for an overall system volume increase of 10 % and an overall system loss increase at $\hat{i}_{opt}$ of 56 % compared to the Miller capacitor approach (efficiency reduction from 99.4 % to 99 %). Further, the relatively large filter inductors may prevent automated assembly of the power stage and the filter approach is sensitive to the selected motor since the filter capacitor C_o must dominate the motor capacitance [31]. The proposed Miller capacitor approach is, in contrast, not sensitive to the motor characteristics, as any additional parasitic capacitance only increases C_{eff} and the kink current I_k but does not influence the dv/dt limit, which depends only on the gate drive configuration (cf. (2) and (3)). This increase in kink current reduces the turn-off losses, while the increased ZCS losses only occur inside the motor.

In sum, then, the combination of SiC MOSFETs and a slew rate limit enforced with an external Miller capacitance uniquely enables high-performance VSD systems — without the significant size, weight, or cost associated with bulky filters — that clearly exceed the IGBT bridge-leg efficiency limit of ≈ 98 % [31] while protecting motors from high voltage slew rates.

V. DESIGN PROCEDURE FOR VOLTAGE-SLEW-RATE-LIMITED BRIDGE LEGS

With a voltage slew rate limitation on the bridge-leg itself attractive in many VSD systems, we provide a design procedure to implement the dv_{DS}/dt-limitations explored in this work. The goal of this section is to summarize the critical design steps for a tangible and straightforward guide to apply dv_{DS}/dt limits in motor drives with a sinusoidal phase current with peak value $\hat{i}$.

1) The specification of the application must be defined, including the maximum slew rate $dv_{DS}/dt|_0$ and DC-link voltage requirements.
2) Select the transistor technology based on the blocking voltage (the DC-link voltage, with margin) and other considerations, including cost and preferred manufacturers.
    a) For this transistor family, devices with a range of on-resistances are typical available.
    b) The loss minimum chip area — based on the on-resistance $R_{DS,on}$ at the desired junction operating temperature $T_{J,op}$, and the output charge

$Q_{oss}(V_{dc}) = \int_0^{V_{dc}} c_{oss}(v)\mathrm{d}v$ (all of which can be determined from the datasheet) — is [31]:

$$R_{DS,on,opt} = R_{DS,on}\frac{1}{\hat{i}}\sqrt{\frac{2V_{dc}Q_{oss}f_{sw}}{R_{DS,on}}} \tag{13}$$

3) With the power transistor now selected, we move to the configuration of a gate drive, where we have to distinguish two cases:
   a) For the known half-bridge configuration of Section II, with existing data from this work for the *C3M0016120K* [33] and a gate driver with an output clamp variant, the designer may straightforwardly select:
      i) $C_M = 50\,\mathrm{pF}$ should be selected for maximum performance, as it achieves minimal losses without causing instability through excessive gate ringing.
      ii) A minimum effort implementation with no Miller capacitor ($C_M = 0\,\mathrm{pF}$) and elevated gate resistors incurs a switching loss increase of 6 % to 8 %.
      iii) The corresponding on and off resistances for the given $\mathrm{d}v_{DS}/\mathrm{d}t|_0$-limit can be selected according to Fig. 7.
   b) If, alternatively, the half-bridge power semiconductors and/or gate drivers have not been characterized:
      i) An evaluation bridge-leg must be constructed to conduct simple voltage slope measurements, as described in Section II.
      ii) Testing should begin with $C_M = 0\,\mathrm{pF}$, and the turn-on resistance should be gradually increased (with $R_{G,off} = 0\,\Omega$) until the voltage slope limit is reached under continuous ZCS conditions, with the switching frequency selected to achieve a junction temperature close to the maximum operating temperature $T_{J,op}$ in the application.
      iii) After this sweep is completed, $R_{G,on}$ should be fixed and $R_{G,off}$ can be selected such that the same voltage slope limit is achieved during turn-off at the maximum phase current and under DPT conditions (room temperature device).
      iv) To further increase the performance, the prior two steps can be repeated for different Miller capacitor values, stopping before a maximum value where additional ringing occurs in the gate-source voltage during transients.
4) With the Miller capacitance selected, the effective capacitance is $C_{eff} = 2C_{dQ,oss} + 2C_M + C_{par}$, where $C_{dQ,oss} = \int_{0.1V_{dc}}^{0.9V_{dc}} c_{oss}(v)\mathrm{d}v$ is the charge-equivalent capacitance of the transistor between 10 % and 90 % of the DC-link voltage and C_{par} includes the parasitic capacitance of the PCB and the load, which appears between switch node and either one of the DC-link rails.
5) Between C_{eff} and the slew rate limit $\mathrm{d}v_{DS}/\mathrm{d}t|_0$, the kink current I_k is fully-known from (1):

$$I_k = C_{eff}\left.\frac{\mathrm{d}v_{DS}}{\mathrm{d}t}\right|_0,$$

and the loss coefficients are:

$$Q_{tot} = Q_{oss}(V_{dc}) + \left(C_M + C_{par}/2\right)V_{dc}$$

$$k_{on} = \frac{1.35}{2}V_{dc}^2 \Big/ \left.\frac{\mathrm{d}v_{DS}}{\mathrm{d}t}\right|_0$$

$$k_{off} = \frac{1}{2}V_{dc}^2 \Big/ \left.\frac{\mathrm{d}v_{DS}}{\mathrm{d}t}\right|_0.$$

6) The half-bridge losses are, from (9):

$$P_{HB} = \frac{1}{2}R_{DS,on}\hat{i}^2 + f_{sw}\left(V_{dc}Q_{tot} + \frac{2}{\pi}k_{on}\hat{i}\right) + \begin{cases} 0 & \text{if } \hat{i} < I_k \\ f_{sw}\frac{2}{\pi}k_{off}\left[\hat{i}\sqrt{1-\left(\frac{I_k}{\hat{i}}\right)^2} - I_k \arccos\left(\frac{I_k}{\hat{i}}\right)\right] & \text{if } \hat{i} \geq I_k \end{cases}$$

7) An appropriate heatsink can now be designed, and the system can be implemented and validated.

VI. CONCLUSION

Variable Speed Drive (VSD) systems utilizing next-generation Wide-Bandgap (WBG) power semiconductors hold the promise of boosting the efficiency, power density, and adoption of electric motors to electrify manufacturing, logistics, and mobility. To realize fully the loss reduction and frequency increase benefits of SiC MOSFETs, however, the voltage slew rate applied to the motor must be limited to values such that the motor will not be damaged by partial discharge phenomena, surge voltages from cable reflections, or unequal distribution of the voltage across motor windings.

In this work, we evaluate the potential of an external Miller capacitor to limit the maximum $\mathrm{d}v_{DS}/\mathrm{d}t$ of a bridge-leg, and derive a detailed understanding of the switching behavior to derive analytical models — across switched current, gate resistance, and Miller capacitance — for the maximum $\mathrm{d}v_{DS}/\mathrm{d}t$ and switching losses during the turn-on and turn-off transitions. The $\mathrm{d}v_{DS}/\mathrm{d}t$ model and matching measurements show that the maximum slew rate occurs, for turn-on, at Zero-Current Switching (ZCS) and at elevated temperatures, while the turn-off $\mathrm{d}v_{DS}/\mathrm{d}t$ saturates after an analytical "kink current" is passed. The kink current derivation, which can be understood in the context of the current paths during switching, helps us arrive at a critical finding for the broader field: that switching losses in a bridge-leg are not quadratic with current (at least under limited $\mathrm{d}v_{DS}/\mathrm{d}t$ conditions), as long modelled, but are rather piecewise linear on current, with the second linear function starting at the kink current itself.

The dv_{DS}/dt and loss models are validated on a SiC MOSFET bridge-leg for a 10 kW 800 V DC-link VSD system with dv_{DS}/dt limitations of 10 V/ns and 15 V/ns, where we find excellent matching between the model and the measured bridge-leg losses. The Miller capacitor-based technique achieves lower losses for the same maximum dv_{DS}/dt than a gate resistor-only technique, highlighting the promise of realizing VSD systems with SiC MOSFETs that simultaneously achieve high efficiency, high power density, and limited voltage slew rates.

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