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Dynamic On-Resistance in GaN-on-Si HEMTs: Origins, Dependencies, and Future Characterization Frameworks

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Dynamic On-Resistance in GaN-on-Si HEMTs: Origins, Dependencies, and Future Characterization Frameworks

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***Abstract*—Gallium nitride high-electron-mobility transistors (GaN HEMTs) exhibit dynamic on-resistance ($\mathrm{d}R_{\mathrm{on}}$), where the on-resistance immediately after turn-on is higher than the DC value at the same junction temperature. A proliferation of recent literature reports $\mathrm{d}R_{\mathrm{on}}$, with some publishing an 8× increase in conduction losses and others finding that the problem is nonexistent. This variation can be largely attributed to the standardized double-pulse-test (DPT) method, which does not specify blocking time and will ignore any effects that accumulate over multiple switching cycles. Absent consistent measurements, designers are left without an accurate conduction loss estimate in converters with GaN HEMTs. We discuss the underlying causes of charge trapping to find the key influences over $\mathrm{d}R_{\mathrm{on}}$, and show that the DPT technique gives invalid results. Our measurements validate that each operating parameter must be independently controlled and that only steady-state $\mathrm{d}R_{\mathrm{on}}$ measurements will predict *in situ* performance. For the commercial GaN HEMT tested in this paper, the worst-case $\mathrm{d}R_{\mathrm{on}}$ is nearly 2× higher than the DC resistance at the same temperature, confirming that accurate $\mathrm{d}R_{\mathrm{on}}$ characterization remains critical to predicting converter characteristics. Finally, we provide a reporting framework for GaN HEMT manufacturers and methods to estimate conduction losses in converters with GaN HEMTs.**

***Index Terms*— Dynamic On-State Resistance, Gallium Nitride, Power Transistors, Wide Bandgap Semiconductors.**

I. Introduction

Compared to majority-carrier silicon power semiconductors, gallium nitride-on-silicon high-electron-mobility transistors (GaN-on-Si HEMTs) have much lower specific on-resistance at a given blocking voltage up to the maximum commercially-available rating of 900 V [1]. These HEMTs, however, are known to exhibit "dynamic on-resistance," where the on-resistance (R_{on}) immediately after turn-on is significantly higher than its DC value (R_{dc}) [2]. In many applications, this dynamic on-resistance ($\mathrm{d}R_{\mathrm{on}}$) completely determines conduction losses since dynamic effects dominate the effective on-resistance for the entire conduction period (**Fig. 1a**). The criticality of accurate $\mathrm{d}R_{\mathrm{on}}$ characterization is further underscored by the recent JEDEC standard on the subject, which recommends to use the double-pulse-test method but does not specify test parameters [3].

This importance has resulted in a proliferation of recent papers on $\mathrm{d}R_{\mathrm{on}}$ that can be separated into four themes (with some overlap): *a)* new devices that compare "their" $\mathrm{d}R_{\mathrm{on}}$ to existing devices [4]–[9], *b)* physics-level investigations of the origins of $\mathrm{d}R_{\mathrm{on}}$ [10]–[22], *c)* novel measurement techniques of $\mathrm{d}R_{\mathrm{on}}$ [23]–[41], and *d)* papers attempting to account for unexplained losses in power converters [42]–[46]. A survey of these papers finds such widely-varying values of $\mathrm{d}R_{\mathrm{on}}$ that designers cannot use the literature to determine losses. For example, **Fig. 1b** shows a selection of previous $\mathrm{d}R_{\mathrm{on}}$ measurements on commercial 600/650 V HEMTs from three manufacturers at the same blocking voltage (400 V). For $\mathrm{d}R_{\mathrm{on}}$ evaluated near 1 µs after turn-on (measurement time, $t_{\mathrm{m}} = 1\,\mu\mathrm{s}$), dynamic effects could increase conduction losses by 5-8× or be essentially negligible, and similar discrepancies exist at other operating points. Since power semiconductors typically drive the most stringent thermal requirements, neither converter efficiency nor heat sink demands can be accurately predicted *a priori*.

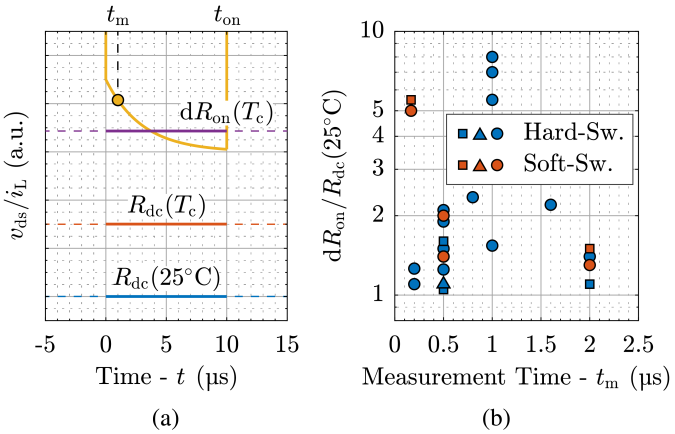

Fig. 1: a) GaN HEMT conduction period ($0 < t < t_{\mathrm{on}}$) showing the effect of dynamic on-resistance ($\mathrm{d}R_{\mathrm{on}}$), where the conduction-time-averaged on-state resistance ($\mathrm{d}R_{\mathrm{on}}\,(T_{\mathrm{c}})$) is higher than the DC resistance at the same temperature ($R_{\mathrm{dc}}\,(T_{\mathrm{c}})$). The measurement time (t_{m}) indicates the time after turn-on at which $\mathrm{d}R_{\mathrm{on}}$ is reported in existing literature. **b)** Previously-reported $\mathrm{d}R_{\mathrm{on}}$, normalized to $R_{\mathrm{dc}}\,(25\,°\mathrm{C})$, for commercially-available 600/650 V GaN-on-Si HEMTs at 400 V blocking voltage (note that blocking times and temperatures vary). Near 1 µs after turn-on, $\mathrm{d}R_{\mathrm{on}}$ could result in a 5-8× increase in conduction losses or be negligible. Marker shapes (□, △, ○) indicate manufacturer of the tested device.

Extra barriers to understanding $\mathrm{d}R_{\mathrm{on}}$ abound. Some literature confuses soft-switching losses with $\mathrm{d}R_{\mathrm{on}}$ losses, since both are high-frequency effects. Device physicists often use diagnostic operating modes (e.g. floating substrate, extreme gate stress) to understand the physics of $\mathrm{d}R_{\mathrm{on}}$, but these conditions are not seen in real power converters and these $\mathrm{d}R_{\mathrm{on}}$ values should not be directly used. To add to the confusion, GaN manufacturers advertise that the problem is essentially "solved" and/or has no system-level effects [47], [48].

Missing from this previous literature is a simple explanation – in circuit-level terms relevant to the power electronics engineer – of the drivers and values of $\mathrm{d}R_{\mathrm{on}}$ in power converters. The goal of this Letter is to provide a physics-based understanding to develop a standardized method and parameter set for future $\mathrm{d}R_{\mathrm{on}}$ work. **Section II** explains the physical origins of $\mathrm{d}R_{\mathrm{on}}$. These underlying trapping processes are then related to power electronics circuit operation, resulting in eight parameters that affect $\mathrm{d}R_{\mathrm{on}}$. In **Section III**, we measure $\mathrm{d}R_{\mathrm{on}}$ in a commercial HEMT to validate the effects of these parameters and show that the standard double-pulse-test method gives incorrect results. **Section IV** proposes a reporting framework for GaN HEMT manufacturers and two methodologies to translate the multi-dimensional $\mathrm{d}R_{\mathrm{on}}$ space into on-state losses in power converters.

II. Influences on $\mathrm{d}R_{\mathrm{on}}$

The cause of $\mathrm{d}R_{\mathrm{on}}$ can be identified as the trapping of electrons in undesired locations in the GaN HEMT structure (see **Fig. 2**).

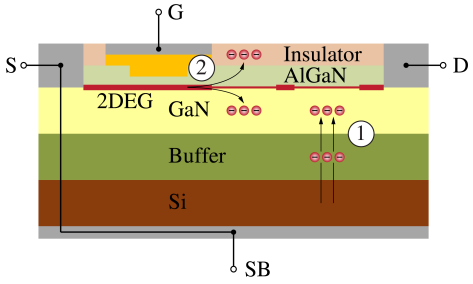

Fig. 2: Simplified GaN-on-Si HEMT cross-section showing key charge trapping sites, which reduce the 2DEG density and increase R_{on}. ① *Off-state trapping:* large off-state biases ionize the traps at the surface, in the buffer, and/or in the GaN channel. ② *Hot-electron trapping:* during hard turn-on, electrons from the 2DEG are accelerated and trapped in the dielectric, at the surface, in the GaN channel, and/or in the buffer.

The concentration of electrons in the 2-D electron gas (2DEG) must be proportionally reduced to maintain overall charge neutrality, decreasing the drain-source current [2]. Detrapping these electrons requires finite time with the switch in the on-state, during which the device exhibits higher-than-expected R_{on}, or dR_{on}.

The causes of these net negative charges can be segmented into two categories: off-state trapping and hot electron trapping [15]–[17].

- *Off-state trapping* occurs when a large electric field is applied between the drain and substrate and/or the drain and gate, both of which exist with a large V_{ds} bias (assuming source and substrate are shorted, as typically recommended or connected internally by manufacturers). While under bias, deep-level acceptors in the buffer and GaN channel layers are ionized, or filled with electrons, from leakage currents through the Si substrate. The quantity of trapped electrons increases with **blocking voltage (V_b)**, which increases the number of acceptors that may be ionized, and blocking time (t_b), which increases the quantity of filled traps.
- *Hot-electron trapping* exists when a large electric field and a large current occur simultaneously in the drain region, recognizable as the voltage-current (V-I) overlap during hard-switching [12]. In this case, the high-energy electrons in the 2DEG are the source of trapped electrons, and may be trapped in the same deep-level acceptors in the buffer, GaN channel, and gate-drain region. With sufficiently high energy, these electrons may also be injected into the dielectric layer near the gate and drain. The quantity of hot-electron-trapped electrons is affected by **blocking voltage (V_b)**, which affects the electron acceleration and therefore trapping efficacy, **current (I_{sw})**, which is proportional to the number of accelerated electrons, and **gate resistance (R_g)**, which affects the switching speed and the time-integrated quantity of trapped electrons. Hot-electron trapping does not occur, to first order, under soft-switching conditions [12].

Increased gate threshold voltage is another potential adverse dynamic effect, and occurs if traps located near the gate insulator are filled [15], [49]. Threshold shifts from dynamic trapping are approximately 1 V in magnitude [49]–[51] and starting gate threshold voltages in commercial enhancement-mode HEMTs are no more than 2.6 V [52]; in most power applications, HEMTs are driven with $5\,\text{V} - 6\,\text{V}$ gate voltages, guaranteeing fully-enhanced operation even with a 1 V shift above the starting 2.6 V threshold. Indeed, Ref. [49] experimentally validates that a 5 V gate drive voltage is sufficient to eliminate any additional, measurable dynamic effects from a threshold shift. If lower on-state voltages are used (e.g. $3\,\text{V} - 4\,\text{V}$), however, dynamic effects are reintroduced, and preliminary data indicates that the off-state voltage may also affect dR_{on} [22]. Therefore, while applications driven with the standard $5\,\text{V} - 6\,\text{V}$ gate voltages can ignore the threshold shift effect, generally the **positive and negative gate drive voltages (v_{gs})** affect dR_{on} and must be controlled.

The time constants associated with trapping and detrapping depend on the physical location of the trapped charges, their energy levels, and the device temperature. These kinetics add dR_{on} dependencies on conduction time (t_{on}), elapsed time after turn-on (t_m), and **junction temperature (T_j)**. On-time, measurement time, and blocking time should be transformed into the converter parameters **switching frequency (f_s)** and **duty cycle (d)**. Most studies use – and the JEDEC standard recommends – a double-pulse-test (DPT) to measure dR_{on}; this mode of operation is unrealistic for steady-state power converters, and long t_b increases the reported dR_{on} [47]. Even more concerning: if detrapping takes longer than the device's on-time, traps accumulate and the DPT measurement could significantly *underestimate* the actual dR_{on} [29], [37]. dR_{on} measurements, therefore, must be taken under steady-state, continuous-switching conditions.

Two additional best practices for reporting dR_{on} also facilitate understanding. Firstly, dR_{on} values are often reported at a single measurement time, but because dR_{on} changes during the on-time, dR_{on} should instead be defined as the time-averaged R_{on} during the conduction period. Secondly, R_{on} can be normalized by the DC on-resistance value *at the correct temperature*, $R_{dc}(T_j)$. When normalized with respect to the room-temperature R_{dc}, there is the potential for confusion between dR_{on} and the R_{dc} increase due to elevated T_j [47].

Finally, we arrive at the key influences on dR_{on} – and the parameters that we propose to be independently tested, controlled, and reported:

1) Blocking voltage (V_b)
2) Switching frequency (f_s)
3) Duty cycle (d)
4) Gate resistance (R_g)
5) Gate drive voltage (v_{gs})
6) Junction temperature (T_j)
7) Device current (I_{sw})
8) Switching condition (hard or soft)

III. Dynamic R_{on} Measurements

To validate these understandings, we measure dR_{on} on a commercially-available GaN HEMT (device parameters hidden for anonymity, with the device voltage rating indicated as BV_{ds}). We use the method from [28], which measures accurate on-state voltage within 100 ns of the switch turn-on transition. In Ref. [28], the circuit and method are benchmarked on a Si MOSFET, which shows the expected lack of dR_{on}, and the key measurement considerations and error terms are outlined in detail. A simplified circuit of the measurement setup is shown in **Fig. 3** and representative measurement waveforms are shown in **Fig. 4** under both hard- and soft-switching. The test setup varies extracted heat using speed-modulation of air flow across a heat sink to control case temperature (T_c) to within $\pm 0.5\,^\circ\text{C}$ of the reported value. The difference between the junction temperature and the case temperature is given by the product of the dissipated power (P_d) and the case-to-junction thermal resistance ($R_{\theta JC}$) given in the datasheet as $T_j - T_c = R_{\theta JC} P_d$. The worst-case $T_j - T_c$ deviation for our operating conditions is $< 3\,^\circ\text{C}$, and we therefore safely assume that $T_j \approx T_c$ at all tested operating points. A single calibrated device is used for every measurement to avoid any part-to-part variation, with the DC calibration across temperature shown in **Fig. 5b**.

We first measure dR_{on} with the standard DPT technique under hard-switching with the on-time fixed to 50 µs, $I_{sw} = 15\,\text{A}$, and

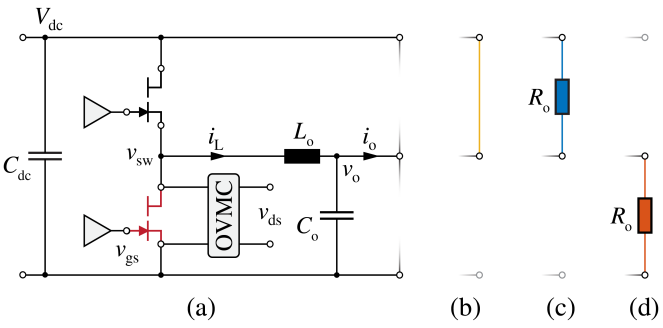

Fig. 3: **a)** Simplified circuit schematic for the three test modes, with different load connections for each test method. The low-side HEMT is the device-under-test and the on-state voltage measurement circuit (OVMC) from [28] measures on-resistance. **b)** Double-pulse-test circuit, with the inductor shorted to V_{dc}. **c)** Steady-state hard-switching circuit, with the load connected to V_{dc}. **d)** Steady-state soft-switching circuit, with the load connected to ground.

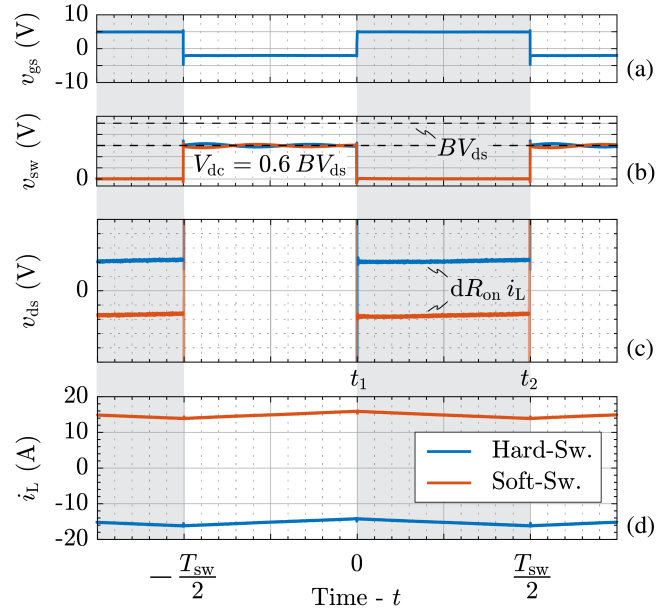

Fig. 4: Key waveforms measured on the circuit in **Fig. 3** for continuous hard-switching and continuous soft-switching with $V_{dc} = 0.6BV_{ds}$, $I_{sw} = \pm 15\,A$, $T_c = 50\,°C$, and $f_s = 10\,kHz$. Current ripple is neglected. dR_{on} is reported as the average R_{on} between t_1 and t_2. **a)** gate-source voltage, v_{gs}, $+5\,V/-2\,V$ (identical waveforms in soft- and hard-switching). **b)** switch node voltage, v_{sw}. **c)** OVMC-measured drain-source voltage, v_{ds}. **d)** inductor current, i_L.

$T_c = 35\,°C$. t_b is controlled by an off-board digital signal processor that triggers the double-pulse test after the predefined time. **Fig. 5a** reports this DPT-measured, on-time-averaged dR_{on}, and we observe the familiar monotonic increase of dR_{on} with V_b and t_b. While the DPT technique is common, these results are invalid, as arbitrary blocking times heavily influence dR_{on} and accumulated trapping is completely ignored [29]. Accumulated trapping time constants have been observed on orders from 100 µs [34] to 1 ms [29] to seconds [17], [21], so the time needed to stabilize dR_{on} is driven by the longer of the thermal time constant of the system-under-test and the accumulated trapping time constant(s) of the device-under-test. Overall, dR_{on} measurements must be recorded under steady-state conditions, and our subsequent results are taken after tens of seconds of converter operation.

Fig. 5b uses these steady-state conditions (hard-switching), but measured dR_{on} is normalized to $R_{dc}\,(25\,°C)$, another common but

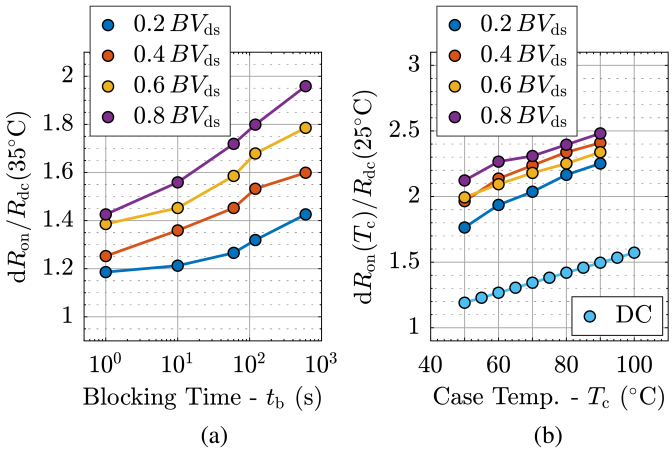

Fig. 5: Misleading dR_{on} measurements and normalization. **(a)** Double-pulse-test at 15 A average current and 50 µs on-time. **(b)** Steady-state hard-switched $I_{sw} = 15\,A$, $f_s = 10\,kHz$, $d = 50\,\%$ but normalized to $R_{dc}\,(25\,°C)$. All measurements at $R_g = 10\,\Omega$, $v_{gs} = +5\,V/-2\,V$. Legend indicates V_{dc} as % of BV_{ds}.

misleading practice. This reporting method overstates the dynamic degradation, as dR_{on} and the device's positive temperature coefficient are lumped together in the overall R_{on} increase. dR_{on} measurements should be normalized by $R_{dc}\,(T_c)$, as reported for our "best practices" dR_{on} measurements in the remainder of the paper.

Fig. 6a shows measured dR_{on} under hard-switching across V_b and T_c with $I_{sw} = 15\,A$ and $f_s = 10\,kHz$. These measurements drive home the importance of both controlling temperature and measuring dR_{on} at realistic operating temperatures. For example, dR_{on} increases monotonically with higher V_b near 50 °C, but at higher temperatures (e.g. 90 °C), dR_{on} is nearly flat with voltage. This non-monotonic relationship with V_b that we observe at elevated temperatures is also reported in [12], [39], [40], [49], [53], and Ref. [12] offers a physical explanation of the counteracting trapping effects that occur with increasing V_b. A decrease in dR_{on} with T_c is reported in [12], [29], [41], [43] due to reduced hot-electron trapping [12], [54], although because both trapping and detrapping kinetics are affected, a universal rule of thumb for the influence of T_c on dR_{on} cannot be determined [53]. These trends and magnitudes directly contradict the DPT measurements, again highlighting the importance of temperature-controlled, steady-state measurements.

Fig. 6b keeps the identical test conditions but operates with soft-switching, which eliminates hot-electron trapping by removing the V-I overlap during turn-on [12], [34] and leaves dR_{on} dominated by off-state trapping. Zero-voltage-switching (ZVS), versus zero-current-switching, is the preferred soft-switching mode for unipolar power semiconductors, including HEMTs, because switching losses due to energy stored in the parasitic output capacitor are ideally eliminated. To achieve ZVS, the device must turn-on with negative current, and there are two well-known choices for implementing ZVS in our test circuit: triangular current mode (TCM, see [28]) or with a constant, negative-current (see **Fig. 3d**, which is similar to, for example, the soft-switching operation in a dual-active-bridge converter [55]). In TCM, the current polarity changes from negative (at turn-on) to positive during the conduction period. This large current variation, firstly, renders an "average" current value meaningless, complicating comparisons to hard-switched operating points. More importantly, the high di/dt and unavoidable parasitic inductance introduce errors in dR_{on} characterization that must be calibrated out [28]. In contrast, the

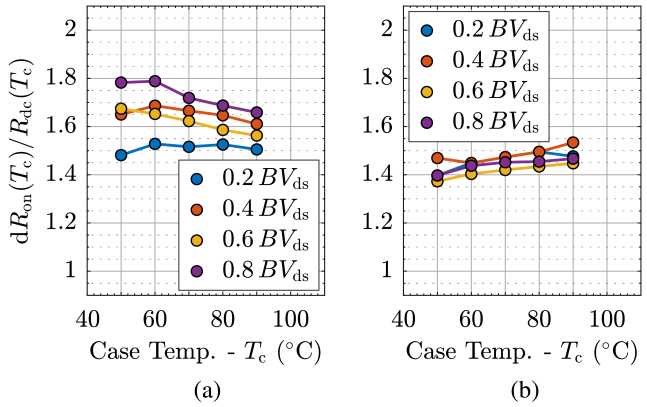

Fig. 6: $\mathrm{d}R_{\mathrm{on}}$ measurements at steady-state and normalized to $R_{\mathrm{dc}}\,(T_\mathrm{c})$. **(a)** Hard-switching, $I_{\mathrm{sw}} = 15\,\mathrm{A}$, $f_\mathrm{s} = 10\,\mathrm{kHz}$. **(b)** Soft-switching, $I_{\mathrm{sw}} = -15\,\mathrm{A}$, $f_\mathrm{s} = 10\,\mathrm{kHz}$. All measurements at $R_\mathrm{g} = 10\,\Omega$, $v_{\mathrm{gs}} = +5\,\mathrm{V}/-2\,\mathrm{V}$, and 50 % duty cycle. Legend indicates V_{dc} as % of BV_{ds}.

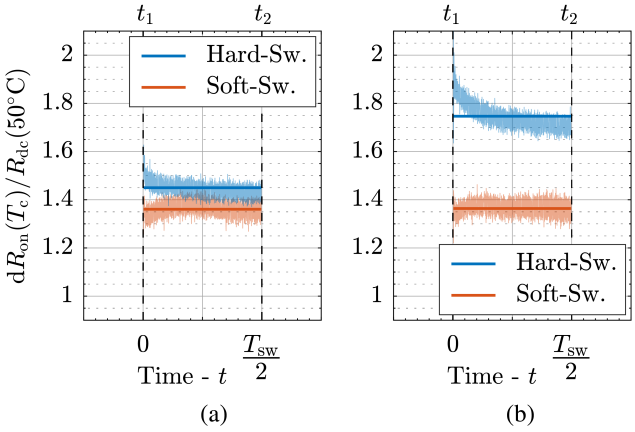

Fig. 7: $\mathrm{d}R_{\mathrm{on}}$ measurements, normalized to $R_{\mathrm{dc}}\,(50\,°\mathrm{C})$, in steady-state hard- and soft-switching operation at $I_{\mathrm{sw}} = \pm 15\,\mathrm{A}$, $f_\mathrm{s} = 10\,\mathrm{kHz}$, $R_\mathrm{g} = 10\,\Omega$, $d = 50\,\%$, $v_{\mathrm{gs}} = +5\,\mathrm{V}/-2\,\mathrm{V}$, and $T_\mathrm{c} = 50\,°\mathrm{C}$. **(a)** $V_{\mathrm{dc}} = 0.2BV_{\mathrm{ds}}$. **(b)** $V_{\mathrm{dc}} = 0.8BV_{\mathrm{ds}}$. In hard-switching, detrapping occurs during the on-state due to the fast hot-electron time constants. In soft-switching, which is dominated by off-state traps, no detrapping occurs due to the slow time constant of these traps. The average values over the conduction period (shown as solid lines) match the reported values in **Fig. 6**.

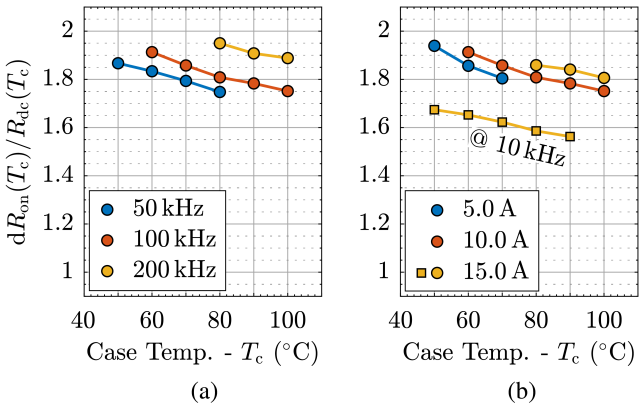

Fig. 8: $\mathrm{d}R_{\mathrm{on}}$ measurements at steady-state and normalized to $R_{\mathrm{dc}}\,(T_\mathrm{c})$. **(a)** Hard-switching, $V_{\mathrm{dc}} = 0.6BV_{\mathrm{ds}}$, $I_{\mathrm{sw}} = 10\,\mathrm{A}$. **(b)** Hard-switching, $V_{\mathrm{dc}} = 0.6BV_{\mathrm{ds}}$, $f_\mathrm{s} = 100\,\mathrm{kHz}$. All measurements at $R_\mathrm{g} = 10\,\Omega$, $v_{\mathrm{gs}} = +5\,\mathrm{V}/-2\,\mathrm{V}$, and 50 % duty cycle. Excluded temperatures for particular sweeps were not achievable with the cooling power range of our test setup.

constant negative-current (ignoring the minor current ripple) method implemented here maintains very low $\mathrm{d}i/\mathrm{d}t$ (less than $1\,\mathrm{A/\mu s}$), and the influence of parasitic inductance (on the order of up to a few nH) on the measured $\mathrm{d}R_{\mathrm{on}}$ can be safely neglected. This mode only characterizes 3rd quadrant operation of the HEMT, but this will be the operating quadrant in the vicinity of turn-on (where $\mathrm{d}R_{\mathrm{on}}$ is most important) for most soft-switched converters utilizing GaN HEMTs. Three contrasts with the hard-switched measurements are highlighted. Firstly, the dependence on V_b is weak. With realistic operating frequencies for GaN HEMTs (tens of kHz and above), the blocking time is relatively short, and off-state trapping accumulation appears only marginally affected by larger V_b. Secondly, $\mathrm{d}R_{\mathrm{on}}$ slightly increases with T_c instead of broadly decreasing, as increased electron scattering is no longer important. Lastly, the magnitude of $\mathrm{d}R_{\mathrm{on}}$ with soft-switching is lower than under hard-switching at the same current magnitude. While there is one less trapping mechanism in soft-switching, the relative $\mathrm{d}R_{\mathrm{on}}$ magnitudes between soft- and hard-switching are impacted by specific device structures [34], [56], and this relationship should not be broadly extrapolated.

By comparing $\mathrm{d}R_{\mathrm{on}}$ during the on-time between hard- and soft-switching, we can gain further insights on the detrapping mechanisms and time constants (for this device, at a minimum, as trapping dynamics will likely be quite device-specific). **Fig. 7** plots measured $\mathrm{d}R_{\mathrm{on}}$ at $I_{\mathrm{sw}} = \pm 15\,\mathrm{A}$, $f_\mathrm{s} = 10\,\mathrm{kHz}$, and $T_\mathrm{c} = 50\,°\mathrm{C}$ for each operating mode. In hard-switching, there is significant detrapping (which manifests as steadily decreasing $\mathrm{d}R_{\mathrm{on}}$) during the $50\,\mu\mathrm{s}$ on-time, while in soft-switching, no measurable detrapping occurs over the same conduction period.

Recalling that hard-switching has *both* off-state and hot-electron trapping while soft-switching has *only* off-state trapping, we can ascertain that the time constants of some of the hot-electron traps must be on the order of the switching frequency, while the off-state trap time constants are much longer. Indeed, off-state buffer traps are measured on the order of $1\,\mathrm{s} - 10\,\mathrm{s}$ in GaN-on-Si HEMTs [17], [21], supporting these measurement results. Our hard-switched measurements at $100\,\mathrm{kHz}$ ($t_{\mathrm{on}} = 5\,\mu\mathrm{s}$), however, do not show much detrapping during the conduction period, indicating that some of the key hot-electron traps in the tested device have time constants between $5\,\mu\mathrm{s} - 50\,\mu\mathrm{s}$. Prior work confirms this estimate, with hot-electron traps measured with time constants on the order of $10\,\mu\mathrm{s}$ [16]. These results further underscore the importance of measuring $\mathrm{d}R_{\mathrm{on}}$ under steady-state operation to ensure that the slow off-state traps are included.

The measurements in **Fig. 8a** and **Fig. 8b** return to hard-switching, but vary frequency and current respectively to show the effects of each individual parameter. **Fig. 8a** highlights the expected trend of increasing $\mathrm{d}R_{\mathrm{on}}$ at higher f_s, with an extra 20 % increase between $50\,\mathrm{kHz}$ and $200\,\mathrm{kHz}$. An increase of $\mathrm{d}R_{\mathrm{on}}$ with frequency is expected and observed in nearly all prior measurements, but we do not expect this trend to continue monotonically to all frequencies. Higher frequency decreases the on-time, which increases $\mathrm{d}R_{\mathrm{on}}$, but also decreases the blocking time, which is expected to reduce $\mathrm{d}R_{\mathrm{on}}$. These counteracting effects point towards the existence of some (much higher) frequency where $\mathrm{d}R_{\mathrm{on}}$ may actually start to *decrease* with higher f_s, at least under soft-switching conditions. This counter-intuitive hypothesis can be justified by considering that under ZVS conditions, $\mathrm{d}R_{\mathrm{on}}$ is only caused by trapping during the blocking time, and at some very high frequency, this blocking time decreases to such a short interval (zero in the limiting case) that no trapping can

occur. This preliminary hypothesis cannot be observed in a DPT setup because the blocking time (t_b) is not adjusted accordingly with f_s, as discussed in **Section II**.

Fig. 8b shows a weak increase of dR_{on} with larger I_{sw}, following increased hot-electron trapping at higher hard-switched currents. For this particular device and operating condition, frequency is much more influential than current (cf., 10 kHz comparison in **Fig. 8b**). Varying duty cycle, d, is similar to a variation of frequency, as higher d reduces the blocking time and increases on-time. **Fig. 9**, which is explained in more depth in **Section IV**, shows this strong dependence on duty cycle at two currents, with a nearly 30 % difference in dRon between 25 % and 75 % duty cycles.

Measurements with varying R_g and varying v_{gs} are excluded for brevity. Switching speed affects dR_{on} where hot electron effects are important – higher R_g slows the switching transition, resulting in a larger V-I overlap time (expected to increase dR_{on}) but smaller peak current during hard-switching (expected to decrease dR_{on}). Ref. [26] reports a dramatic increase in dR_{on} with higher R_g, but the weights of these counterbalancing effects and overall trend of dR_{on} with R_g will likely be device-specific. Expected trends with non-standard v_{gs} values are discussed in **Section II**.

Taken together, these plots demonstrate that dR_{on} is influenced by each parameter, and therefore only one can be varied at a time to understand trends. This multi-dimensional space complicates both the reporting and translation of dR_{on} measurements to *in situ* on-state losses, and the following section proposes solutions for each of these.

IV. Practical Design Procedure

With the multi-dimensional parameter set that influences dR_{on}, care must be taken to translate measurements into on-state semiconductor losses in realistic power converters. In this section, we propose a reporting framework for GaN HEMT manufacturers and a method to include dR_{on} in the converter design process.

Fig. 9 shows a measurement set and a proposed mapping for GaN HEMT manufacturers to report dR_{on} in datasheets, with a four-point measurement set across duty cycle (d) and current (I_{sw}) and the other operating parameters fixed at values that are realistic for *in situ* converter operation ($V_{dc} = 0.6BV_{ds}$, $f_s = 100$ kHz, $R_g = 10\,\Omega$, $T_c = 70\,^{\circ}$C). With eight parameters that influence dR_{on}, reporting measurements such as this at all relevant points would place an undue burden on manufacturers. We propose a two-dimensional linearization around the four measurement points to estimate dR_{on} in the remainder of the operating region and allow the converter designer to estimate on-state losses across duty cycle and current. This linearization around a sparse number of data points is proposed as a middle ground between accuracy and measurement requirements, and is intended only as an estimate at operating points that are not directly measured – **Section III** shows that dR_{on} has complicated, non-linear, and potentially non-monotonic dependencies on each parameter that can only be very roughly approximated as linear. A two-dimensional linear fitting for four points, further, will incur some error from an overspecified space. In our case, the worst-case relative error between measurement and fitting in the dR_{on} factor is 1.2 %.

Nonetheless, GaN HEMT datasheets could include maps, like the one shown in **Fig. 9**, for a subset of these parameters that are especially valuable in widely-adopted topologies. For example, one such subset of maps (four dR_{on} measurements each) might include I_{sw}-d maps for both hard- and soft-switching at two frequencies, which would give an estimate over the chosen frequency range for half-bridge-based converters (e.g. power-factor-correction rectifiers, buck and boost converters, multi-level converters). An additional mapping of I_{sw} vs. f_s for soft-switching would suffice to estimate losses for soft-switched converters that utilize frequency control (e.g. LLC converters). Of course, manufacturers must tradeoff the extent of the maps with the required number of measurements, but could work toward a tool for dR_{on} similar to the configurable core loss software offered by magnetics manufacturers [57] (a similarly-large parameter space that also requires large-signal measurements).

With these maps (or a similar tool) provided by HEMT manufacturers, designers could *a priori* estimate on-state losses in a wide variety of converters utilizing GaN HEMTs. We provide an example for this prediction in a 2 kW totem-pole bridgeless power-factor-correction rectifier (**Fig. 10a**), where 600/650 V GaN HEMTs are advantageous and increasingly used for the high-frequency bridge-leg at operating frequencies ranging from tens of kHz [58] to over 1 MHz [59]. As shown in **Fig. 10a**, the high-frequency GaN HEMT bridge-leg is often paired with a line-frequency "unfolder," the analysis of which is ignored here.

During the positive half-line-cycle shown in **Fig. 10b**, the low-side

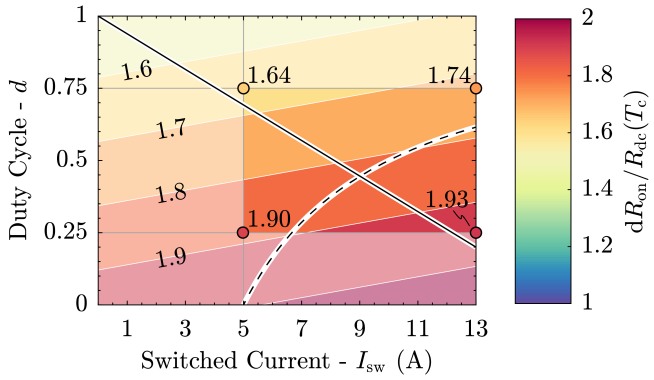

Fig. 9: $dR_{on}/R_{dc}(T_c)$ across I_{sw} and d with hard-switching at $V_{dc} = 0.6BV_{ds}$, $f_s = 100$ kHz, $R_g = 10\,\Omega$, $v_{gs} = +5\,\text{V}/-2\,\text{V}$, $T_c = 70\,^{\circ}$C. Four measured dR_{on} values are labeled, with a two-dimensional linearization performed to interpolate and extrapolate to other values of I_{sw} and d. Solid line is the locus for the bridgeless totem-pole 2 kW PFC rectifier in **Fig. 10**. Dashed line is the locus for a constant-power 2 kW DC/DC buck converter with 400 V input voltage and varying output voltage. For both loci, the duty cycle refers to the low-side switch.

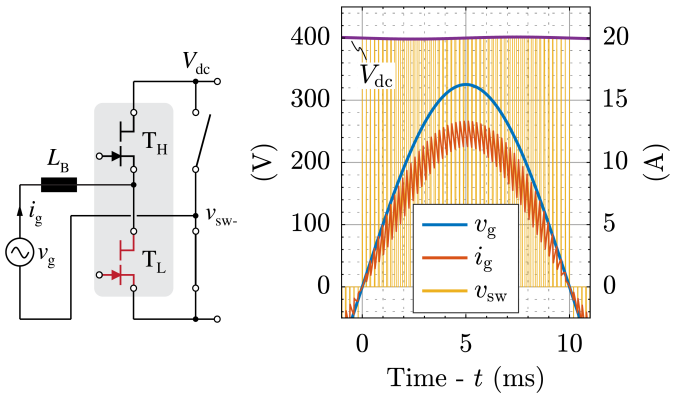

Fig. 10: **(a)** Circuit schematic and **(b)** key operating waveforms for a 2 kW, 400 V V_{dc}, 230 V $V_{g,rms}$ totem-pole bridgeless power-factor-correction (PFC) rectifier in the positive half of the line cycle. The highlighted GaN HEMT bridge leg operates at high-frequency and the other leg is a line-frequency unfolder. The large variation in switch current and duty cycle complicates the prediction of on-state losses with dR_{on}.

GaN HEMT (T_L) is hard-switched with a duty cycle (d_L) of:

$$d_L = 1 - \frac{V_{g,pk}}{V_{dc}} \sin w_g t, \quad (1)$$

and, ignoring the current ripple, the switch current (I_{sw}) is:

$$I_{sw} = I_{g,pk} \sin w_g t. \quad (2)$$

In the I_{sw}-d plane, these equations form the locus shown as the solid line in **Fig. 9**. With this large variation in d and I_{sw}, the converter designer could estimate on-state losses in the presence of dR_{on} in two ways. Conservatively, the designer could assume the maximum value along the locus of $1.97R_{dc}\,(T_c)$ for the entire half-cycle. More accurately, the energy dissipated in each conduction period can be summed along the half-line-cycle as:

$$E_{dRon} = \sum I_{sw}^2 \times dR_{on}\,(d_L, I_{sw}) \times d_L T_s, \quad (3)$$

where $T_s = 1/f_s$, which appropriately weights the dR_{on} impact from each conduction period. In the example here, this method results in an increase of conduction losses in the low-side switch of $1.86\times$ over the losses calculated with $R_{dc}\,(T_c)$. This multiple approaches the conservative estimate in this case because *a)* the majority of conduction losses are accrued at high currents due to the square dependence on current, *b)* these high currents coincide with the highest dR_{on} multiples, and *c)* sine wave modulation is time-weighted towards these higher current values by the nature of the waveform.

During this positive half-line-cycle, the high-side switch is soft-switched with duty cycle $1 - d_L$. As shown in **Section III**, dR_{on} is different between hard- and soft-switching conditions, and therefore a soft-switching I_{sw}-d dR_{on} map would be necessary to fully predict conduction losses in this example PFC converter. In soft-switched converters, dR_{on} estimation is even more critical, as conduction losses generally dominate total semiconductor losses more than in hard-switched applications. Under soft-switching conditions, the dR_{on} factor increases semiconductor losses by the same factor (ignoring soft-switching losses [5], [60]); in hard-switched converters, the increase of overall semiconductor losses due to dR_{on} depends on the application-specific ratio between conduction and switching losses.

Fig. 9 includes a similar locus (dashed line) for a constant-power 2 kW DC/DC buck converter with 400 V input voltage and varying output voltage; the converter designer could appropriately weight dR_{on} by the percentage of time at each output voltage to estimate the effective dR_{on} in the application. Similar maps could be utilized to accurately or conservatively estimate dR_{on} in a range of converter topologies with GaN HEMTs.

V. Conclusion

Existing dynamic on-resistance measurements on GaN HEMTs give such a wide variance of test methods and results that conduction losses currently cannot be accurately predicted in converters utilizing these power devices. In this Letter, we provide a simplified physics-based explanation for the key causes of dR_{on}, and use this background to propose frameworks for future dR_{on} characterization, reporting, and estimation.

Firstly, dR_{on} must be measured under steady-state operating conditions (e.g. with the configurations shown in **Fig. 3**) with an accurate on-state voltage measurement circuit. The standard double-pulse-test method does not give correct values for dR_{on}, as these measurements depend strongly on an arbitrary blocking time and ignore accumulated trapping effects.

The eight key circuit parameters derived in **Section II** influence dR_{on}, and our measurements show that these must be individually controlled for accurate comparisons, trends, and magnitudes. For the commercial GaN HEMT characterized here, dR_{on} remains important, nearly doubling conduction losses for realistic frequencies, currents, and voltages.

We propose a framework for including dR_{on} in GaN HEMT datasheets, with a few key linearized maps forming the basis for conduction loss estimation in a wide range of common topologies. This framework is then used to estimate the effective dR_{on} in a totem-pole PFC rectifier, an emerging application for GaN HEMTs. Eventually, these maps could give way to a software tool similar to those used for core loss estimation, where a number of parameters can be varied on an application-specific basis.

Overall, understanding and standardizing dynamic on-resistance measurements will expedite progress in mitigating this problem and lead to faster, broader adoption of wide-bandgap devices.

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