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***Abstract*—AC power amplifiers are e.g. used to emulate the power grid for testing three-phase power electronics mains interfaces of renewable energy systems or measuring the inner impedance of power distribution grids. Typically, the output stages of the test systems are realized as analog amplifiers and thus achieve very high dynamics and a very high signal quality, but also have significant drawbacks, especially high losses and/or poor efficiencies, which leads to a large cooling volume and weight that dominates the full system power density. In addition, analog amplifiers cannot easily handle bidirectional power flow, i.e., power fed back from active loads such as renewable energy inverter systems is dissipated internally. Furthermore, future power distribution systems, e.g., of More Electric Aircraft, will have fundamental frequencies exceeding 1 kHz, thus ultra-high bandwidth (> 100 kHz) power amplifiers with multiple kW output power are required to emulate harmonic distortions and variations of voltage and/or frequency in such power grids. Currently available analog power amplifiers reach bandwidths of up to 30 kHz, which is too low for all desired applications. Switched-mode, i.e., class-D power amplifiers achieve a high efficiency, however, bandwidths of no more than 5 kHz are reached today due to the high required switching frequency (around a factor of 50 higher than the output bandwidth). However, as shown in this paper, novel wide bandgap semiconductor technology and suitable circuit techniques such as series interleaving (multi-level converter topologies) and parallel interleaving render a switched-mode realization with an effective switching frequency of 4.8 MHz and/or 100 kHz large signal bandwidth possible, while still keeping the switching losses at a moderate level. An analysis of designs with different numbers of voltage levels and interleaved branches is performed and shows that with a triple-interleaved three-level flying capacitor converter, where each switching cell operates at 800 kHz, the targeted effective switching frequency is reached and an efficiency above 95 % is feasible for both directions of power flow. Furthermore, a virtual prototype of the selected design is presented, showing that thanks to the high effective switching frequency, an extremely power-dense overall realization is possible (50 kW/dm^3). Finally, simulations of the control behavior verify excellent control dynamics of the presented concept.**

***Index Terms*—Renewable Energy Systems, High Bandwidth Inverter, Wide Bandgap Semiconductors, Class-D Power Amplifier, Multi-Level Converter, Parallel Interleaving, Ultra-High Bandwidth DC/AC Converter**

I. Introduction

The proliferation of renewable energy sources such as photovoltaics in recent years [1]–[3] requires accurate verification of the corresponding three-phase mains interfaces in terms of compatibility with the power grid (grid codes), e.g., their behavior under certain grid conditions such as voltage and frequency variations, transients, distortions and/or general fault conditions. Typically, those tests are performed with AC power amplifiers featuring a bandwidth exceeding 10 kHz, offering very low distortions of the output voltage (low total harmonic distortion, THD), i.e., a high output voltage quality, and capability to deliver multiple kWs of output power. These characteristics in combination with full four-quadrant operation capability allow the emulation of a power grid under extreme conditions and to perform the required tests in a reasonable period of time and with reasonable costs [4], [5]. For example, operated as AC power *sink*, inverter stages of renewable energy systems can be tested (cf. **Fig. 1**). Similarly, the amplifier can act as an AC electronic load to emulate various load types, e.g., electric machines for testing motor-drive inverter systems [6]–[8], or active and reactive load profiles (impressed current mode) to characterize power electronic converter systems in general. Operated as AC power *source*, different grid-tied systems under test (SUTs) such as three-phase PFC rectifier systems can be tested by emulating the aforementioned power grid behavior for nominal or extreme conditions. The emulated power grid shows almost ideal output voltages and thereby, e.g., the harmonic content of the input current of PFC rectifier systems can easily be quantified as required by international regulations [9]. The aforementioned applications are typically used in conjunction with power hardware-in-the-loop simulations [10]. Furthermore, the inner impedance of the SUT is obtained by injecting test signals into the SUT with the wide-band AC power amplifier while simultaneously measuring the corresponding response. One example for this application is the measurement of the power grid impedance to account for its influence on the stability of grid-connected inverters [11]. Finally, general large-signal power amplification and/or arbitrary waveform generation is easily realized with such a system.

An overview of a system typically used for the above described tasks is shown in **Fig. 1** and comprises an isolated three-phase AC/DC stage (rectifier) and an ultra-high bandwidth, bidirectional DC/AC output stage (class-D power amplifier), whose output is connected to the SUT. The design and realization of an ultra-high bandwidth class-D power amplifier with specifications according to **Table I** is the subject of this paper.

Due to high output signal quality and bandwidth requirements, today typically linear power amplifiers are employed in test systems. However, linear amplifiers are in principle characterized by

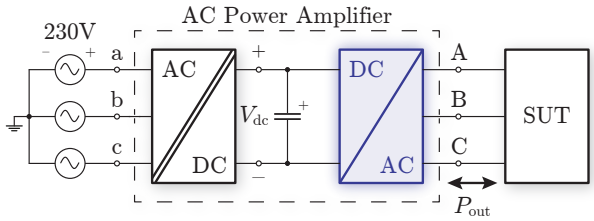

Fig. 1. Block diagram of a bidirectional three-phase AC power amplifier used for testing the three-phase mains interface of a System Under Test (SUT), e.g., the inverter stage of a renewable energy system (power flow from the SUT to the amplifier) or a three-phase PFC rectifier (power flow from the amplifier to the SUT). The three-phase AC/DC stage typically features galvanic isolation and the AC power source analyzed in this paper (highlighted in blue) provides a very high bandwidth and high output voltage quality.

TABLE I. Key specifications for one phase module of the considered AC amplifier.

Parameter	Symbol	Value
Peak Output Voltage per Phase	$V_{\mathrm{out,pk}}$	$0 \ldots 350$ V
Output Frequency	f_{out}	DC$\ldots 100$ kHz
Output Power per Phase	P_{out}	$0 \ldots 10$ kW
DC Link Voltage	V_{dc}	800 V
Effective Switching Frequency	$f_{\mathrm{sw,eff}}$	4.8 MHz
Output Total Harmonic Distortion	THD	1 %

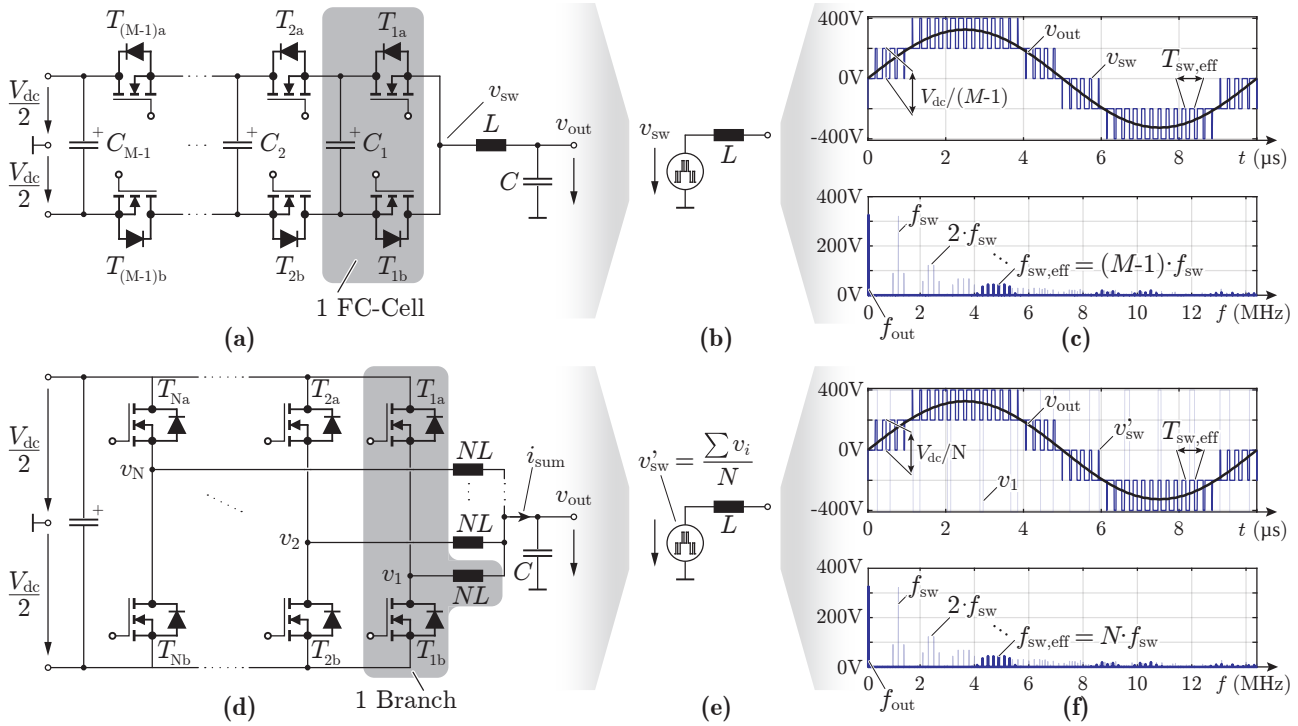

Fig. 2. (a) Circuit diagram of a M-level Flying Capacitor Converter (FCC) with one FC-cell highlighted, **(b)** resulting equivalent circuit for the switch-node voltage v_{sw} and **(c)** corresponding time- and frequency-domain representations of v_{sw} for $M = 5$, i.e., a 5-level converter (4 FC-cells), clearly indicating the multi-level nature of the output voltage with the first occurring frequency component in the spectrum above the fundamental frequency at the effective switching-frequency $f_{\mathrm{sw,eff}} = (M-1) \cdot f_{\mathrm{sw}}$. **(d)** Parallel interleaving of multiple (N) two-level (2L) branches leading to **(e)** the equivalent circuit with the effective switch-node voltage v'_{sw}. The same multi-level waveform **(f)** as for **(a)** is achieved by taking the mean of all individual switch-node voltages and thus the first frequency component in the spectrum above the fundamental component is located at $f_{\mathrm{sw,eff}} = N \cdot f_{\mathrm{sw}}$ (here shown for 4 interleaved 2L branches).

a low efficiency (typically below 78 %) [12]. Accordingly, a large converter volume and weight results due to the required cooling effort. Additionally, linear amplifiers typically show a pronounced reduction of output power capabilities for non-ohmic loads, i.e., for a phase-shift between output voltage and current [13] due to the high internal losses [14]. Another severe drawback is the severely limited capability of regenerative operation, i.e., power from an active load cannot be fed back to the AC power source and is simply dissipated inside the unit, which on the one hand is very inefficient, especially considering long-time tests of high-power SUTs, and on the other hand requires corresponding output power derating due to the limited cooling performance, which restricts the testing capabilities.

Implementations using switched-mode (class-D) power amplifiers [15] with a maximum bandwidth of 5 kHz exist on the market, which are suitable for emulating 50/60 Hz grids but are for example not fast enough to perform tests on grids intended for future More Electric Aircraft targeting a fundamental on-board grid frequency of 1.4 kHz [16].

Hence, there is the need for high-power class-D AC power amplifiers with significantly larger bandwidth, e.g., approaching 100 kHz, while at the same time high efficiency (preferably above 95 %) under any type of load should be ensured. To reach a large-signal bandwidth of 100 kHz, the switching frequency must be chosen approximately 20 . . . 50 times higher, i.e., between 2 MHz and 5 MHz, in order to have sufficient controller bandwidth and to achieve the required output voltage filtering with reasonable effort. The aim of this paper is to realize a system for the presented applications by using a suitable circuit topology in combination with modern power semiconductor technologies, i.e., wide bandgap devices, to achieve the high required switching frequency without an increase in switching losses in order to overcome the drawbacks of currently available solutions. The main target specifications are listed in **Table I** and are serving as basis for the following analyses.

In **Section II**, the proposed circuit topology is presented before in **Section III**, the achievable performance is determined including an analysis of the corresponding limitations. The design of the filter inductor is described in detail in **Section IV** and after the presentation of a virtual hardware prototype in **Section V**, in **Section VI**, a brief overview of the control structure for such a high bandwidth AC power amplifier is given and finally, conclusions are drawn in **Section VII**.

II. Proposed Converter Topology

A high-frequency buck-type voltage source inverter (VSI) topology allows to achieve the aforementioned goals, in particular, the bidirectional power flow and the generation of arbitrary output voltage profiles. Since the classical two-level bridge leg approach would require a switching frequency in the range of 2 . . . 5 MHz, thus generating unacceptably high switching losses, alternative concepts are required.

As very comprehensively shown in [17], there are two principles that allow to increase the effective switching frequency of a VSI without increasing the switching-losses compared to a two-level bridge leg (one switching cell or half-bridge), namely series interleaving (multi-level converters) and parallel interleaving, which are both briefly explained hereinafter.

A. Series Interleaving: Multi-Level Output Voltage Characteristic

Multi-level converters are used to increase the number of levels of the voltage v_{sw} that is applied to the output filter inductor by phase-shifting the operation of $(M-1)$ series-connected switching cells, each operated with f_{sw}, generating M voltage levels at the switch-node as depicted in **Fig. 2 (b)-(c)**. The high-frequency harmonics of v_{sw} are determined by the effective switching frequency $f_{\mathrm{sw,eff}} = (M-1) \cdot f_{\mathrm{sw}}$. Furthermore, the blocking voltage stress of the switches is reduced to $V_{\mathrm{dc}}/(M-1)$. From the various multi-level topologies described in literature, such as the T-Type converter, Neutral Point Clamped (NPC) converter and respective variations [18], the Flying Capacitor Converter (FCC) depicted in **Fig. 2 (a)** has the fundamental advantage that it can generate a high number of voltage levels with reasonable semiconductor effort and

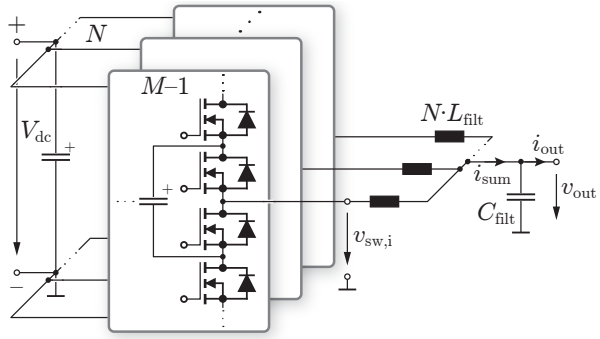

Fig. 3. Representation of N parallel-interleaved M-level branches using N branch inductors, which are connected together at a common output filter capacitor C_{filt}.

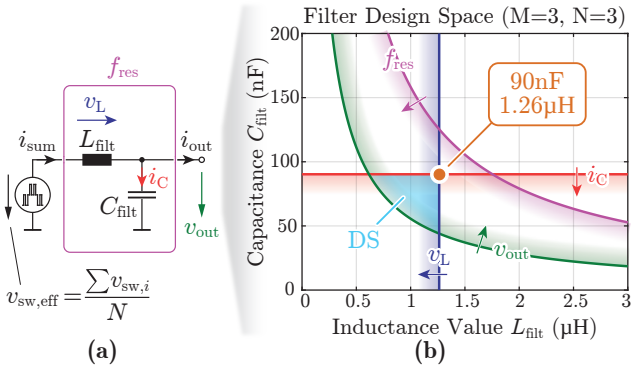

Fig. 4. (a) Equivalent circuit of N parallel-interleaved M-level branches indicating the effective switch-node voltage $v_{\text{sw,eff}}$, the effective filter inductance L_{filt} and the filter capacitance C_{filt} for a single-stage output filter. **(b)** Representation of various criteria that define the valid range for the filter components in the filter design space for $M = N = 3$ according to [25], with the valid design space and the preferred solution highlighted.

is capable of generating a DC output without auxiliary circuits for active balancing of voltages of the stacked DC link capacitors [19]. Therefore, it is identified as a viable converter candidate. As the operation of the M-level FCC, which comprises $(M-1)$ flying capacitors (FCs), has been widely discussed in literature [20]–[22], a further explanation should be omitted here.

B. Parallel Interleaving: Current Ripple Cancellation

Phase-shifted operation of parallel-interleaved half-bridges as shown in **Fig. 2 (d)**, hereinafter called branches, leads to current ripple cancellation, and hence drastically reduces the ripple of the total output current seen by the filter capacitance C_{filt}. At the same time, an increased effective switching frequency $f_{\text{sw,eff}} = N \cdot f_{\text{sw}}$ is obtained at the output capacitor as illustrated in **Fig. 2 (e)-(f)** [23], [24], with f_{sw} being the switching frequency of each individual half-bridge and N denominating the number of interleaved branches.

The resulting effective switch-node voltage $v_{\text{sw,eff}}$ is equal for both, a single M-level bridge leg and $N = M-1$ times interleaved two-level half-bridges (cf. **Fig. 2** for $M = 5$). In both cases the voltage spectrum contains no components between f_{out} and $f_{\text{sw,eff}}$, and therefore the filtering effort can be drastically reduced while keeping a moderate switching frequency f_{sw} of each half-bridge, which is favorable in terms of switching losses. Because multi-level topologies distribute the voltage stress among several devices and parallel interleaved operation distributes the current stress across the parallel branches, a combination of the two approaches, as shown in **Fig. 3** gives additional degrees of freedom in terms of loss and stress distribution. For a parallel-interleaved multi-level converter, the effective switching frequency of the current ripple at the filter capacitor C_{filt} is given as $f_{\text{sw,eff}} = N \cdot (M-1) \cdot f_{\text{sw}}$, which means that combining both approaches allows for an even smaller f_{sw} to reach a given $f_{\text{sw,eff}}$.

III. Quantitative Performance Evaluation

This section presents the performed analysis for a combination of N parallel-interleaved M-level branches as shown in **Fig. 3** to achieve the performance goals given in **Table I**. Since a three-phase system (cf. **Fig. 1**) is formed using three independent output channels/phases, it is sufficient to focus the analysis on one channel/phase only.

A. Filter Design Space

In a first step, the branch inductances need to be known to calculate the converter waveforms. The required output filter is dimensioned based on the high-frequency equivalent circuit depicted in **Fig. 4 (a)**. Using the filter design space (DS) approach presented in [25], various criteria are plotted in the LC-plane (corresponding to the elements in a single-stage output filter), which define the valid DS, highlighted in light blue in **Fig. 4 (b)**. As indicated with different colors, the DS is limited by the following criteria, assuming full output power operation and 100 kHz output frequency: (i) the filter capacitor current i_C is limited to 30 % of the nominal AC output current amplitude (red), which limits the filter capacitance to an upper value of $C_{\text{filt}} = 90$ nF, (ii) the inductor voltage drop v_L is limited to 15 % of the nominal AC output voltage amplitude (blue), limiting the filter inductance to a value below $L_{\text{filt}} = 1.26$ µH, (iii) the maximum output voltage ripple $\Delta v_{\text{out,pp}}$ is set to 1 %pp (peak-to-peak) of the nominal AC output voltage amplitude (green), which defines a minimum filter cutoff frequency and thus a minimum product of C_{filt} and L_{filt}, and finally (iv) the filter resonance frequency f_{res} is chosen to be at least a factor of 4 higher than the maximum output frequency of 100 kHz (pink), resulting in a maximum product of C_{filt} and L_{filt}. There, only the output voltage ripple criterion depends on the number of levels M and number of branches N. In **Fig. 4 (b)** the limits for a design with $M = 3$ and $N = 3$ are shown. For designs with $M \geq 3$ and/or $N \geq 3$, assuming a given fixed $f_{\text{sw,eff}}$, the ripple criterion is easier to fulfill due to smaller voltage steps of the effective switch-node voltage $v_{\text{sw,eff}}$, thus the minimum required filter capacitance and/or inductance move to smaller values, which enlarges the DS area. Therefore, the minimum DS is defined by the design with minimum allowable M and N.

To prevent a large current ripple in the individual branches and to minimize the voltage ripple at the output, i.e., to achieve the highest filter performance for the given design-independent limits, the maximum allowed inductance $L_{\text{filt}} = 1.26$µH and the maximum capacitance $C_{\text{filt}} = 90$ nF are chosen for all combinations of M and N in a first step.

B. Performance Analysis

A comprehensive simulation model is used to generate the characteristic waveforms for an ohmic load based on the specifications compiled in **Table I** and therefrom the performance metrics depicted in **Fig. 5** are calculated for realizations with varying numbers of levels M and branches N. For the semiconductor loss calculations, the 600 V 70 mΩ GaN E-HEMT (IGOT60R70D1 from Infineon [26]) is selected, where the hard switching (HSW) and soft switching (SSW) losses were first measured using a calorimetric measurement method described in [27] and [28] and serve as a solid basis for the analysis of the semiconductor losses. The measured switching losses are presented in **Fig. 6** where positive switched currents I_{sw} correspond to the HSW losses and negative I_{sw} correspond to the SSW losses. The sum of the total conduction and switching losses (cf. **Fig. 5 (a)-(b)**) yields the semiconductor efficiency (cf. **Fig. 5 (c)**). The overall semiconductor losses directly lead to the maximum allowed thermal resistance $R_{\text{th,c-hs}}$ of the interface between the switch case and the heat sink (cf. **Fig. 5 (d)**), where the latter is modeled as a cold plate with $T_{\text{hs}} = 50°\text{C}$. A maximum junction temperature of $T_{\text{j,max}} = 120°\text{C}$ for the switches and the datasheet value of $R_{\text{th,j-c}} = 1$ K/W for the junction-to-case thermal resistance of the semiconductor package are assumed. Furthermore,

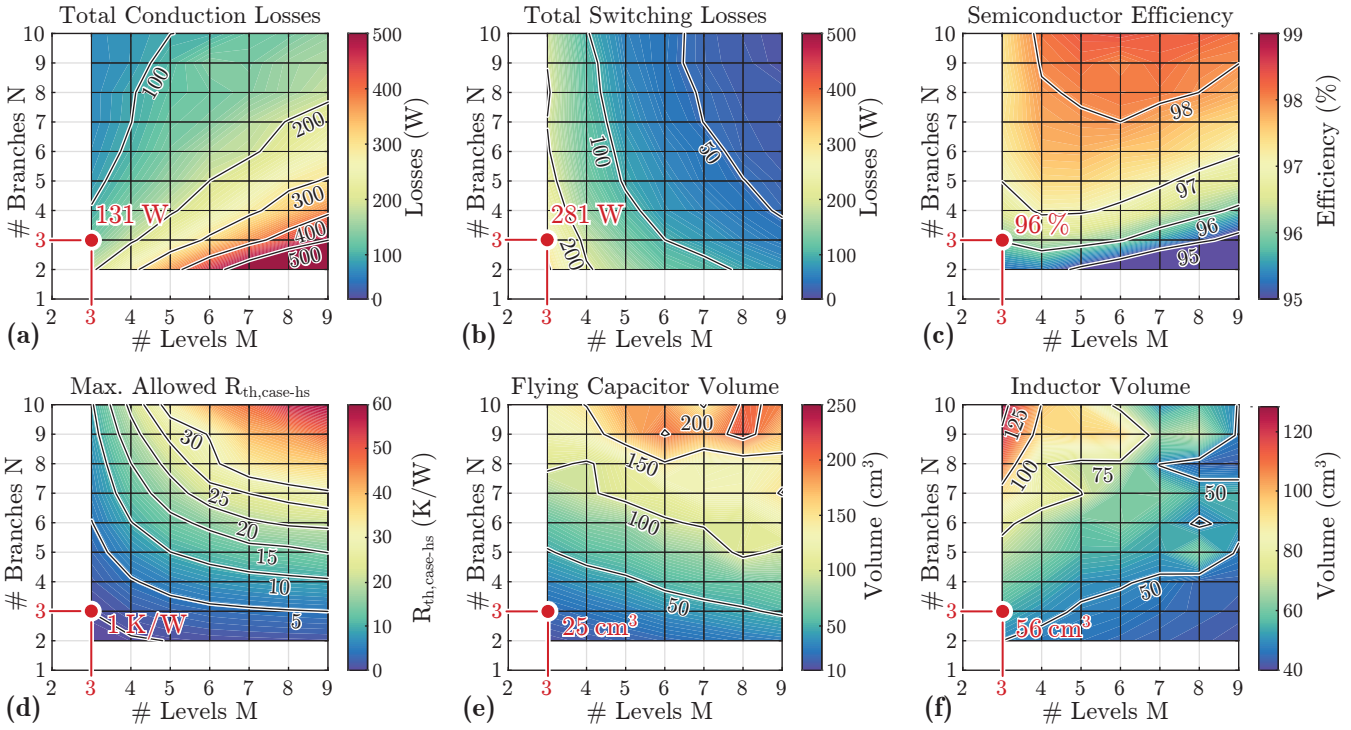

Fig. 5. Characteristics of a class-D amplifier inverter stage realization using N parallel-interleaved M-level FCC branches. **(a)-(b)** Total power semiconductor conduction and switching losses and **(c)** resulting efficiency considering only the total semiconductor losses. **(d)** Allowed maximum case-to-heat sink thermal resistance and **(e)** resulting volume of the flying capacitors, assuming an allowed voltage ripple of 5 Vpp independent of the capacitor position in the branch structure together with **(f)** the required total inductor volume.

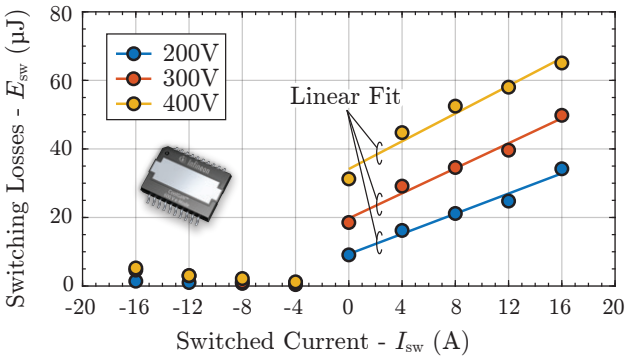

Fig. 6. Measured values of the total switching energy E_{sw}, which is dissipated during one switching transition of a 600 V, 70 mΩ CoolGaN switch [26] for different switched currents I_{sw} and voltages V_{ds}. Negative currents I_{sw} denote Soft Switching (SSW) losses and $I_{\mathrm{sw}} > 0$ denote Hard Switching (HSW) losses. The exact measurement points are indicated with dots whereas for the HSW energies a linear interpolation using the least mean squares method is included for each voltage.

a polynomial fit of the capacitance density vs. the rated voltage based on commercially available ceramic capacitors is used to estimate the volume of the flying capacitors (cf. **Fig. 5 (e)**). The branch inductor volume is approximated using the volume of the realized prototype (cf. **Section IV**), which is scaled according to $L_{\mathrm{br}} \cdot i_{\mathrm{L,pk}} \cdot I_{\mathrm{L,rms}}$ for different M and N (cf. **Fig. 5 (f)**), where L_{br} denotes the branch inductance and $i_{\mathrm{L,pk}}$ and $I_{\mathrm{L,rms}}$ the peak and rms inductor current, respectively.

While an increasing number of levels M and interleaved branches N results in a higher efficiency, the utilization of the switches decreases. Furthermore, a larger volume must be accepted and the circuit complexity increases substantially, since with each additional voltage level in every branch another pair of switches, isolated gate drivers, auxiliary gate drive power supplies and an additional flying capacitor is required. Therefore, as the design specifications of **Table I** can already be met with $M = 3$ and $N = 3$, this design is selected, considering that only one flying capacitor per branch is required, and a power-dense realization is feasible due to the low number of switches, while still achieving a semiconductor efficiency of 96 %. The respective values for this design are highlighted in **Fig. 5**. Given the semiconductor efficiency of 96 %, each switch in the selected design dissipates around 34 W for $P_{\mathrm{out}} = 10$ kW and an adequate cooling system, i.e., forced-air or water cooling, has to be implemented. There, the utilization of the 70 mΩ switches gives a good sharing between conduction and switching losses of roughly 1 : 2.1. In contrast, 650 V 25 mΩ GaN switches [29], [30] would result in almost identical total semiconductor losses, but the sharing between conduction and switching losses becomes almost 1 : 4, which degrades partial load performance, since the switching losses scale approximately linear with the switched current (cf. **Fig. 6**) whereas the conduction losses scale quadratically with the current. Hence, a device with smaller die area in a package with sufficient area for cooling should be selected.

C. Design Evaluation

In **Fig. 7 (a)-(d)**, the simulated waveforms for the nominal operating point of $V_{\mathrm{out,rms}} = 230$ V, $P_{\mathrm{out}} = 10$ kW and $f_{\mathrm{out}} = 100$ kHz with ohmic load are depicted, clearly indicating the effective switching frequency of $f_{\mathrm{sw,eff}} = 4.8$ MHz, even though the individual half-bridges are switched with $f_{\mathrm{sw}} = f_{\mathrm{sw,eff}}/(N \cdot (M-1)) = 800$ kHz only. The high number of voltage levels, i.e., $(M-1) \cdot N + 1 = 7$ in the effective switch-node voltage $v_{\mathrm{sw,eff}}$ seen by the equivalent filter inductor L_{filt} is also apparent. Following the triple-interleaved approach with a targeted $L_{\mathrm{filt}} = 1.26$ µH, each branch requires a branch inductor with an inductance $L_{\mathrm{br}} = 3 \cdot L_{\mathrm{filt}} = 3.8$µH whose current has a ripple Δi_{Lpp} with a frequency equal to $f_{\mathrm{iLpp}} = f_{\mathrm{sw,eff}} \,/\, N = 1.6$ MHz. Thanks to the interleaving, the three inductor current ripples cancel to a great extent and the resulting summed current i_{sum} shows only a very small ripple with a frequency $f_{\mathrm{sw,eff}}$, which is then attenuated by the filter capacitor such that the resulting fundamental output voltage and/or current is entirely sinusoidal.

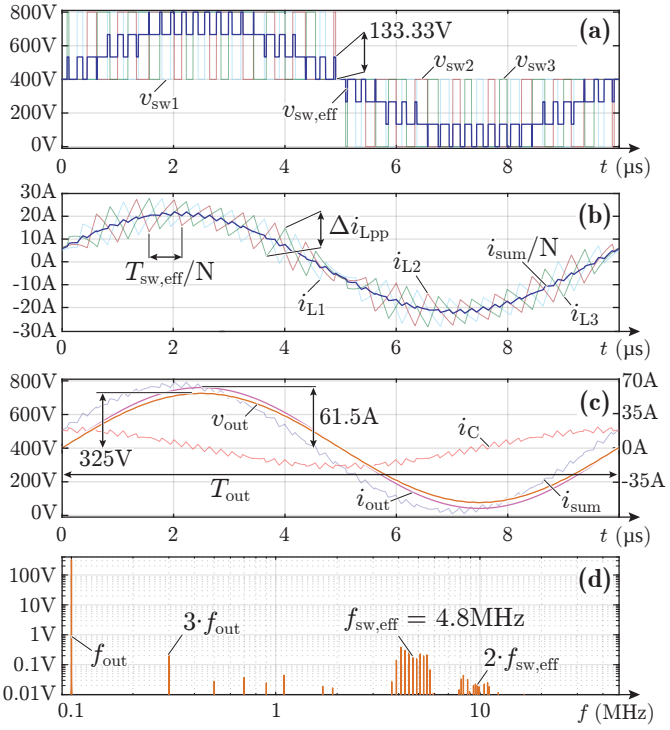

Fig. 7. Simulated waveforms of the selected solution with $N = 3$ parallel-interleaved branches of $M = 3$ levels each, with **(a)** the corresponding switch-node voltages $v_{sw1..3}$ and the equivalent $v_{sw,eff}$, **(b)** inductor currents $i_{L1..3}$ (assuming a branch inductance $L_{br} = N \cdot L_{filt} = 3.8\mu H$) including the sum of the branch output currents (inductor currents) i_{sum}/N (divided by N for better visualization), **(c)** the output voltage v_{out} and current i_{out}, the sum of the inductor currents i_{sum} together with the filter capacitor current i_C and **(d)** the resulting output voltage spectrum.

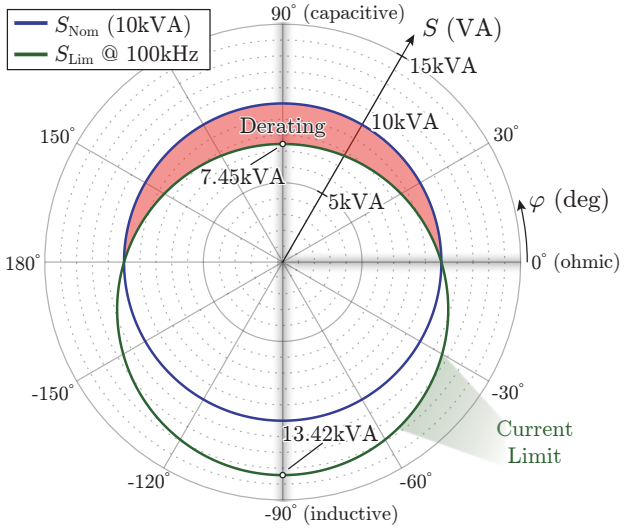

Fig. 8. Theoretical limitation S_{Lim} (green) of the apparent output power versus the load angle φ (phase-shift between the output voltage and current waveforms) for the given selection of the filter elements ($L_{filt} = 1.26\,\mu H$, $C_{filt} = 90\,nF$) for a 100 kHz sinusoidal output signal with 230 Vrms relative to a nominal output power of 10 kVA (blue) and ohmic loads ($\varphi = 0\,°$). The limitation is derived from the switch rms current for $M = 3$ and $N = 3$ under the assumption of a worst-case peak-to-peak current ripple of 100 % (with respect to the fundamental component). The required derating of around 25 % of the output power for capacitive loads is highlighted in red.

D. Theoretical Performance Limitation

Given the sinusoidal nature of the output voltage and current, theoretical output power limitations for the proposed converter can directly be derived using the phasor representation of voltage and current. For the nominal operating point at $f_{out} = 100\,kHz$ and $V_{out,rms} = 230\,V$, the theoretical possible apparent output power S_{Lim} for each load angle φ (phase-shift between output voltage and current waveforms) is depicted in **Fig. 8** in green. It is limited by two constraints, (i) the maximum possible voltage amplitude that can be generated at the switch node, basically given by $V_{dc}/2$, here set to $0.95 \cdot V_{dc}/2$ to have a certain margin (corresponds to a modulation depth $m_M = 0.95$) and (ii) the maximum possible switch rms current, which is limited by the semiconductor losses and thus highly depends on the thermal design. The rms current derived from the conduction losses occurring for $M = 3$ and $N = 3$ and ohmic load in the nominal operating point is taken as a reference (cf. **Fig. 5 (a)**), i.e., $I_{sw,rms} = 11.6\,A$. The inductor current relates the switch current to the output current and its rms value is calculated under the assumption of a triangular peak-to-peak current ripple of 100 % (with respect to the amplitude of the fundamental component) as worst-case approximation (cf. **Fig. 7**). Since the current limit is derived from the ohmic load case, the S_{Lim} circle intersects with the blue circle representing the nominal power $S_{Nom} = 10\,kVA$ at $\varphi = 0\,°$ and $\varphi = 180\,°$. It is shown that for capacitive-resistive loads ($\varphi > 0\,°$) the current limitation leads to an output power derating of around 25 %, which is much smaller compared to state-of-the-art linear power amplifiers [13]. For all other load cases, there is a sufficient margin, especially for inductive loads (> 30 % margin), which partially compensate the reactive power of the output filter. If higher currents would be allowed, the maximum possible converter voltage would limit the maximum output power for inductive loads ($\varphi = -90\,°$). This cannot be seen in **Fig. 8** due to the strong current limit and because the inductance is chosen based on limiting the maximum inductor voltage to 15 % of the peak output voltage for an ohmic load scenario.

IV. Inductor Design

A. Core Material and Geometry

In this section, the design of the branch inductors L_{br} is presented. Since both, the fundamental and the ripple components of the inductor current are at comparably high frequencies, a core material with good high-frequency properties such as NiZn or MnZn has to be considered. In particular, it has to be ensured that the magnetic material still features a sufficient permeability at frequencies in the MHz-range without generating excessive core losses. A survey of different materials revealed that the *3F46* [31] and *3F4* [32] ferrites from Ferroxcube are suitable candidates, since both are designed to be operated up to $2 - 3\,MHz$.

To prevent saturation of the magnetic core material, the core cross-section A_E, as well as the number of turns N_T, are chosen such that the peak magnetic flux density B_{pk} remains at a value well below the material-specific saturation flux density B_{sat}, i.e., $B_{pk} = k_B \cdot B_{sat}$ with $k_B \in [0, 1]$. From the definition of the flux linkage Ψ follows

$$N_T \cdot A_E \geq \frac{\Psi_{pk}}{B_{pk}} = \frac{\Psi_{pk}}{k_B \cdot B_{sat}} = \frac{L_{br} \cdot i_{L,pk}}{k_B \cdot B_{sat}}. \quad (1)$$

Typically, the excitation of high-frequency core materials must be limited to values well below the saturation flux density, in order to prevent excessive core losses and non-linear material behavior. Therefore, the maximum flux density excitation, based on basic calculations and initial core loss measurements, is limited to 0.25 T, which is significantly lower than the corresponding B_{sat} values of both considered materials. Together with the peak inductor current $i_{L,pk} = 30\,A$ obtained from the circuit simulation at the nominal operating point ($V_{out,rms} = 230\,V$, $P_{out} = 10\,kW$, $f_{out} = 100\,kHz$) and the required branch inductance $L_{br} = 3.8\,\mu H$, the product $N_T \cdot A_E$ must be larger than $456\,mm^2$ (cf. (1)). Given the list of available cores of the materials under consideration as well as considering typical wire diameters and aiming for a very compact realization, the selected design with $A_E = 77\,mm^2$ and $N_T = 6$ is a good compromise between A_E and the available winding window A_W; the required 6 turns can be fitted with a high fill factor. The

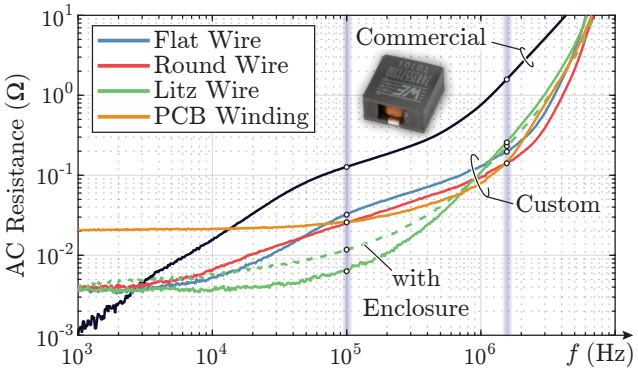

Fig. 9. Measurements and comparison of the AC resistance of a coil with 6 turns using flat wire (4 mm × 0.6 mm, blue), round wire ($d_{\mathrm{cu}} = 1.7$ mm, red) and litz wire (630 × 71 µm, green), each measured with a gapped E-core of the selected *3F46* material, including an air gap of 0.5 mm in each leg. Further depicted is the AC resistance of the realization with PCB integrated winding (orange) and the AC resistance of a commercially available 3.3 µH inductor (black) [35] used as volume benchmark. The highlighted values at 100 kHz and 1.6 MHz are listed in **Table II**.

required total air gap $\delta = 0.92$ mm to achieve the desired inductance is very small and advantageously leads to a low fringing field. The core is realized with a E32/6/20 core set cut to a length of 12 mm from the original 20 mm in order to achieve the desired A_{E}; the air gap is realized in all three legs.

B. Core Losses

For the desired frequency and flux density values there are no Steinmetz parameters of the *3F46* material available, however, a rough approximation of the core losses is obtained by injecting a current in a test inductor using a power amplifier (NF Corporation IE-1125B) driven by an arbitrary waveform generator (Tektronix AFG3102), which impresses a certain flux density in the core material. Due to the constant losses, the core temperature increases with a certain slope and based on the thermal capacitance of the core material the core losses can be calculated [33]. The test inductor is designed in such a way that the injected current results in the same flux density profile as obtained in the branch inductor determined with the circuit simulation of the proposed converter at the previously described operating point including the limitation of $B_{\mathrm{pk}} = 0.25$ T. For simplicity, the current ripple superimposed to the fundamental current is approximated with a sinusoidal signal at 1.6 MHz. An overall loss-density of 3.3 W/cm^3 is found for the flux density profile composed of the superposition of the 100 kHz fundamental and the 1.6 MHz ripple component, whereas the same method considering only either the sinusoidal fundamental component with a flux density amplitude of 0.19 T at 100 kHz or the sinusoidal ripple component with 0.065 T at 1.6 MHz yields 1.4 W/cm^3 and 1.05 W/cm^3, respectively. Therefore, the biasing of the high-frequency ripple with the "low"-frequency fundamental component leads to approximately 35 % of additional core losses. Given the branch inductor prototype core volume of 3.5 cm^2, core losses of 11.55 W result for the *3F46* material.

For the *3F4* material, Steinmetz parameters are available for the desired frequency and flux density range [34]. A comparison of the measured losses of the *3F46* material with the calculated losses of the *3F4* material reveals that for the given flux densities the former shows approximately 35 % higher losses at 100 kHz and almost three times lower losses at 1.6 MHz than the latter. Without considering low-frequency biasing effects, the *3F4* material has approximately 65 % higher core losses for the given flux density profile. Therefore, the preferred material for the inductor prototype is *3F46*.

C. Optimal Winding Type and Conduction Losses

To find the optimal winding type, in **Fig. 9** measurements of the AC resistance of a flat wire winding (0.6 × 4 mm, blue), a round wire winding ($d_{\mathrm{cu}} = 1.7$ mm, red) and a litz wire winding (630 × 71 µm, green) with 6 turns each on the selected magnetic core set are presented. The dimensions of the different wires are chosen in such a way that approximately equal DC resistances are achieved in all cases. As a comparison, the AC resistance of a commercial 3.3 µH inductor (74435580330 from Würth Elektronik [35]) with similar current rating ($i_{\mathrm{L,pk}} = 45$ A), which serves as a volume benchmark ($V_{\mathrm{L}} = 6$ cm^3) is measured as well. From **Fig. 9** it is clearly visible that the litz wire performs best at frequencies up to 900 kHz and is therefore yielding the lowest losses for the dominating fundamental frequency current component. At elevated frequencies and particularly at the current ripple frequency of 1.6 MHz it is outperformed by both, the flat and the round wire due to the high inner proximity losses appearing in litz wire windings. The commercial inductor is apparently optimized for very low-frequency applications and offers the smallest DC resistance but is not suitable for this application due to its immense AC losses. The total AC winding losses are calculated and listed in **Table II**, considering the branch current spectral components located at the fundamental frequency (100 kHz) as well as the components around the current ripple frequency (1.6 MHz, also considering sidebands), resulting from the circuit simulation using ideal components. The final inductor prototype is wound with litz wire due to the lowest overall AC winding losses of 4.5 W. Furthermore, the dashed line in **Fig. 9** considers the effect of a metallic enclosure on the AC resistance, which is required to cool the inductor. The influence is mainly visible at fundamental frequency (approximately double losses), which is explained with induced eddy currents in the conductive enclosure, whereas at ripple frequency, almost no increase is measured. Including the additional 1.7 W attributed to the metallic enclosure, total AC losses of around 6.1 W result for the inductor. It has to be noted, that the provided data is only valid for an ambient temperature of 25 °C and the corresponding losses are expected to increase by 30 % when considering a winding temperature of 100 °C based on the temperature dependent conductivity of copper.

Adding up core and winding losses, the total inductor losses are in the order of 18 W at 25 °C (20 W at 100 °C) and to limit the

TABLE II. AC resistance at 100 kHz and 1.6 MHz with corresponding power loss for the four compared winding types, each measured with core. As a comparison, the figures for the considered commercial inductor [35] are given as well.

Type		R_{AC} (mΩ)		P_{AC} (W)		
		100 k	1.6 M	100 k	1.6 M	**Total**
Flat		32	200	7.8	2.6	**10.4**
Round		25	140	6.1	1.8	**7.9**
Litz	No case	5.8	240	1.4	3.0	**4.4**
Litz	With case	12.2	245	3.0	3.1	**6.1**
PCB		26.8	158	6.6	2.0	**8.6**
Commercial		127	1650	31.3	21.2	**52.5**

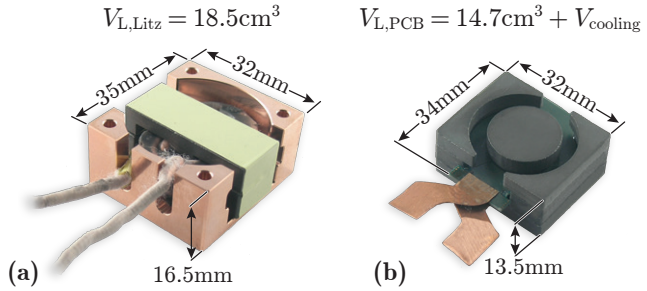

Fig. 10. Picture and boxed volume of **(a)** the inductor prototype with litz wire winding and customized E32/6/20 core halves placed inside a metallic enclosure for cooling and **(b)** alternative realization as PCB integrated winding with custom milled magnetic core, however, without cooling enclosure, which would add roughly another $4 - 5\,\mathrm{cm}^3$.

temperature $T_{\mathrm{L,HS}}$ of the inductor hotspot to 100 °C, the temperature difference ΔT between hotspot and heat sink baseplate must not exceed 50 °C, if again a constant heat sink temperature $T_{\mathrm{hs}} = 50\,^{\circ}\mathrm{C}$ is assumed. This means that the interface must have a thermal resistance smaller than 2.5 K/W. To achieve this, the inductor will be potted with a thermally conductive material inside a metallic enclosure as depicted in **Fig. 10 (a)** (without the potting yet).

To ensure the intended operation of the inductor, its self-resonance frequency (SRF) needs to be sufficiently above the current ripple frequency (1.6 MHz). The assembled prototype without potting has a SRF in the order of 25 MHz. A thermal gap filling material with a certain relative permittivity ε_{r} leads to a decrease of the SRF according to $1/\sqrt{\varepsilon_{\mathrm{r}}}$, given the worst-case assumption that the parasitic capacitance is solely defined by the metallic enclosure around the inductor. Typically, thermal gap-filler materials show a permittivity in the range of $4-10$ and therefore would decrease the SRF in the worst-case to around 8 MHz, which is still sufficiently above the current ripple frequency.

D. PCB Integrated Winding

For a comparison, an inductor with a PCB integrated winding based on the compensating fringing field concept (CFFC) proposed in [36] and [37] with very similar dimensions is built as depicted in **Fig. 10 (b)**. As shown in **Fig. 9** its DC and low-frequency resistance is substantially higher compared to the litz wire realization, however, at frequencies between 1 and 3 MHz it performs better. For the PCB integrated inductor, custom milled cores are required and to facilitate the milling process, a larger core cross-section A_{E} is chosen in this case, which for a given current and inductance reduces the flux density and therefore also the specific core losses but at the same time increases the overall inductor volume. Due to the increased core volume of 7.5 cm^3, the resulting calculated core losses of 5.5 W are lower compared to the litz wire realization. The total winding losses are calculated as 8.6 W using the same procedure as described above (cf. **Table II**). Therefore, the PCB realization gives around 20 % lower total losses (14.2 W at 25 °C and 16.8 W at 100 °C) at roughly the same volume, however, the volume V_{cooling} of the required cooling enclosure ($4-5\,\mathrm{cm}^3$) is not yet considered there.

Due to the comparably small differences in volume and losses, the preferred solution depends on whether one aims at minimum volume or minimum losses and/or aspects such as mechanical constraints (e.g. if it is feasible to place the core around the PCB), manufacturing capabilities (e.g. PCB winding with custom milled ferrite cores or litz winding with a simpler core geometry) and the design of a sophisticated cooling system, which has to ensure sufficient cooling of the winding in case of the conventional inductor where it is typically easier to cool the core and vice versa for the PCB integrated realization.

V. Virtual Prototype

Fig. 11 shows a virtual prototype (3D CAD model) of the selected design composed of the three branch inductors L_{br} (litz wire realization with metallic enclosure), a power stage including the switches and commutation and flying capacitors, a gate drive PCB and a control and measurement board, which also generates the auxiliary supply voltages. The resulting total volume is in the order of 195 cm^3 including the base plate for the water cooling, where the latter contributes 30 cm^3. This roughly corresponds to twice the volume of a conventional three-phase power module comprising six 1200 V Si IGBTs and antiparallel diodes with same power rating, however, not including the output filter, cooling, control and measurement circuitry as well as auxiliary supplies. Based on this virtual prototype, a theoretical power density of more than 50 kW/dm^3 (820 W/in^3) is achieved.

VI. Control Principle

To have an idea about the dynamic performance, the responses for a step in the control variable (output voltage v_{out}) and for a load

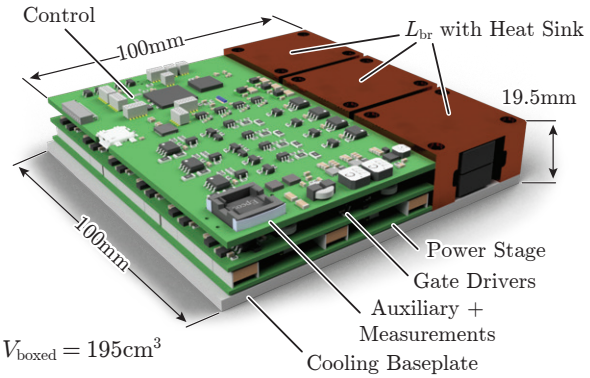

Fig. 11. Virtual prototype of the proposed 10 kW class-D amplifier according to **Fig. 3** ($M = 3$, $N = 3$) with an overall boxed volume of 195 cm^3 (> 50 kW/dm^3) including a 3 mm thick baseplate for the water cooling to be installed with all relevant converter elements labeled.

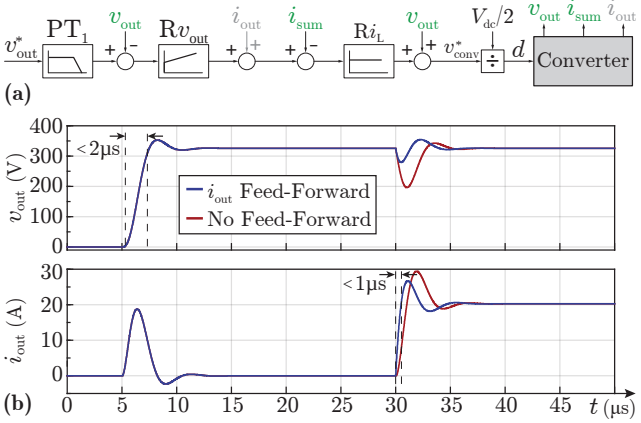

Fig. 12. (a) Cascaded output voltage control structure with inner P-type current and outer PI-type voltage controller and optional feed-forward of the output current i_{out}. The quantities to be measured for a physical realization are labeled in green. **(b)** Step responses of the output voltage (at $t = 5$ µs) and output current ($t = 30$ µs) for the case with (blue) and without (red) load current feed-forward.

step (output current i_{out}) are simulated. **Fig. 12 (a)** shows a classical cascaded structure with inner current control (P-type) of the summed branch current i_{sum} (cf. **Fig. 3**) and outer voltage control (PI-type). The corresponding step responses for a control step (output voltage from 0 V to 325 V at $t = 5$ µs) and a load step (i_{out} from 0 A to 20 A at $t = 30$ µs) are given in **Fig. 12 (b)**. An optional feed-forward of the output current (indicated with a gray arrow in **Fig. 12 (a)**) can be implemented to improve the dynamic performance for a load step as indicated with the blue curves. Alternatively, the inner current control loop can be replaced by a simple feedback of the capacitor current i_{C} [38] to have the same effect as a differentiator component in the voltage control loop. As explained in detail in [38], the dynamic performance achievable with such a control structure closely matches the performance of the classical approach presented in **Fig. 12 (a)**, with which, as seen in **Fig. 12 (b)**, a rise time of less than 2 µs for a step in the output voltage and less than 1 µs for a load step results. This clearly indicates the achievable excellent dynamic performance of the proposed amplifier concept.

VII. Conclusion

It is shown that with the utilization of modern WBG semiconductors in combination with a suitable circuit topology, i.e., multi-level bridge legs and parallel interleaving, an ultra-high bandwidth switched-mode AC power amplifier with DC capability and an effective switching frequency of 4.8 MHz can be realized. The analysis of the semiconductor losses and the required volume vs. the number of voltage levels M and interleaved branches N shows that

the target specifications of 100 kHz large-signal bandwidth at output power levels up to 10 kW can be reached with a triple-interleaved three-level flying capacitor converter with a total volume of only $195\,\mathrm{cm}^3$ per phase ($> 50\,\mathrm{kW/dm}^3$) including the output filter as well as the baseplate of the water cooling system as illustrated with a virtual prototype. The $M = 3$ and $N = 3$ design achieves a semiconductor efficiency of $96\,\%$. While a higher number of levels and/or more parallel-interleaved branches would improve efficiency and semiconductor loss distribution, circuit complexity would increase drastically, which would make a proper high-frequency PCB layout very difficult. The limitations regarding output filter design are presented and therefrom the design of the branch inductors is derived. An inductor with an inductance of $3.8\,\mu\mathrm{H}$ rated for the given frequency and current is realized. Total losses (winding + core) are estimated as 18 W per inductor and the volume of all three inductors together is around $55\,\mathrm{cm}^3$ including the metallic enclosure for cooling. An alternative inductor realization with a PCB integrated winding achieves a very similar performance in terms of losses and volume, hence depending on the requirements, both solutions are suitable. Considering the two main loss contributors, i.e., semiconductors and inductors, an overall system efficiency of more than $95\,\%$ is achieved. Finally, the excellent dynamic properties of the amplifier stage, i.e., a full-scale step response time of only $2\,\mu\mathrm{s}$ should be highlighted.

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